More than 3 PCI Masters with STPC Client

by M. Zoppi and M. Tabet

1.   Overview.

This document provides detailed information regarding the way to implement a PAL device that will allow an STPC Client Motherboard to support more than 3 PCI master devices. This document is intended to support the following device:

STPC Client

For additional information on the STPC Client specifications, please refer to the STPC Client Databook. Information in this document is subject to change without notification.

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2.   Background.

The STPC Client implements the internal logic to handle up to 3 PCI Master Devices. That means that STPC Client support 3 PCIREQ# and 3 PCIGNT# signals.
The PAL described here below is intended to handle more than 3 PCI Master Devices in a design using the STPC Client. As one PAL is capable to manage up to 4 PCI Master Devices, up to 12 Masters can be connected to the STPC Client.

2.1   Description.

The four Req# signal from the Master Devices are connected to the PAL that generates just one REQ# to the STPC Client. Then The STPC generates the GNT# signal that is forwarded to the requesting master.

The PAL 'remembers' the last master served in order to avoid to always serve first the same master, when two or more requests are pending simultaneously.
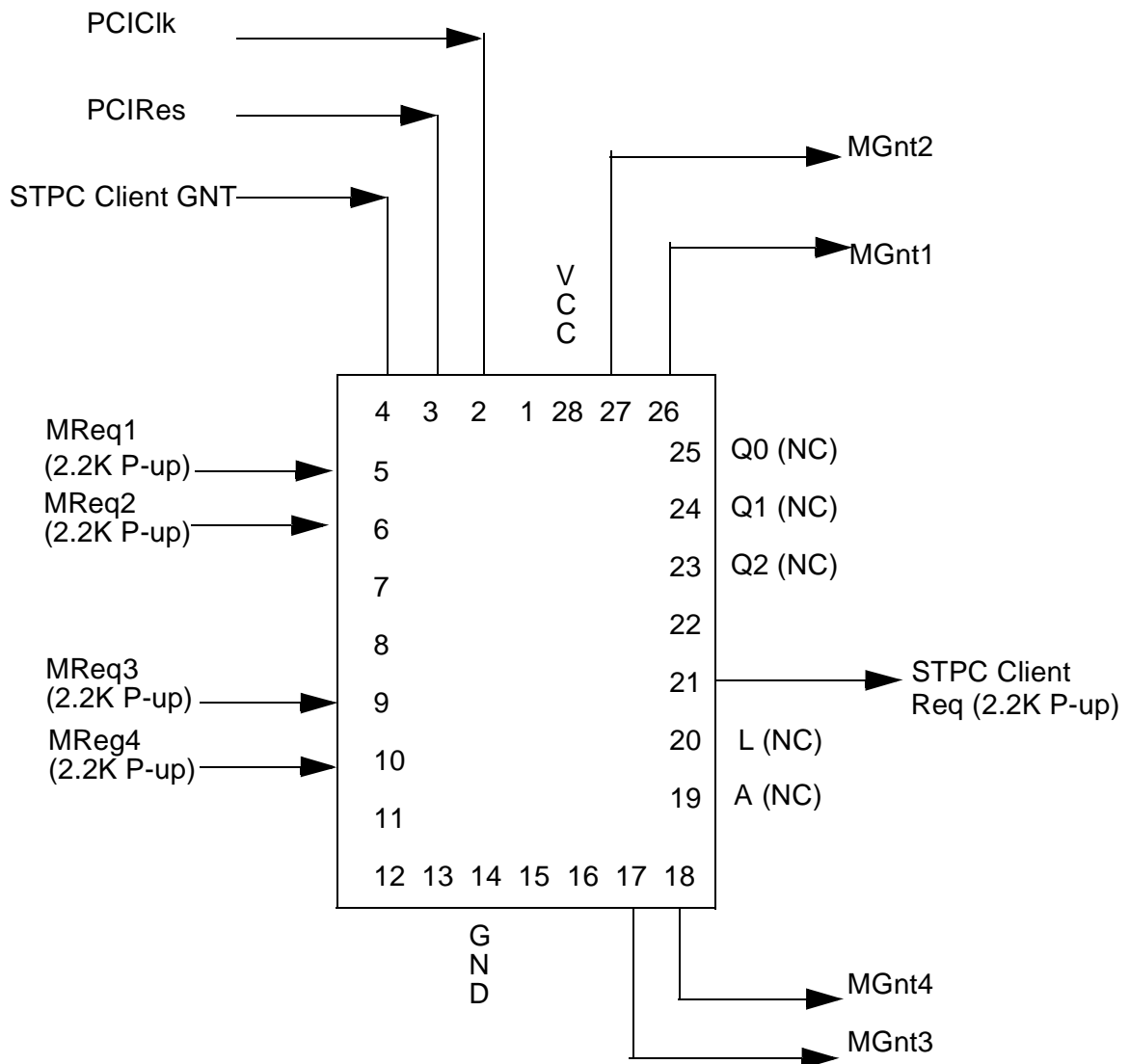
The device used is a 22V10-10. 2.2K pull-up resistors are needed for the four input Master Requests and for the STPC Client Req# signal.

All other pins not mentioned in the following drawing must be Not Connected.

The PAL has been checked with simulation Test Vectors but has not been implemented on a STPC Client Motherboard by ourself

2.2 Pinout

2.3 Equations and Test Vectors

The following equations have been used to generate the JEDEC file able to program the PAL described above:

Module mm1

Title 'Four PCI Masters Handler for STPC Client' by M. Zoppi 28/5/98
    STMicroelectonics
    165, rue E. Branly
    01637 Saint-Genis Pouilly Cedex
    France

```
    mm1    device  'p22v10c' ;
    q0,q1,q2           pin  23,24,25  istype 'reg,invert';
    clock              pin  2 ;
    reset              pin  3  ;
    R1,R2,SIPG,R3,R4   pin  5,6,4,9,10 ;
    A, L               pin  19,20  istype 'reg';
    G1,G2,SIPR,G3,G4   pin  26,27,21,17,18 ;
    sreg               =    [q2,q1,q0];
```

"State Values...

S = 0;   B = 1;   C = 2;   D = 3 ; E = 4;   F = 5;   G = 6;   K = 7 ;

Equations

```
    [q2,q1,q0,A,L].clk = clock;
    [q2,q1,q0,A,L].ar  = !reset ;
```

state_diagram sreg;

State K :

```
    SIPR = 1 ;
    A:=1 ; L:=1 ;
    G1 = 1 ; G2 = 1 ;
    G3 = 1 ; G4 = 1 ;
    goto S with
     {
    SIPR = 1 ;
    A:=1 ; L:=1 ;
    G1 = 1 ; G2 = 1 ;
    G3 = 1 ; G4 = 1 ;
```

```
        }
```

State S:

```
    A:= A ; L:=L ;
    SIPR = R1*R2*R3*R4 ;
    G1 = 1 ; G2 = 1 ;
    G3 = 1 ; G4 = 1 ;
    if (A*L*!R2)  then    C
    else
    if (A*L*!R3)  then    D
    else
    if (A*L*!R4)  then    E
    else
    if (A*L*!R1)  then    B
    else
    if (!A*L*!R3) then    D
    else
    if (!A*L*!R4) then    E
    else
    if (!A*L*!R1) then    B
    else
    if (!A*L*!R2) then    C
    else
    if (!A*!L*!R4) then   E
    else
    if (!A*!L*!R1) then   B
    else
    if (!A*!L*!R2) then   C
    else
    if (!A*!L*!R3) then   D
    else
    if (A*!L*!R1) then    B
    else
    if (A*!L*!R2) then    C
    else
    if (A*!L*!R3) then    D
    else
    if (A*!L*!R4) then    E
    else S with
{
 SIPR = 1 ;
 G1 = 1 ; G2 = 1 ;
 G3 = 1 ; G4 = 1 ;
 A:= A ; L:=L ;
```

```
  }
```

State B:

```
  SIPR = R1*R2*R3*R4 ;
  G1 = SIPG ;
  G2 = 1; G3 = 1; G4 = 1;
  A := 1 ;  L :=1 ;
  if (!R1) then   B with
   {
  SIPR = R1*R2*R3*R4 ;
  G1 = SIPG ;
  G2 = 1; G3 = 1; G4 = 1;
  A := 1 ;  L :=1 ;
   }
  else  S  with
    {
  SIPR = R1*R2*R3*R4 ;
  G1 = SIPG ;
  G2 = 1; G3 = 1; G4 = 1;
  A := 1 ;  L :=1 ;
   }
```

State C:

```
  SIPR = R1*R2*R3*R4 ;
  G2 = SIPG ;
  G1 = 1; G3 = 1; G4 = 1;
  A := 0 ;  L :=1 ;
  if (!R2) then   C with
   {
  SIPR = R1*R2*R3*R4 ;
  G2 = SIPG ;
  G1 = 1; G3 = 1; G4 = 1;
  A := 0 ;  L :=1 ;
   }
   else  S  with
    {
  SIPR = R1*R2*R3*R4 ;
  G2 = SIPG ;
  G1 = 1; G3 = 1; G4 = 1;
  A := 0 ;  L :=1 ;
    }
```

State D:

```
    SIPR = R1*R2*R3*R4 ;
    G3 = SIPG ;
    G2 = 1; G1 = 1; G4 = 1;
    A := 0 ;  L :=0 ;
    if (!R3) then  D with
     {
    SIPR = R1*R2*R3*R4 ;
    G3 = SIPG ;
    G2 = 1; G1 = 1; G4 = 1;
    A := 0 ;  L :=0 ;
     }
    else  S  with
     {
    SIPR = R1*R2*R3*R4 ;
    G3 = SIPG ;
    G2 = 1; G1 = 1; G4 = 1;
    A := 0 ;  L :=0 ;
     }
```

State E:

```
    SIPR = R1*R2*R3*R4 ;
    G4 = SIPG ;
    G2 = 1; G1 = 1; G3 = 1;
    A := 1 ;  L :=0 ;
    if (!R4) then  E with
     {
    SIPR = R1*R2*R3*R4 ;
    G4 = SIPG ;
    G2 = 1; G1 = 1; G3 = 1;
    A := 1 ;  L :=0 ;
     }
    else  S  with
     {
    SIPR = R1*R2*R3*R4 ;
    G4 = SIPG ;
    G2 = 1; G1 = 1; G3 = 1;
    A := 1 ;  L :=0 ;
     }
```

State F :
  goto K ;

State G :

goto K ;

```
test_vectors([clock,reset,R1,R2,R3,R4,SIPG]->[sreg,G1,G2,G3,G4,A,L,SIP])
            [ .c.  , 0 , 1 , 1,1 , 1, 1  ] ->[ K ,1  , 1 ,1 ,  1,0,0,   1 ];
            [ .c.  , 1 , 1 , 1,1 , 1, 1  ] ->[ S ,1  , 1 ,1 ,  1,1,1,   1 ];
            [ .c.  , 1 , 1 , 0,1 , 1, 1  ] ->[ C ,1  , 1 ,1 ,  1,1,1,   0 ];
            [ .c.  , 1 , 1 , 0,1 , 1, 1  ] ->[ C ,1  , 1 ,1 ,  1,0,1,   0 ];
            [ .c.  , 1 , 1 , 0,1 , 0, 0  ] ->[ C ,1  , 0 ,1 ,  1,0,1,   0 ];
            [ .c.  , 1 , 1 , 0,1 , 0, 0  ] ->[ C ,1  , 0 ,1 ,  1,0,1,   0 ];
            [ .c.  , 1 , 1 , 0,1 , 0, 0  ] ->[ C ,1  , 0 ,1 ,  1,0,1,   0 ];
            [ .c.  , 1 , 1 , 1,1 , 0, 0  ] ->[ S ,1  , 1 ,1 ,  1,0,1,   0 ];
            [ .c.  , 1 , 1 , 1,1 , 0, 0  ] ->[ E ,1  , 1 ,1 ,  0,0,1,   0 ];
            [ .c.  , 1 , 1 , 1,1 , 0, 0  ] ->[ E ,1  , 1 ,1 ,  0,1,0,   0 ];
            [ .c.  , 1 , 1 , 1,1 , 0, 0  ] ->[ E ,1  , 1 ,1 ,  0,1,0,   0 ];
            [ .c.  , 1 , 1 , 1,1 , 1, 0  ] ->[ S ,1  , 1 ,1 ,  1,1,0,   1 ];
            [ .c.  , 1 , 1 , 1,1 , 1, 1  ] ->[ S ,1  , 1 ,1 ,  1,1,0,   1 ];
            [ .c.  , 1 , 1 , 1,0 , 0, 1  ] ->[ D ,1  , 1 ,1 ,  1,1,0,   0 ];
            [ .c.  , 1 , 1 , 1,0 , 0, 1  ] ->[ D ,1  , 1 ,1 ,  1,0,0,   0 ];
            [ .c.  , 1 , 1 , 1,0 , 0, 0  ] ->[ D ,1  , 1 ,0 ,  1,0,0,   0 ];
end.
```

3.   Technical Support

STMicroelectronics is on the Internet with a World Wide Web (WWW) site on which product presentation, technical literature as well as product support information can be found.

A dedicated STPC section is available providing up to date hardware documentation and software tools.

The Web and e-mail addresses are:

> **WWW :** *http//www.st.com/products/support/stpc*
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