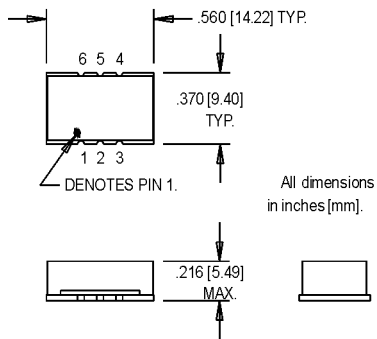


F17250B/F17350B & F17255B/F17355B Series

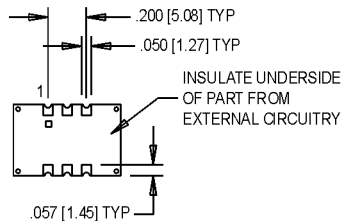
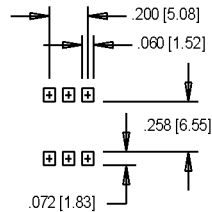
9x14 mm FR-4, 5.0 or 3.3 Volt, PECL, VCXO



- Former **Champion TECHNOLOGIES, INC.** Product
- Clock Recovery, PLL, Optic Transmission Equipment, Digital Cross Connect Equipment



SUGGESTED SOLDER PAD LAYOUT



Enable/Disable Control

Pin 1	Outputs	
	Pin 4	Pin 5
"0" Enables	Active	Active
"1" Disables	Low	High

Pin Connections

PIN	FUNCTION
1	Control Voltage
2	Enable/Disable
3	Vss/Ground
4	Output
5	Output
6	+Vcc

Ordering Information

Product Series	Logic	Temperature Range	RoHS Compliance	Frequency (customer specified)
2: 5.0 Volt 3: 3.3 Volt	0: PECL - 100E Logic 5: PECL - 10E Logic	Blank: 0°C to +70°C M: -40°C to +85°C	Blank: non-RoHS compliant part -R: RoHS compliant part	00.0000 MHz

PARAMETER	Symbol	Min.	Typ.	Max.	Units	Condition/Notes	
Frequency Range	F	75		180	MHz		
Operating Temperature	T _A	(See Ordering Information)					
Storage Temperature	T _s	-45		+125	°C		
Frequency Stability Overall	ΔF/F	Inclusive of Calibration, Temperature, Voltage, Load, and Aging					
0°C to +70°C				±30	ppm		
-40°C to +85°C				±50	ppm		
Aging 1st Year		-4		+4	ppm		
10 Year		-10		+10	ppm		
Pullability/APR		±80 ±60		±140 ±140	ppm ppm	75 to 156 MHz 156.1 to 180 MHz	
Control Voltage	V _c	0.5 0.3	2.5 1.65	4.5 3.0	V V	F17250B & F17255B F17350B & F17355B	
Linearity				10	%	Positive Monotonic Slope	
Modulation Bandwidth	f _m	10			kHz	±3dB	
Input Impedance	Z _{in}	50k			Ohms	@ 10 kHz	
Input Voltage	V _{cc}	4.75 3.135	5.0 3.3	5.25 3.465	V V	F17250B & F17255B F17350B & F17355B	
Input Current	I _{cc}			70	mA		
Output Type						PECL	
Load						See Note 1	
Symmetry (Duty Cycle)		45		55	%	V _{cc} -1.3 VDC	
Output Skew				50	ps		
Logic "1" Level	V _{oh}	V _{cc} -1.1		V _{cc} -0.88	V	50Ω into V _{cc} -2	
Logic "0" Level	V _{ol}	V _{cc} -1.95		V _{cc} -1.55	V	50Ω into V _{cc} -2	
Rise Time	T _r			450	ps	50Ω into 20% to 80%	
Fall Time	T _f			450	ps	50Ω into 80% to 20%	
Enable Function		PECL low: output active PECL high: output disables					
Start up Time				10	ms		
Phase Jitter @ 155.52 MHz	φ _J			1	ps RMS	Integrated 12 kHz - 20 MHz	
Phase Noise (Typical) @ 155.52 MHz		10 Hz -40	100 Hz -70	1 kHz -100	10 kHz -120	100 kHz -140	Offset from carrier dBc/Hz

1. PECL load - see load circuit diagram #5

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Please see www.mtronpti.com for our complete offering and detailed datasheets. Contact us for your application specific requirements: MtronPTI 1-800-762-8800.