NEC

MOS INTEGRATED CIRCUIT

MC-2311100

MCP (MULTI-CHIP PACKAGE) MOBILE SPECIFIED RAM AND SRAM
16M-BIT CMOS MOBILE SPECIFIED RAM AND 4M-BIT CMOS SRAM

Description

The MC-2311100 is a stacked type MCP (Multi-Chip Package) of 16,777,216 bits (1,048,576 words by 16 bits) Mobile specified RAM and 4,194,304 bits (BYTE mode : 524,288 words by 8 bits, WORD mode : 262,144 words by 16 bits) SRAM.

The MC-2311100 is packaged in a 61-pin TAPE FBGA.

General Features

- Supply voltage : $V_{CC}m$ / $V_{CC}s$ = 2.6 to 3.0 V
- Wide operating temperature : T_A = –20 to +70 °C
- Output Enable input for easy application
- Byte data control : /LB (I/O0 to I/O7), /UB (I/O8 to I/O15)

Mobile specified RAM Features

- Memory organization : 1,048,576 words by 16 bits
- Fast access time : t_{AA} = 80, 90, 100 ns (MAX.)
- Supply current : At operating : 35 mA (MAX.)
  At Standby Mode 1 : 100 μA (MAX.) Normal standby (Memory cell data hold valid)
  At Standby Mode 2 : 10 μA (MAX.) Memory cell data hold invalid
- Chip Enable inputs : /CEm
- Standby Mode input : MODE

SRAM Features

- Memory organization : 524,288 words × 8 bits (BYTE mode)
  262,144 words × 16 bits (WORD mode)
- Fast access time : t_{AA} = 70 ns (MAX.)
- Supply current : At operating : 40 mA (MAX.)
  At Standby Mode : 7 μA (MAX.)
- Low V_{CC} data retention: 1.0 V (MIN.)
- Two Chip Enable inputs: /CE1s, CE2s

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Ordering Information

Part number	Access time ns (MAX.)		Package
	Mobile specified RAM	SRAM	
MC-2311100F9-B80-BQ1	80	70	61-pin TAPE FBGA (9 × 7)
MC-2311100F9-B90-BQ1[Note]	90	70	
MC-2311100F9-B10-BQ1	100	70	

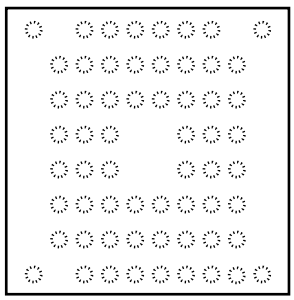
Note Under development

Pin Configuration

/xxx indicates active low signal.

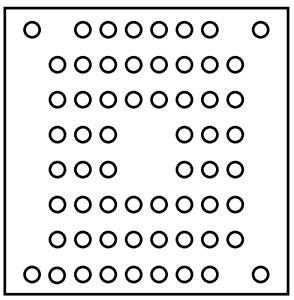
61-pin TAPE FBGA (9 × 7)

Top View



A B C D E F G H J K

Bottom View



8 7 6 5 4 3 2 1

K J H G F E D C B A

Top View

	A	B	C	D	E	F	G	H	J	K
8	NC		A15	NC	V_{SS}	A16	NC	V_{SS}		NC
7		A11	A12	A13	A14	SA	I/O15	I/O7	I/O14	
6		A8	A19	A9	A10	I/O6	I/O13	I/O12	I/O5	
5		/WE	MODE	NC			I/O4	V_{CC}m	CIOs	
4		NC	CE2	NC			I/O3	V_{CC}s	I/O11	
3		/LB	/UB	A18	A17	I/O1	I/O9	I/O10	I/O2	
2		A7	A6	A5	A4	V_{SS}	/OE	I/O0	I/O8	
1	NC		A3	A2	A1	A0	/CE1s	/CEm	NC	NC

Common Pins

A0 - A19 : Address inputs
I/O0 - I/O15 : Data inputs / outputs
/OE : Output Enable
/WE : Write Enable
/LB, /UB : Byte data select
V_{SS} : Ground
NC [Note] : No Connection

Mobile specified RAM Pins

/CEm : Chip Enable
MODE : Standby mode select
V_{CC}m : Supply Voltage

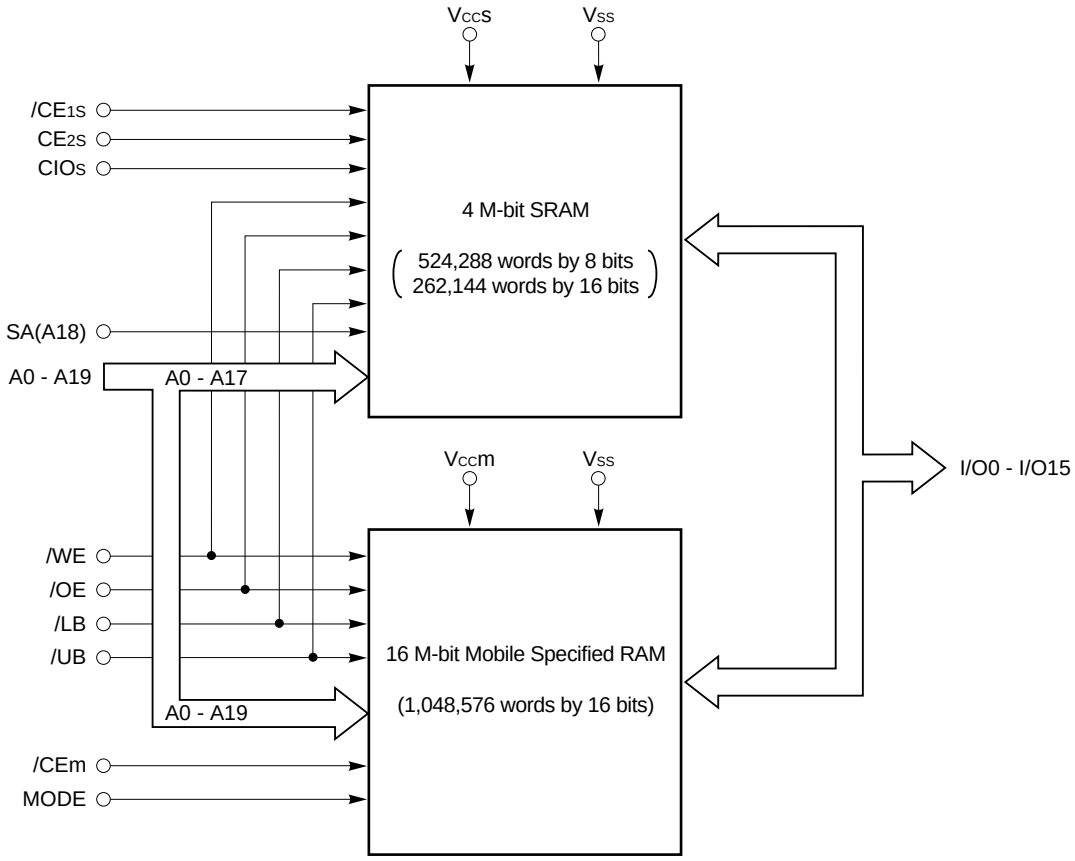
SRAM Pins

/CE1s : Chip Enable
CE2s : Chip Enable
SA : Address input (A18)
CIOs : Selects 8-bit or 16-bit mode
V_{CC}s : Supply Voltage

Note Some signals can be applied because this pin is not internally connected.

Remark Refer to **5. Package Drawing** for the index mark.

Block Diagram



CONTENTS

1. Bus Operations

Table 1-1. Bus Operations

Operation		Mobile specified RAM		SRAM			Common					
		/CS	MODE	/CE1	CE2	CIOs	/OE	/WE	/LB	/UB	I/O0 to I/O7	I/O8 to I/O15
Full standby	Standby Mode1	H	H	H	x	x	x	x	x	x	Hi-Z	Hi-Z
				x	L							
	Standby Mode2		L	H	x							
				x	L							
Output disable		L	H	L	H	x	H	H	x	x		

Mobile specified RAM		/CS	MODE	/CE1	CE2	CIOs	/OE	/WE	/LB	/UB	I/O0 to I/O7	I/O8 to I/O15
WORD Read	(1M x 16)	L	H	**Note1**		x	L	H	L	L	D_{OUT}	D_{OUT}
	Lower byte read								L	H	D_{OUT}	Hi-Z
	Upper byte read								H	L	Hi-Z	DOUT
Output disable									H	H	Hi-Z	Hi-Z
WORD Write	(1M x 16)						x	L	L	L	D_{IN}	D_{IN}
	Lower byte write								L	H	D_{IN}	Hi-Z
	Upper byte write								H	L	Hi-Z	D_{IN}
Write impossible									H	H	Hi-Z	Hi-Z

SRAM		/CS	MODE	/CE1	CE2	CIOs	/OE	/WE	/LB	/UB	I/O0 to I/O7	I/O8 to I/O15
BYTE Read	(512K x 8)	**Note2**		L	H	L	L	H	L	L	D_{OUT}	Hi-Z
WORD Read	(256K x 16)					H			L	L	D_{OUT}	D_{OUT}
	Lower byte read								L	H	D_{OUT}	Hi-Z
	Upper byte read								H	L	Hi-Z	D_{OUT}
Output disable		L	H	x	x	x	x	x	H	H	Hi-Z	Hi-Z
BYTE Write	(512K x 8)	**Note2**		L	H	L	x	L	L	L	D_{IN}	Hi-Z
WORD Write	(256K x 16)					H			L	L	D_{IN}	D_{IN}
	Lower byte write								L	H	D_{IN}	Hi-Z
	Upper byte write								H	L	Hi-Z	D_{IN}

Caution Other operations except for indicated in this table are inhibited.

Notes 1. SRAM should be Standby.

2. Mobile specified RAM should be Standby.

Remarks 1. H : V_{IH}, L : V_{IL}, × : V_{IH} or V_{IL}

2. MODE pin must be fixed to H during active operation.

2. Mobile specified RAM

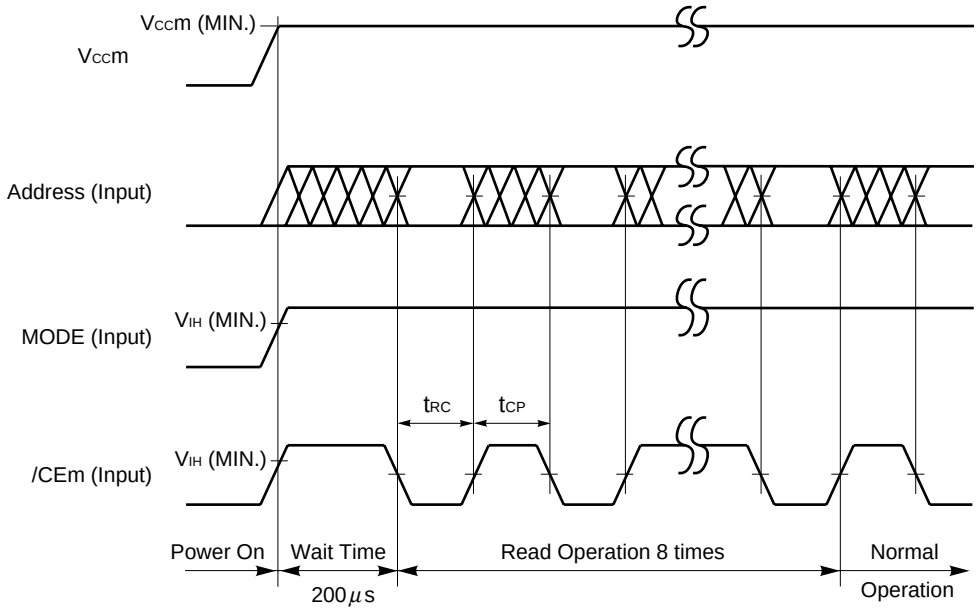
2.1 Initialization

The MC-2311100 is initialized in the power-on sequence according to the following.

(1) To stabilize internal circuits, before turning on the power, a 200 μs or longer wait time must precede any signal toggling.

(2) After the wait time, read operation must be performed at least 8 times. After that, it can be normal operation.

Figure 2-1. Initialization Timing Chart



Cautions 1. Following power application, make MODE and /CEm high level during the wait time interval.

2. Following power application, make MODE high level during the wait time and eight read operations.

3. The read operation must satisfy the specs described on page 14 (Read Cycle (Mobile specified RAM)).

4. The address is don't care (V_{IH} or V_{IL}) during read operation.

5. Read operation must be executed with toggled the /CEm pin.

6. To prevent bus contention, it is recommended to set /OE to high level. However, do not input data to the I/O pins if /OE is low level during a read operation.

2.2 Standby Mode

Standby Mode 1 and Standby Mode 2 differ as shown below.

Table 2-1. Standby Mode Characteristics

Standby Mode	Memory Cell Data Hold	Standby Supply Current (μA)
Mode 1	Valid	100 (I_{SB1})
Mode 2	Invalid	10 (I_{SB2})

2.2.1 Standby Mode State Machine

(1) From Active

To shift from this state to Standby Mode 1, change /CEm from V_{IL} to V_{IH}.

To shift from this state to Standby Mode 2, change /CEm from V_{IL} to V_{IH} and change MODE from V_{IH} to V_{IL}.

(2) From Standby Mode 1

To shift from this state to Active, change /CEm from V_{IH} to V_{IL}.

To shift from this state to Standby Mode 2, change MODE from V_{IH} to V_{IL}.

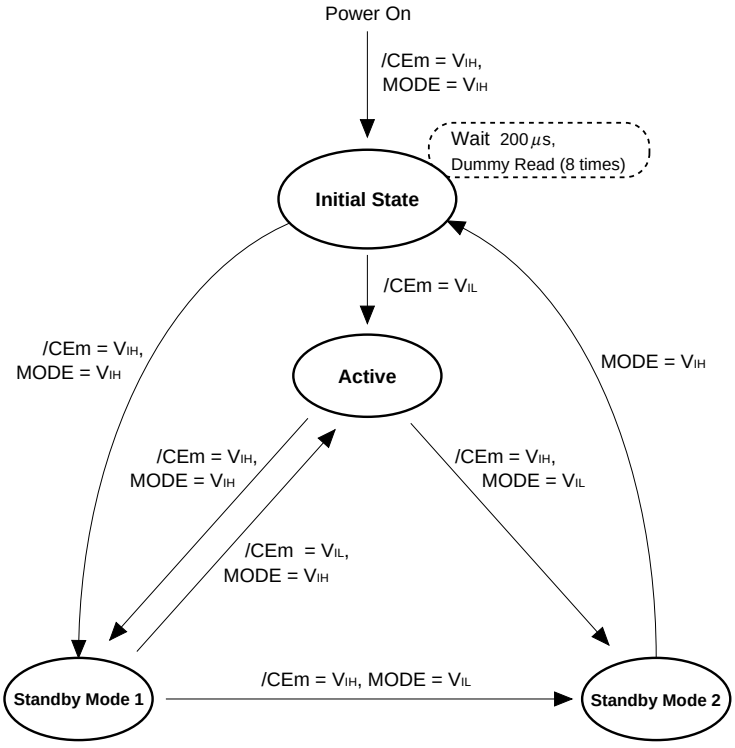
(3) From Standby Mode 2

When shifting from this state to the Active state or to Standby Mode 1, it is necessary to set MODE to V_{IH} and perform a Dummy Read operation 8 times after waiting for 200 μs, in the same way as at power application. Refer to **Figure 4-16. Standby Mode 2 entry and recovery Timing Chart (Mobile specified RAM)**.

After shifting to Active state, change /CEm to V_{IL}.

After shifting to Standby Mode 1, do not change either MODE or /CEm.

Figure 2-2. Standby Mode State Machine



3. Electrical Specifications

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Supply voltage	$V_{CC}m$	with respect to V_{SS}	–0.5 Note to +4.0	V
	$V_{CC}s$	with respect to V_{SS}	–0.5 to +4.0	
Input / Output voltage	V_T	with respect to V_{SS}	–0.5 Note to $V_{CC}m$, $V_{CC}s$ + 0.4 (4.0 V MAX.)	V
Ambient operation temperature	T_A		–20 to +70	°C
Storage temperature	T_{stg}		–55 to +125	°C

Note –1.0 V (MIN.) (Pulse width ≤ 30 ns)

Caution Exposing the device to stress above those listed in Absolute Maximum Rating could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Common

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Supply voltage	$V_{CC}m$, $V_{CC}s$		2.6		3.0	V
Ambient operation temperature	T_A		–20		+70	°C

Mobile specified RAM

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
High level input voltage	V_{IH}		$V_{CC}m$ x 0.8		$V_{CC}m$ + 0.3	V
Low level input voltage	V_{IL}		–0.3 Note		$V_{CC}m$ x 0.2	V

Note –0.5 V (MIN.) (Pulse width ≤ 30 ns)

SRAM

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
High level input voltage	V_{IH}		2.4		$V_{CC}s$ + 0.4	V
Low level input voltage	V_{IL}		–0.3 Note		+0.5	V

Note –0.5 V (MIN.) (Pulse width ≤ 30 ns)

Capacitance (T_A = 25 °C, f = 1 MHz)

Parameter	Symbol	Test condition	MIN.	TYP.	MAX.	Unit
Input capacitance	C_{IN}	V_{IN} = 0 V			TBD	pF
Output capacitance	C_{OUT}	V_{OUT} = 0 V			TBD	pF

Remarks 1. V_{IN} : Input voltage, V_{OUT} : Output voltage

2. These parameters are not 100% tested.

DC Characteristics (Recommended Operating Conditions Unless Otherwise Noted)

Mobile specified RAM

Parameter		Symbol	Test condition	MIN.	TYP.	MAX.	Unit
Input leakage current		I_{LI}	V_{IN} = 0 V to V_{CC}m	–1.0		+1.0	μA
I/O leakage current		I_{LO}	$V_{I/O}$ = 0 V to V_{CC}m, /CEm = V_{IH} or /WE = V_{IL} or /OE = V_{IH}	–1.0		+1.0	μA
Operating supply current		I_{CCA}	/CEm = V_{IL}, Minimum cycle time, $I_{I/O}$ = 0 mA			35	mA
Standby supply current	Standby Mode 1	I_{SB1}	/CEm ≥ V_{CC}m – 0.2 V, MODE ≥ V_{CC}m – 0.2 V			100	μA
	Standby Mode 2	I_{SB2}	/CEm ≥ V_{CC}m – 0.2 V, MODE ≤ 0.2 V			10	
High level output voltage		V_{OH}	I_{OH} = –0.5 mA	V_{CC}m × 0.8			V
Low level output voltage		V_{OL}	I_{OL} = 1 mA			V_{CC}m × 0.2	V

SRAM

Parameter	Symbol	Test condition	MIN.	TYP.	MAX.	Unit
Input leakage current	I_{LI}	V_{IN} = 0 V to V_{CC}s	–1.0		+1.0	μA
I/O leakage current	I_{LO}	$V_{I/O}$ = 0 V to V_{CC}s, /CE1s = V_{IH} or CE2s = V_{IL} or /WE = V_{IL} or /OE = V_{IH}	–1.0		+1.0	μA
Operating supply current	I_{CCA1}	/CE1s = V_{IL}, CE2s = V_{IH}, $I_{I/O}$ = 0 mA, Minimum cycle time		–	40	mA
	I_{CCA2}	/CE1s = V_{IL}, CE2s = V_{IH}, $I_{I/O}$ = 0 mA, Cycle time = ∞		–	10	
	I_{CCA3}	/CE1s ≤ 0.2 V, CE2s ≥ V_{CC}s – 0.2 V, $I_{I/O}$ = 0 mA, Cycle time = 1 μs V_{IH} ≥ V_{CC}s – 0.2 V, V_{IL} ≤ 0.2 V		–	8	
Standby supply current	I_{SB}	/CE1s = V_{IH} or CE2s = V_{IL} or /LB = /UB = V_{IH}		–	0.6	mA
	I_{SB1}	/CE1s ≥ V_{CC}s – 0.2 V, CE2s ≥ V_{CC}s – 0.2 V		0.5	7	μA
	I_{SB2}	CE2s ≤ 0.2 V		0.5	7	
	I_{SB3}	/LB = /UB ≥ V_{CC}s – 0.2 V, /CE1s ≤ 0.2 V, CE2s ≥ V_{CC}s – 0.2 V		0.5	7	
High level output voltage	V_{OH}	I_{OH} = –0.5 mA	2.4			V
Low level output voltage	V_{OL}	I_{OL} = 1.0 mA			0.4	V

Remarks 1. V_{IN} : Input voltage

$V_{I/O}$: Input / Output voltage

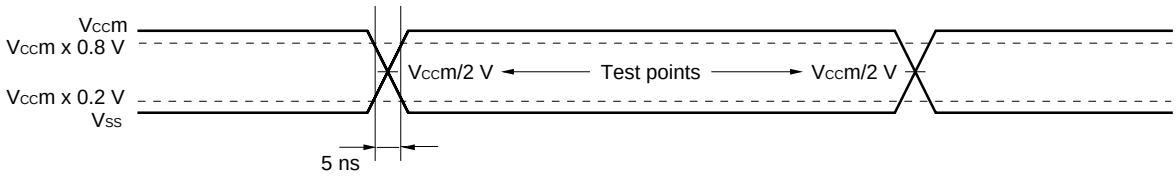
2. These DC characteristics are in common regardless products classification.

AC Characteristics (Recommended Operating Conditions Unless Otherwise Noted)

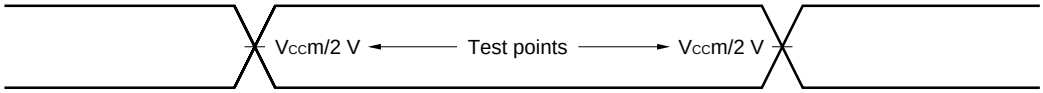
AC Test Conditions

Mobile specified RAM

Input Waveform (Rise and Fall Time ≤ 5 ns)



Output Waveform

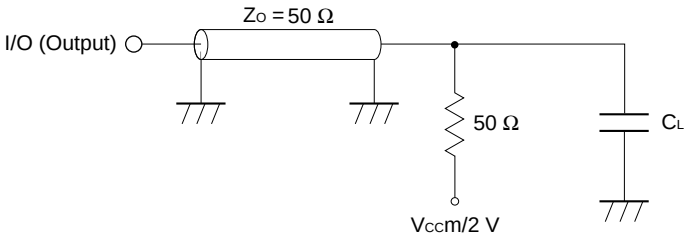


Output Load

AC characteristics directed with the note should be measured with the output load shown in Figure.

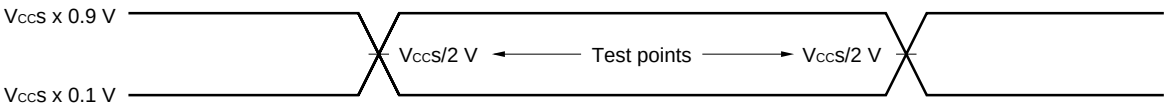
C_L: 50 pF

5 pF (t_{CLZ}, t_{OLZ}, t_{BLZ}, t_{CHZ}, t_{OHZ}, t_{BHZ}, t_{WHZ}, t_{OW})

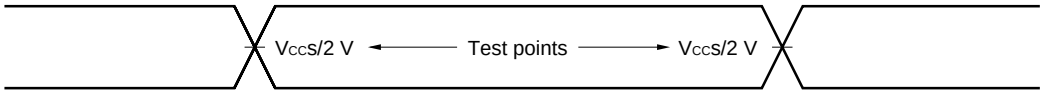


SRAM

Input Waveform (Rise and Fall Time ≤ 5 ns)



Output Waveform



Output Load

1 TTL + 50 pF

/CEm, /CEs Timing

Parameter	Symbol	Test Condition	MIN.	TYP.	MAX.	Unit	Note
/CEm, /CEs recover time	t_{CCR}		0			ns	

Read Cycle (Mobile specified RAM)

Parameter	Symbol	MC-2311100-B80		MC-2311100-B90		MC-2311100-B10		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Read cycle time	t_{RC}	80	10,000	90	10,000	110	10,000	ns	1
Identical address read cycle time	t_{RC1}	80	10,000	90	10,000	110	10,000	ns	2
Address skew time	t_{SKEW}		10		15		20	ns	3
/CEm pulse width	t_{CP}	10		10		10		ns	
Address access time	t_{AA}		80		90		100	ns	4
/CEm access time	t_{ACS}		80		90		100	ns	
/OE to output valid	t_{OE}		35		40		50	ns	5
/LB, /UB to output valid	t_{BA}		35		40		50	ns	
Output hold from address change	t_{OH}	10		10		10		ns	
/CEm to output in low impedance	t_{CLZ}	10		10		10		ns	
/OE to output in low impedance	t_{OLZ}	5		5		5		ns	
/LB, /UB to output in low impedance	t_{BLZ}	5		5		5		ns	
/CEm to output in high impedance	t_{CHZ}		25		25		25	ns	
/OE to output in high impedance	t_{OHZ}		25		25		25	ns	
/LB, /UB to output in high impedance	t_{BHZ}		25		25		25	ns	

Notes 1. One read cycle (t_{RC}) must satisfy the minimum value ($t_{RC(MIN.)}$) and maximum value ($t_{RC(MAX.)}$ = 10 μs). t_{RC} indicates the time from the /CEm low level input point or address determination point, whichever is later, to the /CEm high level input point or the next address change start point, whichever is earlier. As a result, there are the following four conditions for t_{RC}.

1) Time from address determination point to /CEm high level input point (address access)
2) Time from address determination point to next address change start point (address access)
3) Time from /CEm low level input point to next address change start point (/CEm access)
4) Time from /CEm low level input point to /CEm high level input point (/CEm access)

2. The identical address read cycle time (t_{RC1}) is the cycle time of one read operation when performing continuous read operations toggling /OE , /LB, and /UB with the address fixed and /CEm low level. Perform settings so that the sum (t_{RC}) of the identical address read cycle times (t_{RC1}) is 10 μs or less.

3. t_{SKEW} indicates the following three types of time depending on the condition.

1) When switching /CEm from high level to low level, t_{SKEW} is the time from the /CEm low level input point until the next address is determined.
2) When switching /CEm from low level to high level, t_{SKEW} is the time from the address change start point to the /CEm high level input point.
3) When /CEm is fixed to low level, t_{SKEW} is the time from the address change start point until the next address is determined.

Since specs are defined for t_{SKEW} only when /CEm is active, t_{SKEW} is not subject to limitations when /CEm is switched from high level to low level following address determination, or when the address is changed after /CEm is switched from low level to high level.

4. Regarding t_{AA} and t_{ACS}, only t_{AA} is satisfied during address access (refer to 1) and 2) of **Note 1**), and only t_{ACS} is satisfied during /CEm access (refer to 3) of **Note 1**).

5. Regarding t_{BA} and t_{OE}, only t_{BA} is satisfied if /OE becomes active later than /UB and /LB, and only t_{OE} is satisfied if /UB and /LB become active before /OE.

Write Cycle (Mobile specified RAM)

Parameter	Symbol	MC-2311100-B80		MC-2311100-B90		MC-2311100-B10		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Write cycle time	t_{WC}	80	10,000	90	10,000	110	10,000	ns	1
Identical address write cycle time	t_{WC1}	80	10,000	90	10,000	110	10,000	ns	2
Address skew time	t_{SKEW}		10		15		20	ns	3
/CEm to end of write	t_{CW}	40		50		60		ns	4
/LB, /UB to end of write	t_{BW}	30		35		40		ns	
Address valid to end of write	t_{AW}	35		45		55		ns	
Write pulse width	t_{WP}	30		35		40		ns	
Write recovery time	t_{WR}	20		20		20		ns	5
/CEm pulse width	t_{CP}	10		10		10		ns	
Address setup time	t_{AS}	0		0		0		ns	
Byte write hold time	t_{BWH}	20		20		20		ns	
Data valid to end of write	t_{DW}	20		25		30		ns	
Data hold time	t_{DH}	0		0		0		ns	
/OE to output in low impedance	t_{OLZ}	5		5		5		ns	
/WE to output in high impedance	t_{WHZ}		25		25		25	ns	
/OE to output in high impedance	t_{OHZ}		25		25		25	ns	
Output active from end of write	t_{OW}	5		5		5		ns	

Notes 1. One write cycle (t_{WC}) must satisfy the minimum value ($t_{WC(MIN.)}$) and the maximum value ($t_{WC(MAX.)}$ = 10 μs). t_{WC} indicates the time from the /CEm low level input point or address determination point, whichever is after, to the /CEm high level input point or the next address change start point, whichever is earlier. As a result, there are the following four conditions for t_{WC}.

1) Time from address determination point to /CEm high level input point
2) Time from address determination point to next address change start point
3) Time from /CEm low level input point to next address change start point
4) Time from /CEm low level input point to /CEm high level input point

2. The identical address read cycle time (t_{WC1}) is the cycle time of one write cycle when performing continuous write operations with the address fixed and /CEm low level, changing /LB and /UB at the same time, and toggling /WE, as well as when performing a continuous write toggling /LB and /UB. Make settings so that the sum (t_{WC}) of the identical address write cycle times (t_{WC1}) is 10 μs or less.

3. t_{SKEW} indicates the following three types of time depending on the condition.

1) When switching /CEm from high level to low level, t_{SKEW} is the time from the /CEm low level input point until the next address is determined.
2) When switching /CEm from low level to high level, t_{SKEW} is the time from the address change start point to the /CEm high level input point.
3) When /CEm is fixed to low level, t_{SKEW} is the time from the address change start point until the next address is determined.

Since specs are defined for t_{SKEW} only when /CEm is active, t_{SKEW} is not subject to limitations when /CEm is switched from high level to low level following address determination, or when the address is changed after /CEm is switched from low level to high level.

4. Definition of write start and write end

	/CEm	/WE	/LB, /UB	Status
Write start pattern 1	H to L	L	L	If /WE, /LB, /UB are low level, time when /CEm changes from high level to low level
Write start pattern 2	L	H to L	L	If /CEm, /LB, /UB are low level, time when /WE changes from high level to low level
Write start pattern 3	L	L	H to L	If /CEm, /WE are low level, time when /LB or /UB changes from high level to low level
Write end pattern 1	L	L to H	L	If /CEm, /WE, /LB, /UB are low level, time when /WE changes from low level to high level
Write end pattern 2	L	L	L to H	When /CEm, /WE, /LB, /UB are low level, time when /LB or /UB changes from low level to high level

5. Definition of write end recovery time (t_{WR})

1) Time from write end to address change start point, or from write end to /CEm high level input point
2) When /CEm, /LB, /UB are low level and continuously written to the identical address, time from /WE high level input point to /WE low level input point
3) When /CEm, /WE are low level and continuously written to the identical address, time from /LB or /UB high level input point, whichever is later, to /LB or /UB low level input point, whichever is earlier.
4) When /CEm is low level and continuously written to the identical address, time from write end to point at which /WE , /LB, or /UB starts to change from high level to low level, whichever is earliest.

Read Write Cycle (Mobile specified RAM)

Parameter	Symbol	MC-2311100-B80		MC-2311100-B90		MC-2311100-B10		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Read write cycle time	t_{RWC}		10,000		10,000		10,000	ns	1, 2
Byte write setup time	t_{BWS}	20		20		20		ns	
Byte read setup time	t_{BRS}	20		20		20		ns	

Notes 1. Make settings so that the sum (t_{RWC}) of the identical address read cycle time (t_{RC1}) and the identical address write cycle time (t_{WC1}) is 10 μs or less when a write is performed at the identical address using /UB following a read using /LB with /CEm low level, or when a write is performed using /LB following a read using /UB.

2. Make settings so that the sum (t_{RWC}) of the identical address read cycle time (t_{RC1}) and the identical address write cycle time (t_{WC1}) is 10 μs or less when a read is performed at the identical address using /UB following a write using /LB with /CEm low level, or when a read is performed using /LB following a write using /UB.

Read Cycle (SRAM)

Parameter	Symbol	MC-2311100-B80, B90, B10		Unit	Notes
		MIN.	MAX.		
Read cycle time	t_{RC}	70		ns	
Address access time	t_{AA}		70	ns	1
/CE1s access time	t_{CO1}		70	ns	
CE2s access time	t_{CO2}		70	ns	
/OE to output valid	t_{OE}		35	ns	
/LB, /UB to output valid	t_{BA}		70	ns	
Output hold from address change	t_{OH}	10		ns	
/CE1s to output in low impedance	t_{LZ1}	10		ns	2
CE2s to output in low impedance	t_{LZ2}	10		ns	
/OE to output in low impedance	t_{OLZ}	0		ns	
/LB, /UB to output in low impedance	t_{BLZ}	10		ns	
/CE1s to output in high impedance	t_{HZ1}		25	ns	
CE2s to output in high impedance	t_{HZ2}		25	ns	
/OE to output in high impedance	t_{OHZ}		25	ns	
/LB, /UB to output in high impedance	t_{BHZ}		25	ns	

Notes 1. The output load is 1TTL + 50 pF.

2. The output load is 1TTL + 5 pF.

Write Cycle (SRAM)

Parameter	Symbol	MC-2311100-B80, B90, B10		Unit	Note
		MIN.	MAX.		
Write cycle time	t_{WC}	70		ns	
/CE1s to end of write	t_{CW1}	55		ns	
CE2s to end of write	t_{CW2}	55		ns	
/LB, /UB to end of write	t_{BW}	55		ns	
Address valid to end of write	t_{AW}	55		ns	
Address setup time	t_{AS}	0		ns	
Write pulse width	t_{WP}	50		ns	
Write recovery time	t_{WR}	0		ns	
Data valid to end of write	t_{DW}	30		ns	
Data hold time	t_{DH}	0		ns	
/WE to output in high impedance	t_{WHZ}		25	ns	1
Output active from end of write	t_{OW}	5		ns	

Note 1. The output load is 1TTL + 50 pF.

Low V_{CC} Data Retention Characteristics (T_A = –20 to +70°C)

Parameter	Symbol	Test Condition	MC-2311100-B80, B90, B10			Unit
			MIN.	TYP.	MAX.	
Data retention supply voltage	V_{CCDR1}	/CE1s ≥ V_{CC}s – 0.2 V,CE2s ≥ V_{CC}s – 0.2 V	1.0		3.6	V
	V_{CCDR2}	CE2s ≤ 0.2 V	1.0		3.6	
	V_{CCDR3}	/LB = /UB ≥ V_{CC}s – 0.2 V, /CE1s ≤ 0.2 V, CE2s ≥ V_{CC}s – 0.2 V	1.0		3.6	
Data retention supply current	I_{CCDR1}	V_{CC}s = 1.5 V, /CE1s ≥ V_{CC}s – 0.2 V, CE2s ≥ V_{CC}s – 0.2 V or CE2s ≤ 0.2 V		0.3	3.0	μA
	I_{CCDR2}	V_{CC}s = 1.5 V, CE2s ≤ 0.2 V		0.3	3.0	
	I_{CCDR3}	V_{CC}s = 1.5 V, /LB = /UB ≥ V_{CC}s – 0.2 V, /CE1s ≤ 0.2 V, CE2s ≥ V_{CC}s – 0.2 V		0.3	3.0	
Chip deselection to data retention mode	t_{CDR}		0			ns
Operation recovery time	t_R		t_{RC}[Note]			ns

Note t_{RC} : Read cycle time

4. Timing Charts

Figure 4-1. Alternating Mobile specified RAM to SRAM Timing Chart

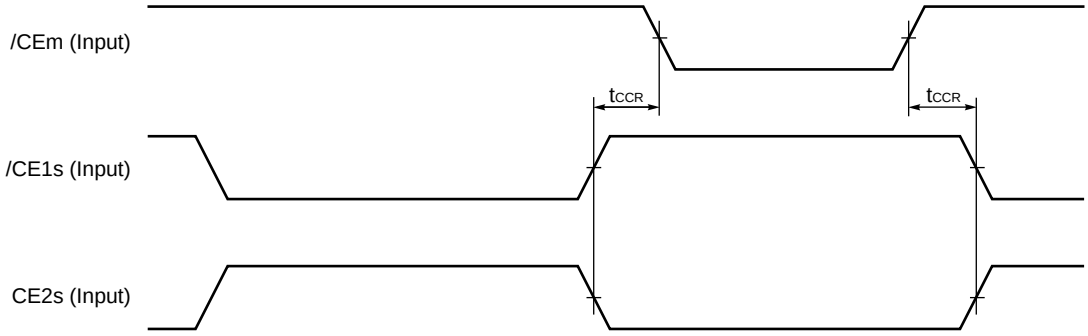
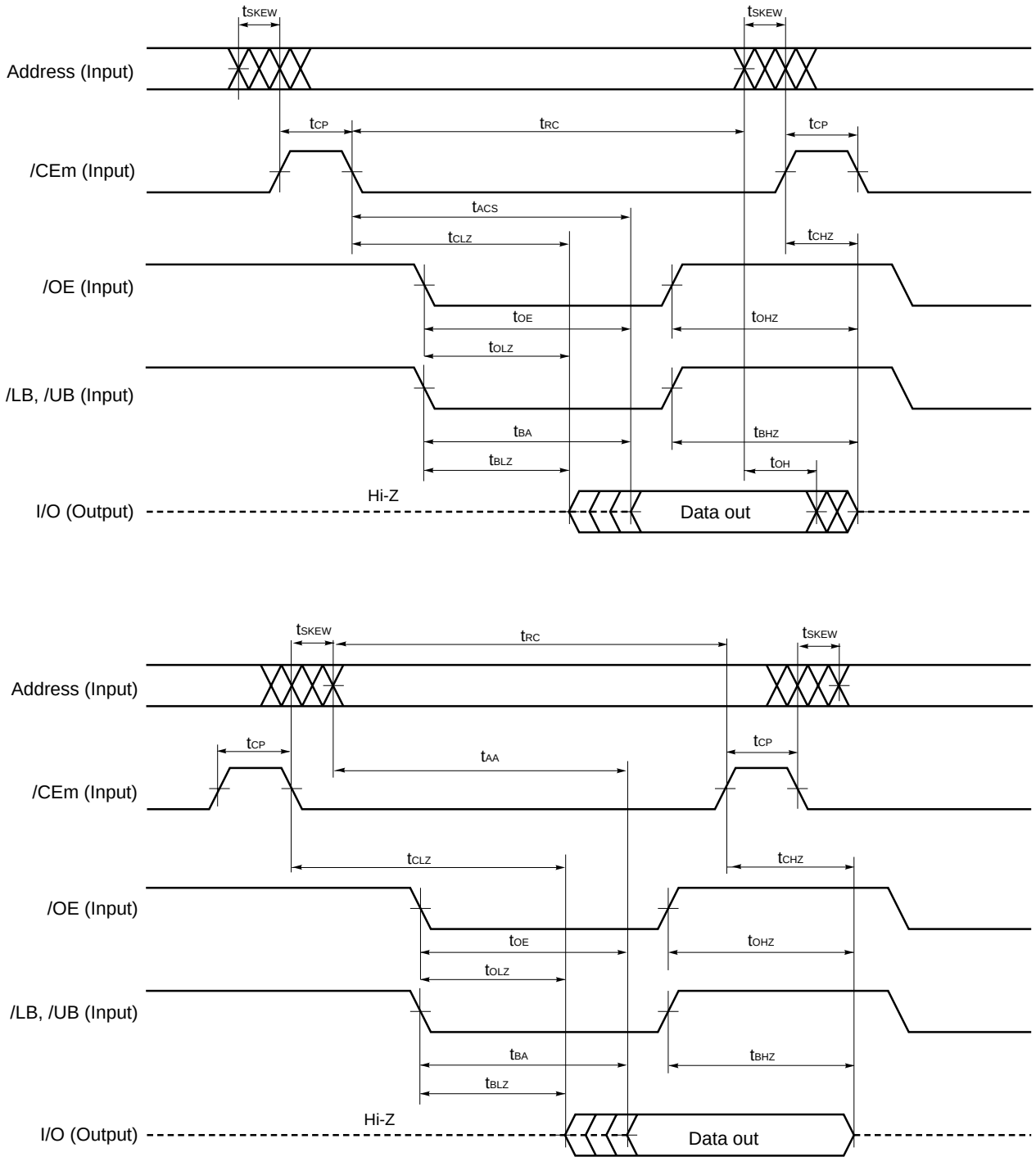


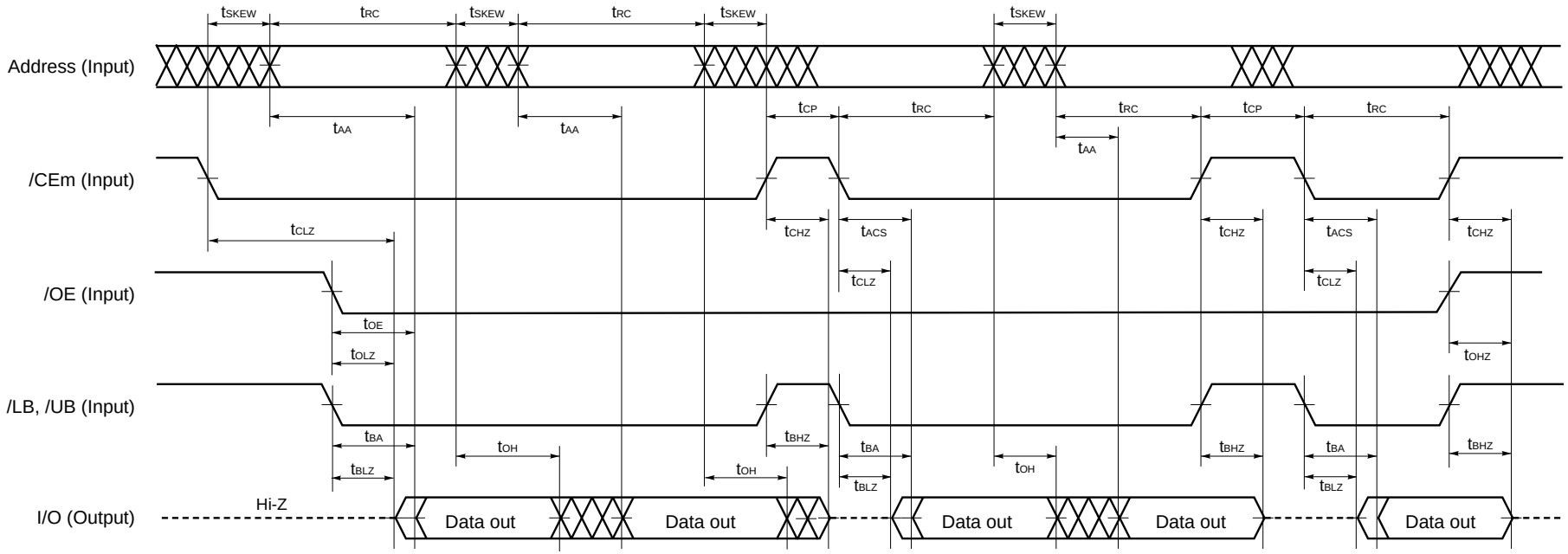
Figure 4-2. Read Cycle Timing Chart 1 (Mobile specified RAM)



Caution If the address is changed using a value that is either lower than the minimum value or higher than the maximum value for the read cycle time (t_{RC}), none of the data can be guaranteed.

Remark In read cycle, /WE should be fixed to High.

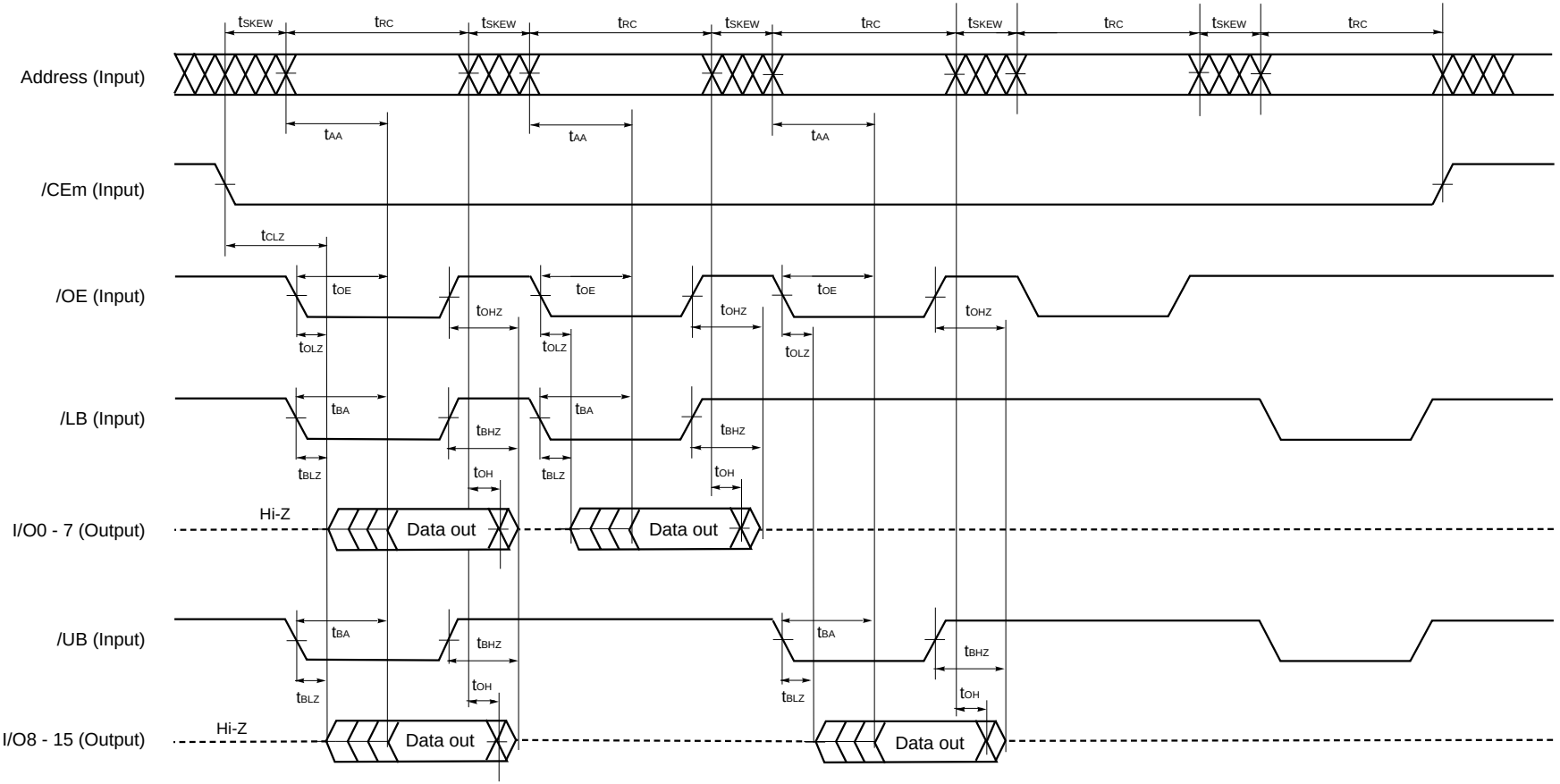
Figure 4-3 Read Cycle Timing Chart 2 (Mobile specified RAM)



Caution If the address is changed using a value that is either lower than the minimum value or higher than the maximum value for the read cycle time (t_{RC}), none of the data can be guaranteed.

Remark In read cycle, /WE should be fixed to High.

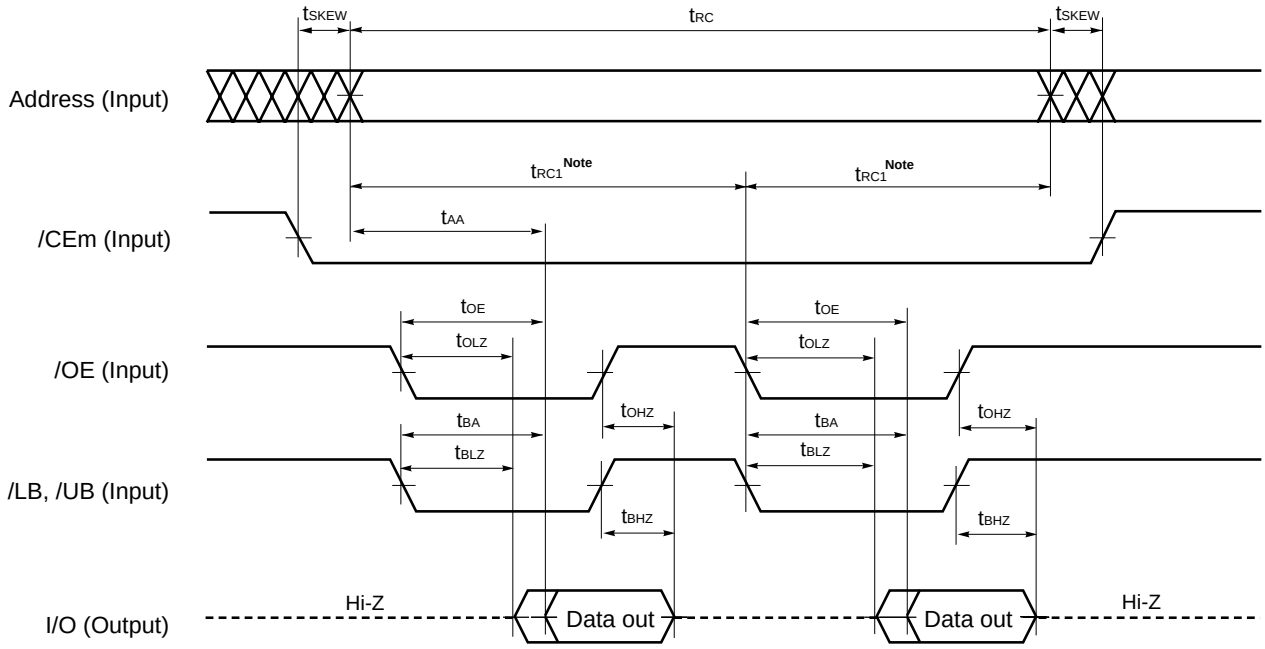
Figure 4-4. Read Cycle Timing Chart 3 (Mobile specified RAM)



Caution If the address is changed using a value that is either lower than the minimum value or higher than the maximum value for the read cycle time (t_{RC}), none of the data can be guaranteed.

Remark In read cycle, /WE should be fixed to High.

Figure 4-5. Read Cycle Timing Chart 4 (Mobile specified RAM)

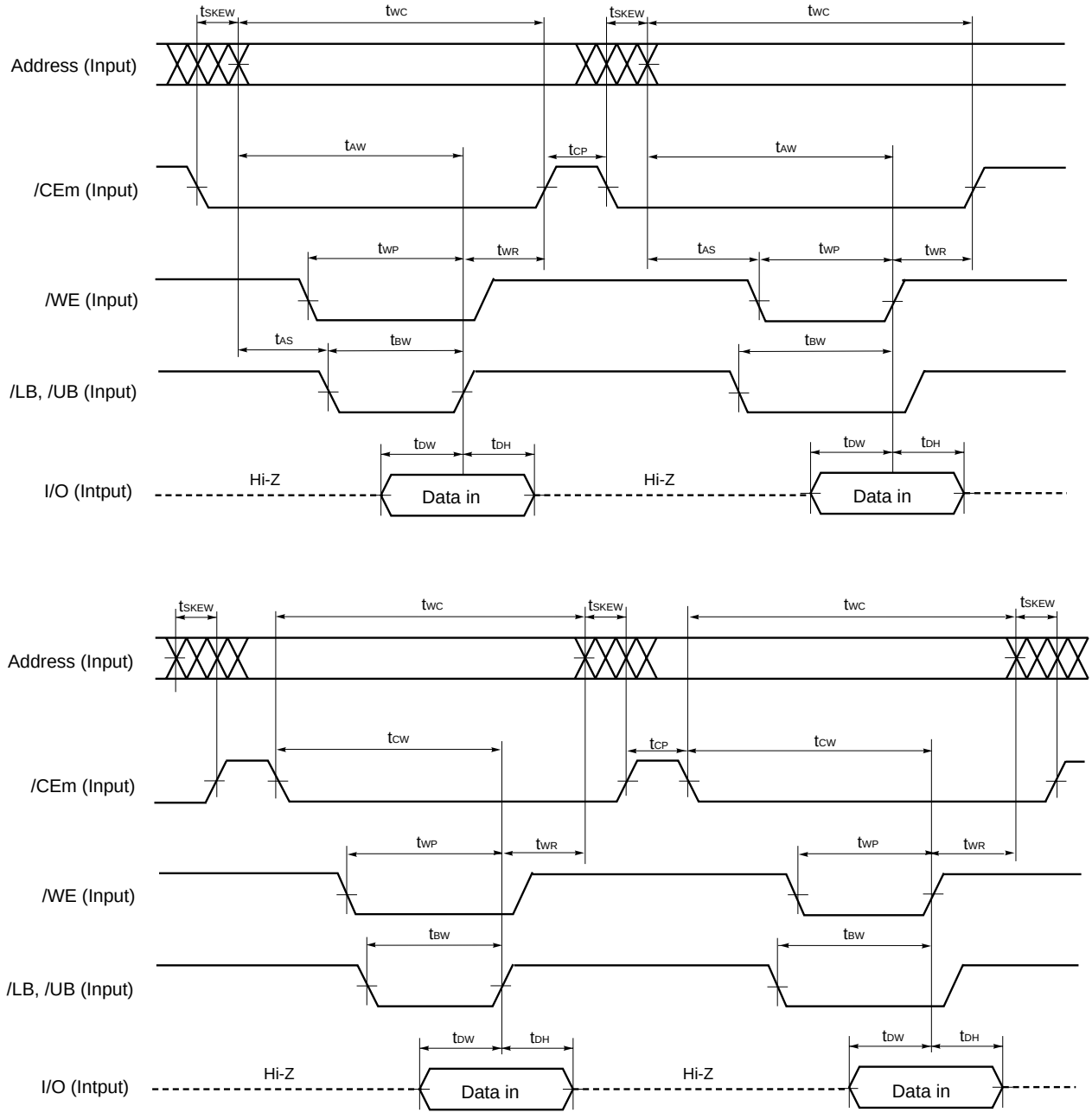


Caution If the address is changed using a value that is either lower than the minimum value or higher than the maximum value for the read cycle time (t_{RC}), none of the data can be guaranteed.

Note To perform a continuous read toggling /OE, /UB, and /LB with /CEm low level at an identical address, make settings so that the sum (t_{RC}) of the identical address read cycle times (t_{RC1}) is 10 μs or less.

Remark In read cycle, /WE should be fixed to High.

Figure 4-6. Write Cycle Timing Chart 1 (Mobile specified RAM)



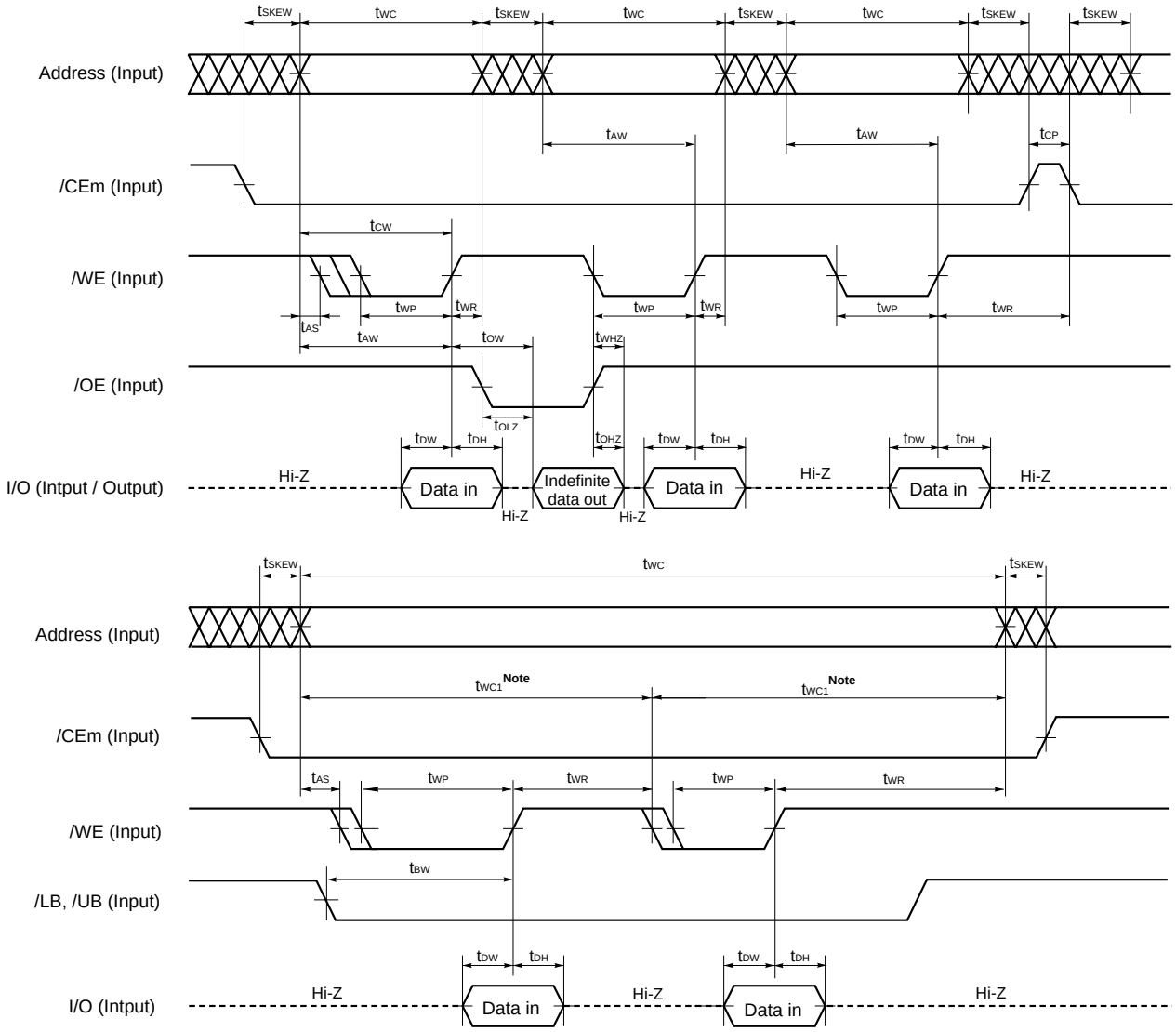
Cautions 1. During address transition, at least one of pins /CEm, /WE should be inactivated.

2. Do not input data to the I/O pins while they are in the output state.

3. If the address is changed using a value that is either lower than the minimum value or higher than the maximum value for the write cycle time (t_{WC}), none of the data can be guaranteed.

Remark Write operation is done during the overlap time of a Low /CEm, /WE, /LB and/or /UB.

Figure 4-7. Write Cycle Timing Chart 2 (Mobile specified RAM)



Cautions 1. During address transition, at least one of pins /CEm, /WE should be inactivated.

2. Do not input data to the I/O pins while they are in the output state.

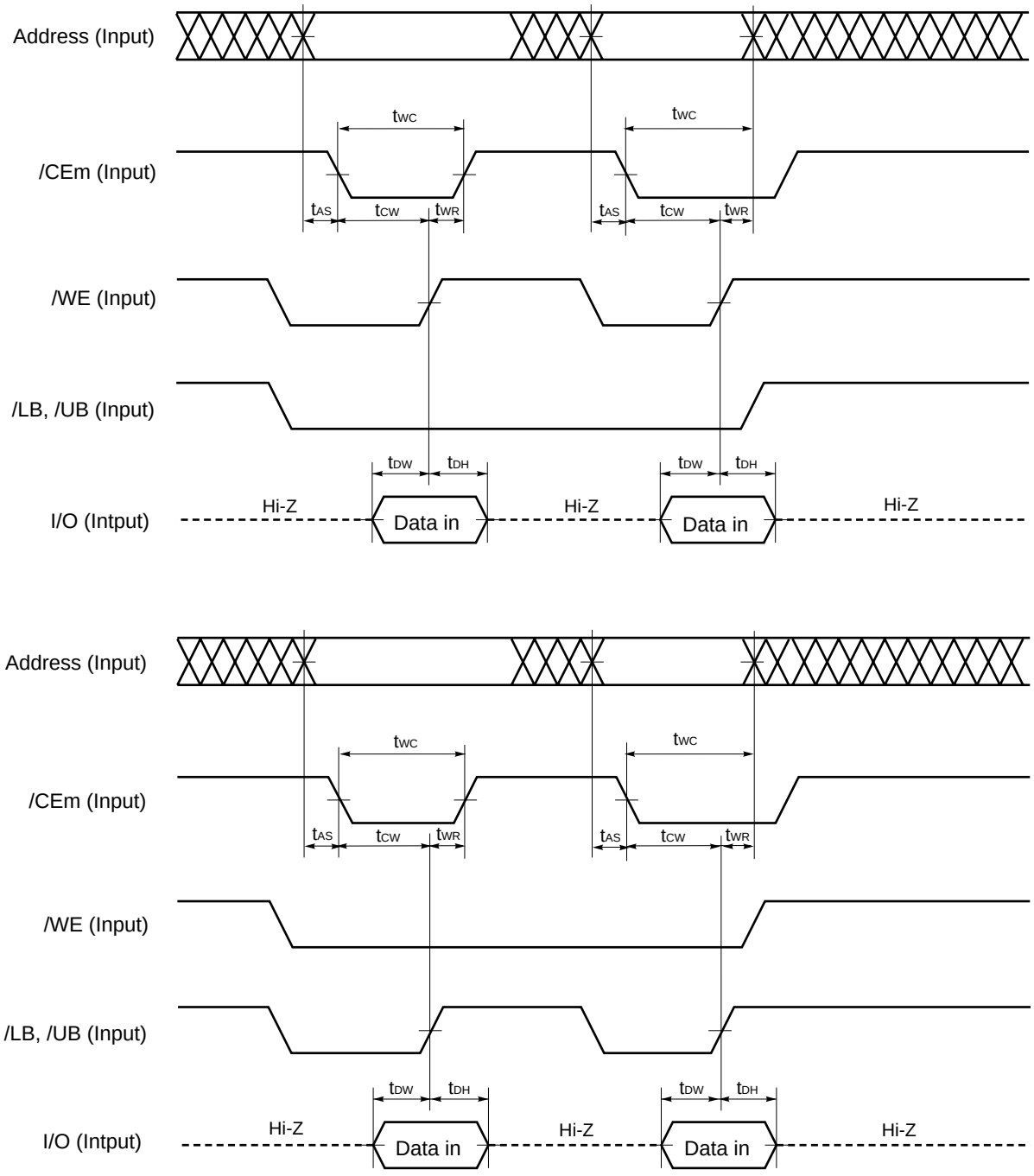
3. If the address is changed using a value that is either lower than the minimum value or higher than the maximum value for the write cycle time (t_{WC}), none of the data can be guaranteed.

Note If /LB and /UB are changed at the same time with /CEm low level and a continuous write operation toggling /WE is performed, make settings so that the sum (t_{WC}) of the identical address write cycle time (t_{WC1}) is 10 μs or less.

Remarks 1. Write operation is done during the overlap time of a Low /CEm, /WE, /LB and/or /UB.

2. When /WE is at Low, the I/O pins are always high impedance. When /WE is at High, read operation is executed. Therefore /OE should be at High to make the I/O pins high impedance.

Figure 4-8. Write Cycle Timing Chart 3 (/CEm Controlled) (Mobile specified RAM)



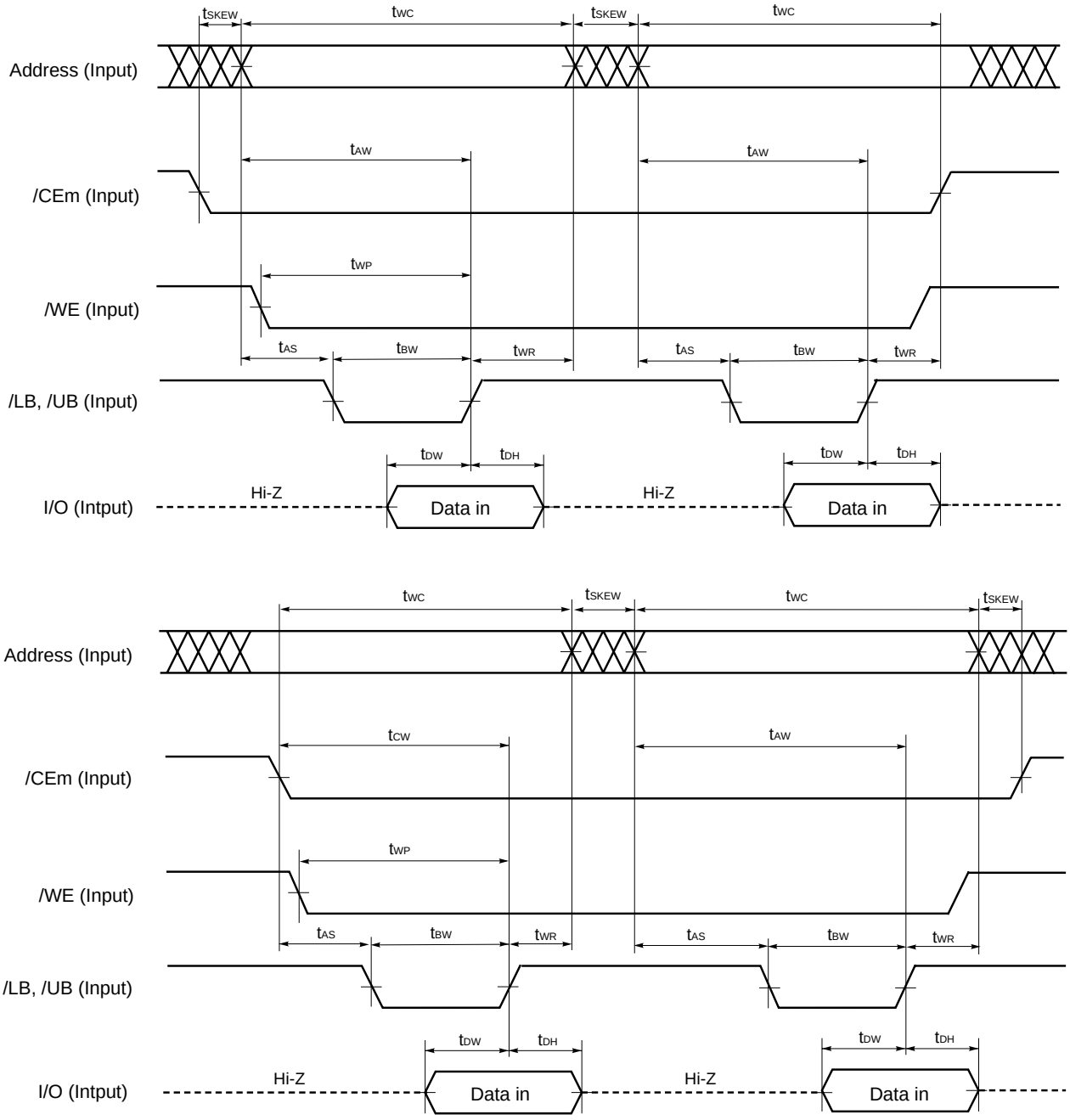
Cautions 1. During address transition, at least one of pins /CEm, /WE should be inactivated.

2. Do not input data to the I/O pins while they are in the output state.

3. If the address is changed using a value that is either lower than the minimum value or higher than the maximum value for the write cycle time (t_{WC}), none of the data can be guaranteed.

Remark Write operation is done during the overlap time of a Low /CEm, /WE, /LB and/or /UB.

Figure 4-9. Write Cycle Timing Chart 4 (/LB, /UB Controlled 1) (Mobile specified RAM)



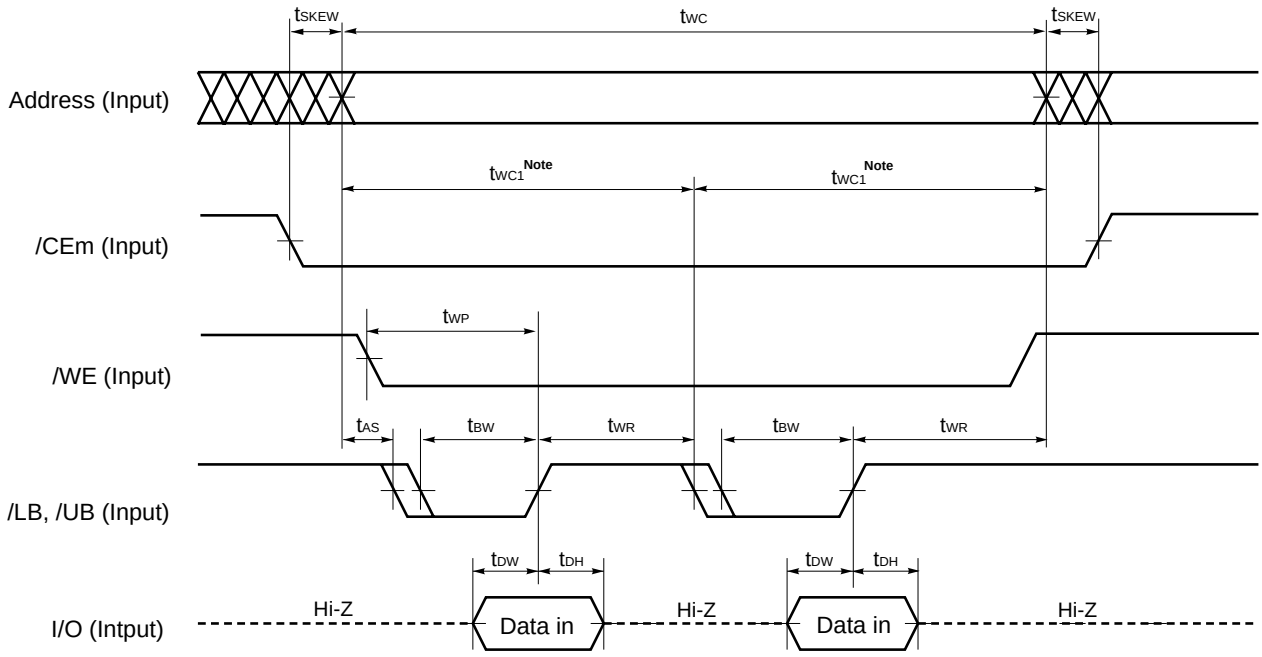
Cautions 1. During address transition, at least one of pins /CEm, /WE should be inactivated.

2. Do not input data to the I/O pins while they are in the output state.

3. If the address is changed using a value that is either lower than the minimum value or higher than the maximum value for the write cycle time (t_{WC}), none of the data can be guaranteed.

Remark Write operation is done during the overlap time of a Low /CEm, /WE, /LB and/or /UB.

Figure 4-10. Write Cycle Timing Chart 5 (/LB, /UB Controlled 2) (Mobile specified RAM)



Cautions 1. During address transition, at least one of pins /CEm, /WE should be inactivated.

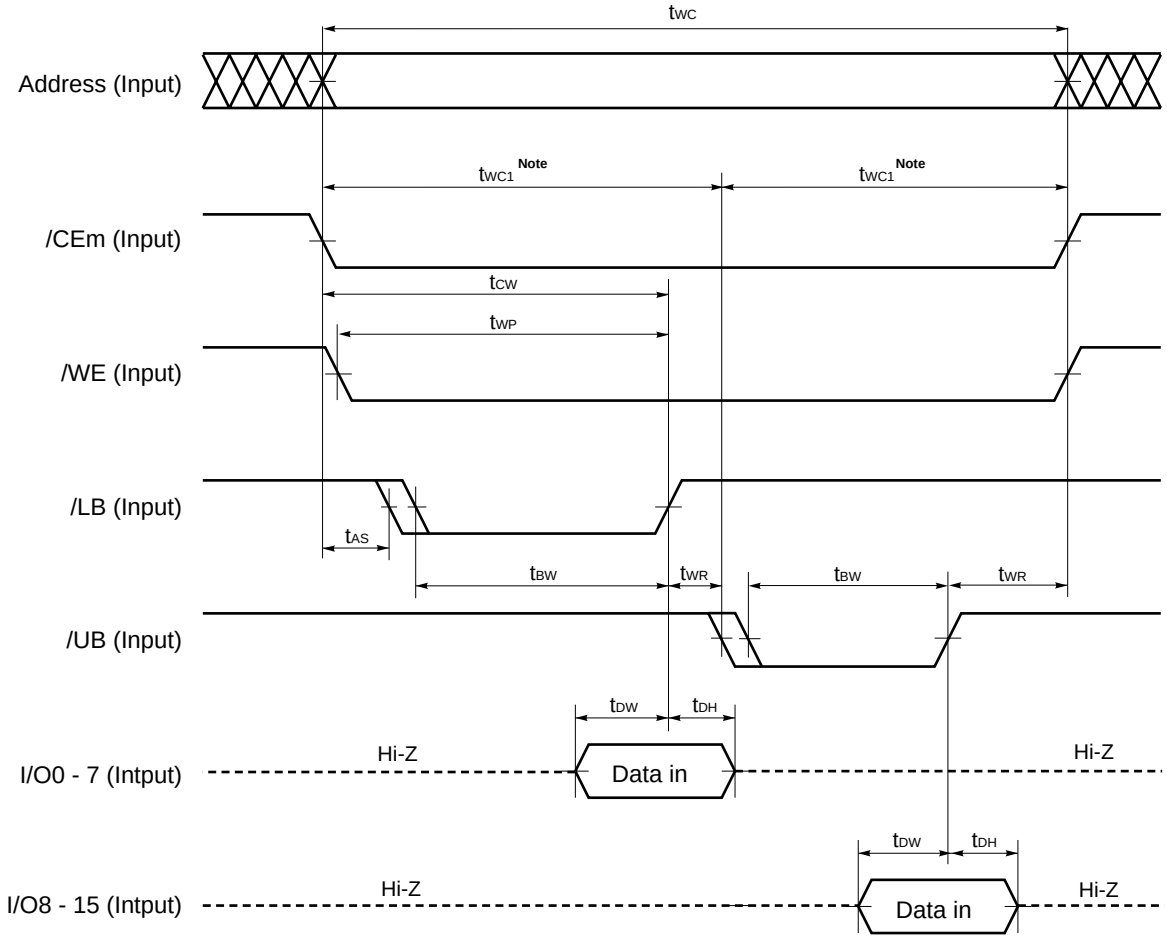
2. Do not input data to the I/O pins while they are in the output state.

3. If the address is changed using a value that is either lower than the minimum value or higher than the maximum value for the write cycle time (t_{WC}), none of the data can be guaranteed.

Note If /LB and /UB are changed at the same time with /CEm low level and a continuous write operation toggling /WE is performed, make settings so that the sum (t_{WC}) of the identical address write cycle time (t_{WC1}) is 10 μs or less.

Remark Write operation is done during the overlap time of a Low /CEm, /WE, /LB and/or /UB.

Figure 4-11. Write Cycle Timing Chart 6 (/LB, /UB Independent Controlled 1) (Mobile specified RAM)



Cautions 1. During address transition, at least one of pins /CEm, /WE should be inactivated.

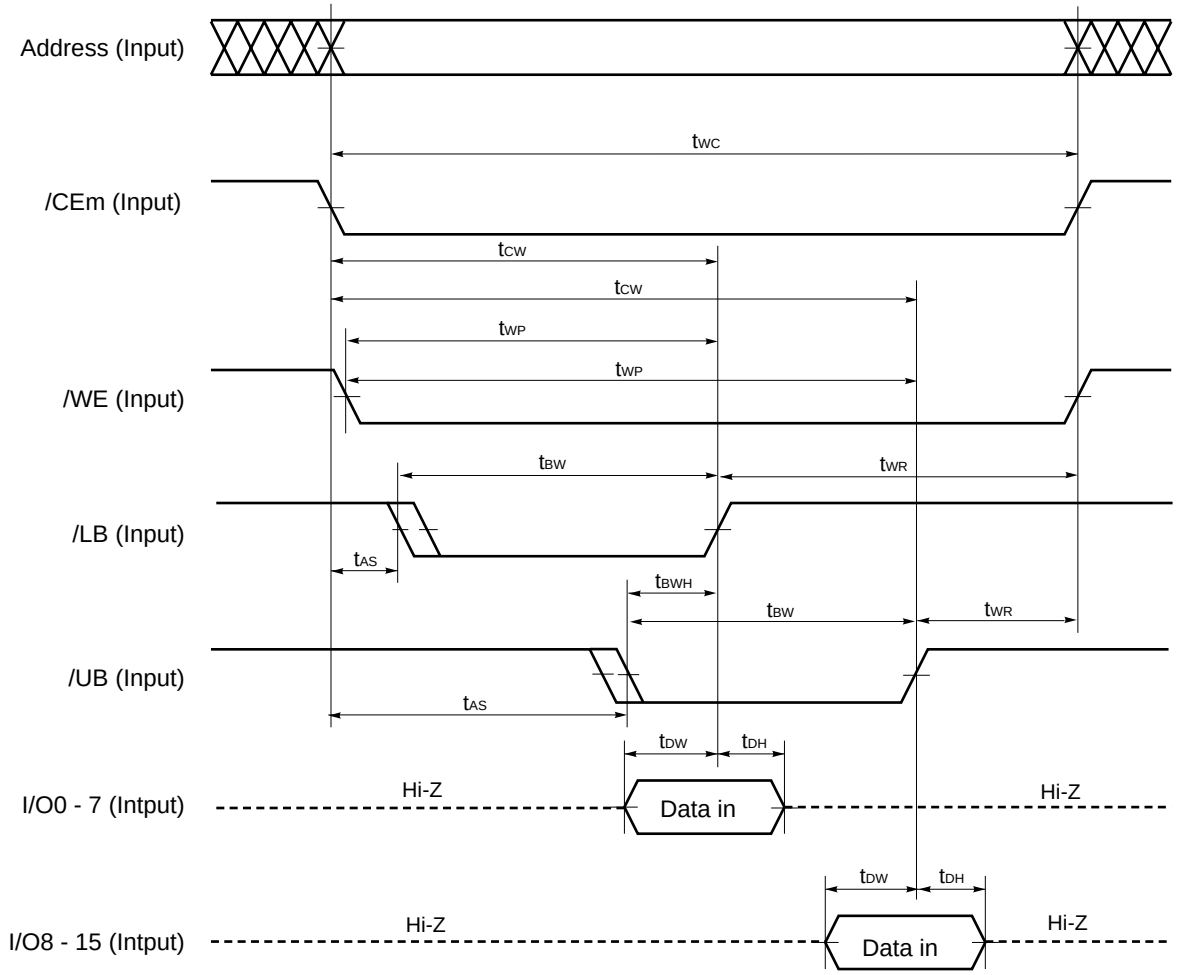
2. Do not input data to the I/O pins while they are in the output state.

3. If the address is changed using a value that is either lower than the minimum value or higher than the maximum value for the write cycle time (t_{WC}), none of the data can be guaranteed.

Note If /LB and /UB are changed at the same time with /CEm low level and a continuous write operation toggling /WE is performed, make settings so that the sum (t_{WC}) of the identical address write cycle time (t_{WC1}) is 10 μs or less.

Remark Write operation is done during the overlap time of a Low /CEm, /WE, /LB and/or /UB.

Figure 4-12. Write Cycle Timing Chart 7 (/LB, /UB Independent Controlled 2) (Mobile specified RAM)



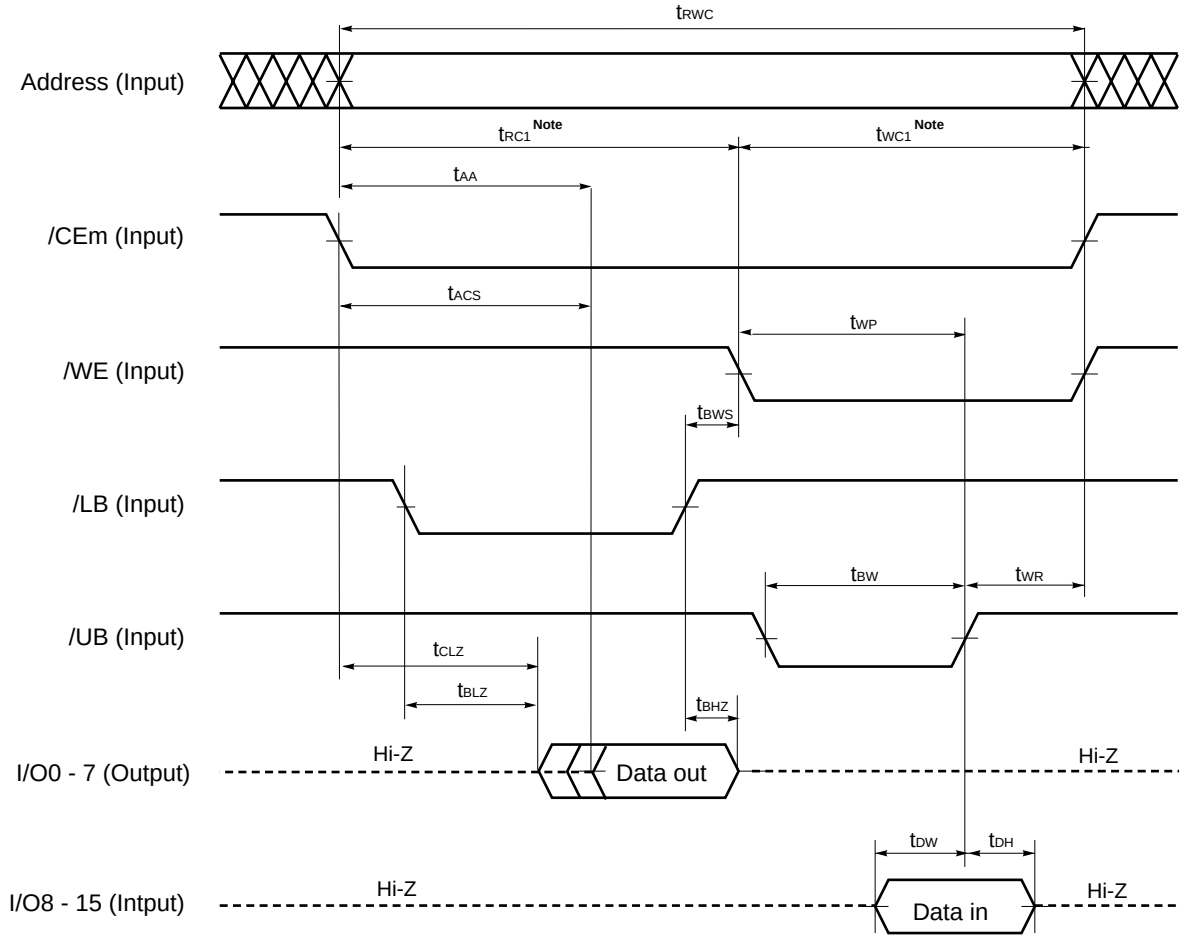
Cautions 1. During address transition, at least one of pins /CEm, /WE should be inactivated.

2. Do not input data to the I/O pins while they are in the output state.

3. If the address is changed using a value that is either lower than the minimum value or higher than the maximum value for the write cycle time (t_{WC}), none of the data can be guaranteed.

Remark Write operation is done during the overlap time of a Low /CEm, /WE, /LB and/or /UB.

Figure 4-13. Read Write Cycle Timing Chart 1 (/LB, /UB Independent Controlled 1) (Mobile specified RAM)



Cautions 1. During address transition, at least one of pins /CEm, /WE should be inactivated.

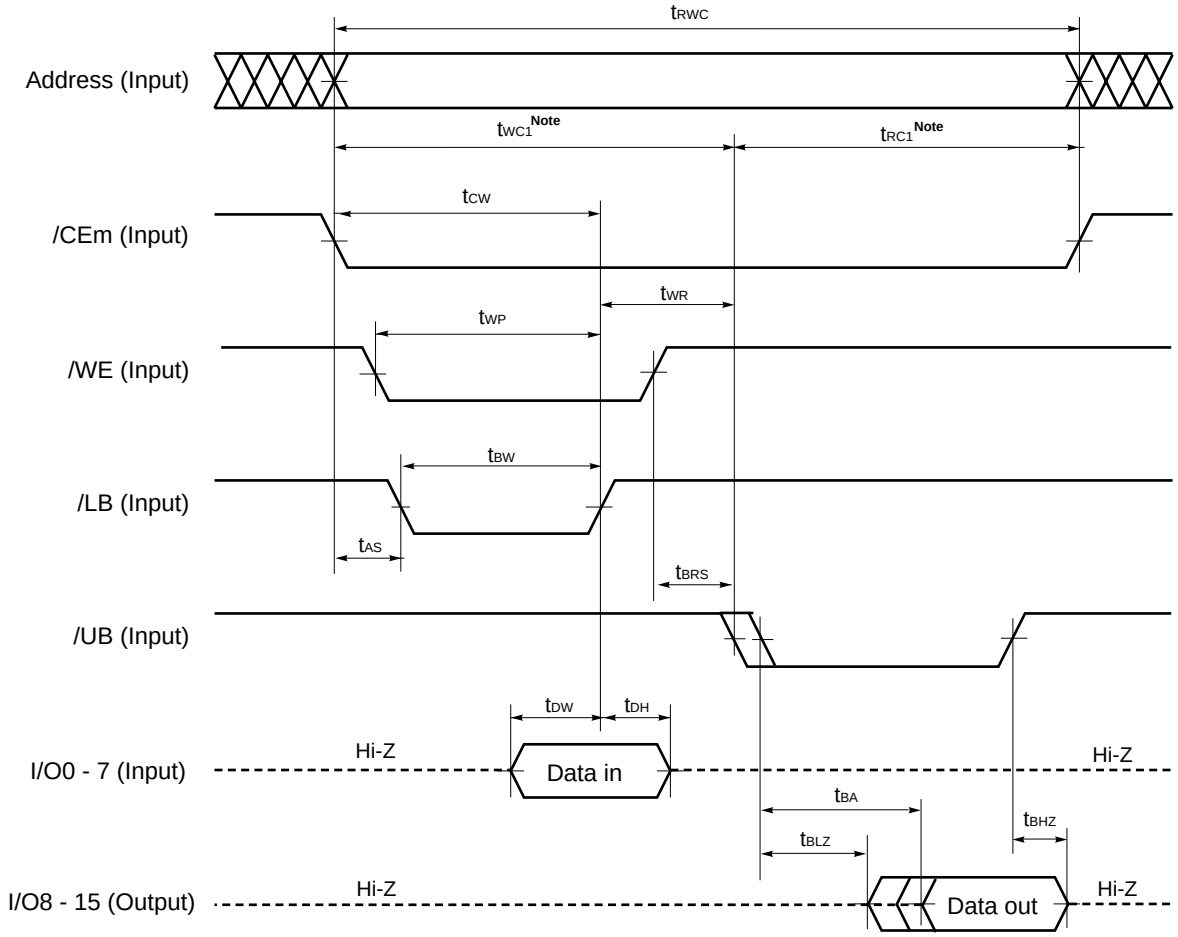
2. Do not input data to the I/O pins while they are in the output state.

3. If the address is changed using a value that is either lower than the minimum value or higher than the maximum value for the identical address read cycle time (t_{RC1}) and the identical address write cycle time (t_{WC1}), none of the data can be guaranteed.

Note Make settings so that the sum (t_{RWC}) of the identical address read cycle time (t_{RC1}) and the identical address write cycle time (t_{WC1}) is 10 μs or less when a write is performed at the identical address using /UB following a read using /LB with /CEm low level, or when a write is performed using /LB following a read using /UB.

Remark Write operation is done during the overlap time of a Low /CEm, /WE, /LB and/or /UB.

Figure 4-14. Read Write Cycle Timing Chart 2 (/LB, /UB Independent Controlled 2) (Mobile specified RAM)



Cautions 1. During address transition, at least one of pins /CEm, /WE should be inactivated.

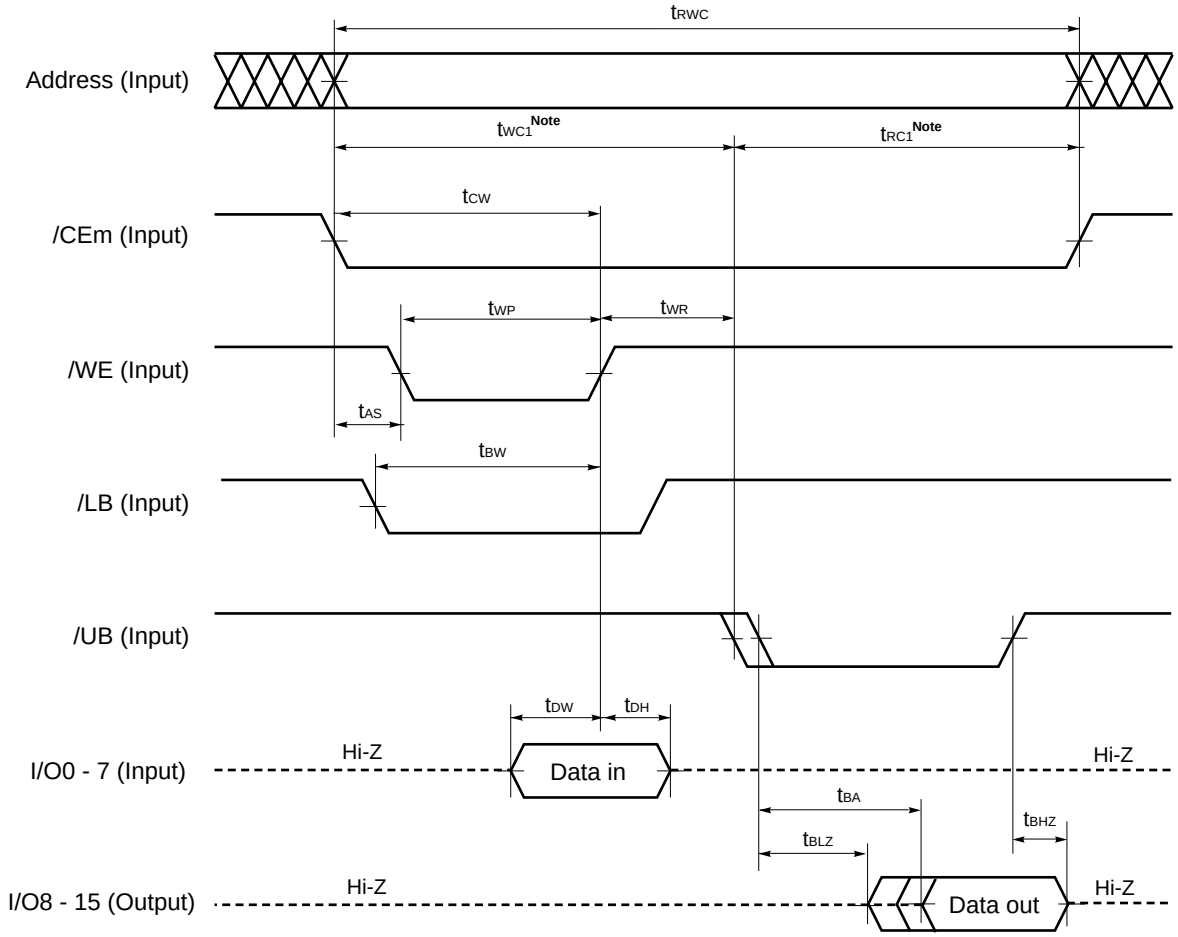
2. Do not input data to the I/O pins while they are in the output state.

3. If the address is changed using a value that is either lower than the minimum value or higher than the maximum value for the identical address read cycle time (t_{RC1}) and the identical address write cycle time (t_{WC1}), none of the data can be guaranteed.

Note Make settings so that the sum (t_{RWC}) of the identical address read cycle time (t_{RC1}) and the identical address write cycle time (t_{WC1}) is 10 μs or less when a write is performed at the identical address using /UB following a read using /LB with /CEm low level, or when a write is performed using /LB following a read using /UB.

Remark Write operation is done during the overlap time of a Low /CEm, /WE, /LB and/or /UB.

Figure 4-15. Read Write Cycle Timing Chart 3 (/LB, /UB Independent Controlled 3) (Mobile specified RAM)



Cautions 1. During address transition, at least one of pins /CEm, /WE should be inactivated.

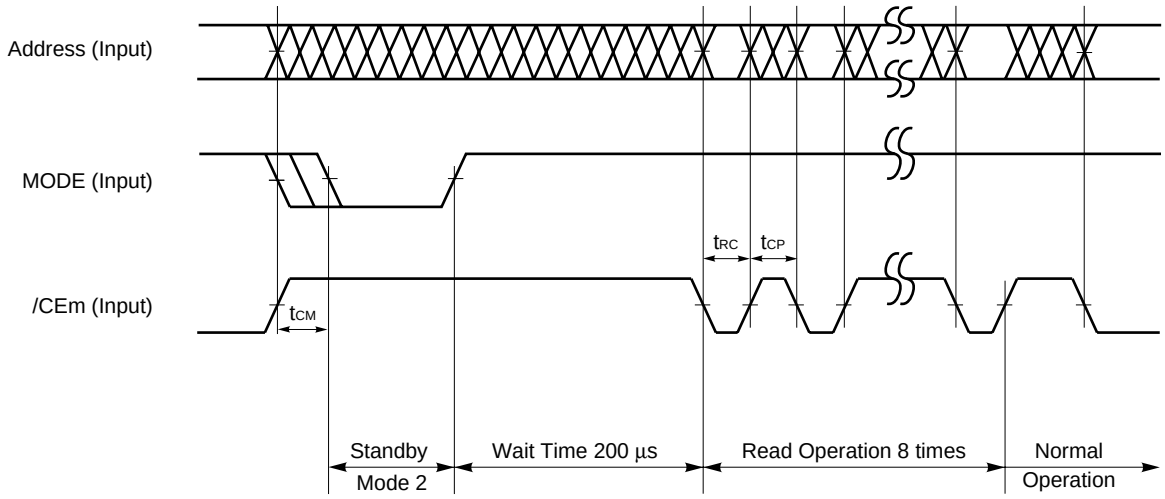
2. Do not input data to the I/O pins while they are in the output state.

3. If the address is changed using a value that is either lower than the minimum value or higher than the maximum value for the identical address read cycle time (t_{RC1}) and the identical address write cycle time (t_{WC1}), none of the data can be guaranteed.

Note Make settings so that the sum (t_{RWC}) of the identical address read cycle time (t_{RC1}) and the identical address write cycle time (t_{WC1}) is 10 μs or less when a write is performed at the identical address using /UB following a read using /LB with /CEm low level, or when a write is performed using /LB following a read using /UB.

Remark Write operation is done during the overlap time of a Low /CEm, /WE, /LB and/or /UB.

Figure 4-16. Standby Mode 2 entry and recovery Timing Chart (Mobile specified RAM)



Parameter	Symbol	MIN.	MAX.	Unit	Note
/CEm High to MODE Low	t_{CM}	0		ns	

Cautions 1. Make MODE and /CEm high level during the wait time.

2. Make MODE high level during the wait time and eight read operations.

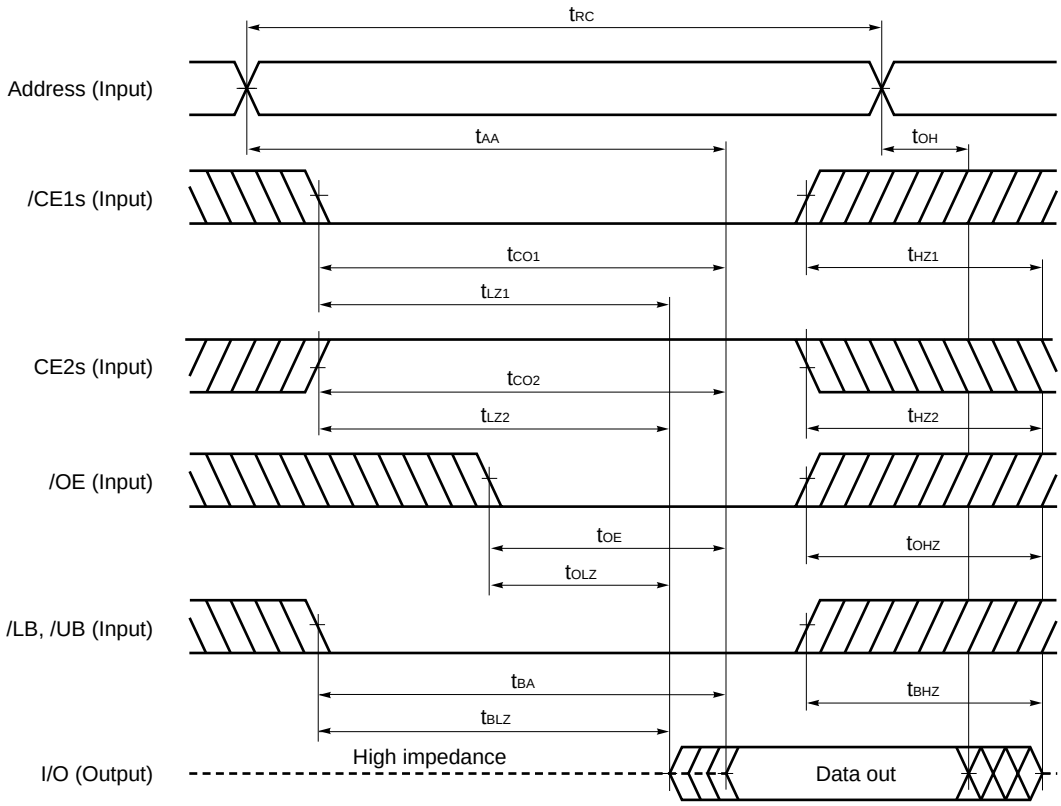
3. The read operation must satisfy the specs described on page 34 (Read Cycle (Mobile specified RAM)).

4. The read operation address can be either V_{IH} or V_{IL}.

5. Perform reading by toggling /CEm.

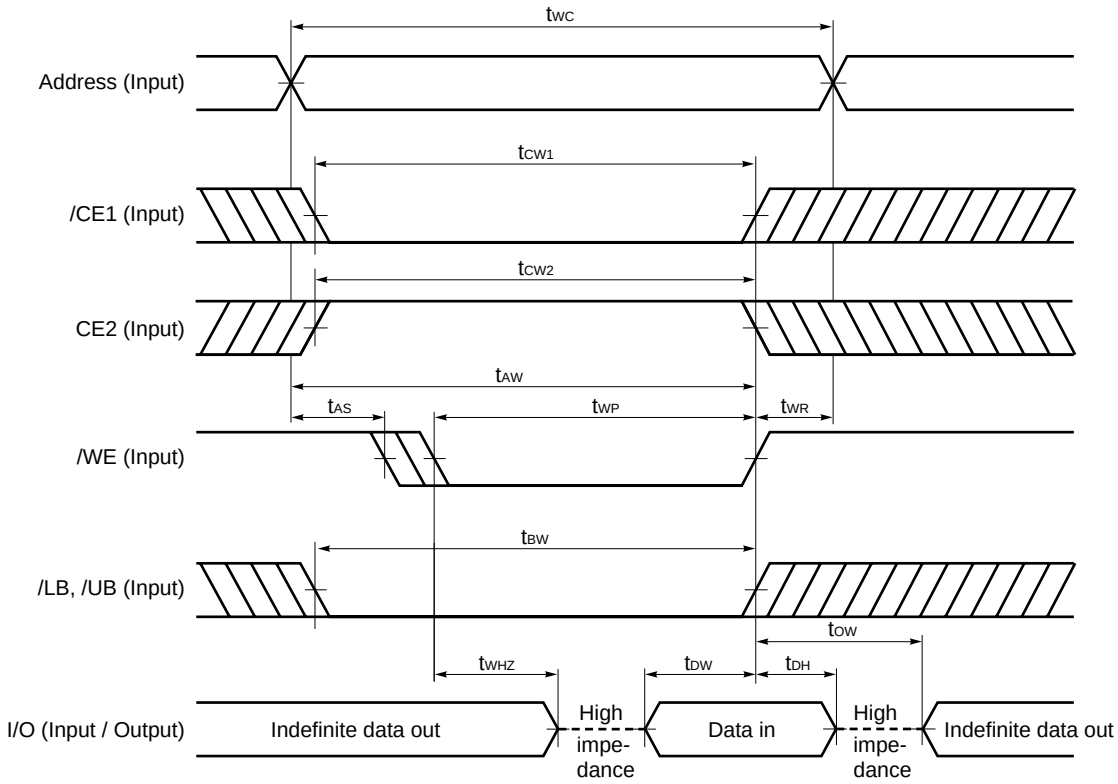
6. To prevent bus contention, it is recommended to set /OE to high level. However, do not input data to the I/O pins if /OE is low level during a read operation.

Figure 4-17. Read Cycle Timing Chart (SRAM)



Remark In read cycle, /WE should be fixed to high level.

Figure 4-18. Write Cycle Timing Chart 1 (/WE Controlled) (SRAM)



Cautions 1. During address transition, at least one of pins /CE1s, CE2s, /WE should be inactivated.

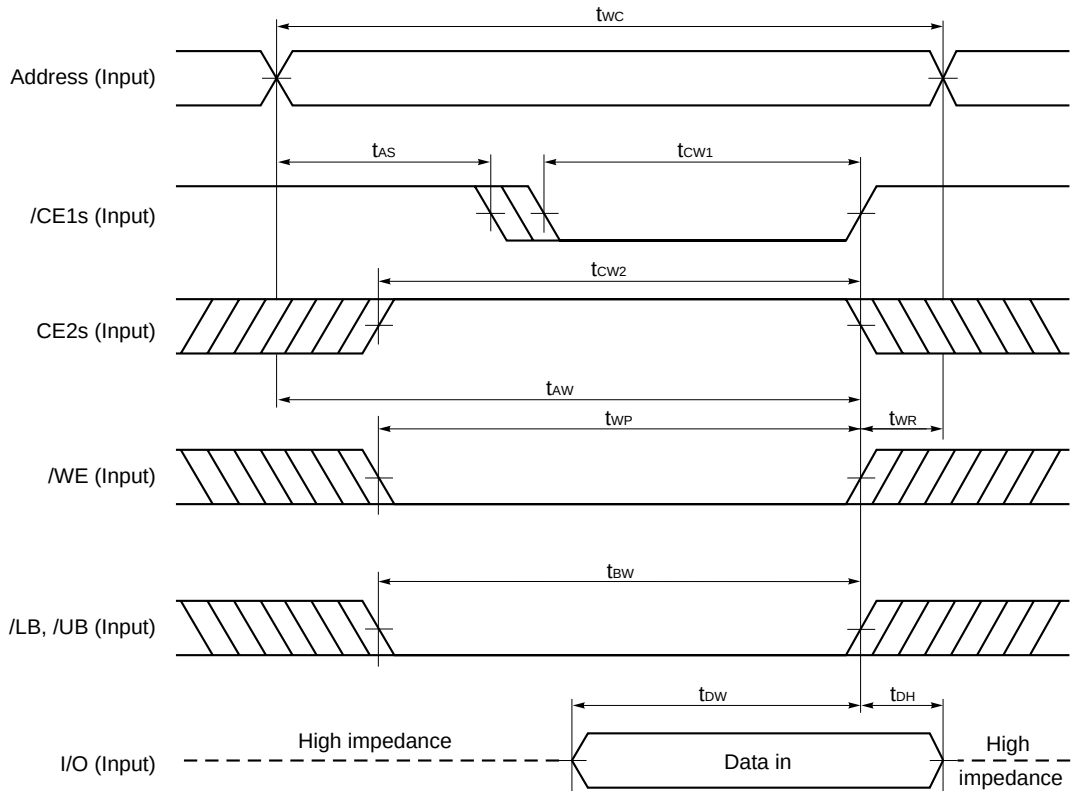
2. Do not input data to the I/O pins while they are in the output state.

Remarks 1. Write operation is done during the overlap time of a low level /CE1s, /WE, /LB and/or /UB, and a high level CE2s.

2. If /CE1s changes to low level at the same time or after the change of /WE to low level, or if CE2s changes to high level at the same time or after the change of /WE to low level, the I/O pins will remain high impedance state.

3. When /WE is at low level, the I/O pins are always high impedance. When /WE is at high level, read operation is executed. Therefore /OE should be at high level to make the I/O pins high impedance.

Figure 4-19. Write Cycle Timing Chart 2 (/CE1s Controlled) (SRAM)

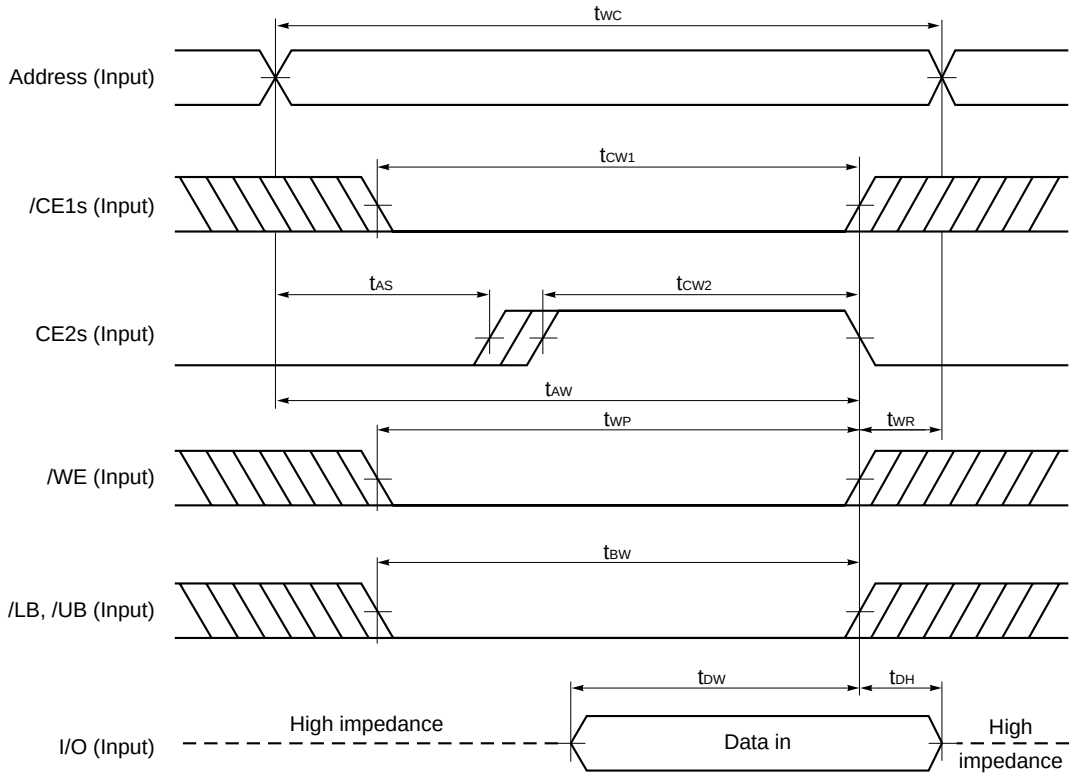


Cautions 1. During address transition, at least one of pins /CE1s, CE2s, /WE should be inactivated.

2. Do not input data to the I/O pins while they are in the output state.

Remark Write operation is done during the overlap time of a low level /CE1s, /WE, /LB and/or /UB, and a high level CE2s.

Figure 4-20. Write Cycle Timing Chart 3 (CE2s Controlled) (SRAM)

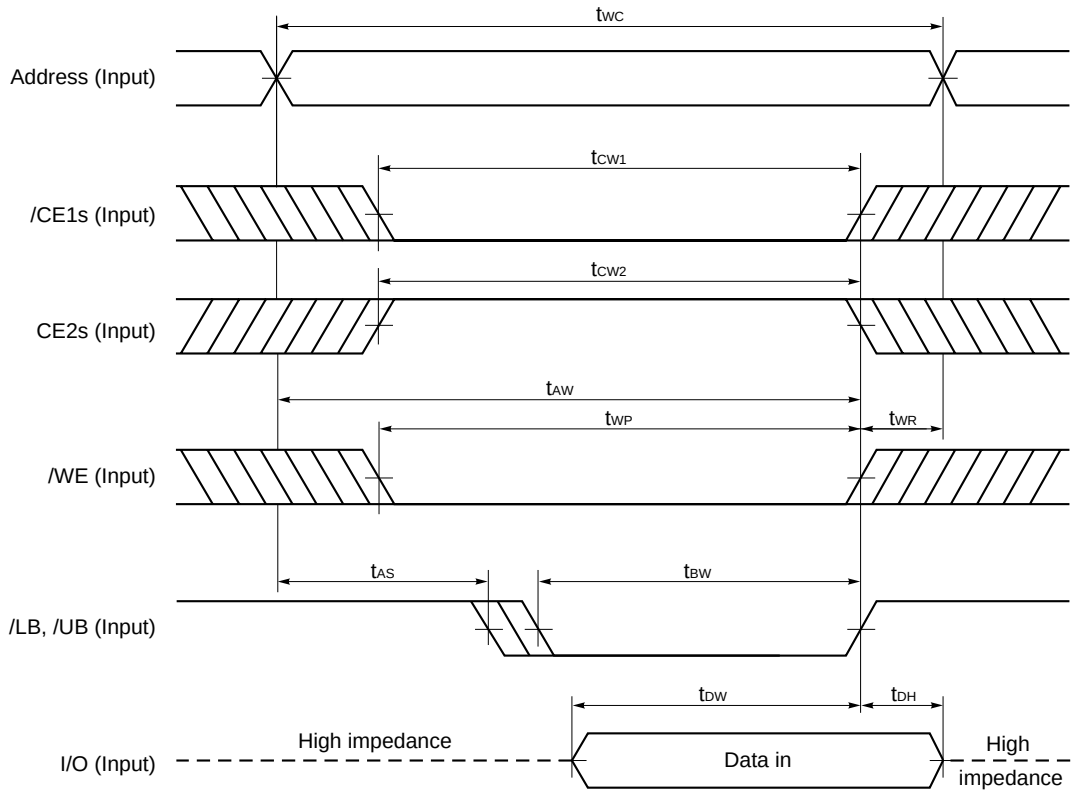


Cautions 1. During address transition, at least one of pins /CE1s, CE2s, /WE should be inactivated.

2. Do not input data to the I/O pins while they are in the output state.

Remark Write operation is done during the overlap time of a low level /CE1s, /WE, /LB and/or /UB, and a high level CE2s.

Figure 4-21. Write Cycle Timing Chart 4 (/LB, /UB Controlled) (SRAM)

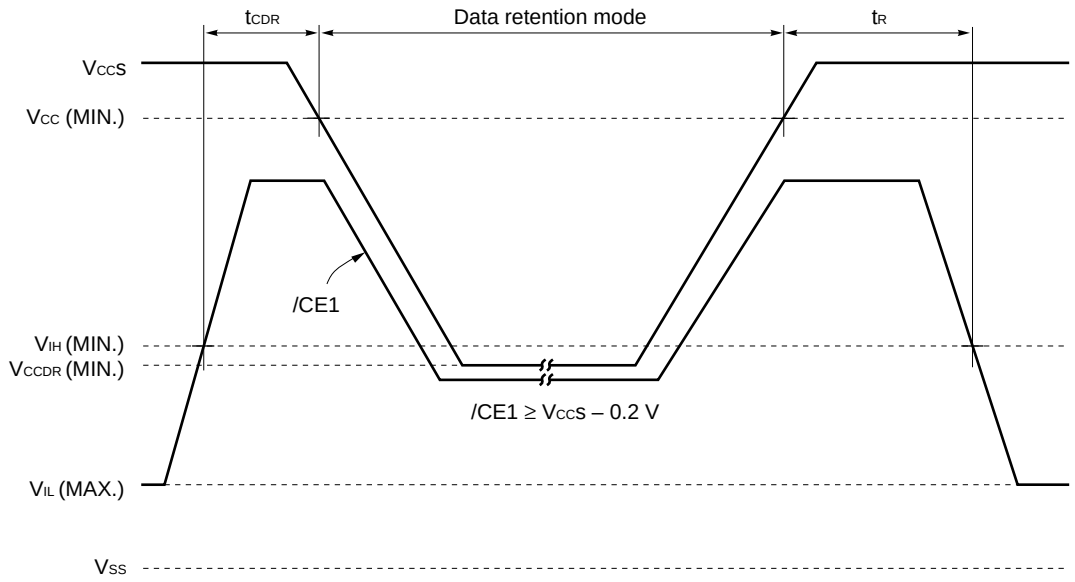


Cautions 1. During address transition, at least one of pins /CE1s, CE2s, /WE should be inactivated.

2. Do not input data to the I/O pins while they are in the output state.

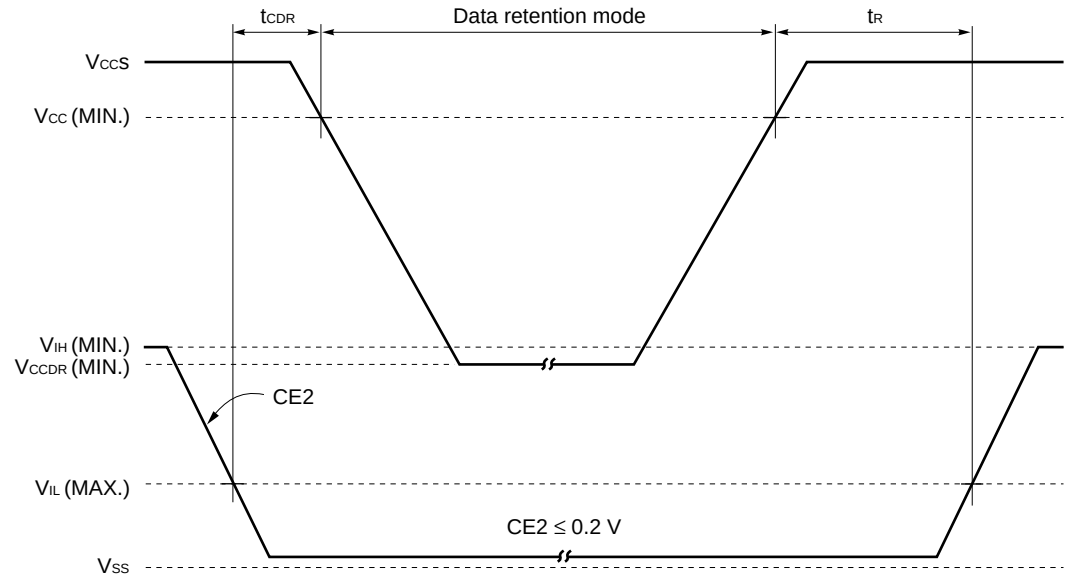
Remark Write operation is done during the overlap time of a low level /CE1s, /WE, /LB and/or /UB, and a high level CE2s.

Figure 4-22. Data Retention Timing Chart 1 (/CE1s Controlled) (SRAM)



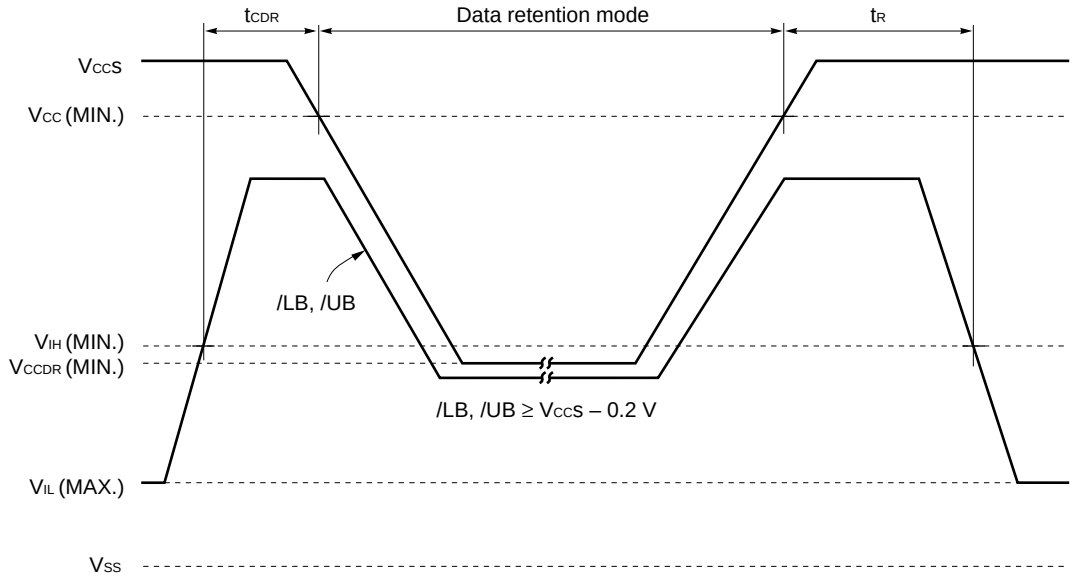
Remark On the data retention mode by controlling /CE1s, the input level of CE2s must be ≥ V_{CC} – 0.2 V or ≤ 0.2 V. The other pins (Address, I/O, /WE, /OE, /LB, /UB) can be in high impedance state.

Figure 4-23. Data Retention Timing Chart 2 (CE2s Controlled) (SRAM)



Remark On the data retention mode by controlling CE2s, The other pins (/CE1s, Address, I/O, /WE, /OE, /LB, /UB) can be in high impedance state.

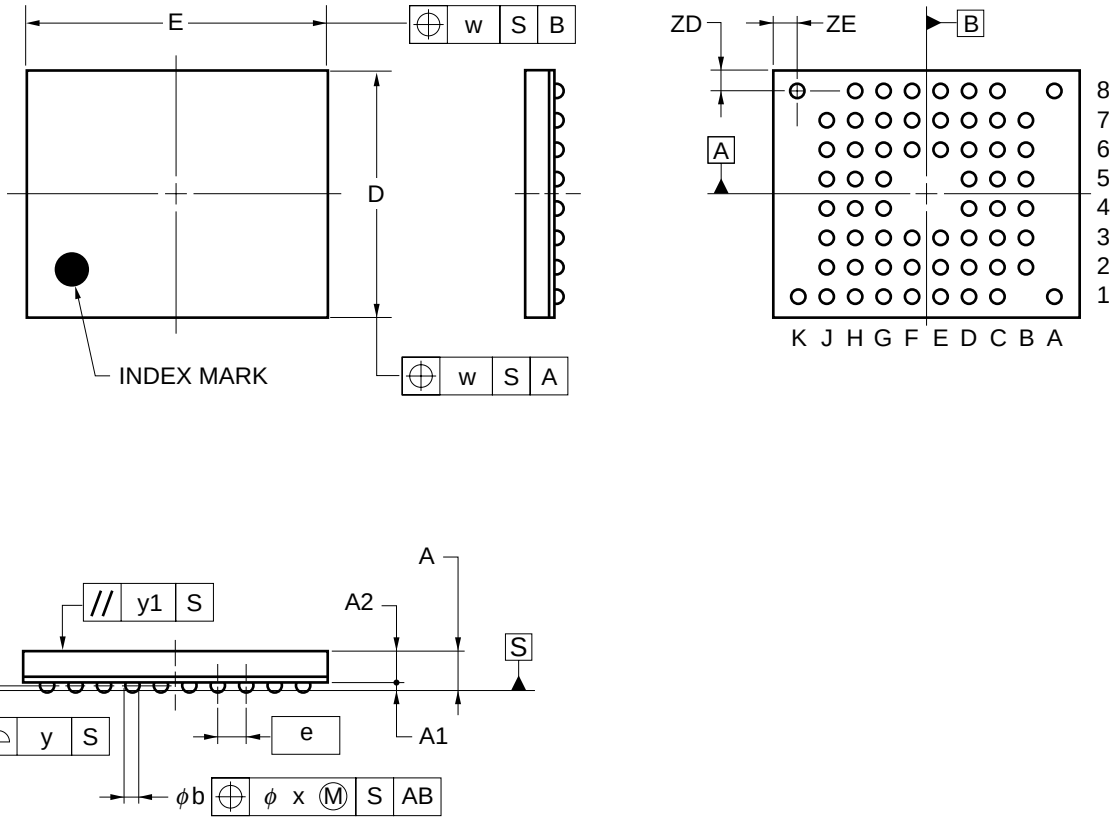
Figure 4-24. Data Retention Timing Chart 3 (/LB, /UB Controlled) (SRAM)



Remark On the data retention mode by controlling /LB and /UB, the input level of /CE1s and CE2s must be ≥ V_{CC} – 0.2 V or ≤ 0.2 V. The other pins (Address, I/O, /WE, /OE) can be in high impedance state.

5. Package Drawing

61-PIN TAPE FBGA (9x7)



ITEM	MILLIMETERS
D	7.0±0.1
E	9.0±0.1
w	0.2
A	1.1±0.1
A1	0.26±0.05
A2	0.84
e	0.8
b	0.45±0.05
x	0.08
y	0.1
y1	0.1
ZD	0.7
ZE	0.8

6. Recommended Soldering Conditions

Please consult with our sales offices for soldering conditions of the MC-2311100.

Types of Surface Mount Device

MC-2311100F9-B80-BQ1 : 61-pin TAPE FBGA (9 × 7)
MC-2311100F9-B90-BQ1 : 61-pin TAPE FBGA (9 × 7)
MC-2311100F9-B10-BQ1 : 61-pin TAPE FBGA (9 × 7)

[MEMO]

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

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