SHARP

LM320081

LCD Data Sheet

Passive Matrix LCD Unit

FEATURES

- Display Format: 320 × 240
- Overall Dimensions:
  134 (W) × 96 (H) × 6.5 (D) mm
- Active Area: 100 (W) × 76 (H) mm
- Dot Pitch: 0.28 (W) × 0.28 (H) mm

DESCRIPTION

The SHARP LM320081 Passive Matrix LCD consists of 320 × 240 dots with an FSTN, reflective, positive-type panel.

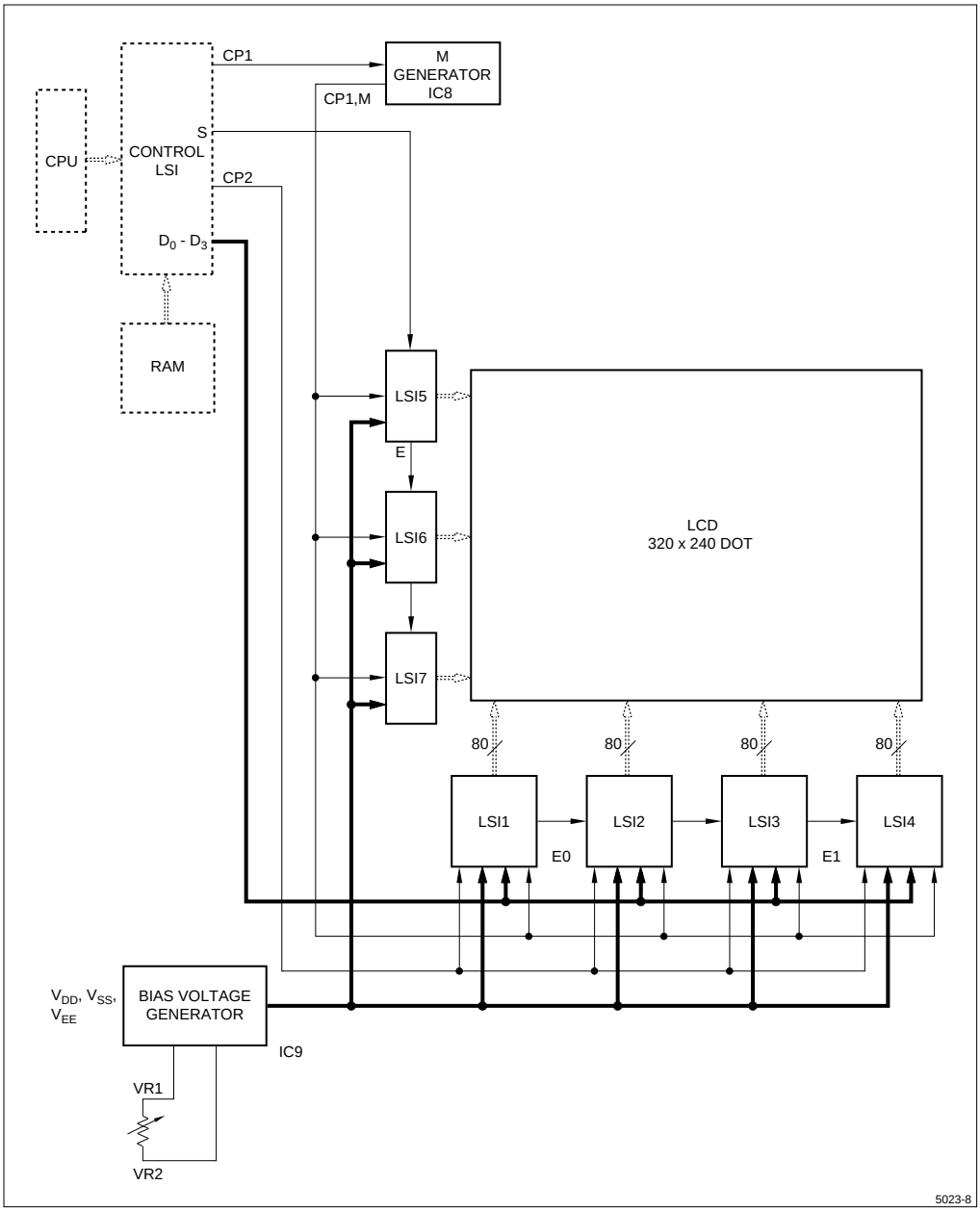


Figure 1. LM320081 Block Diagram

MECHANICAL SPECIFICATIONS

PARAMETER	SPECIFICATIONS	UNIT	NOTE
Outline Dimensions	134 (W) × 96 (H) × 6.5 max (D)	mm	1
Active Area	100 (W) × 76 (H)	mm	–
Display Format	320 (W) × 240 (H) Full Dot	–	–
Dot Size	0.28 (W) × 0.28 (H)	mm	–
Dot Spacing	0.02	mm	–
Character Color	Black	–	2
Background Color	White	–	2
Weight	Approximately 105	g	–

NOTES:

1. Excludes the mounting tab (refer to the Outline Dimensions diagram).
2. Due to the characteristics of the LC material, the colors vary with environmental temperature.

ABSOLUTE MAXIMUM RATINGS (t_A = 25°C)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD} – V_{SS}	Supply Voltage (Logic)	0	6.0	V
V_{DD} – V_{EE}	Supply Voltage (LCD Driver)	0	28.5	V
V_{IN}	Input Voltage	0	V_{DD}	V

ENVIRONMENTAL CONDITIONS

ITEM	Tstg		Topr		CONDITION	NOTE
	MIN.	MAX.	MIN.	MAX.		
Ambient Temperature	–25°C	+60°C	0°C	+45°C	–	–
Humidity	–		–		No condensation	1
Vibration	–		–		3 Directions (X/Y/Z)	2
Shock	–		–		6 Directions (±X/±Y/±Z)	3

NOTES:

1. t_A ≤40°C, 90% RH maximum.
   t_A >40°C, Absolute humidity less than t_A = 40°C at 90% RH.
2. These test conditions are in accordance with IEC 68-2-6.
   Two hours for each direction of X/Y/Z (six hours total).

Frequency	10 Hz to 55 Hz
Vibration Width	1.5 mm
Interval	10 Hz to 55 Hz to 10 Hz (1.0 min)

3. Acceleration: 490 m/s^2 (50 g)
   Pulse width: 11 ms
   Three times for each direction of ±X/±Y/±Z.

ELECTRICAL CHARACTERISTICS (t_A = 25°C, V_{DD} = 5.0 V ±5%)

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT	NOTE
$V_{DD} – V_{SS}$	Supply Voltage (Logic)	–	4.75	5.0	5.25	V	–
$V_{EE} – V_{SS}$	Supply Voltage (LCD Drive)	V_{DD} = 5.0 V	–19.5	–18.5	–17.5	V	1
V_{IN}	Input Signal Voltage	'H' Level	0.8 V_{DD}	–	V_{DD}	V	–
		'L' Level	0	–	0.2 V_{DD}	V	–
I_{IL}	Input Leakage Current	'H' Level	–	–	20	µA	–
		'L' Level	–20.0	–	–	µA	–
I_{DD}	Supply Current (Logic)	V_{DD} = 5.0 V, V_{EE} = –18.5 V, V_R = 100 kΩ F = 80 HZ	–	9	13	mA	2
I_{EE}	Supply Current (LCD)		–	7	11	mA	
P_DLCD	Power Consumption (LCD)		–	185	270	mW	

NOTES:

1. The viewing angle (θ) with optimum contrast is set by adjusting the variable resistor between VR1 and VR2. Refer to Figure 6 for the definition of θ.
2. Refer to the display high frequency pattern in Figure 2.

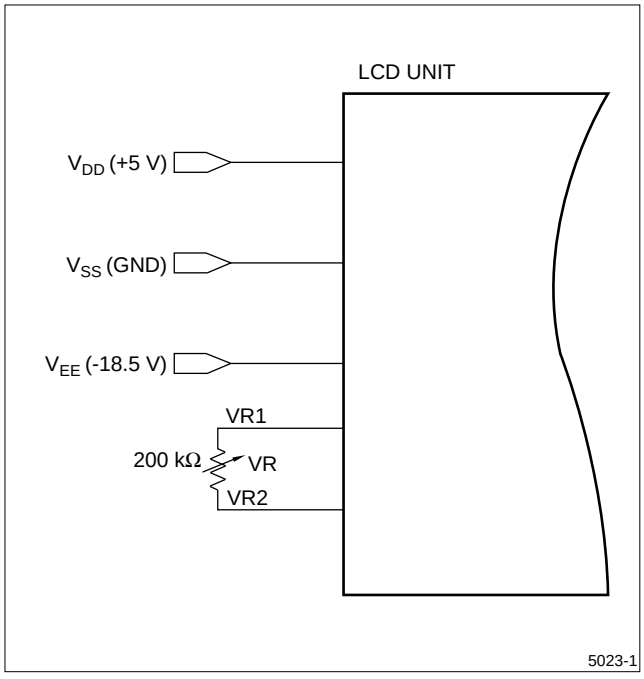


Figure 2. Display High Frequency Pattern

INTERFACE SIGNALS

CN1 [1]

PIN NUMBER	SYMBOL	PARAMETER	LEVEL
1	S	Scan Startup Signal	'H'
2	CP1	Input Data Latch Signal	H → L
3	CP2	Data Input Clock Signal	H → L
4	V_{DD}	Power Supply for Logic and LCD (+5 V)	–
5	V_{SS}	Ground Potential (0 V)	–
6	V_{EE}	Power Supply for LCD	–
7	D_0	Display Data Signal	H (ON), L (OFF)
8	D_1		
9	D_2		
10	D_3		
11	VR1	LCD Contrast Adjust (A)	–
12	VR2	LCD Contrast Adjust (B)	–

NOTE:

1. Connector used: 52103-1217 (Molex).
   Mating cable: 1.0 mm pitch, 12 pins F.F.C.

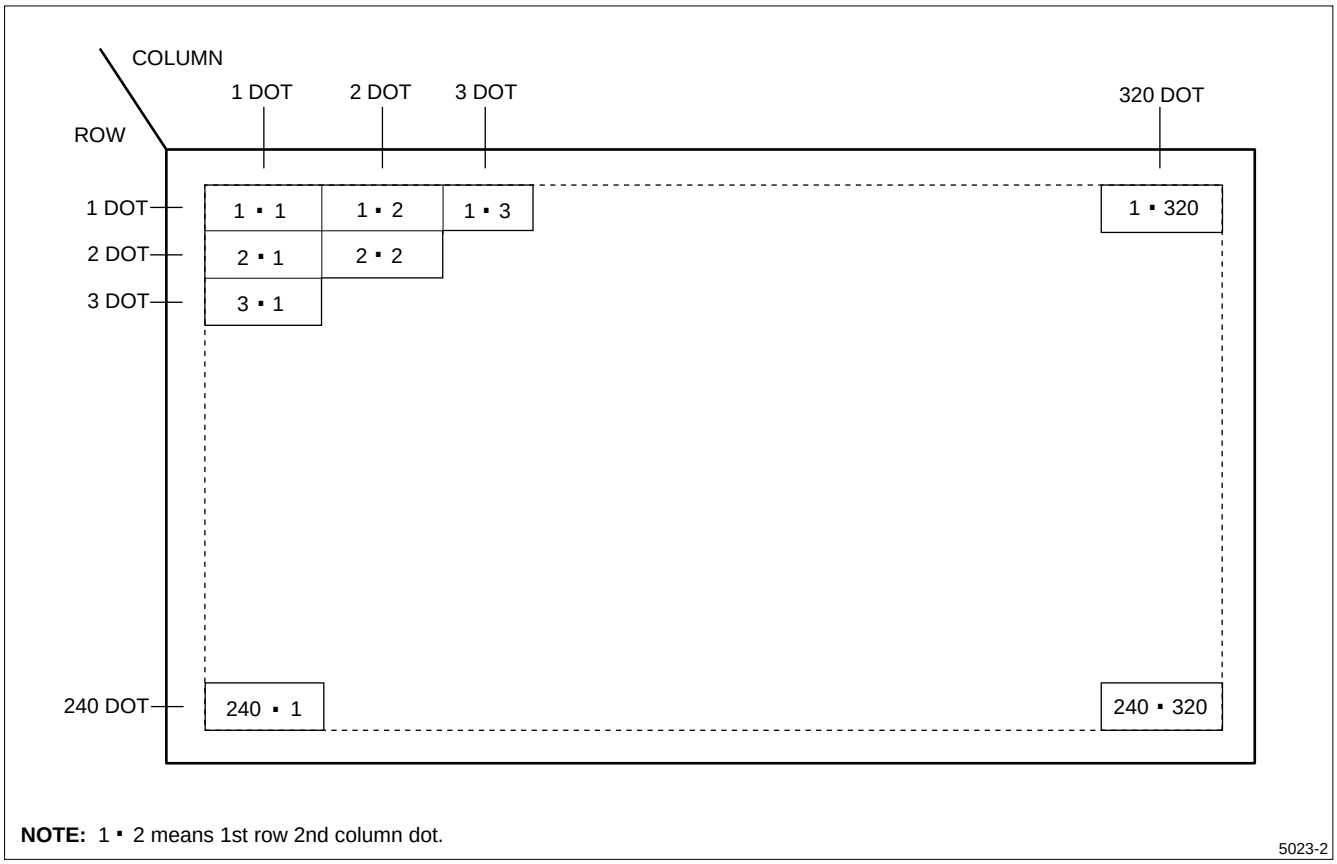


Figure 3. Dot Chart of Display Area

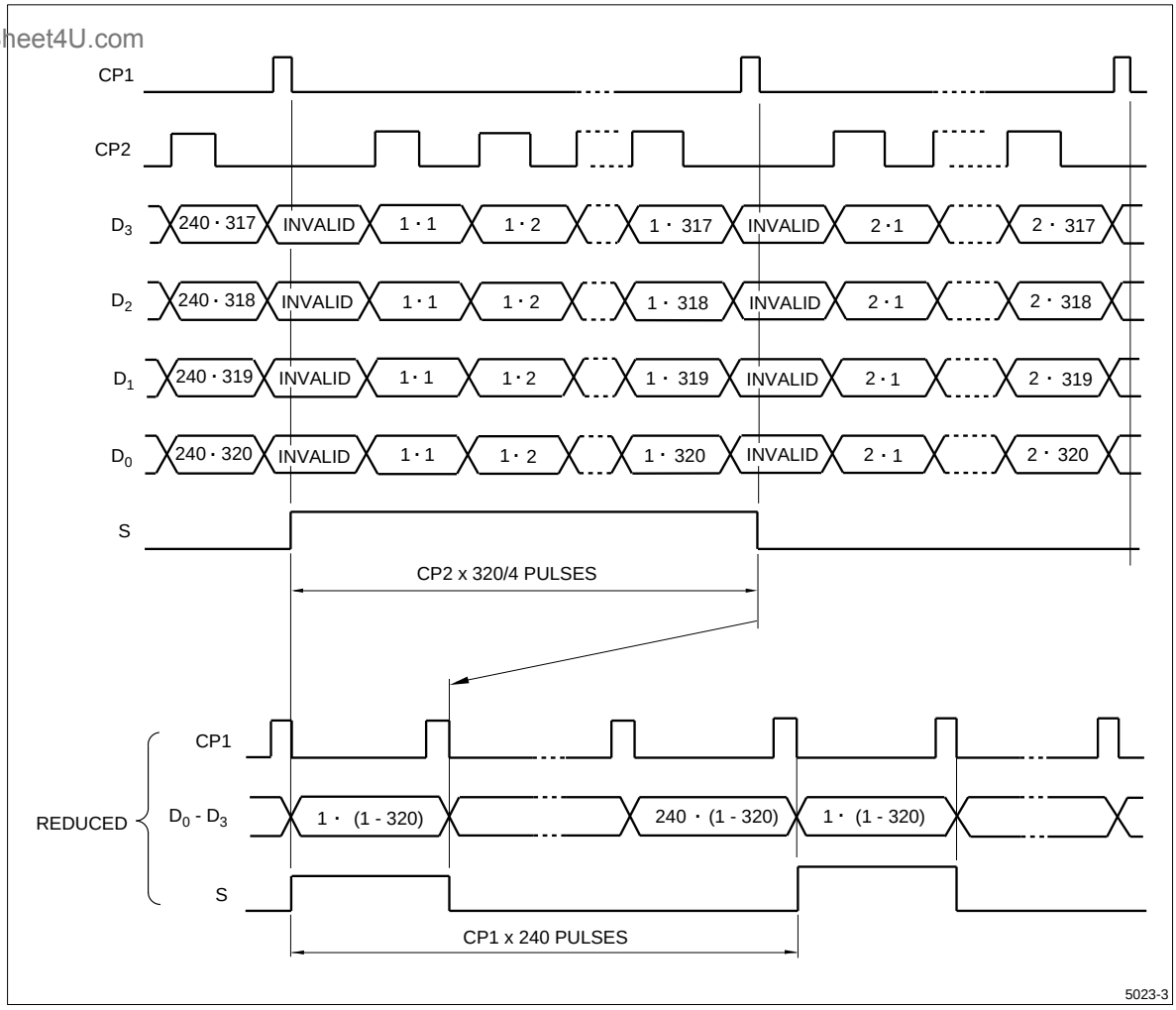
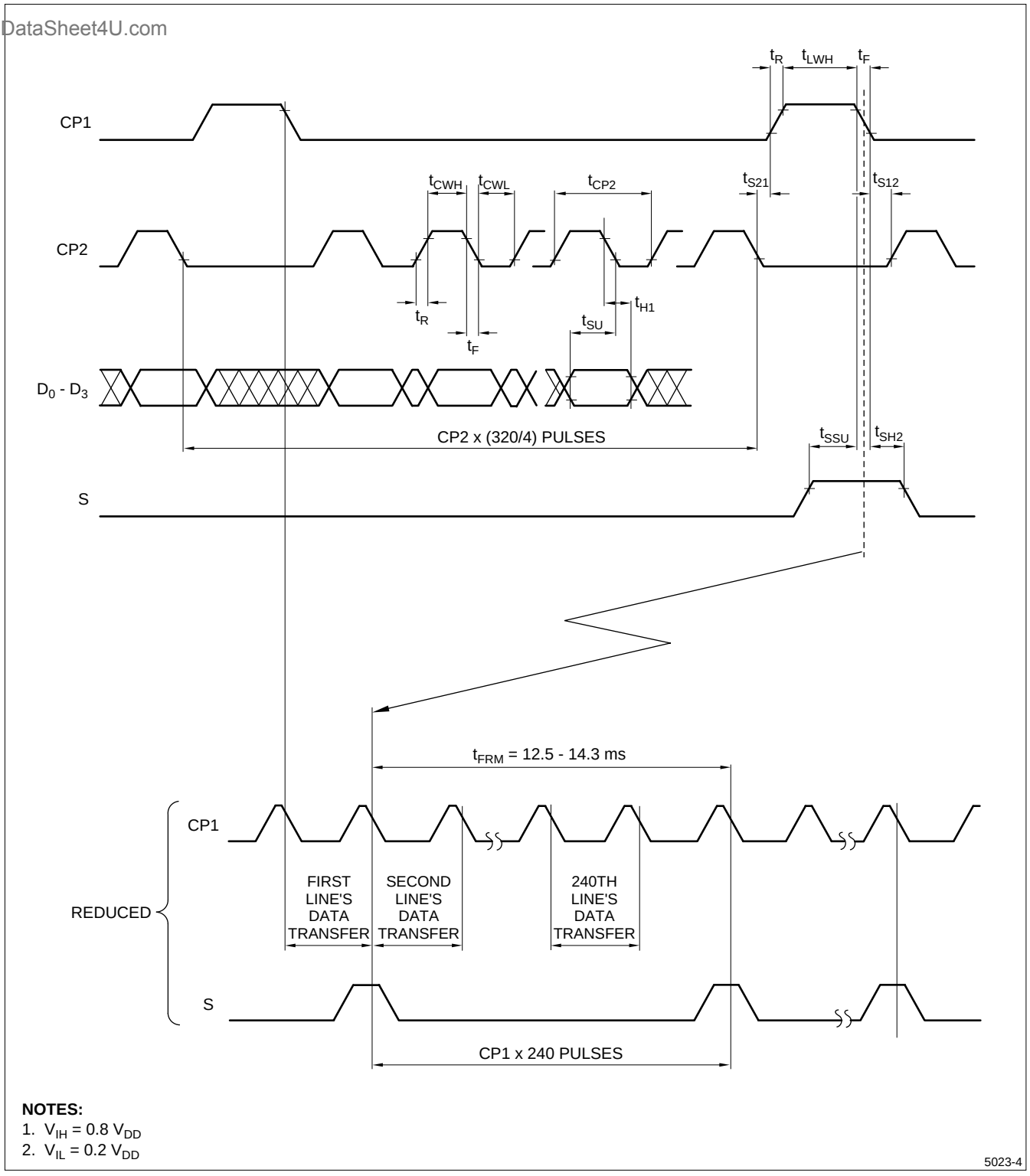


Figure 4. Data Input Timing

INTERFACE TIMING RATINGS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
t_{FRM}	Frame Cycle	12.5	–	14.3	s
t_{CP2}	CP2 Clock Cycle	170	–	–	ns
t_{CWH}	'H' Level Clock Width	100	–	–	ns
t_{CWL}	'L' Level Clock Width	100	–	–	ns
t_{LWH}	'H' Level Latch Clock Width	100	–	–	ns
t_{SU}	Data Setup Time	80	–	–	ns
t_{H1}	Data Hold Time	80	–	–	ns
t_{s12}	CP2 ↑ Clock Allowance Time From CP1 ↓	0	–	–	ns
t_{s21}	CP1 ↑ Clock Allowance Time From CP2 ↓	0	–	–	ns
t_R, t_F	Clock Rise/Fall Time	–	–	50	ns
t_{SSU}	S Signal Data Setup Time	100	–	–	ns
t_{SH2}	S Signal Data Hold Time	100	–	–	ns



NOTES:
1. $V_{IH} = 0.8\ V_{DD}$
2. $V_{IL} = 0.2\ V_{DD}$

Figure 5. Interface Timing Chart

UNIT DRIVING METHOD

Circuit Configuration

Figure 1 shows the block diagram of the Unit's circuitry.

Display Face Configuration

The display face electrically consists of a signal display segment of 320 × 240 dots.

Input Data and Control Signal

The LCD driver is 80 bits LSI, consisting of shift registers, latch circuits, and LCD driver circuits.

Display data which are externally divided into data for each row (320 dots) is sequentially transferred in the form of 4-bit parallel data through shift registers by Clock Signal CP2 from the left top of the display face.

When data of one row (320 dots) have been input, they are latched in the form of parallel data for 320 lines of signal electrodes by Latch Signal CP1. Then the corresponding drive signal is transmitted to the 320 lines of column electrodes of the LCD panel by the LCD drive circuits.

At this time, scan startup signal S is transferred from the scan signal driver to the first row of scan electrodes, and the contents of the data signals are displayed on the first rows of the display face according to the combinations of voltages applied to the scan and signal electrodes of the LCD.

While the first rows of data are being displayed, the second rows of data are entered. When 320 dots of data have been transferred, then latched, on the falling edge of CP1 clock, the display face proceeds to the second rows of display.

Such data input is repeated up to the 240th row of each display segment, from upper to lower rows, to complete one frame of display using the time-sharing method. Then data input proceeds to the next display face.

Scan startup signal S generates scan signal to drive horizontal electrodes. To avoid flickering, drive the unit at 70 – 80 Hz/frame.

Since DC voltage, if applied to the LCD panel, causes a chemical reaction which deteriorates the LCD panel, invert the drive waveform to prevent the generation of such DC voltage. To prevent such a problem, AC waveform circuit generated by counting CP1 (M generator) is built into this circuit.

Because of the characteristics of the CMOS driver LSI, the power consumption of the unit goes up as the operating frequency CP2 increases. Thus, the driver LSI applies the system of transferring 4-bit parallel data through the four lines of shift resistors to reduce the data transfer speed CP2. This system minimizes power consumption of the unit.

In this circuit configuration, 4-bit display data are input to data input pins D_0 – D_3.

The LCD unit also adopts a bus line system for data input to minimize the power consumption. In this system, the data input terminal of each driver LSI is activated only when relevant data input is fed.

Data input for column electrodes of both the upper and the lower display segment and chip select of driver LSI are made as follows:

- The driver LSI at the left end of the display face is first selected, and the adjacent driver LSI of the right side is selected when 80 dots data (20 CP2) is fed. This process continues sequentially until data is fed to the driver LSI at the right end of the display face.
- This process is immediately followed at the column driver's LSIs of both the upper and the lower display segments. Thus, data input must be fed through 4-bit bus line sequentially from the left end of the display face.

Since this graphic display unit contains no refresh RAM, it requires data and timing pulse inputs even for static display.

The timing chart of input signals is shown in Figure 5.

OPTICAL CHARACTERISTICS (V_{DD} = 5.0 V, t_A = 25°C)

The following specifications show the optical characteristics when the viewing angle obtaining the maximum contrast (ϕ) is adjusted to 0 degrees. The optical characteristics are detected when the LCD applied voltage waveforms are at the highest frequency (the most critical condition for the characteristics of the LCD).

SYMBOL	PARAMETER	CONDITION		MIN.	TYP.	MAX.	UNIT	NOTE
$\theta_2 - \theta_1$	Viewing Angle Range	ϕ = 0° $\theta_1 < \theta_2$	$C_O \geq 4.0$	60	–	–	degrees	1
θ_1			C_O = 4.0	–	–	–30		
θ_2				25	–	–		
$\theta_2 - \theta_1$		ϕ = 90° $\theta_1 < \theta_2$	$C_O \geq 4.0$	65	–	–		
θ_1			C_O = 4.0	–	–	–35		
θ_2				25	–	–		
C_O	Contrast Ratio	θ = 0°, ϕ = 0°		8.0	10.0	–	–	2
t_R	Response Speed – Rise	θ = 0°, ϕ = 0°		–	100	150	ms	3
t_D	Response Speed – Decay	θ = 0°, ϕ = 0°		–	150	200	ms	

NOTES:

1. The viewing angle is defined in Figure 6.
2. Contrast Ratio is calculated by using the following formula when the waveform voltage (Figure 8) is applied in optical characteristics test method (Figure 7):

$$\text{Contrast Ratio} = \frac{\text{Photodetector output voltage with non–select waveform being applied}}{\text{Photodetector output voltage with select waveform being applied}}$$

3. The response characteristics of photodetector output are measured as shown in Figure 8, assuming that input signals are applied to select and deselect the dots to be measured, in the optical characteristics test method shown in Figure 7.

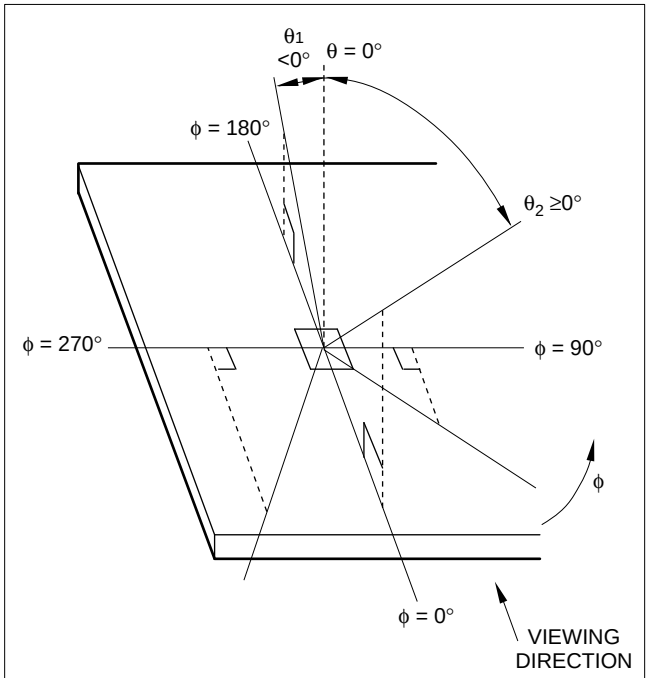


Figure 6. Definition of Viewing Angle

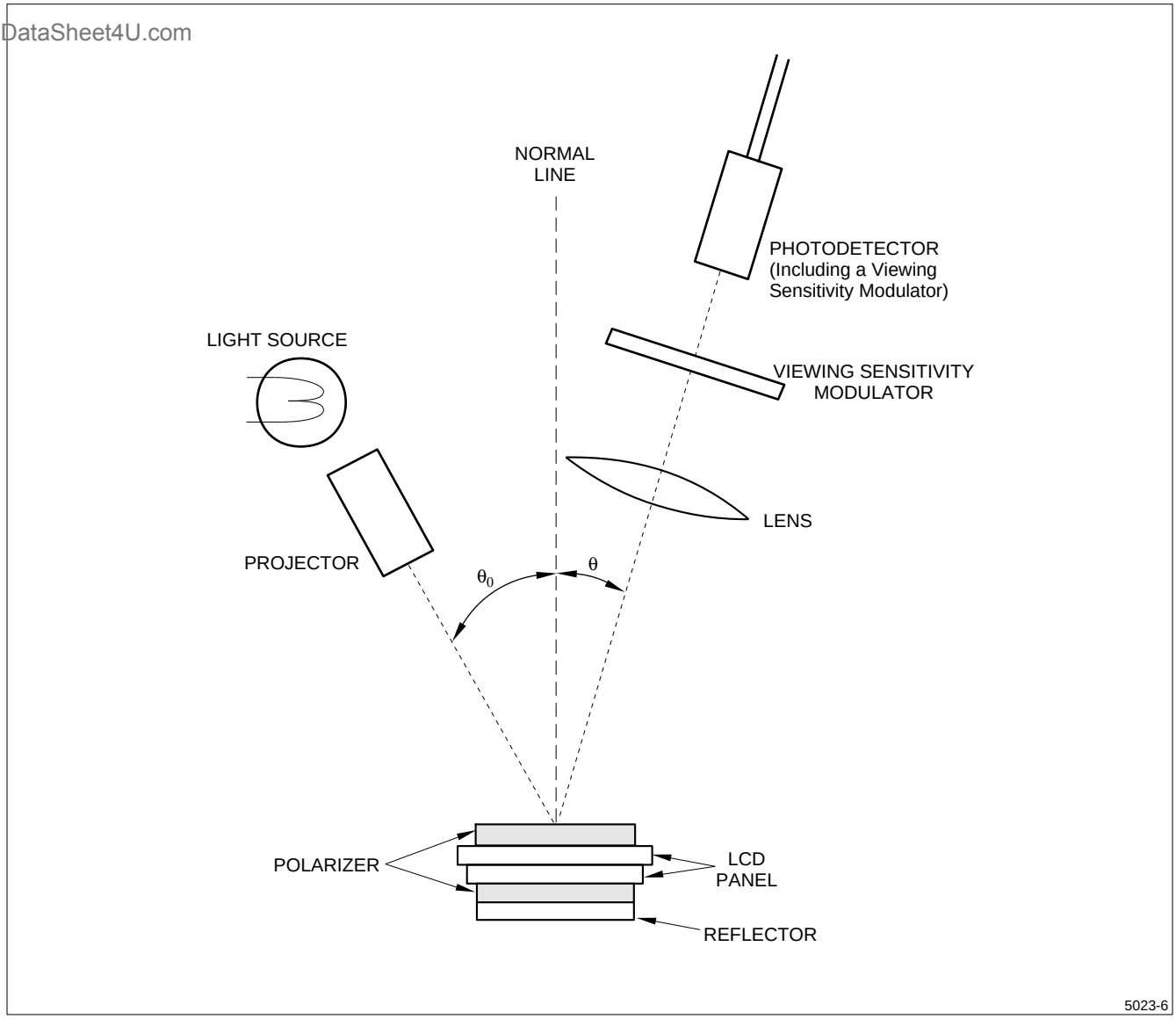


Figure 7. Optical Characteristics Test Method

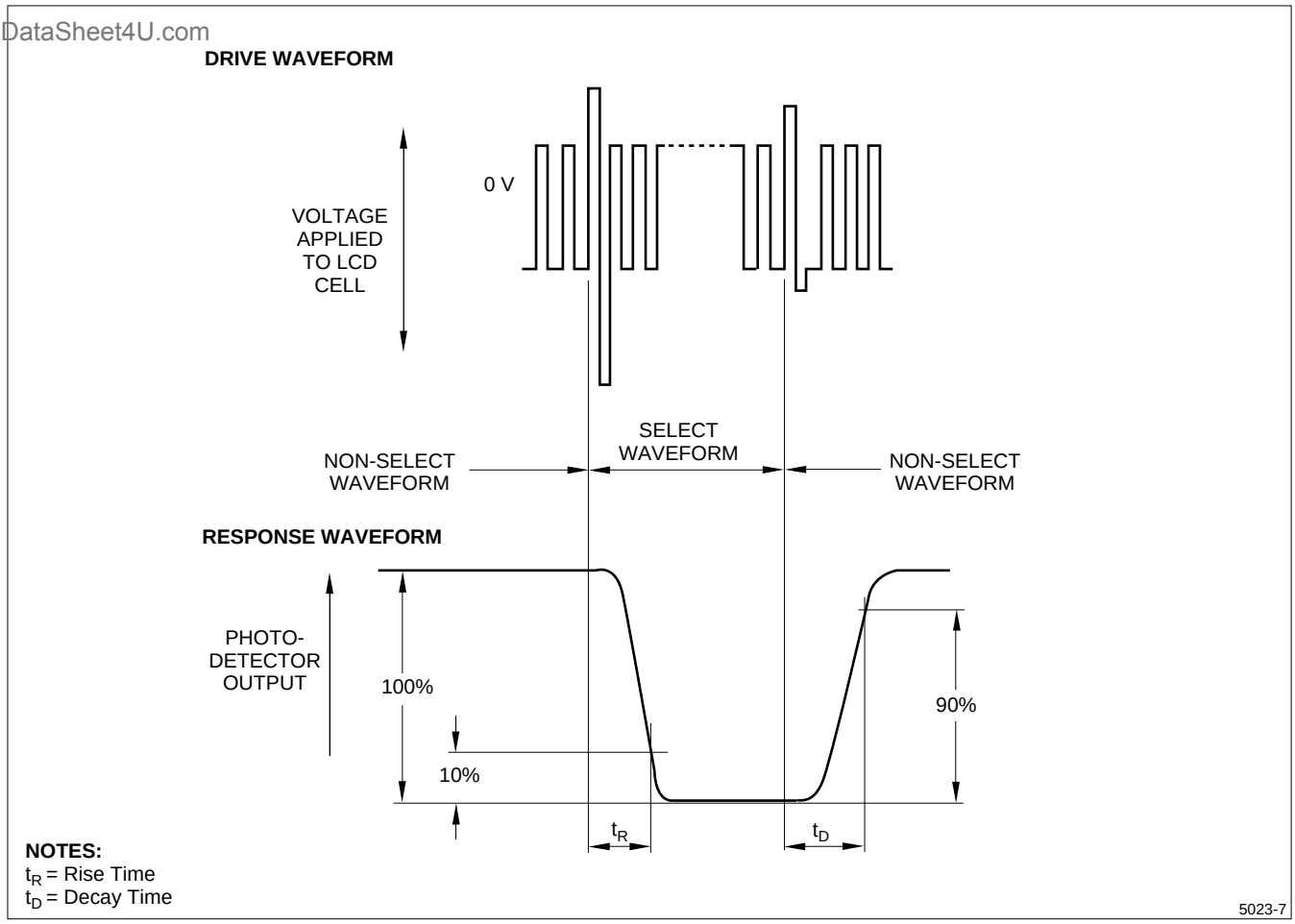


Figure 8. Definition of Response Time

PRECAUTIONS

- This unit's viewing angle is illustrated in Figure 9 and as follows:
  - θ_1 < viewing angle < θ_2 ($\theta_1 < 0°$, $\theta_2 \geq 0°$) Consider the optimum viewing conditions according to the purpose when installing the unit.

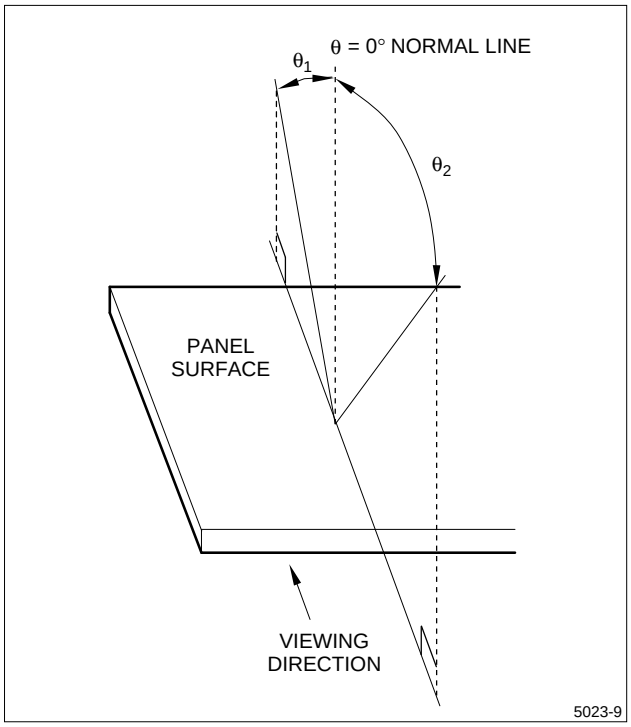


Figure 9. Dot Matrix LCD Viewing Angle

This unit is installed using mounting tabs at the four corners of PCB or bezel. During installation, avoid undue stress on the unit such as twisting or bending. A transparent acrylic resin board or other type of protective panel should be attached to the front of the unit to protect the polarizer, LCD cells, etc.

- Since the front polarizer is easily damaged, use care to not scratch the face.
- If the surface of the LCD cells need cleaning, wipe it with a soft cloth.
- Wipe liquid off immediately since it can cause color changes and staining.
- The LCD is made of glass plates. Use care when handling it to avoid breakage.
- This unit contains CMOS LSIs which are sensitive to electrostatic charges. The following measures should be taken to protect the unit from electrostatic discharge:
  - Ground the metallic case of the main system (contact of the unit and main system).
  - Insulate the unit and main system by attaching insulating washers made of bakelite or nylon.
- The unit should be driven according to the specified ratings to avoid malfunction or permanent damage. DC voltage drive leads to rapid deterioration of LC, so ensure that the drive is alternating waveform by continuous application of the signal M. Avoid latch-up of driver LSIs and application of DC voltage to the LCD panel by following the ON/OFF sequence shown in Figure 10.
- Do not expose the unit to direct sunlight, strong ultraviolet light, etc., for prolonged periods.
- Store the unit at normal room temperature to prevent the LC from converting to liquid (due to excessive temperature changes).
- Do not disassemble the unit.

WARNING: Avoid using any materials which emit gas from epoxy resin (Amines' hardener) and silicon adhesive agent (dealcohol or deoxym) to prevent polarizer color change caused by gas.

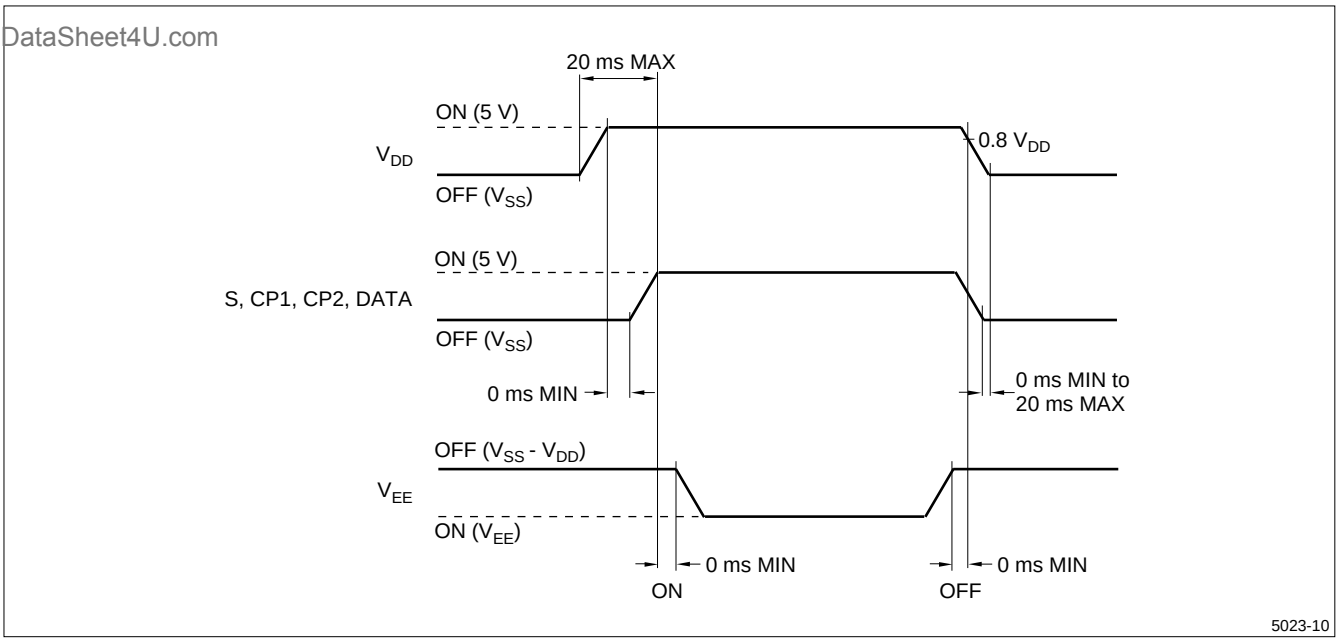
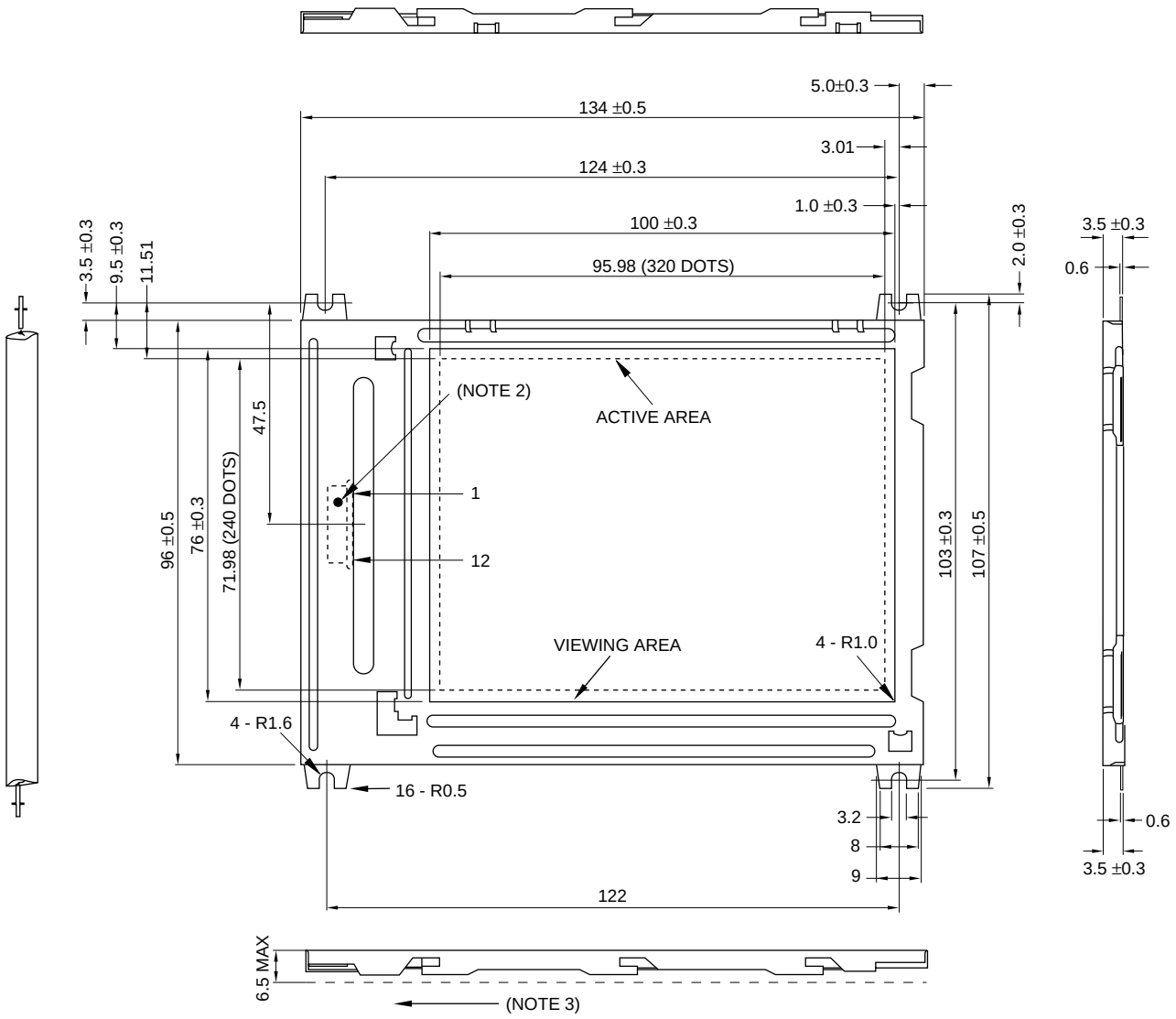
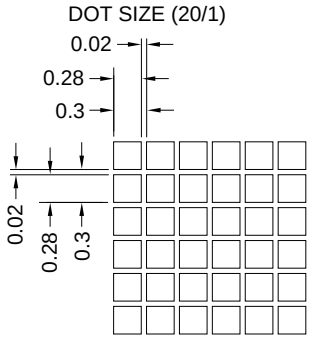


Figure 10. Power ON/OFF Sequence

OUTLINE DIMENSIONS





PIN #	SIGNAL	PIN #	SIGNAL
1	S	7	D_0
2	CP_1	8	D_1
3	CP_2	9	D_2
4	V_{DD}	10	D_3
5	V_{SS}	11	VR_1
6	V_{EE}	12	VR_2

NOTES:
1. Bezel is plated with white-zinc.
2. Connector: 52103-1217 (Molex).
3. Inserting direction of the flat cable.

5023-11