NEC

MOS INTEGRATED CIRCUIT

μPD424100

4 M-BIT DYNAMIC RAM
4 M-WORD BY 1-BIT, FAST PAGE MODE

DESCRIPTION

The μPD424100 is a 4 194 304 words by 1 bit dynamic CMOS RAM. The fast page mode capability realize high speed access and low power consumption.

These are packed in 26-pin plastic TSOP, 26-pin plastic SOJ and 20-pin plastic ZIP.

FEATURES

- 4 194 304 words by 1 bit organization
- Single +5.0 V±10 % power supply
- Fast access and cycle time

Part number	Power consumption		Access time (MAX.)	R/W cycle time (MIN.)	Fast page mode cycle time (MIN.)
	Active (MAX.)	Standby(MAX.)			
μPD424100-60	660 mW	5.5 mW (CMOS level input)	60 ns	120 ns	40 ns
μPD424100-70	550 mW		70 ns	140 ns	45 ns
μPD424100-80	495 mW		80 ns	160 ns	50 ns
μPD424100-10	440 mW		100 ns	190 ns	60 ns

- 1 024 refresh cycles/16 ms
- $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$ only refresh, Hidden refresh
- Multiplexed address inputs ····· Row address : A0 to A10, Column address : A0 to A10

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The mark ★ shows revised points.

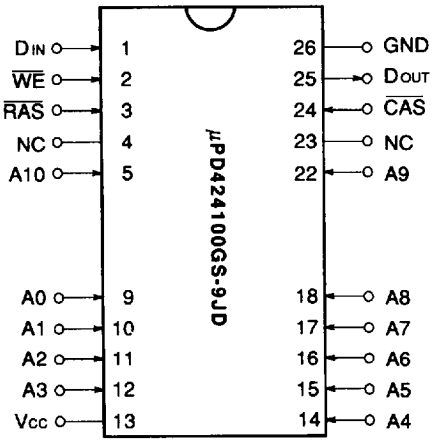
★ ORDERING INFORMATION

Part number	Access time (MAX.)	Package	Quality grade
μPD424100GS-60-9JD	60 ns	26-pin Plastic TSOP (300 mil)	Standard
μPD424100GS-70-9JD	70 ns		
μPD424100GS-80-9JD	80 ns		
μPD424100GS-10-9JD	100 ns		
μPD424100GS-60-9KD	60 ns	26-pin Plastic TSOP (300 mil) Reverse bent	
μPD424100GS-70-9KD	70 ns		
μPD424100GS-80-9KD	80 ns		
μPD424100GS-10-9KD	100 ns		
μPD424100LA-60	60 ns	26-pin Plastic SOJ (300 mil)	
μPD424100LA-70	70 ns		
μPD424100LA-80	80 ns		
μPD424100LA-10	100 ns		
μPD424100V-60	60 ns	20-pin Plastic ZIP (400 mil)	
μPD424100V-70	70 ns		
μPD424100V-80	80 ns		
μPD424100V-10	100 ns		

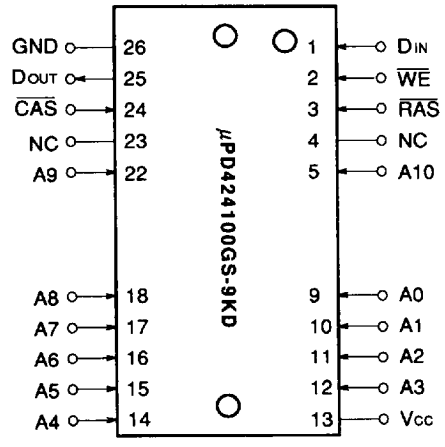
Please refer to "Quality grade on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

PIN CONFIGURATIONS (Marking Side) ★

26-pin Plastic TSOP (300 mil)

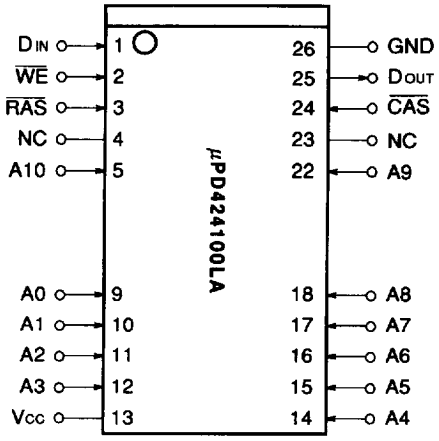


Reverse bent

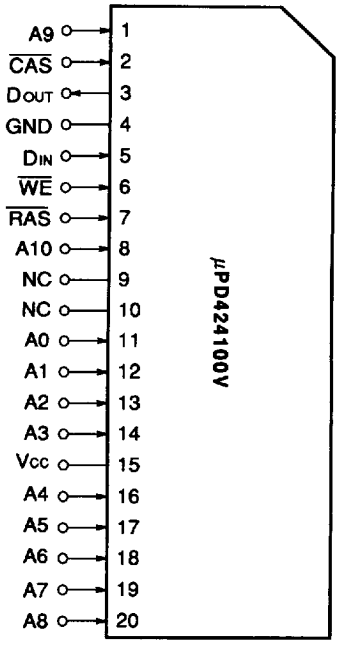


A0 to A10	: Address Inputs
DIN	: Data Input
DOUT	: Data Output
$\overline{RAS}$	: Row Address Strobe
$\overline{CAS}$	: Column Address Strobe
$\overline{WE}$	: Write Enable
VCC	: Supply Voltage
GND	: Ground
NC	: No Connection

26-pin Plastic SOJ (300 mil)



20-pin Plastic ZIP (400 mil)



A0 to A10	: Address Inputs
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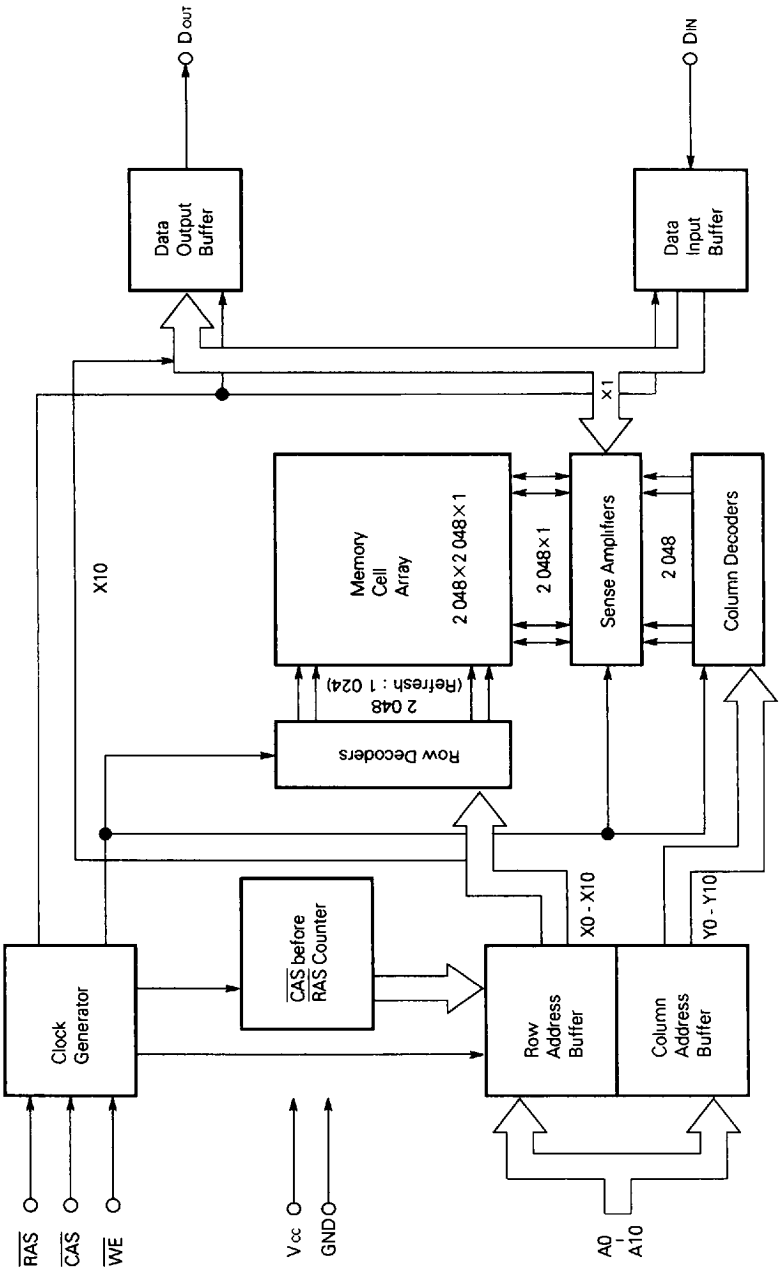
GND	: Ground
NC	: No Connection

BLOCK DIAGRAM ★



★ INPUT/OUTPUT PIN FUNCTIONS

The μPD424100 has input pins $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, A0 to A10, D_{IN} and output pin D_{OUT}.

Pin name	Input/ Output	Function
$\overline{RAS}$ (Row address strobe)	Input	$\overline{RAS}$ activates the sense amplifier by latching a row address and selecting a corresponding word line. It refreshes memory cell array of one line selected by the row address. It also selects the following function. • $\overline{CAS}$ before $\overline{RAS}$ refresh.
$\overline{CAS}$ (Column address strobe)		$\overline{CAS}$ activates data input/output circuit by latching column address and selecting a digit line connected with the sense amplifier.
A0 to A10 (Address input)		Address bus. Input total 22-bit of address signal, upper 11-bit and lower 11-bit in sequence (address multiplex method). Therefore, one word is selected from 4 194 304-word by 1-bit memory cell array. In actual operation, latch row address by specifying row address and activating $\overline{RAS}$. Then, switch the address bus to column address and activate $\overline{CAS}$. Each address is taken into the device when $\overline{RAS}$ and $\overline{CAS}$ are activated. Therefore, the address input setup time (t_{ASR}, t_{ASC}) and hold time (t_{RAH}, t_{CAH}) are specified for the activation of $\overline{RAS}$ and $\overline{CAS}$.
$\overline{WE}$ (Write enable)		Write control signal. Write operation is executed by activating $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$.
D_{IN} (Data input)		Data bus. D_{IN} is used to input data.
D_{OUT} (Data output)	Output	Data bus. D_{OUT} is used to output data.

ELECTRICAL SPECIFICATIONS Notes 1, 2

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Rating	Unit
Voltage on any pin relative to GND	V_T		−1.0 to +7.0	V
Supply voltage	V_{CC}		−1.0 to +7.0	V
Output current	I_O		50	mA
Power dissipation	P_D		1	W
Operating temperature	T_{opt}		0 to +70	°C
Storage temperature	T_{stg}		−55 to +125	°C

Remark Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{CC}		4.5	5.0	5.5	V
High level input voltage	V_{IH}		2.4		V_{CC} +1.0	V
Low level input voltage	V_{IL}		−1.0		+0.8	V
Ambient temperature	T_a		0		70	°C

CAPACITANCE (T_a = +25 °C, f = 1 MHz)

Parameter	Symbol	Test condition	MIN.	TYP.	MAX.	Unit
Input capacitance	C_{I1}	A0 to A10, D_{IN}			5	pF
	C_{I2}	$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$			7	pF
Data Output capacitance	C_O	D_{OUT}			7	pF

DC CHARACTERISTICS (Recommended Operating Conditions unless otherwise noted)

Parameter	Symbol	Test condition		MIN.	MAX.	Unit	Notes
Operating current	I_{CC1}	$\overline{RAS}$, $\overline{CAS}$ Cycling $t_{RC} = t_{RC(MIN)}$ I_O = 0 mA	t_{RAC} = 60 ns		120	mA	3,4
			t_{RAC} = 70 ns		100		
			t_{RAC} = 80 ns		90		
			t_{RAC} = 100 ns		80		
Standby current	I_{CC2}	$V_{IH(MIN)} \leqq \overline{RAS}, \overline{CAS}$	I_O = 0 mA		2	mA	
		V_{CC}–0.2 V $\leqq \overline{RAS}, \overline{CAS}$	I_O = 0 mA		1		
$\overline{RAS}$ only refresh current	I_{CC3}	$\overline{RAS}$ Cycling $V_{IH(MIN)} \leqq \overline{CAS}$ $t_{RC} = t_{RC(MIN)}$ I_O = 0 mA	t_{RAC} = 60 ns		120	mA	3,4
			t_{RAC} = 70 ns		100		
			t_{RAC} = 80 ns		90		
			t_{RAC} = 100 ns		80		
Operating current (Fast page mode)	I_{CC4}	$\overline{CAS}$ Cycling $\overline{RAS} \leqq V_{IL(MAX)}$ $t_{PC} = t_{PC(MIN)}$ I_O = 0 mA	t_{RAC} = 60 ns		90	mA	3,4
			t_{RAC} = 70 ns		80		
			t_{RAC} = 80 ns		70		
			t_{RAC} = 100 ns		60		
$\overline{CAS}$ before $\overline{RAS}$ refresh current	I_{CC5}	$\overline{RAS}$ Cycling $t_{RC} = t_{RC(MIN)}$ I_O = 0 mA	t_{RAC} = 60 ns		120	mA	3,4
			t_{RAC} = 70 ns		100		
			t_{RAC} = 80 ns		90		
			t_{RAC} = 100 ns		80		
Input leakage current	$I_{I(L)}$	V_I = 0 to 5.5 V all other pins except for testing pin = 0 V		–10	+10	μA	
Output leakage current	$I_{O(L)}$	Outputs are disabled (Hi-Z) V_O = 0 to 5.5 V		–10	+10	μA	
High level output voltage	V_{OH}	I_O = –5.0 mA		2.4		V	
Low level output voltage	V_{OL}	I_O = +4.2 mA			0.4	V	

AC CHARACTERISTICS ★

(Recommended Operating Conditions unless otherwise noted) Notes 5, 6

(1/2)

Parameter	Symbol	t_{RAC} = 60 ns		t_{RAC} = 70 ns		t_{RAC} = 80 ns		t_{RAC} = 100 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Random Read or Write Cycle Time	t_{RC}	120		140		160		190		ns	7
Read Write Cycle Time	t_{RWC}	145		165		185		220		ns	7
Fast Page Mode Cycle Time (Read or Write)	t_{PC}	40		45		50		60		ns	7
Read Modify Write Cycle Time (Fast Page Mode)	t_{PRWC}	65		70		75		90		ns	7
Access Time from $\overline{RAS}$	t_{RAC}		60		70		80		100	ns	8, 9
Access Time from $\overline{CAS}$ (Falling Edge)	t_{CAC}		15		20		20		25	ns	8, 9
Access Time from Column Address	t_{AA}		30		35		40		50	ns	8, 9
Access Time from $\overline{CAS}$ Precharge	t_{ACP}		35		40		45		55	ns	9
$\overline{RAS}$ to Column Address Delay Time	t_{RAD}	15	30	15	35	17	40	17	50	ns	8
$\overline{CAS}$ to Data Setup Time	t_{CLZ}	0		0		0		0		ns	9
Output Buffer Turn-off Delay Time ($\overline{CAS}$)	t_{OFF}	0	15	0	15	0	20	0	25	ns	10
Transition Time (Rise and Fall)	t_T	3	50	3	50	3	50	3	50	ns	
$\overline{RAS}$ Precharge Time	t_{RP}	50		60		70		80		ns	
$\overline{RAS}$ Pulse Width (Random Read, Write Cycle)	t_{RAS}	60	10 000	70	10 000	80	10 000	100	10 000	ns	
$\overline{RAS}$ Pulse Width (Fast Page Mode)	t_{RASP}	60	125 000	70	125 000	80	125 000	100	125 000	ns	
$\overline{RAS}$ Hold Time	t_{RSH}	20		20		20		25		ns	
$\overline{CAS}$ Pulse Width	t_{CAS}	15	10 000	20	10 000	20	10 000	25	10 000	ns	
$\overline{CAS}$ Hold Time	t_{CSH}	60		70		80		100		ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RCD}	20	40	20	50	25	60	25	75	ns	8
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	10		10		10		10		ns	11
$\overline{CAS}$ Precharge Time	t_{CPN}	10		10		10		10		ns	
$\overline{CAS}$ Precharge Time (Fast Page Mode)	t_{CP}	10		10		10		10		ns	
$\overline{RAS}$ Precharge $\overline{CAS}$ Hold Time	t_{RPC}	10		10		10		10		ns	
$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	t_{RHCP}	35		40		45		55		ns	
Row Address Setup Time	t_{ASR}	0		0		0		0		ns	
Row Address Hold Time	t_{RAH}	10		10		12		12		ns	
Column Address Setup Time	t_{ASC}	0		0		0		0		ns	
Column Address Hold Time	t_{CAH}	15		15		15		20		ns	
Column Address Lead Time Referenced to $\overline{RAS}$	t_{RAL}	30		35		40		50		ns	
Read Command Setup Time	t_{RCS}	0		0		0		0		ns	
Read Command Hold Time Referenced to $\overline{RAS}$	t_{RRH}	10		10		10		10		ns	12
Read Command Hold Time Referenced to $\overline{CAS}$	t_{RCH}	0		0		0		0		ns	12
Write Command Hold Time Referenced to $\overline{CAS}$	t_{WCH}	15		15		15		20		ns	13
Write Command Pulse Width	t_{WP}	15		15		15		20		ns	13
Data-in Setup Time	t_{DS}	0		0		0		0		ns	14
Data-in Hold Time	t_{DH}	15		15		15		20		ns	14
$\overline{WE}$ Command Setup Time	t_{WCS}	0		0		0		0		ns	15
$\overline{CAS}$ to $\overline{WE}$ Delay Time	t_{CWD}	20		20		20		25		ns	15
$\overline{RAS}$ to $\overline{WE}$ Delay Time	t_{RWD}	60		70		80		100		ns	15

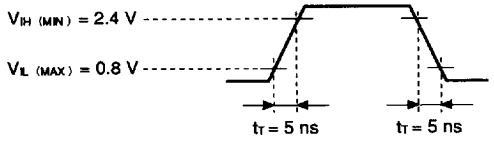
(2/2)

Parameter	Symbol	t_{RAC} = 60 ns		t_{RAC} = 70 ns		t_{RAC} = 80 ns		t_{RAC} = 100 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
$\overline{CAS}$ Precharge Delay Time Referenced to $\overline{WE}$ (Fast Page Mode)	t_{CPWD}	55		60		70		85		ns	15
Column Address Delay Time Referenced to $\overline{WE}$	t_{AWD}	30		35		40		50		ns	15
Write Command Lead Time Referenced to $\overline{RAS}$	t_{RWL}	20		20		20		25		ns	
Write Command Lead Time Referenced to $\overline{CAS}$	t_{CWL}	15		15		15		20		ns	
$\overline{CAS}$ Setup Time for $\overline{CAS}$ before $\overline{RAS}$ Refresh	t_{CSR}	10		10		10		10		ns	
$\overline{CAS}$ Hold Time for $\overline{CAS}$ before $\overline{RAS}$ Refresh	t_{CHR}	15		15		15		20		ns	
$\overline{WE}$ Setup Time	t_{WSR}	10		10		10		10		ns	
$\overline{WE}$ Hold Time	t_{WHR}	15		15		15		20		ns	
Refresh Time	t_{REF}		16		16		16		16	ms	

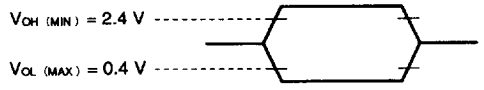
Notes

1. All voltages are referenced to GND.
2. An initial pause of 100 μs is required after power up followed by 8 $\overline{RAS}$ only refresh cycles before proper device operation is achieved. In case of using internal address refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ refresh cycles instead of 8 $\overline{RAS}$ only refresh cycles are required.
3. I_{CC1}, I_{CC3}, I_{CC4} and I_{CC5} depend on t_{RC} and t_{PC} Specified values are obtained with outputs open.
4. Address can be changed once or less while $\overline{RAS}$ = V_{IL} and $\overline{CAS}$ = V_{IH}.
5. AC measurements assume t_T = 5 ns.
6. AC Characteristics test condition

(1) Input timing specification



(2) Output timing specification



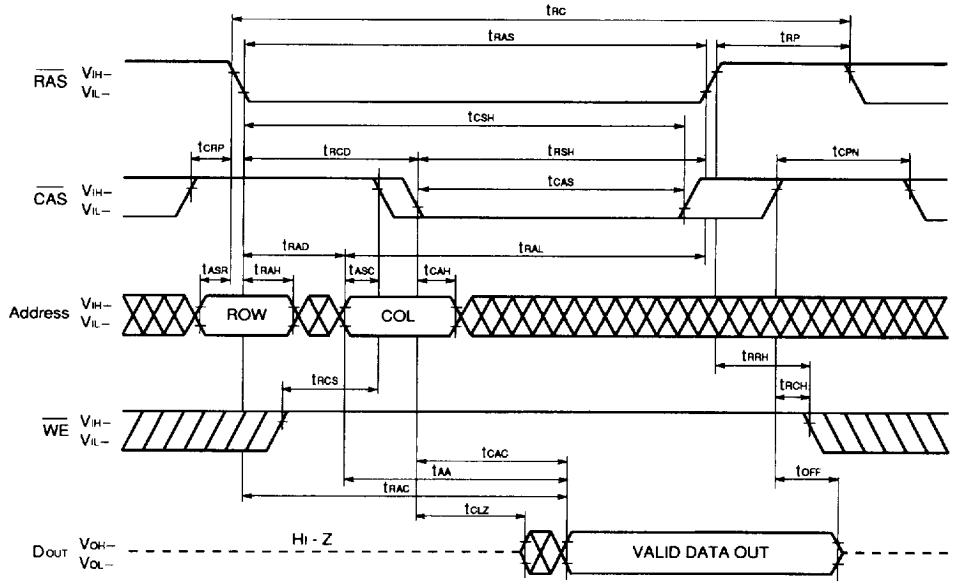
7. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range (T_a = 0 to 70 °C) is assured.
8. In random read cycle, the access time is changed by the conditions of t_{RAD} and t_{RCD} as follows.

CONDITION	ACCESS TIME
$t_{RAD} \leq t_{RAD\ (MAX.)}$ and $t_{RCD} \leq t_{RCD\ (MAX)}$	$t_{RAC\ (MAX)}$
$t_{RAD\ (MAX.)} \leq t_{RAD}$ and $t_{RCD} \leq t_{RCD\ (MAX.)}$	$t_{AA\ (MAX.)}$
$t_{RCD\ (MAX.)} \leq t_{RCD}$	$t_{CAC\ (MAX.)}$

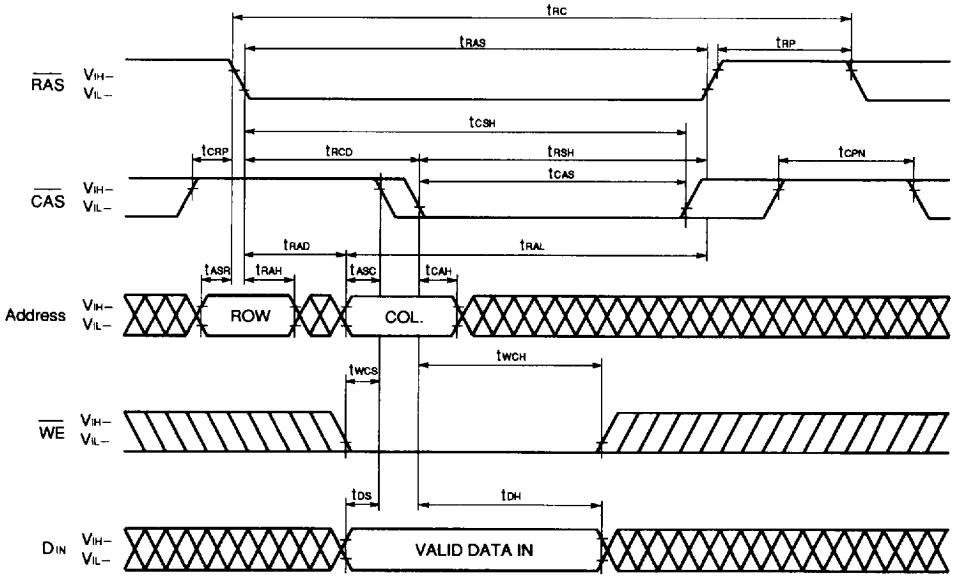
$t_{RAD\ (MAX)}$ and $t_{RCD\ (MAX.)}$ indicate the points which the access time changes and are not the limits of operation.

9. Loading conditions are 2 TTL and 100 pF.
10. $t_{OFF\ (MAX.)}$ defines the time at which the output achieves the open circuit condition and are not referenced to V_{OH} or V_{OL}.
11. $t_{CRP\ (MIN.)}$ requirement should be applicable for $\overline{RAS}$ / $\overline{CAS}$ cycles preceded by any cycles.
12. Either $t_{RCH\ (MIN.)}$ or $t_{RRH\ (MIN.)}$ must be satisfied for a read cycle.
13. $t_{WP\ (MIN.)}$ is applicable for late write cycle or read modify write cycle. In early write cycles, $t_{WCH\ (MIN)}$ should be satisfied.
14. This specification is referenced to $\overline{CAS}$ falling edge in early write cycles and to $\overline{WE}$ falling edge in late write or read modify write cycles.
15. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD} and t_{CPWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS\ (MIN.)} \leq t_{WCS}$, the cycle is an early write cycle and the data out pins will remain Hi-Z through the entire cycle. If $t_{RWD\ (MIN.)} \leq t_{RWD}$, $t_{CWD\ (MIN)} \leq t_{CWD}$, $t_{AWD\ (MIN.)} \leq t_{AWD}$ and $t_{CPWD\ (MIN.)} \leq t_{CPWD}$, the cycle is a read modify write cycle and condition of the data out (at access time) is indeterminate.

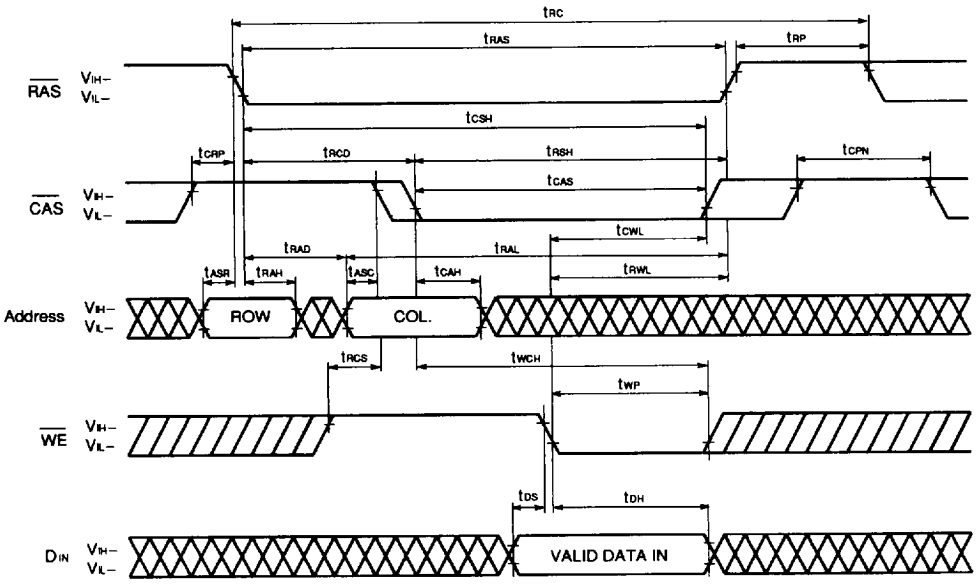
READ CYCLE



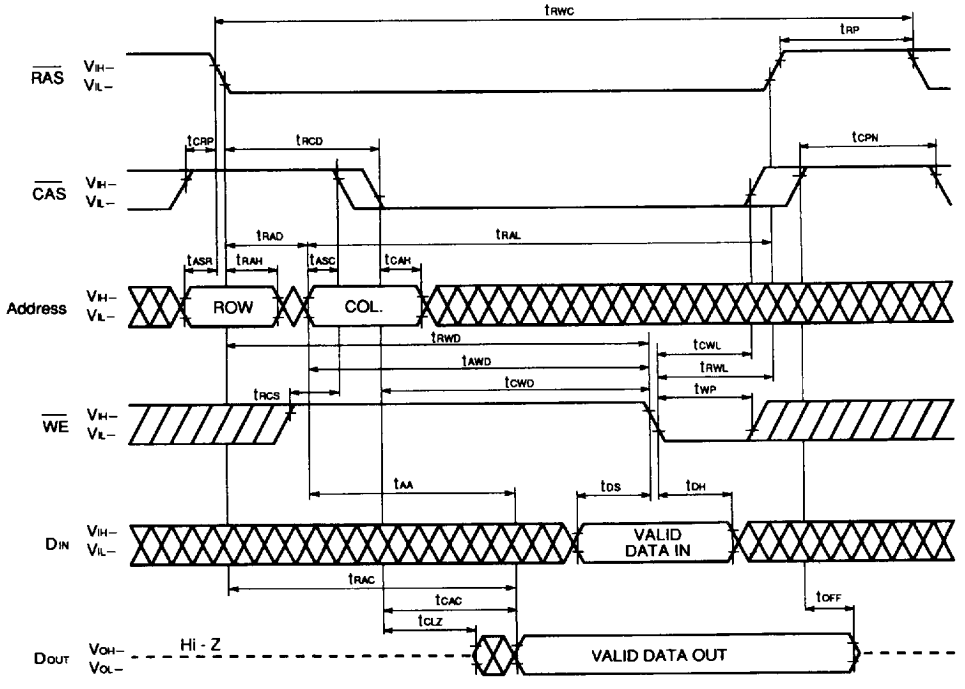
EARLY WRITE CYCLE



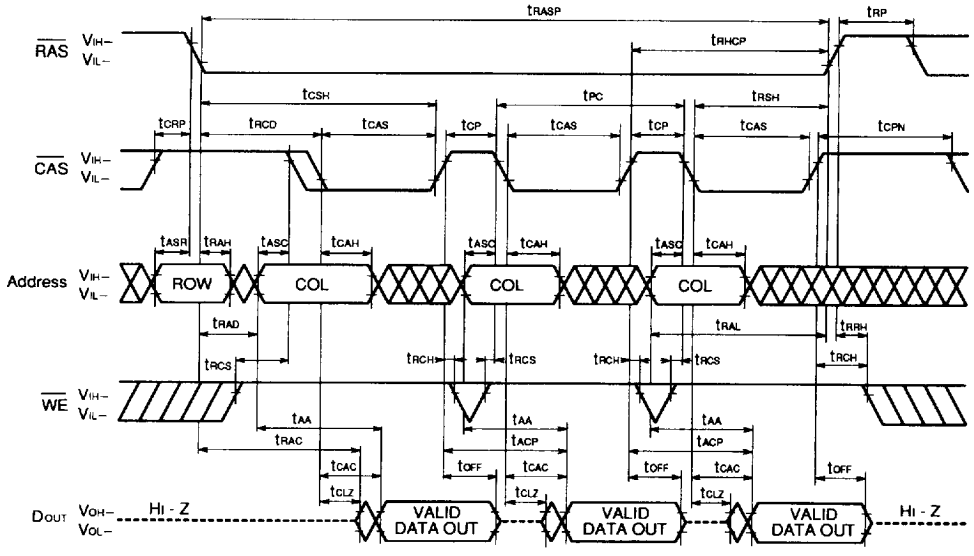
LATE WRITE CYCLE



READ MODIFY WRITE CYCLE

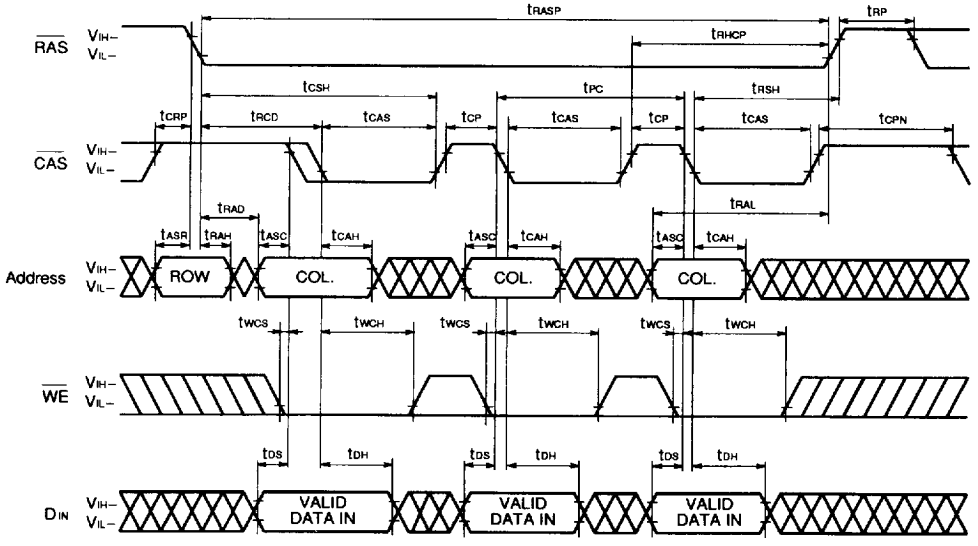


FAST PAGE MODE READ CYCLE



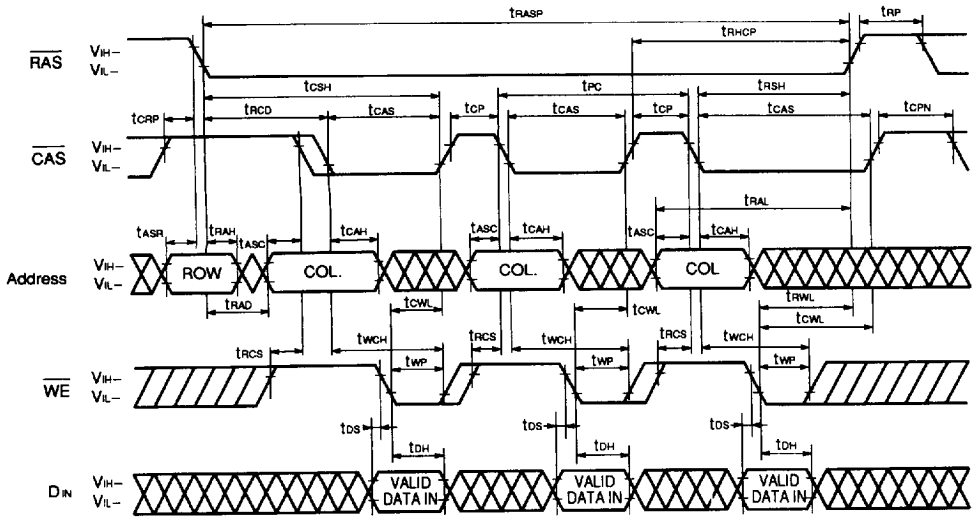
Remark In the fast page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle

FAST PAGE MODE EARLY WRITE CYCLE



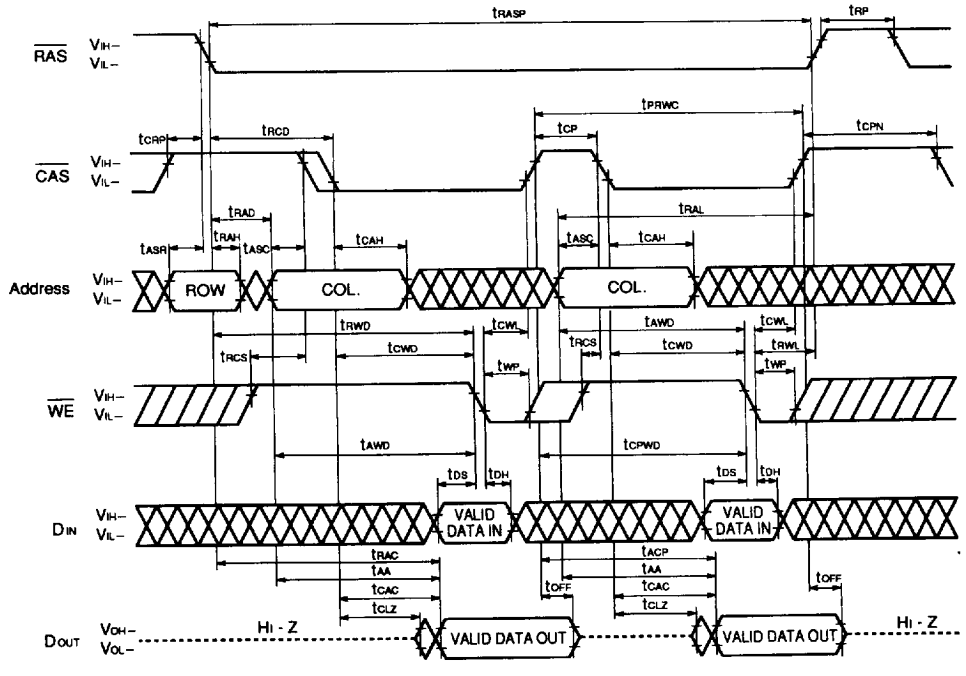
Remark In the fast page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle

FAST PAGE MODE LATE WRITE CYCLE



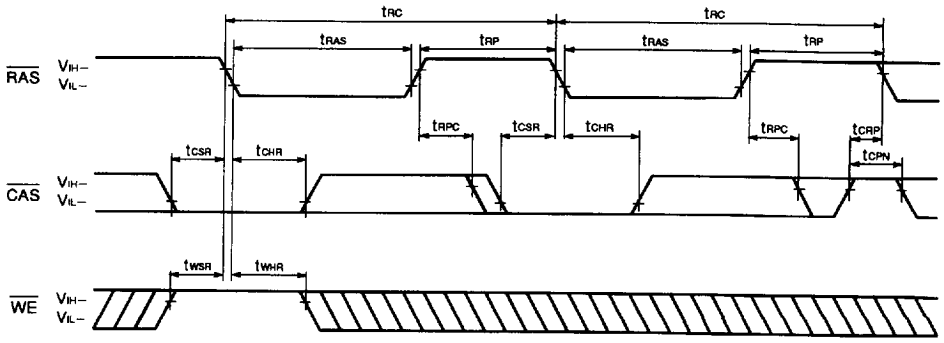
Remark In the fast page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

FAST PAGE MODE READ MODIFY WRITE CYCLE



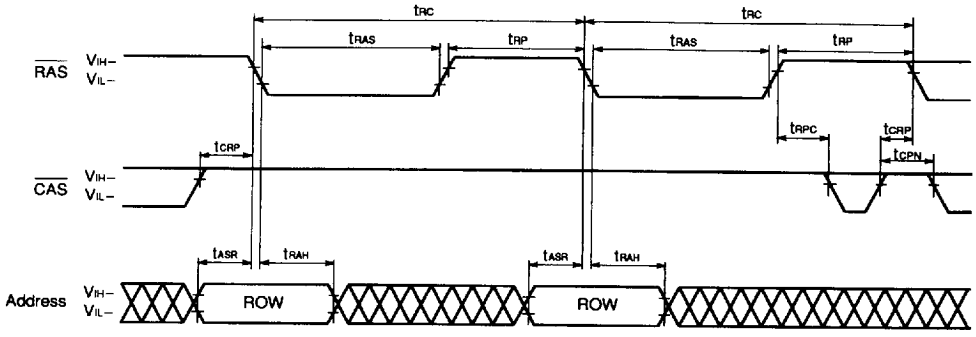
Remark In the fast page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

★ $\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE



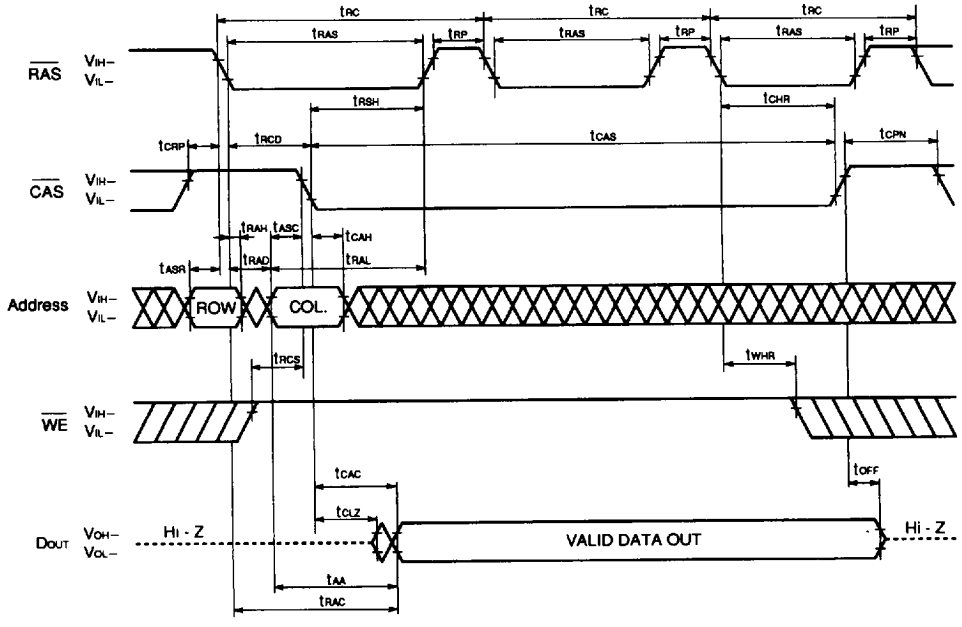
Remark Address, D_{IN} = Don't care D_{OUT} = Hi - Z

★ $\overline{RAS}$ ONLY REFRESH CYCLE



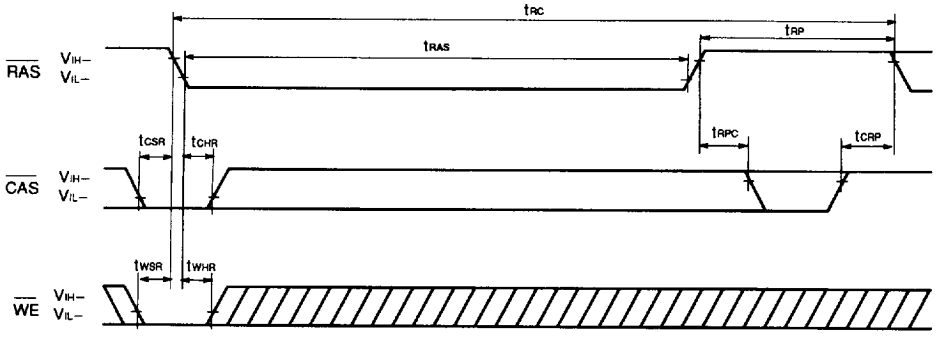
Remark $\overline{WE}$, D_{IN} = Don't care D_{OUT} = Hi - Z

HIDDEN REFRESH CYCLE



Remark D_{IN} = Don't care

TEST MODE SET CYCLE ($\overline{WE}$ AND $\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE)



Remark Address, D_{IN} = Don't care D_{OUT} = HI - Z

TEST MODE

TEST MODE is fast test function. On using this mode, test time is reduced to 1/8. In this TEST MODE, internal organization is 512 K words by 8 bits apparently. Don't care about the input levels of the $\overline{RAS}$ address input A10 and $\overline{CAS}$ address inputs A0, A10.

1. How to enter TEST MODE

Through TEST MODE SET CYCLE ($\overline{WE}$ and $\overline{CAS}$ before $\overline{RAS}$ refresh cycle), the device enters TEST MODE.

2. Write / Read in TEST MODE

Write data of "1" or "0" through D_{IN} by controlling address except for above-mentioned address. So equal data is written to all 8 bits. And read through D_{OUT} to check the written data. When all 8 bits are written rightly, the data is " 1 ". But wrong, data is " 0 ".

3. Refresh in TEST MODE

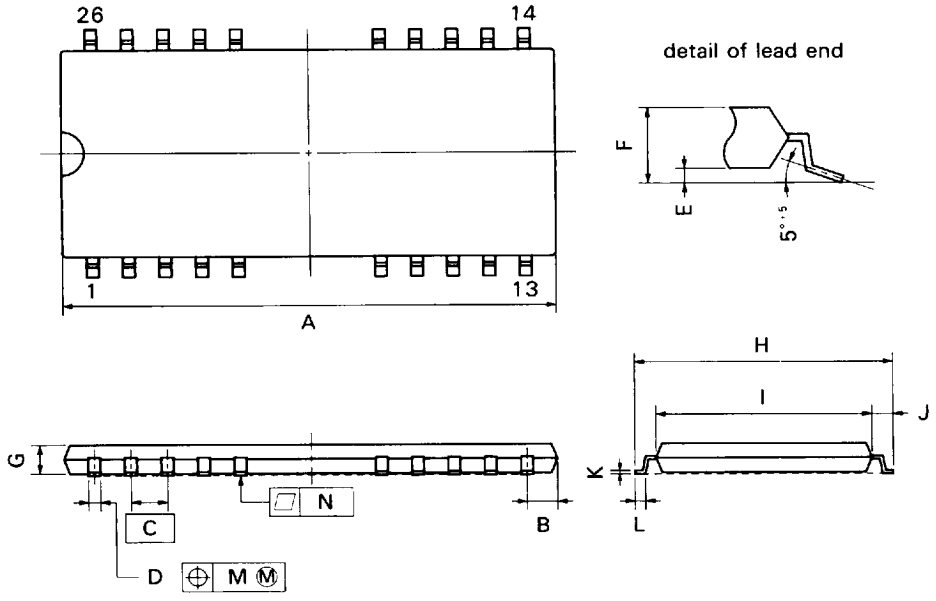
Use normal read cycle or $\overline{WE}$ and $\overline{CAS}$ before $\overline{RAS}$ refresh cycle.

4. How to exit from TEST MODE

Through $\overline{RAS}$ only refresh cycle or $\overline{CAS}$ before $\overline{RAS}$ refresh cycle, the device exits from TEST MODE.

PACKAGE DRAWINGS ★

26 PIN PLASTIC TSOP (300mil)



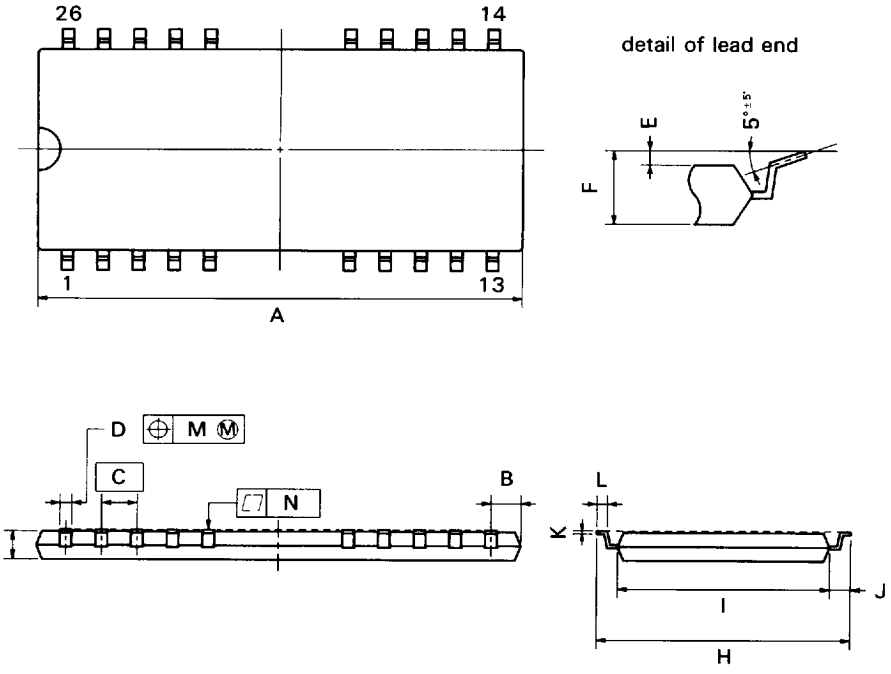
S26GS 50 9JD 1

NOTE

Each lead centerline is located within 0.21 mm (0.009 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	17.54 MAX.	0 691 MAX
B	1 18 MAX.	0 047 MAX
C	1 27 (T P)	0.050 (T.P.)
D	$0\ 40^{\pm 0\ 10}$	$0.016^{+0\ 004}_{-0\ 005}$
E	$0\ 05^{\ \pm 0\ 05}$	$0\ 002^{\ -0\ 002}$
F	1 13 MAX	0 045 MAX
G	1 0	0 039
H	$9.22^{\pm 0\ 2}$	$0.363^{\pm 0\ 008}$
I	$7\ 62^{\pm 0\ 1}$	$0\ 300^{\pm 0\ 004}$
J	$0\ 8^{\pm 0\ 2}$	$0.031^{+0\ 009}_{-0\ 008}$
K	$0\ 125^{+0\ 10}_{-0\ 05}$	$0\ 005^{+0\ 004}_{-0\ 002}$
L	$0\ 5^{\pm 0\ 1}$	$0\ 020^{+0\ 004}_{-0\ 005}$
M	0 21	0 009
N	0.10	0.004

26 PIN PLASTIC TSOP (300mil)



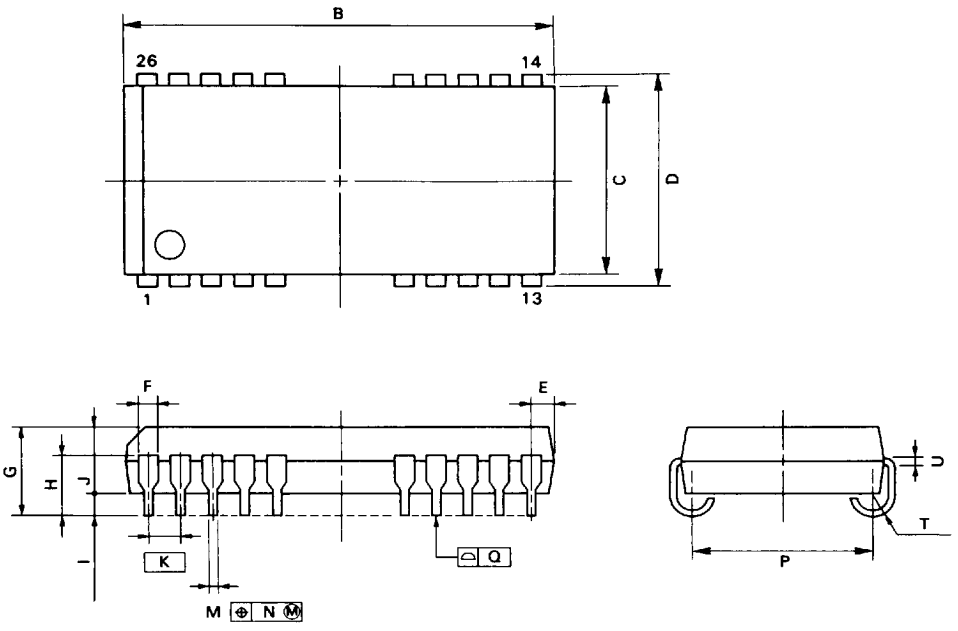
S26GS-50-9KD-1

NOTE

Each lead centerline is located within 0.21 mm (0.009 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	17.54 MAX.	0 691 MAX.
B	1.18 MAX.	0.047 MAX.
C	1.27 (T.P.)	0.050 (T.P.)
D	$0.40^{\pm 0\ 10}$	$0.016^{+0\ 004}_{-0\ 005}$
E	$0\ 05^{\pm 0\ 05}$	$0\ 002^{\pm 0\ 002}$
F	1 13 MAX	0 045 MAX
G	1 0	0 039
H	$9.22^{\pm 0\ 2}$	$0.363^{\pm 0\ 008}$
I	$7.62^{\pm 0\ 1}$	$0.300^{\pm 0\ 004}$
J	$0.8^{\pm 0\ 2}$	$0.031^{+0\ 008}_{-0\ 008}$
K	$0\ 125^{+0\ 10}_{-0\ 05}$	$0\ 005^{+0\ 004}_{-0\ 002}$
L	$0.5^{\pm 0\ 1}$	$0.020^{+0\ 004}_{-0\ 005}$
M	0.21	0.009
N	0 10	0.004

26PIN PLASTIC SOJ (300 mil)



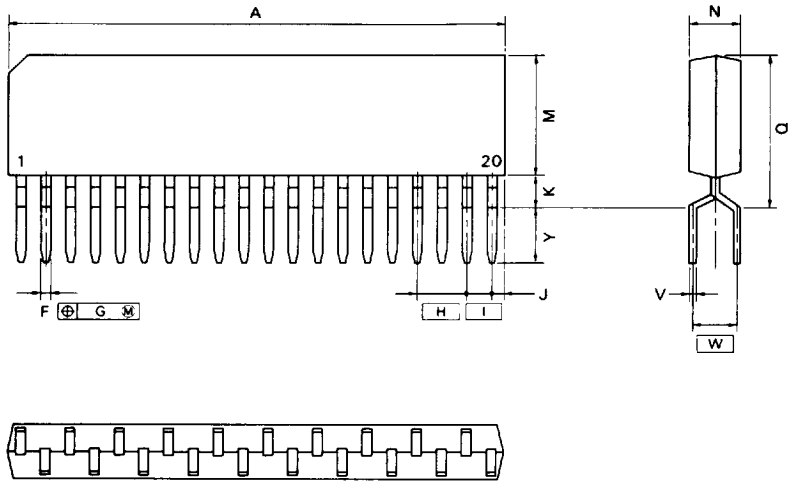
P26LA-50A-1

NOTE

Each lead centerline is located within 0.12 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
B	$17.4^{+0.2}_{-0.35}$	$0.685^{+0.008}_{-0.013}$
C	7.57	0.298
D	$8.47^{\pm0.2}$	$0.333^{+0.009}_{-0.008}$
E	$1.08^{\pm0.15}$	$0.043^{+0.006}_{-0.007}$
F	0.6	0.024
G	$3.5^{\pm0.2}$	$0.138^{\pm0.008}$
H	$2.4^{\pm0.2}$	$0.094^{+0.009}_{-0.008}$
I	0.8 MIN	0.031 MIN
J	2.6	0.102
K	1.27(T.P.)	0.050(T.P.)
M	$0.40^{\pm0.10}$	$0.016^{+0.004}_{-0.005}$
N	0.12	0.005
P	$6.73^{\pm0.20}$	$0.265^{\pm0.008}$
Q	0.15	0.006
T	R 0.85	R 0.033
U	$0.20^{+0.10}_{-0.05}$	$0.008^{+0.004}_{-0.002}$

20PIN PLASTIC ZIP (400 mil)



P20V 254 400A-1

NOTE
Each lead centerline is located within 0.25 mm (0.010 inch) of its true position (T P.) at maximum material condition

ITEM	MILLIMETERS	INCHES
A	26.67 MAX.	1 050 MAX
F	$0.5^{\pm 0.1}$	$0.020^{+0.004}_{-0.005}$
G	ϕ0 25	ϕ0 010
H	2 54	0 100
I	1.27	0 050
J	1.27 MAX.	0 050 MAX.
K	1.0 MIN.	0.039 MIN
M	8.9 MAX	0.350 MAX.
N	$2.8^{\pm 0.2}$	$0.110^{+0.008}_{-0.009}$
Q	10.16 MAX.	0.400 MAX
V	$0.25^{+0.10}_{-0.05}$	$0.010^{+0.004}_{-0.003}$
W	2.54	0.100
Y	$3.3^{\pm 0.5}$	$0.130^{\pm 0.02}$

RECOMMENDED SOLDERING CONDITIONS ★

The following conditions (see tables below and next page) must be met for soldering conditions of the μPD424100.

For more details, refer to our document "SEMICONDUCTOR DEVICE MOUNTING TECHNOLOGY MANUAL" (IEI-1207).

Please consult with our sales offices in case other soldering process is used, or in case other soldering is done under different conditions.

TYPES OF SURFACE MOUNT DEVICE

μPD424100GS : 26-pin plastic TSOP (300 mil)

Soldering process	Soldering conditions	Symbol
Infrared ray reflow	Peak temperature of package surface : 235 ℃ or below, Reflow time: 30 seconds or below (210 ℃ or higher), Number of reflow processes: MAX. 2 Exposure limit[Note]: 7 days (10 hours pre-baking is required at 125 ℃ afterwards) **[Remark]** (1) Please start the second reflow process after the temperature, raised by the first reflow process, returns to normal. (2) Please avoid removing the residual flux with water after the first reflow process .	IR35-107-2
VPS	Peak temperature of package : 215 ℃ or below, Reflow time : 40 seconds or below (200 ℃ or higher), Number of reflow processes: MAX. 2 Exposure limit[Note]: 7 days (10 hours pre-baking is required at 125 ℃ afterwards) **[Remark]** (1) Please start the second reflow process after the temperature, raised by the first reflow process, returns to normal. (2) Please avoid removing the residual flux with water after the first reflow process .	VP15-107-2
Partial heating method	Terminal temperature: 300 ℃ or below, Time : 3 seconds or below (Per one side of the device).	————

Note Exposure limit before soldering after dry-pack package is opened.
Storage conditions: 25 °C and relative humidity at 65 % or less.

Caution Do not apply more than one soldering method at any one time, except for "Partial heating method".

μPD424100LA : 26-pin plastic SOJ (300 mil)

Soldering process	Soldering conditions	Symbol
Infrared ray reflow	Peak temperature of package surface : 235 ℃ or below, Reflow time: 30 seconds or below (210 ℃ or higher), Number of reflow processes: MAX. 2 Exposure limit[Note]: 7 days (20 hours pre-baking is required at 125 ℃ afterwards) **[Remark]** (1) Please start the second reflow process after the temperature, raised by the first reflow process, returns to normal. (2) Please avoid removing the residual flux with water after the first reflow process.	IR35-207-2
VPS	Peak temperature of package : 215 ℃ or below, Reflow time : 40 seconds or below (200 ℃ or higher), Number of reflow processes: MAX. 2 Exposure limit[Note]: 7 days (20 hours pre-baking is required at 125 ℃ afterwards) **[Remark]** (1) Please start the second reflow process after the temperature, raised by the first reflow process, returns to normal. (2) Please avoid removing the residual flux with water after the first reflow process.	VP15-207-2
Partial heating method	Terminal temperature: 300 ℃ or below, Time : 3 seconds or below (Per one side of the device).	———

Note Exposure limit before soldering after dry-pack package is opened.
Storage conditions: 25 °C and relative humidity at 65 % or less.

Caution Do not apply more than one soldering method at any one time, except for "Partial heating method".

TYPE OF THROUGH HOLE MOUNT DEVICE

μPD424100V : 20-pin plastic ZIP (400 mil)

Please consult with our sales offices for soldering conditions of the μPD424100V.