PRELIMINARY DATA SHEET

NEC

MOS INTEGRATED CIRCUIT

μPD70731

V805™
32-/16-BIT MICROPROCESSOR

The V805 is a high-performance microprocessor for embedded control equipment. The V805 is based on the V810™ 32-bit microprocessor and has 16-bit external data bus. Therefore, replacement from existing 16-bit based application system can be realized with ease. This IC is available in small packages suitable for downsizing of application system.

The V805 has high real-time response capability, high-speed integer operation instructions, and floating-point operation instructions, achieving high cost-performance for applications such as facsimile machines, word processors, image processing equipment, and real-time operating equipment.

Its functions are described in details in the manual indicated below. Please read this manual before starting design.

- **V805 User's Manual (Preliminary) : To be published**

FEATURES

- High-performance 32-bit microprocessor for embedded applications, V810, used processor core
  - Address/data separated bus
    - Address bus: 32 bits
    - Data bus: 16 bits
  - On-chip 1KB cache memory
  - 1-clock pitch pipeline architecture
  - 16-bit fixed-length instruction set (except some instructions)
  - Thirty two 32-bit general-purpose registers
  - 4GB linear address space
  - Hardware interlock against register/flag hazard
- Powerful instruction set for various applications
  - Floating-point operation instructions (based upon IEEE754 data format)
  - Bit string instructions
- 16 levels of high-speed interrupt response function
- Clock stop mode by internal static operation
- Maximum operating frequencies (16/20 MHz)

ORDERING INFORMATION

Part Number	Package	Max. Operating Freq. (MHz)	Quality Grade
μPD70731GC-16-7EA	100-pin plastic QFP	16	Standard
μPD70731GC-20-7EA	100-pin plastic QFP	20	Standard

Please refer to "Quality grade on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

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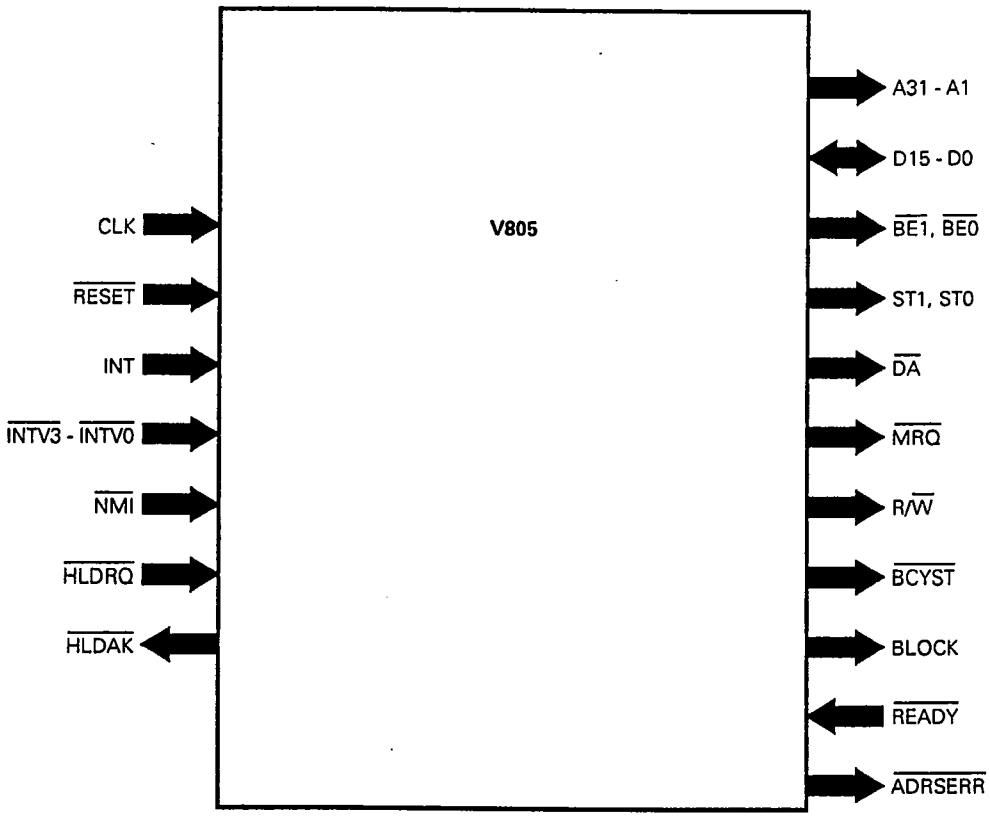
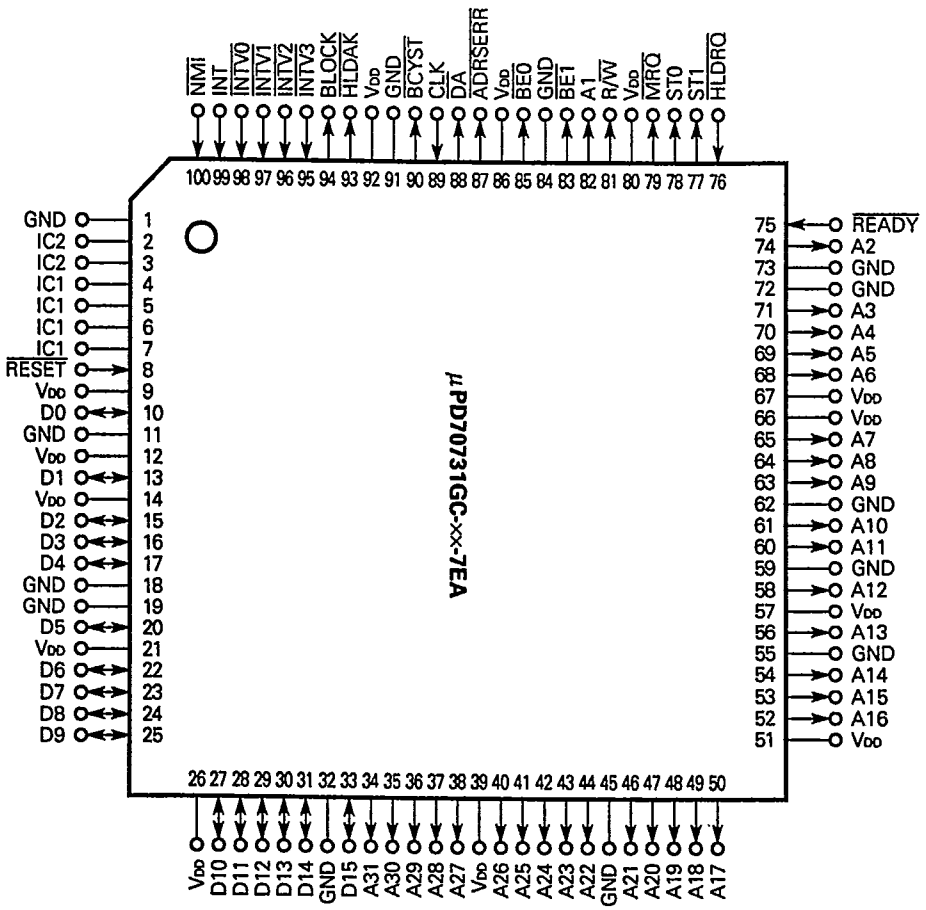
SIMPLIFIED PIN CONFIGURATION



Pin Configurations (Top View)



Cautions 1. IC1 pins should be left open.

2. IC2 pins should be connected to GND line.

Remark IC : Internally Connected

1. PIN FUNCTIONS

1.1 LIST OF PIN FUNCTIONS

(1/2)

Pin name	Input/Output	Functions	Bus holding state during operation	Bus holding state after reset	Bus idling state after reset
A31 - A1 (Address Bus)	3-state output	Address bus	Hi-Z	Hi-Z	H
D15 - D0 (Data Bus)	3-state I/O	Bidirectional data bus	Hi-Z	Hi-Z	Hi-Z
$\overline{BE1}$, $\overline{BE0}$ (Byte Enable 1 to 0)	3-state output	Indicate effective data when accessing data.	Hi-Z	Hi-Z	H
ST1, ST0 (Status 1 to 0)	3-state output	Indicate bus cycle type.	Hi-Z	Hi-Z	H
$\overline{DA}$ (Data Access)	3-state output	Outputs strobe signal in bus cycle.	Hi-Z	Hi-Z	H
$\overline{MRQ}$ (Memory Request)	3-state output	Indicates memory access.	Hi-Z	Hi-Z	H
R/$\overline{W}$ (Read/Write)	3-state output	Indicates read access or write access.	Hi-Z	Hi-Z	H
$\overline{BCYST}$ (Bus Cycle Start)	3-state output	Indicates start of bus cycle.	Hi-Z	Hi-Z	H
$\overline{READY}$ (Ready)	Input	Extends bus cycle.	–	–	–
$\overline{HLDRQ}$ (Hold Request)	Input	Requests bus control.	–	–	–
$\overline{HLDAK}$ (Hold Acknowledge)	Output	Outputs acknowledge signal in response to $\overline{HLDRQ}$.	L	L	H
BLOCK (Bus Lock)	Output	Outputs signal disabling bus control.	L	L	L
INT (Maskable Interrupt)	Input	Inputs interrupt request signals.	–	–	–
$\overline{INTV3}$ - $\overline{INTV0}$ (Interrupt Level 3 to 0)	Input	Input the signal indicating interrupt level.	–	–	–
$\overline{NMI}$ (Non-Maskable Interrupt)	Input	Issue non-maskable interrupt request to CPU.	–	–	–
CLK	Input	Inputs system clock.	–	–	–
$\overline{RESET}$ (Reset)	Input	Resets V810.	–	–	L
$\overline{ADRSERR}$ (Address Error)	Ourput	Indicates incorrect data alignment.	Unchanged	H	H
V_{DD} (Power Supply)	–	Connected to +5 V power supply.	–	–	–

(2/2)

Pin name	Input/Output	Functions	Bus holding state during operation	Bus holding state after reset	Bus idling state after reset
GND (Ground)	–	Connected to ground line (0 V).	–	–	–
IC1 (Internally Connected 1)	–	Internally connected. Should be left open.	–	–	–
IC2 (Internally Connected 2)	–	Internally connected. Should be connected to GND line.	–	–	–

2. ELECTRICAL SPECIFICATIONS (PRELIMINARY)

ABSOLUTE MAXIMUM RATINGS (T_a = 25 °C)

Parameter	Symbol	Conditions	Ratings	Unit
Power supply voltage	V_{DD}		−0.5 to +7.0	V
Input voltage	V_I	V_{DD} = 5 V ±10 %	−0.5 to V_{DD}+0.3	V
Clock input voltage	V_K	V_{DD} = 5 V ±10 %	−0.5 to V_{DD}+0.3	V
Output voltage	V_O	V_{DD} = 5 V ±10 %	−0.5 to V_{DD}+0.3	V
Operating ambient temperature	T_{opt}		−40 to +85	°C
Storage temperature	T_{stg}		−65 to +150	°C

Cautions 1. Do not connect output (and bidirectional) pins each other. Do not connect output (or bidirectional) pins directly to the V_{DD}, Vcc, or GND line. However, open drain pin and open collector pins can be directly connected to V_{DD}, Vcc, or GND line. If timing design is made so that no signal conflict occurs, three-state pins can also be connected directly to three-state pins of external circuit.

2. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The parameters apply independently. The device should be operated within the limits specified under DC and AC Characteristics.

DC CHARACTERISTICS (T_a = −40 °C to +85 °C, V_{DD} = 5 V ±10 %)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Clock input voltage, high	V_{KH}		4.0		V_{DD}+0.3	V
Clock input voltage, low	V_{KL}		−0.5		+0.6	V
Input voltage, high	V_{IH}		2.2		V_{DD}+0.3	V
Input voltage, low	V_{IL}		−0.5		+0.8	V
Output voltage, high	V_{OH}	I_{OH} = −400 μA	2.4			V
Output voltage, low	V_{OL}	I_{OL} = 3.2 mA			0.45	V
Input leakage current, high	I_{LIH}	V_{IN} = V_{DD}			10	μA
Input leakage current, low	I_{LIL}	V_{IN} = 0 V			−10	μA
Output leakage current, high	I_{LOH}	V_O = V_{DD}			10	μA
Output leakage current, low	I_{LOL}	V_O = 0 V			−10	μA
Supply current [Note]	I_{DD}	f = 16 MHz			120	mA
		f = 20 MHz, T_a = −10 to +70 °C			140	
		Clock is stopped		5	T.B.D.	μA

Note When the clock is stopped, V_{IL} = 0 V, V_{IH} = V_{DD}

Remark Power supply current is nearly proportional to operating clock frequency in operation mode.

CAPACITANCE (T_a = 25 °C, V_{DD} = 5 V ±10 %)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
Input capacitance	C_I	f_c = 1 MHz		15	pF
I/O capacitance	C_{IO}			15	pF

AC CHARACTERISTICS (V_{DD} = 5 V ±10 %)

CLOCK

Parameter	Symbol	Conditions	f = 16 MHz (T_a = −40 to +85 °C)		f = 20 MHz (T_a = −10 to +70 °C)		Unit
			MIN.	MAX.	MIN.	MAX.	
Clock cycle	t_{CYK}		62.5		50		ns
Clock pulse high level width	t_{KKH}		26		21		ns
Clock pulse low level width	t_{KKL}		26		21		ns
CLK rise time	t_{KR}			5		4	ns
CLK fall time	t_{KF}			5		4	ns

RESET

Parameter	Symbol	Conditions	f = 16 MHz (T_a = −40 to +85 °C)		f = 20 MHz (T_a = −10 to +70 °C)		Unit
			MIN.	MAX.	MIN.	MAX.	
$\overline{\text{RESET}}$ hold time (from V_{DD} VALID)	t_{HVR}		1000 + 20t_{CYKR}		1000 + 20t_{CYKR}		ns
Clock cycle (at $\overline{\text{RESET}}$)	t_{CYKR}		62.5	1000	50	1000	ns
Clock high level time (at $\overline{\text{RESET}}$)	t_{KKHR}		26		21		ns
Clock low level time (at $\overline{\text{RESET}}$)	t_{KKLR}		26		21		ns
$\overline{\text{RESET}}$ setup time (to CLK ↓, active)	t_{SRKF}		10		10		ns
$\overline{\text{RESET}}$ setup time (to CLK ↓, inactive)	t_{SRKR}		10		10		ns
$\overline{\text{RESET}}$ hold time (from CLK ↓)	t_{HKR}		10		10		ns
$\overline{\text{RESET}}$ pulse low level width (for CLK)	t_{WRL}		20t_{CYKR}		20t_{CYKR}		ns

MEMORY, I/O ACCESS

Parameter	Symbol	Conditions	f = 16 MHz (T_a = −40 to +85 °C)		f = 20 MHz (T_a = −10 to +70 °C)		Unit
			MIN.	MAX.	MIN.	MAX.	
Address, etc., output delay (from CLK ↑)	t_{DKA}		2	20	2	15	ns
Address, etc., output hold time (from CLK ↑)	t_{HKA}		2	20	2	15	ns
$\overline{BCYST}$ output delay (from CLK ↑)	t_{DKBC}		2	20	2	15	ns
$\overline{BCYST}$ output hold time (from CLK ↑)	t_{HKBC}		2	20	2	15	ns
$\overline{DA}$ output delay (from CLK ↑)	t_{DKDA}		2	20	2	15	ns
$\overline{DA}$ output hold time (from CLK ↑)	t_{HKDA}		2	20	2	15	ns
$\overline{READY}$ setup time (to CLK ↓)	t_{SRYK}		6		5		ns
$\overline{READY}$ hold time (from CLK ↓)	t_{HKRY}		5		5		ns
Data setup time (to CLK ↑)	t_{SDK}		6		5		ns
Data hold time (from CLK ↑)	t_{HKD}		5		5		ns
Data output delay (from active, from CLK ↓)	t_{DKDT}		2	20	2	15	ns
Data output hold time (to active, from CLK ↓)	t_{HKDT}		2	20	2	15	ns
Data output delay (from float, from CLK ↓)	t_{LZKDT}		5	25	5	20	ns
Data output hold time (to float, from CLK ↓)	t_{HZKDT}		5	25	5	20	ns

INTERRUPT

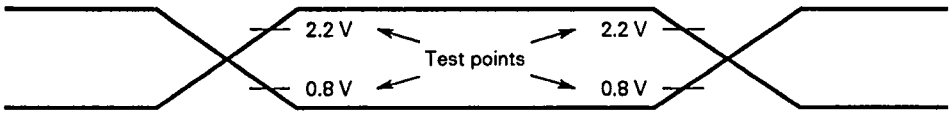
Parameter	Symbol	Conditions	f = 16 MHz (T_a = −40 to +85 °C)		f = 20 MHz (T_a = −10 to +70 °C)		Unit
			MIN.	MAX.	MIN.	MAX.	
$\overline{NMI}$ setup time (to CLK ↓)	t_{SNK}		6		5		ns
$\overline{NMI}$ hold time (from CLK ↓)	t_{HKN}		5		5		ns
INT, etc., setup time (to CLK ↑)	t_{SIK}		6		5		ns
INT, etc., hold time (from CLK ↑)	t_{HKI}		5		5		ns

BUS HOLD

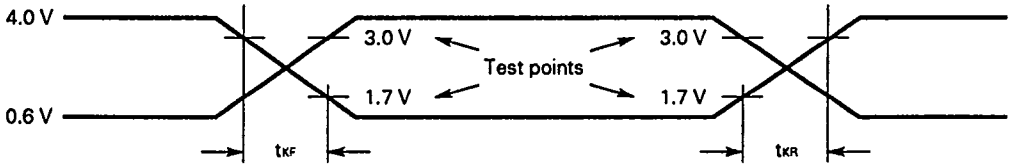
Parameter	Symbol	Conditions	f = 16 MHz (T_a = −40 to +85 °C)		f = 20 MHz (T_a = −10 to +70 °C)		Unit
			MIN.	MAX.	MIN.	MAX.	
$\overline{\text{HLDRQ}}$ setup time (to CLK ↓)	t_{SHQK}		6		5		ns
$\overline{\text{HLDRQ}}$ hold time (from CLK ↓)	t_{HKHQ}		5		5		ns
$\overline{\text{HLDAK}}$ output delay (from CLK ↑)	t_{DKHA}		2	25	2	20	ns
$\overline{\text{HLDAK}}$ output hold time (from CLK ↑)	t_{HKHA}		2	25	2	20	ns
Address, etc., delay (from active, from CLK ↑)	t_{HZKA}		2	25	2	20	ns
Address, etc., delay (from float, from CLK ↑)	t_{LZKA}		2	25	2	20	ns
Data delay (from active, from CLK ↓)	t_{HZKD}		5	25	5	20	ns
Data delay (from float, from CLK ↓)	t_{LZKD}		5	25	5	20	ns
$\overline{\text{DA}}$ output delay (from active, from CLK ↑)	t_{HZKDA}		2	25	2	20	ns
$\overline{\text{DA}}$ output delay (from float, from CLK ↑)	t_{LZKDA}		2	25	2	20	ns

AC CHARACTERISTICS

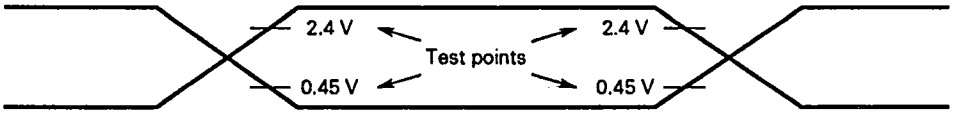
AC test input waveform (except CLK)



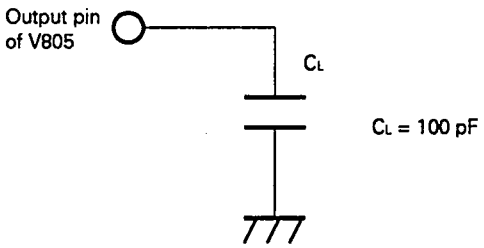
AC test input waveform (CLK)



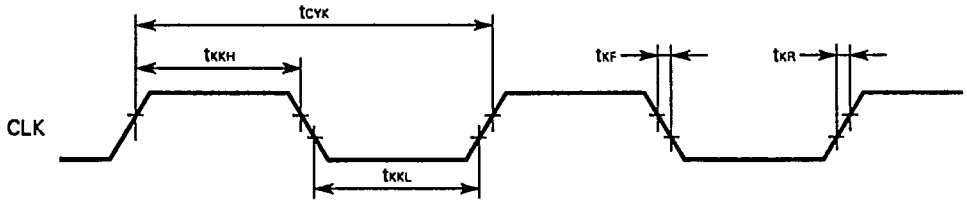
AC test output test points



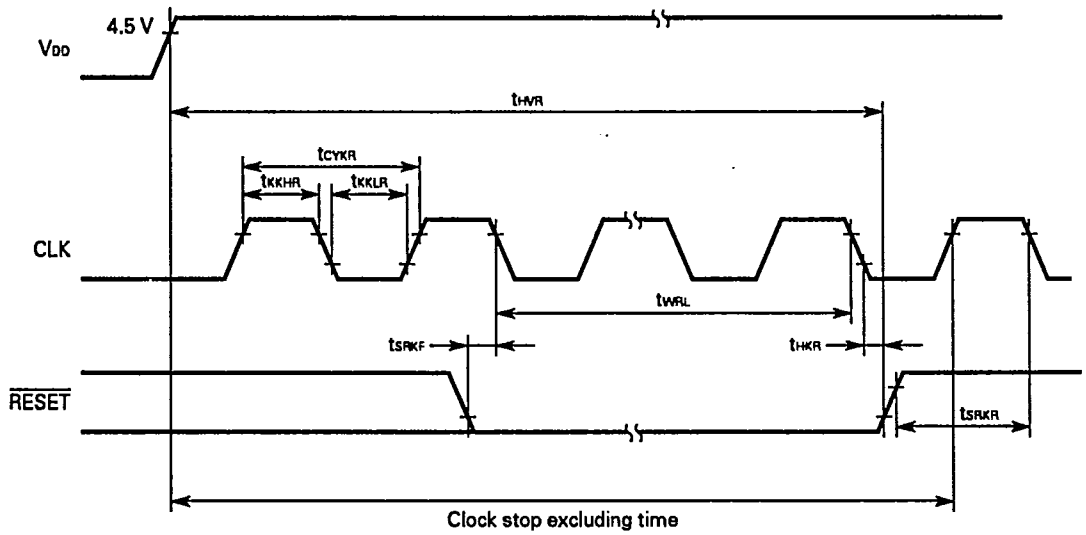
Test load



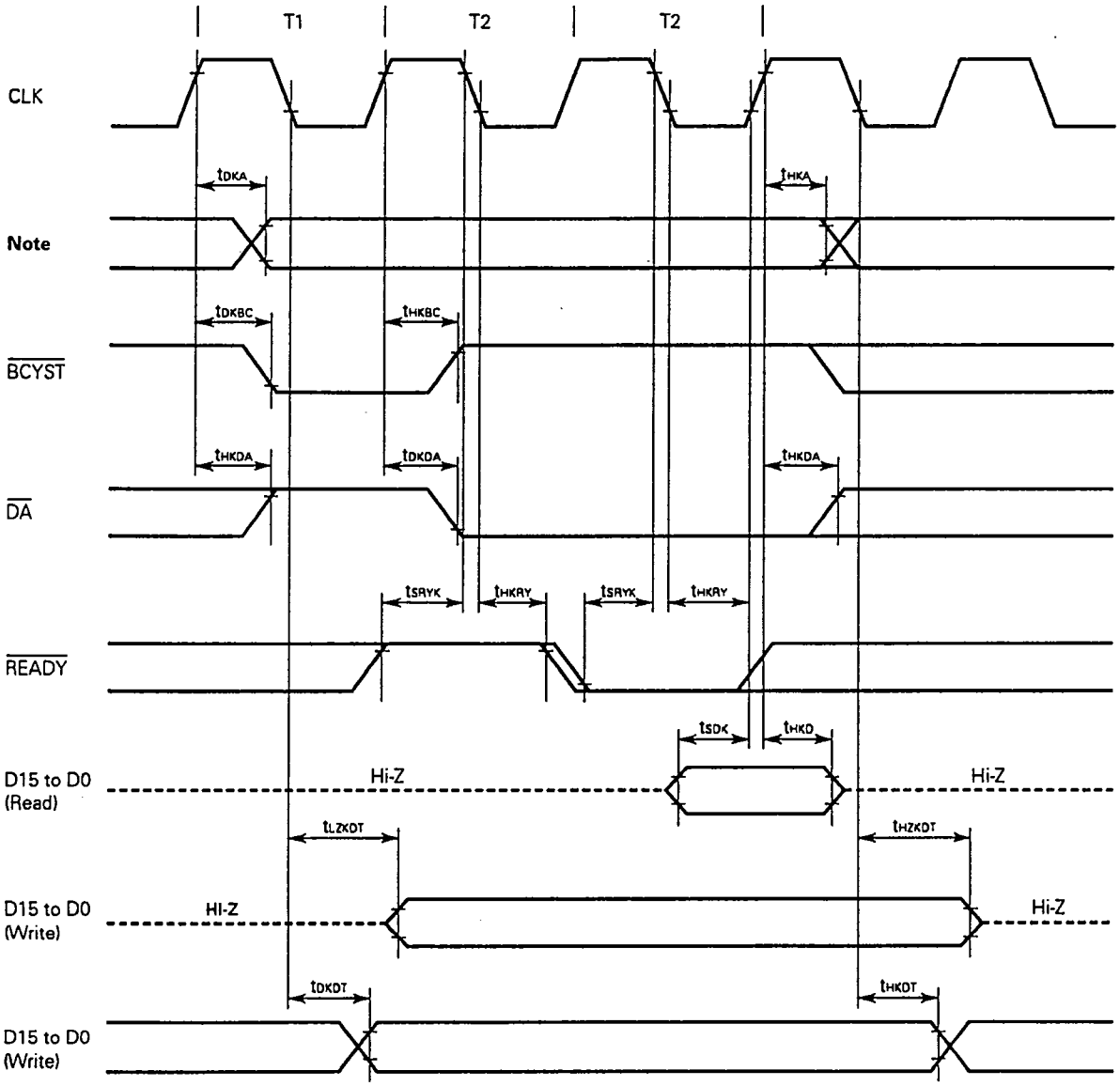
CLOCK TIMING



RESET TIMING

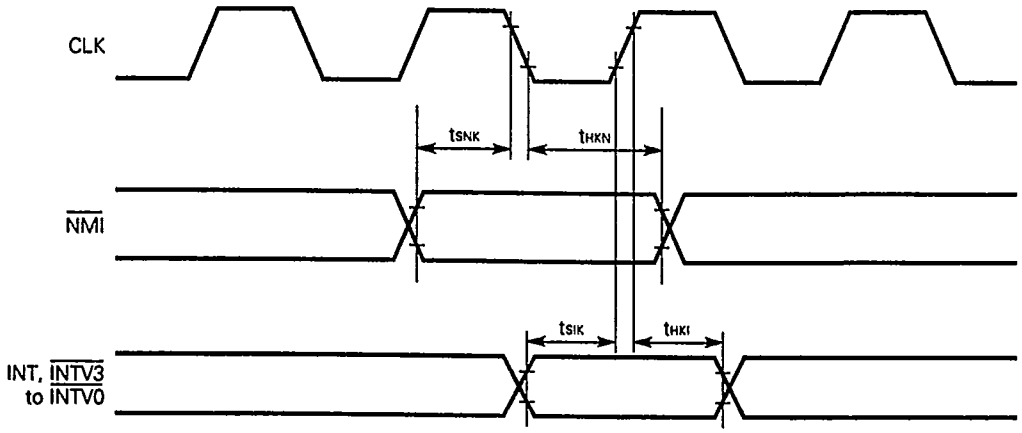


MEMORY, I/O ACCESS TIMING

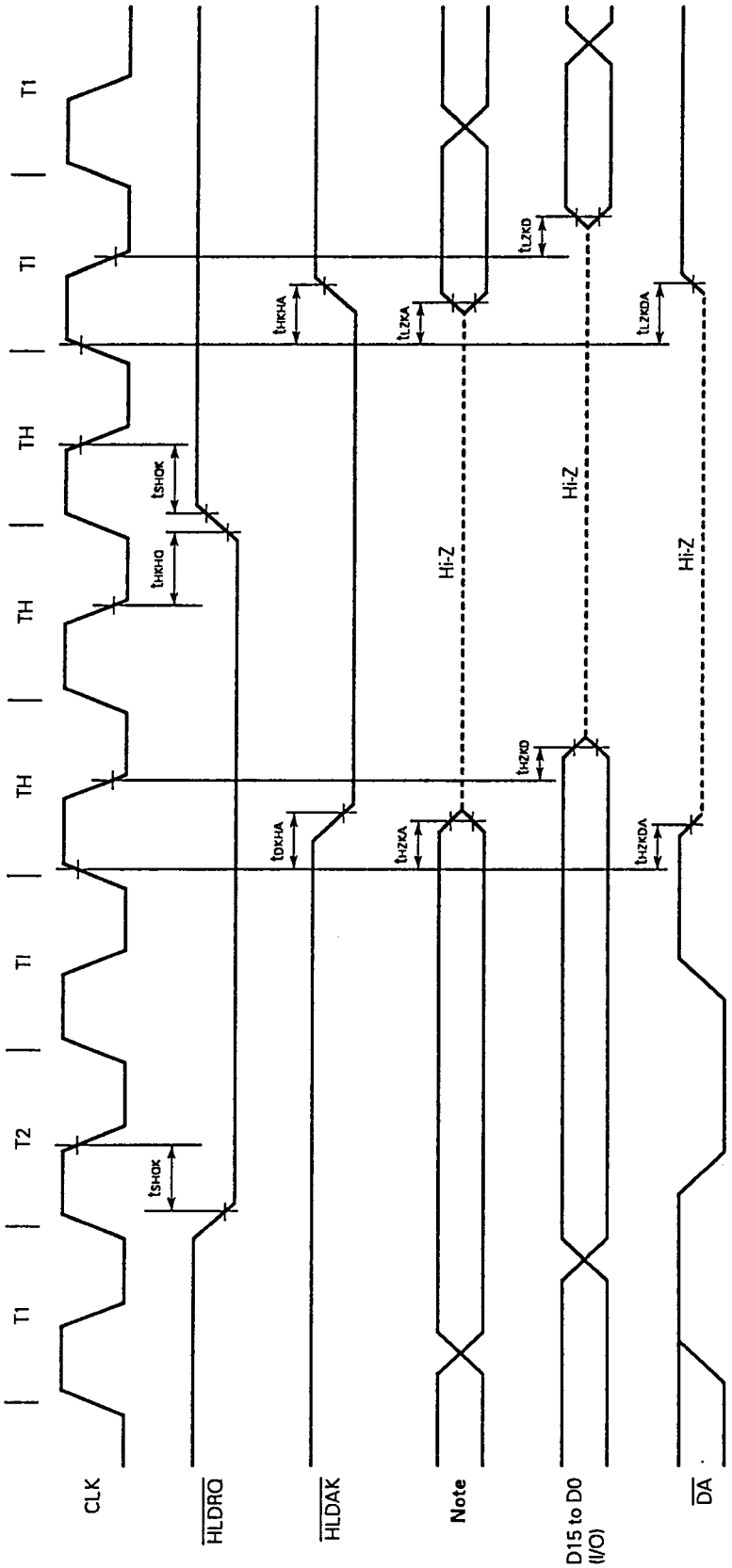


Note A31 - A1, $\overline{BE1}$, $\overline{BE0}$, R/$\overline{W}$, $\overline{MRQ}$, ST1, ST0, BLOCK, $\overline{ADRSERR}$

INTERRUPT TIMING



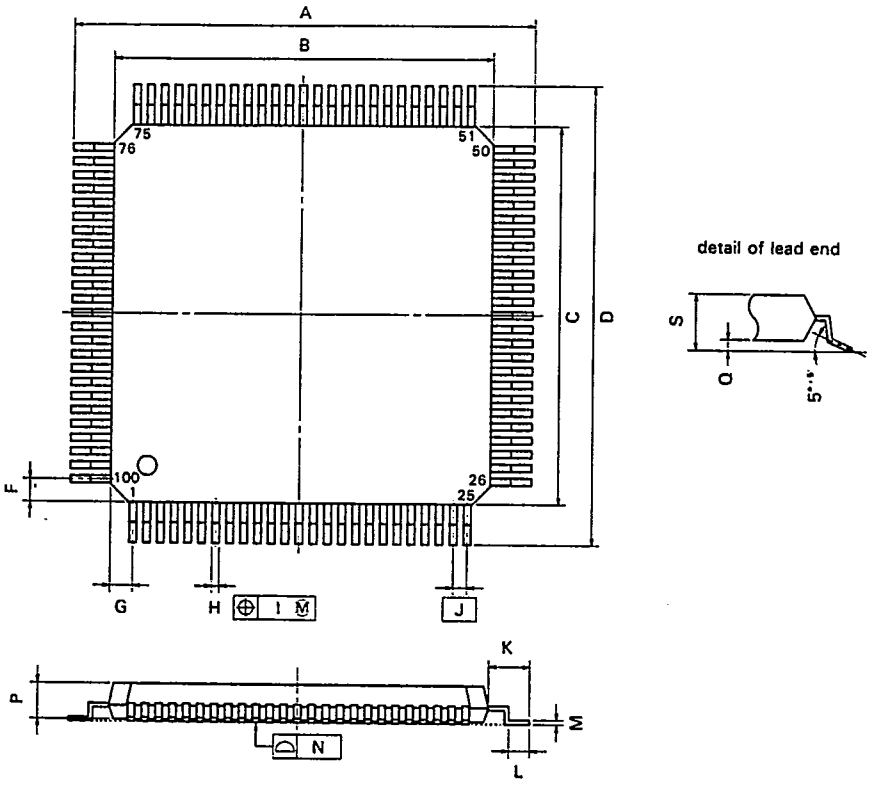
BUS HOLD TIMING



Note A31 - A1, $\overline{BE1}$, $\overline{BE0}$, R/$\overline{W}$, $\overline{MRQ}$, ST1, ST0, $\overline{BCYST}$

3. PACKAGE DRAWINGS

100 PIN PLASTIC QFP (FINE PITCH) (□14)



P100GC-50-7EA

NOTE
Each lead centerline is located within 0.08 mm (0.003 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	$16.0^{\pm 0.4}$	$0.630^{\pm 0.016}$
B	$14.0^{\pm 0.2}$	$0.551^{-0.009}_{-0.008}$
C	$14.0^{\pm 0.2}$	$0.551^{-0.009}_{-0.008}$
D	$16.0^{\pm 0.4}$	$0.630^{\pm 0.016}$
F	1.0	0.039
G	1.0	0.039
H	$0.20^{\pm 0.10}$	$0.008^{\pm 0.004}$
I	0.08	0.003
J	0.5 (T.P.)	0.020 (T.P.)
K	$1.0^{\pm 0.2}$	$0.039^{-0.009}_{-0.008}$
L	$0.5^{\pm 0.2}$	$0.020^{-0.008}_{-0.009}$
M	$0.15^{\pm 0.05}$	$0.006^{\pm 0.002}$
N	0.10	0.004
P	1.45	0.057
Q	$0.1^{\pm 0.1}$	$0.004^{\pm 0.004}$
S	1.7 MAX.	0.067 MAX.