

1.1 GHz LOW-POWER TWO-MODULUS PRESCALER  
 $\div 64/65$ ,  $\div 128/129$  FOR MOBILE TELEPHONE

DESCRIPTION

$\mu$ PB1504GR is a 64/65, 128/129 two modulus prescaler to construct pulse swallow type PLL frequency synthesizer for 800 MHz to 900 MHz mobile telephone. This IC is manufactured using latest high speed bipolar process. This process reduces stray capacitance of internal transistor and wirings to achieve low current consumption. For this reason,  $\mu$ PB1504GR is suitable for battery-operated telephone systems.

FEATURES

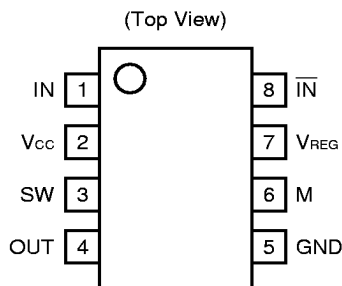
- High toggle frequency : 0.5 GHz to 1.1 GHz
- Supply voltage :  $V_{CC} = V_{REG} = 2.7$  to  $3.6$  V
- Low current consumption :  $2.4$  mA<sub>TYP.</sub> @3.3 V spec. ( $1.9$  mA<sub>TYP.</sub> @3.0 V reference data)
- Pulse swallow control :  $\div 64/65$ ,  $\div 128/129$
- High input frequency :  $-19$  dBm to  $+4$  dBm

ORDER INFORMATION

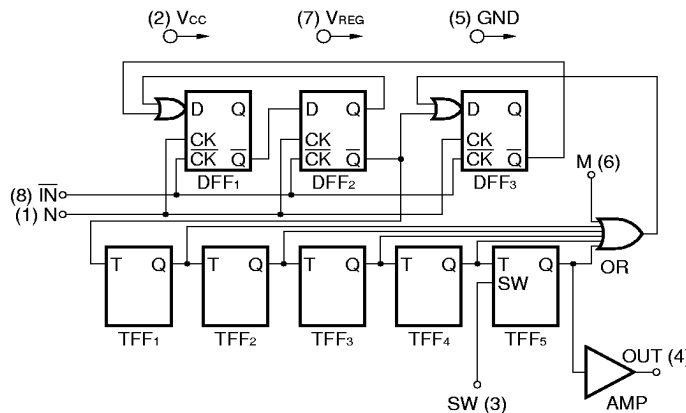
ORDER NUMBER	PACKAGE	SUPPLYING FORM
$\mu$ PB1504GR-E1	8 pin plastic SOP (225 mil)	Embossed tape 12 mm wide. QTY 2.5 k/reel Pin 1 is in tape pull-out direction.
$\mu$ PB1504GR-E2		Embossed tape 12 mm wide. QTY 2.5 k/reel Pin 1 is in tape roll-in direction.

**Remarks** To order evaluation samples, please contact your local NEC sales office.  
 (Order number:  $\mu$ PB1504GR)

PIN ASSIGNMENT



INTERNAL BLOCK DIAGRAM



Caution: Electro-static sensitive devices

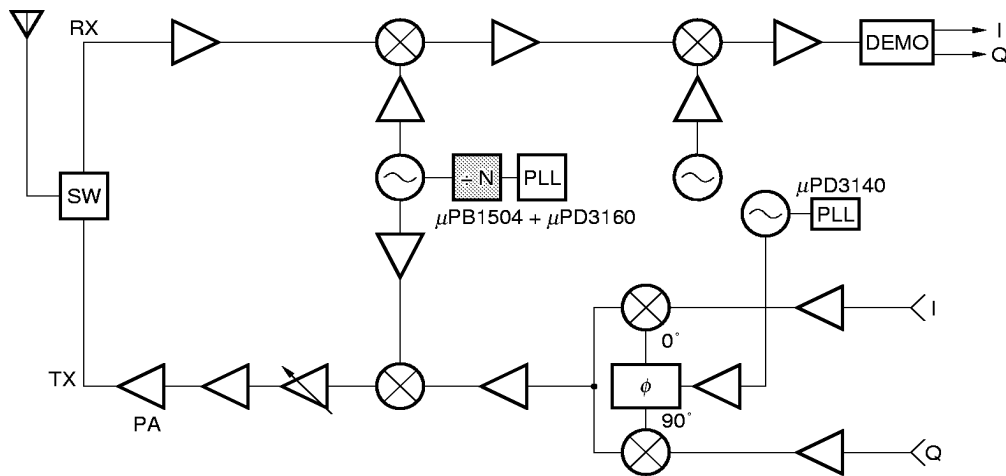
**SELECTOR GUIDE**

TYPE	PART NUMBER	DIVIDE RATIO	V <sub>cc</sub> (V)	I <sub>cc</sub> (mA)	f <sub>in</sub> (GHz)	V <sub>in</sub> (dBm)	PACKAGE
1.1 GHz	$\mu$ PB1504GR	64/65, 128/129	2.7 to 3.6	2.4	0.5 to 1.1	-19 to +4	8 pin SOP
1.7 GHZ	$\mu$ PB1502GR	64/65, 128/129	2.7 to 3.3	6.7	0.5 to 1.7	-15 to -6	8 pin SOP
2.0 GHz	$\mu$ PB1502GR(1)	64/65, 128/129	2.7 to 3.3	6.7	0.5 to 2.0	-15 to -1	8 pin SOP

**Note** The above table lists the typical performance to compare similar ICs. Please refer to ELECTRIC CHARACTERISTICS of each IC's data sheet.

**SYSTEM APPLICATION EXAMPLE**

**Digital cellular phone**



**ABSOLUTE MAXIMUM RATINGS**

PARAMETER	SYMBOL	RATINGS	UNIT	CONDITIONS
Supply Voltage	V <sub>CC</sub>	-0.5 to +4.5	V	T <sub>A</sub> = +25 °C
Regulator Pin Bias	V <sub>REG</sub>	0 to V <sub>CC</sub>	V	T <sub>A</sub> = +25 °C
Input Voltage	V <sub>IN</sub>	-0.5 to V <sub>CC</sub>	V	T <sub>A</sub> = +25 °C
Power Dissipation	P <sub>D</sub>	250	mW	Mounted on double sided copper clad 50 × 50 × 1.6 mm epoxy glass PWB at T <sub>A</sub> = +85 °C
Storage Temperature	T <sub>STG</sub>	-55 to +125	°C	

**RECOMMENDED OPERATING RANGE**

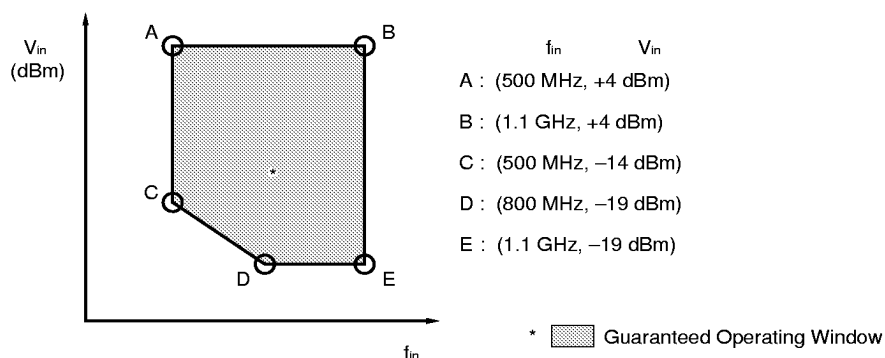
PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply Voltage	V <sub>CC</sub>	2.7	3.0	3.6	V
Regulator Pin Bias	V <sub>REG</sub>	2.7	V <sub>CC</sub>	V <sub>CC</sub>	V
Output Load Capacitance	C <sub>L</sub>	—	—	10	pF
Operation Temperature	T <sub>A</sub>	-30	—	+85	°C

**ELECTRICAL CHARACTERISTICS**

(V<sub>CC</sub> = V<sub>REG</sub> = 2.7 to 3.6 V, T<sub>A</sub> = -30 to +85 °C; Unless otherwise specified)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITIONS
Circuit Current @÷64/65	I <sub>CC</sub>	—	2.47	3.22	mA	V <sub>CC</sub> = V <sub>REG</sub> = 3.3 V T <sub>A</sub> = +25 °C No input signals
Circuit Current @÷128/129		—	2.24	2.93		
Output Voltage Swing	V <sub>O</sub>	0.65	0.9	—	V <sub>P-P</sub>	f <sub>in</sub> = 1.1 GHz
Response Input frequency	f <sub>in</sub>	0.5	—	1.1	GHz	C <sub>L</sub> = 10 pF
Input Power Sensitivity	V <sub>in</sub>	-19	—	+4	dBm	f <sub>in</sub> = 800 MHz to 1.1 GHz
		-14	—	+4		f <sub>in</sub> = 500 MHz
Modulus Control Input High	V <sub>IH</sub>	0.8 V <sub>CC</sub>	—	—	V	6 pin (M)
Modulus Control Input Low	V <sub>IL</sub>	—	—	0.2 V <sub>CC</sub>	V	
Divide Ratio Control Input High	V <sub>IH</sub>	V <sub>CC</sub>			V	3 pin (SW)
Divide Ratio Control Input Low	V <sub>IL</sub>	OPEN			V	
Modulus Setup Time	t <sub>SET</sub>	—	27	33	ns	÷ 64/65, C <sub>L</sub> = 10 pF

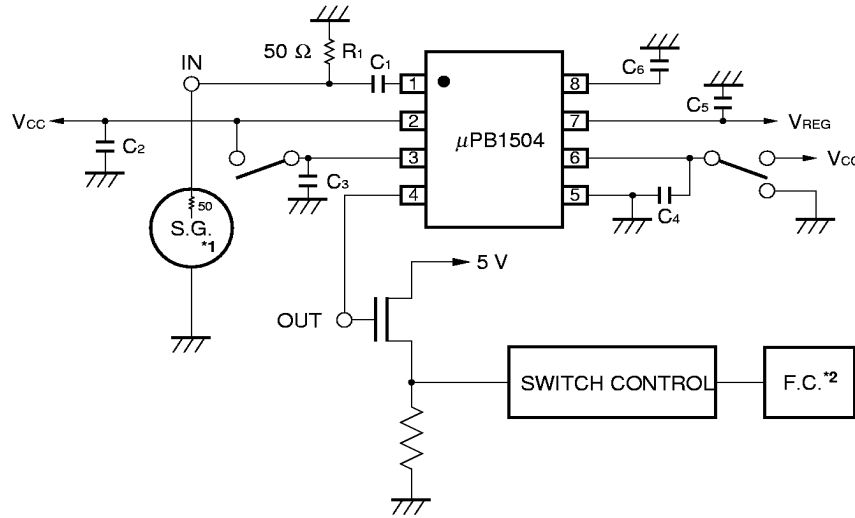
**NOTICE:** Following figure shows relation between RESPONSE INPUT FREQUENCY and INPUT POWER SENSITIVITY



**PIN DESCRIPTIONS**

PIN NO.	SYMBOL	ASSIGNMENT	FUNCTIONS AND EXPLANATION															
1	IN	Frequency input pin	Input frequency from an external VCO output. Must be coupled with capacitor (e.g. 1 000 pF) for DC cut.															
2	V <sub>CC</sub>	Power supply pin	Supply voltage 2.7 to 3.6 V for operation. Must be connected bypass capacitor (e.g. 1 000 pF) to minimize ground impedance.															
3	SW	Divided ratio control input pin	Divided ratio and modulus control can be governed by following input data to these pins.															
6	M	Modulus control input pin (pulse swallow control pin)																
<table border="1"> <tr> <td colspan="2"></td> <td colspan="2">M</td> </tr> <tr> <td colspan="2"></td> <td>H</td> <td>L</td> </tr> <tr> <td rowspan="2">SW</td> <td>H</td> <td>1/64</td> <td>1/65</td> </tr> <tr> <td>L</td> <td>1/128</td> <td>1/129</td> </tr> </table>						M				H	L	SW	H	1/64	1/65	L	1/128	1/129
		M																
		H	L															
SW	H	1/64	1/65															
	L	1/128	1/129															
4	OUT	Divided frequency output pin	This frequency output can be interfaced to CMOS PLL, because of 0.65 V <sub>p-p</sub> MIN. output swing on high-impedance. This output triggers with negative edge.															
5	GND	Ground pin	Must be connected to the system ground with minimum inductance. Ground pattern on the board should be formed as wide as possible. (Track length should be kept as short as possible).															
7	V <sub>REG</sub>	Regulator bias pin	This pin controls regulator circuit. Relation between supply bias and operation is shown below.															
<table border="1"> <tr> <td colspan="2"></td> <td>Operation</td> </tr> <tr> <td rowspan="2">V<sub>REG</sub></td> <td>H</td> <td>ON</td> </tr> <tr> <td>L</td> <td>OFF</td> </tr> </table>						Operation	V <sub>REG</sub>	H	ON	L	OFF							
		Operation																
V <sub>REG</sub>	H	ON																
	L	OFF																
8	$\overline{\text{IN}}$	Frequency-input bypass input	Must be connected bypass capacitor (e.g. 1 000 pF) to minimize ground impedance.															

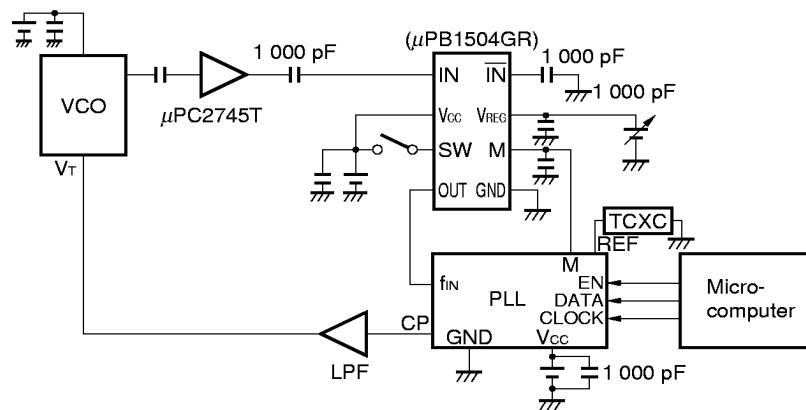
TEST CIRCUIT



SYNTHESIZED SIGNAL SOURCE \*1

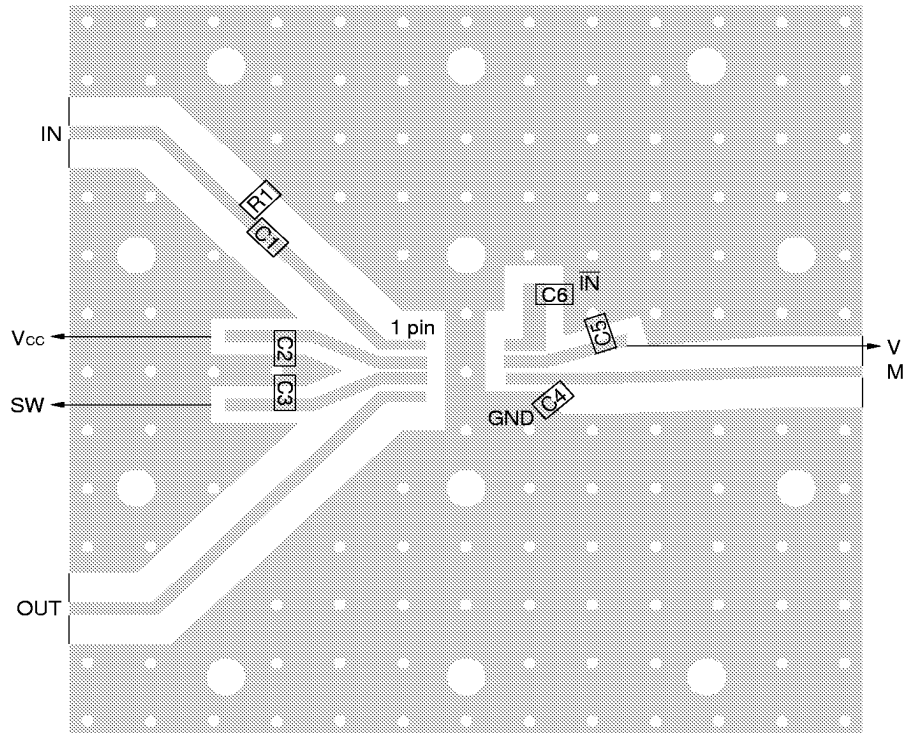
MICROWAVE FREQUENCY COUNTER \*2

SCHEMATIC EXAMPLE FOR APPLICATION OF  $\mu$ PB1504GR



The application circuits and their parameters are for references only and are not intended for use in actual design-in's. To know the real application circuits, please refer to PLL synthesizer LSI's documentations (e.g.  $\mu$ PD3160GS).

TEST CIRCUIT ASSEMBLED ON EVALUATION BOARD



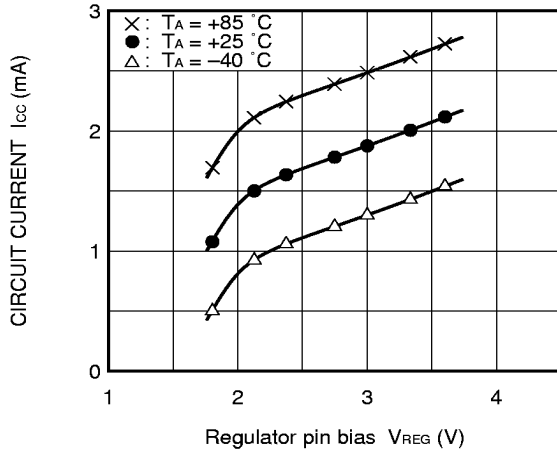
COMMENT LIST

No.	Value
C1 to 6	1 000 pF
R1	50 Ω

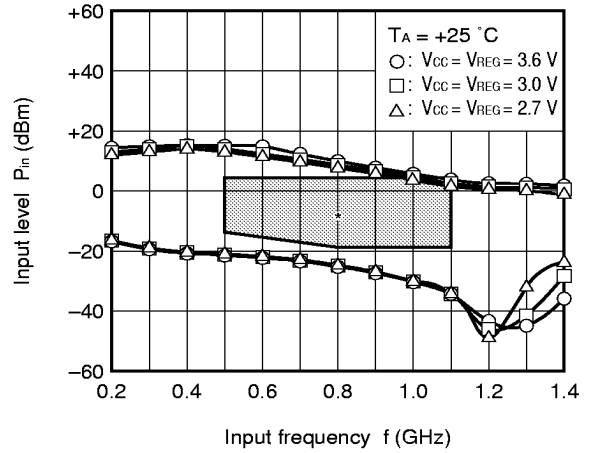
- Note (\*1)** 50 × 50 × 0.4 mm double copper clad polyimide board  
 (\*2) Backside: GND  
 (\*3) Solder plated on pattern  
 (\*4) ○○: Through holes

TYPICAL CHARACTERISTICS

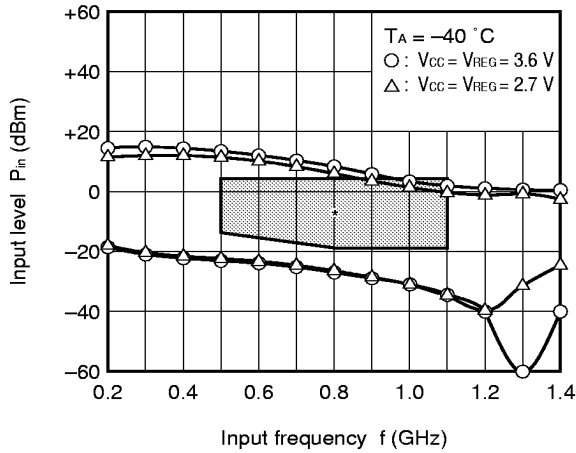
**CIRCUIT CURRENT vs. REGULATOR VOLTAGE**  
( $V_{CC} = 3\text{ V}$ )



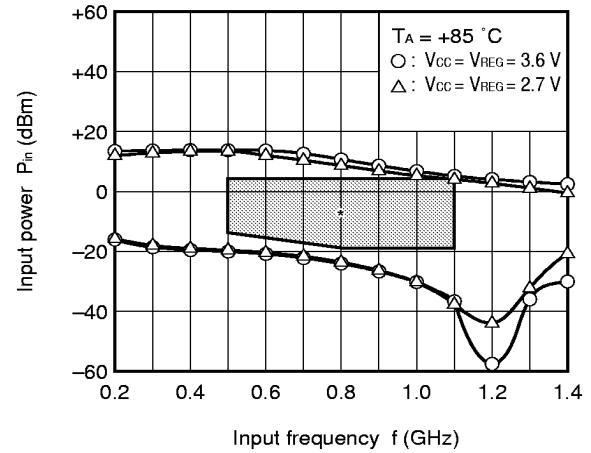
**INPUT POWER vs. FREQUENCY**



**INPUT POWER vs. FREQUENCY**

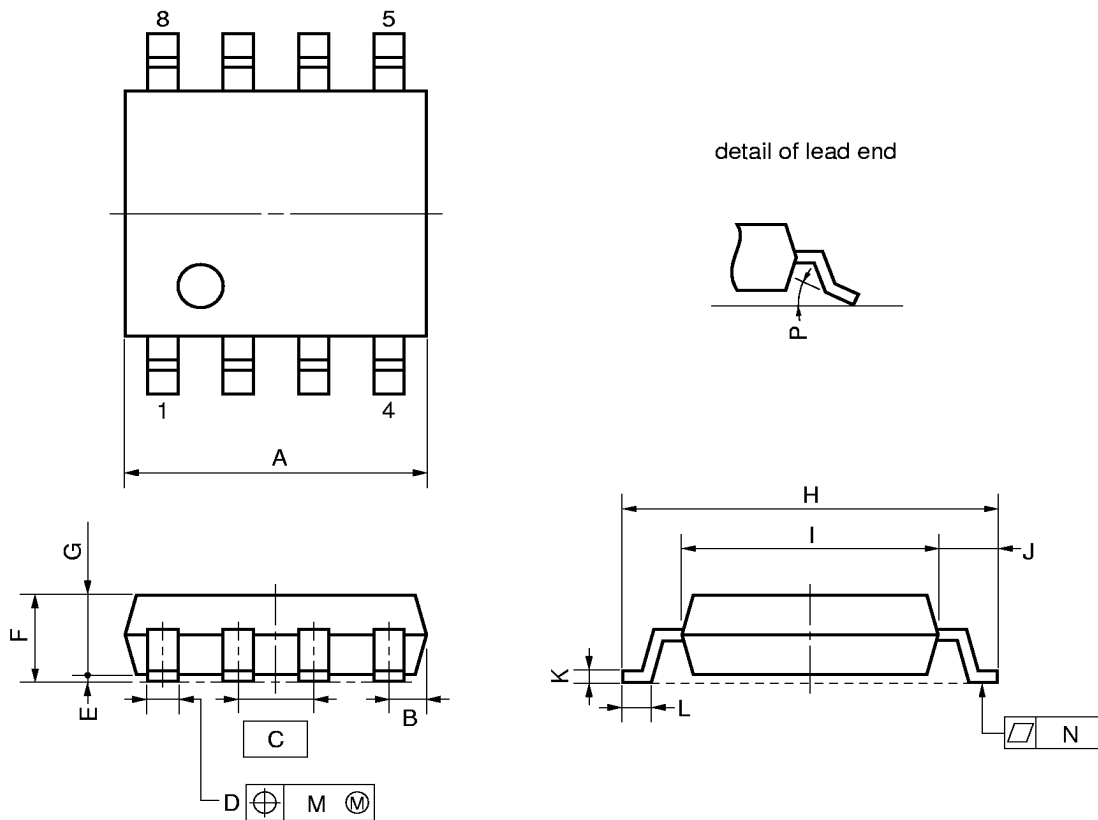


**INPUT POWER vs. FREQUENCY**



\* Guaranteed Operating Window

8 PIN PLASTIC SOP (225 mil)



**NOTE**  
 Each lead centerline is located within 0.12 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	5.37 MAX.	0.212 MAX.
B	0.78 MAX.	0.031 MAX.
C	1.27 (T.P.)	0.050 (T.P.)
D	0.40 <sup>+0.10</sup> <sub>-0.05</sub>	0.016 <sup>+0.004</sup> <sub>-0.003</sub>
E	0.1±0.1	0.004±0.004
F	1.8 MAX.	0.071 MAX.
G	1.49	0.059
H	6.5±0.3	0.256±0.012
I	4.4	0.173
J	1.1	0.043
K	0.15 <sup>+0.10</sup> <sub>-0.05</sub>	0.006 <sup>+0.004</sup> <sub>-0.002</sub>
L	0.6±0.2	0.024 <sup>+0.008</sup> <sub>-0.009</sub>
M	0.12	0.005
N	0.10	0.004
P	3° <sup>+7°</sup> <sub>-3°</sub>	3° <sup>+7°</sup> <sub>-3°</sub>

S8GM-50-225B-4



**NOTE ON CURRENT USE**

- (1) Observe precautions for handling because of electro-static sensitive devices.
- (2) Form a ground pattern as wide as possible to minimize ground impedance (to prevent undesired operation).
- (3) Keep the wiring length of the ground pins as short as possible.
- (4) Connect a bypass capacitor (e.g. 1 000 pF) to the V<sub>CC</sub> pin.

**RECOMMENDED SOLDERING CONDITIONS**

This product should be soldered in the following recommended conditions. Other soldering methods and conditions than the recommended conditions are to be consulted with our sales representatives.

μPB1504GR

SOLDERING METHOD	SOLDERING CONDITIONS	RECOMMENDED CONDITION SYMBOL
Infrared ray reflow	Package peak temperature: 230 °C, Hour: within 30 s. (more than 210 °C), Time: 2 times, Limited days: no.*	IR30-00-2
VPS	Package peak temperature: 215 °C, Hour: within 40 s. (more than 200 °C), Time: 1 time, Limited days: no.*	VP15-00-1
Wave soldering	Soldering tub temperature: less than 260 °C, Hour: within 10 s. Time: 1 time, Limited days: no.	WS60-00-1
Pin part heating	Pin are temperature: less than 300 °C, Hour: within 2 s. Limited days: no.*	

\*: It is the storage days after opening a dry pack, the storage conditions are 25 °C, less than 65 % RH.

**Note** The combined use of soldering method is to be avoided (However, except the pin area heating method)

For details of recommended soldering conditions for surface mounting, refer to information document SEMI-CONDUCTOR DEVICE MOUNTING TECHNOLOGY MANUAL (C10535EJ7V01F00).