NEC

MOS INTEGRATED CIRCUIT

μPD75P3116

4-BIT SINGLE-CHIP MICROCONTROLLER

The μPD75P3116 replaces the μPD753108's internal mask ROM with a one-time PROM, and features expanded ROM capacity.

Because the μPD75P3116 supports programming by users, it is suitable for use in evaluation of systems in the development stage using the μPD753104, 753106, or 753108, and for use in small-scale production.

Detailed information about functions is provided in the following User's Manual. Be sure to read it before designing:

μPD753108 User's Manual : U10890E

FEATURES

- ○ Compatible with μPD753108
- ○ Memory capacity:
  - PROM : 16384 x 8 bits
  - RAM : 512 x 4 bits
- ○ Can be operated in same power supply voltage range as the mask version μPD753108
  - V_{DD} = 1.8 to 5.5 V
- ○ On-chip LCD controller/driver
- ○ QTOP™ microcontroller

Remark QTOP microcontrollers are microcontrollers with on-chip one-time PROM that are totally supported by NEC. The support include writing application programs, marking, screening, and verification.

ORDERING INFORMATION

Part Number	Package
μPD75P3116GC-AB8	64-pin plastic QFP (14 x 14 mm, 0.8-mm pitch)
μPD75P3116GK-8A8	64-pin plastic QFP (12 x 12 mm, 0.65-mm pitch)

Caution This device does not provide an internal pull-up resistor connection function by means of mask option.

The information in this document is subject to change without notice.

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The mark ★ shows major revised points.

FUNCTION OUTLINE

Item		Function	
Instruction execution time		• 0.95, 1.91, 3.81, or 15.3 μs (main system clock: @ 4.19 MHz) • 0.67, 1.33, 2.67, or 10.7 μs (main system clock: @ 6.0 MHz) • 122 μs (subsystem clock: @ 32.768 kHz)	
Internal memory	PROM	16384 x 8 bits	
	RAM	512 x 4 bits	
General-purpose register		• 4-bit manipulation: 8 x 4 banks • 8-bit manipulation: 4 x 4 banks	
I/O ports	CMOS input	8	Internal pull-up resistor connection can be specified by software: 7
	CMOS I/O	20	Internal pull-up resistor connection can be specified by software: 12 Shared by segment pin: 8
	N-ch open-drain I/O	4	13-V withstand voltage
	Total	32	
LCD controller/driver		• Segment number selection: 16/20/24 segments (Switchable to CMOS I/O ports in a batch of 4 pins, max. 8 pins) • Display mode selection : static, 1/2 duty (1/2 bias), 1/3 duty (1/2 bias), 1/3 duty (1/3 bias), 1/4 duty (1/3 bias)	
Timers		5 channels: • 8-bit timer/event counter : 3 channels (Can be used as 16-bit timer/event counter, carrier generator, and timer with gate) • Basic interval timer/watchdog timer : 1 channel • Watch timer : 1 channel	
Serial interface		• 3-wire serial I/O mode ··· MSB/LSB first switchable • 2-wire serial I/O mode • SBI mode	
Bit sequential buffer (BSB)		16 bits	
Clock output (PCL)		Φ, 524, 262, and 65.5 kHz (main system clock: @ 4.19 MHz) Φ, 750, 375, and 93.8 kHz (main system clock: @ 6.0 MHz)	
Buzzer output (BUZ)		• 2, 4, and 32 kHz (main system clock: @ 4.19 MHz or subsystem clock: @ 32.768 kHz) • 2.93, 5.86, 46.9 kHz (main system clock: @ 6.0 MHz)	
Vectored interrupts		• External : 3 • Internal : 5	
Test inputs		• External : 1 • Internal : 1	
System clock oscillation circuit		• Ceramic/crystal oscillation circuit for main system clock • Crystal oscillation circuit for subsystem clock	
Standby function		STOP/HALT mode	
Power supply voltage		V_{DD} = 1.8 to 5.5 V	
Package		• 64-pin plastic QFP (14 x 14 mm, 0.8-mm pitch) • 64-pin plastic QFP (12 x 12 mm, 0.65-mm pitch)	

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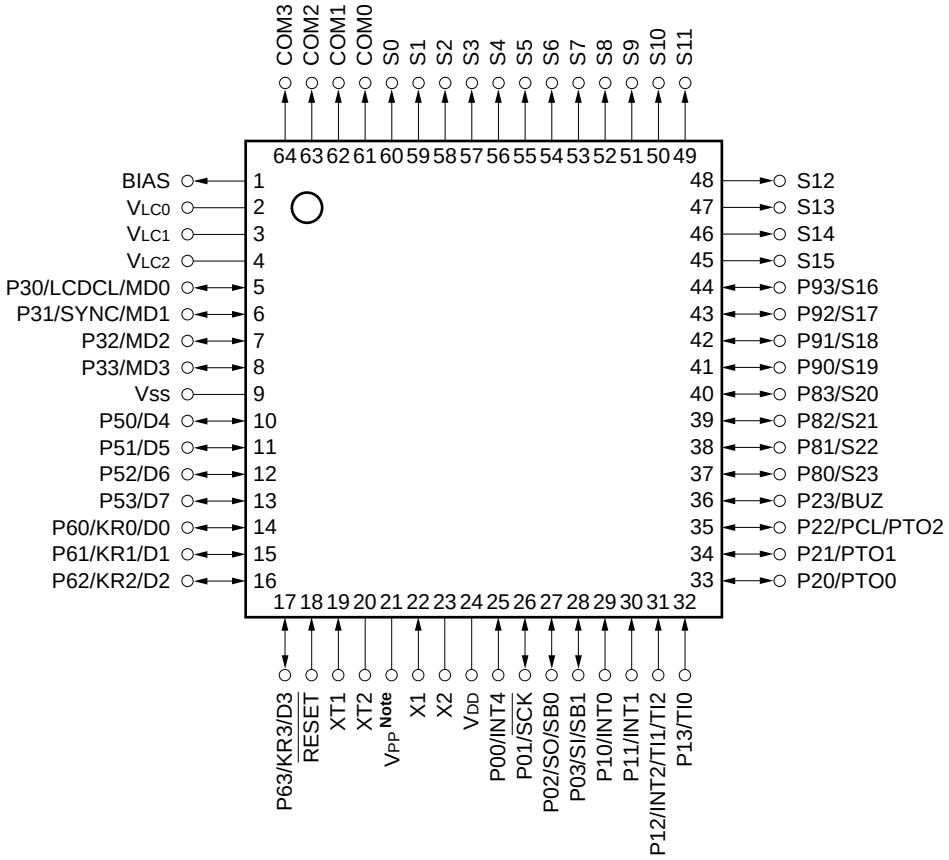
1. PIN CONFIGURATION (Top View)

- 64-pin plastic QFP (14 x 14 mm, 0.8-mm pitch) : μPD75P3116GC-AB8
- 64-pin plastic QFP (12 x 12 mm, 0.65-mm pitch) : μPD75P3116GK-8A8

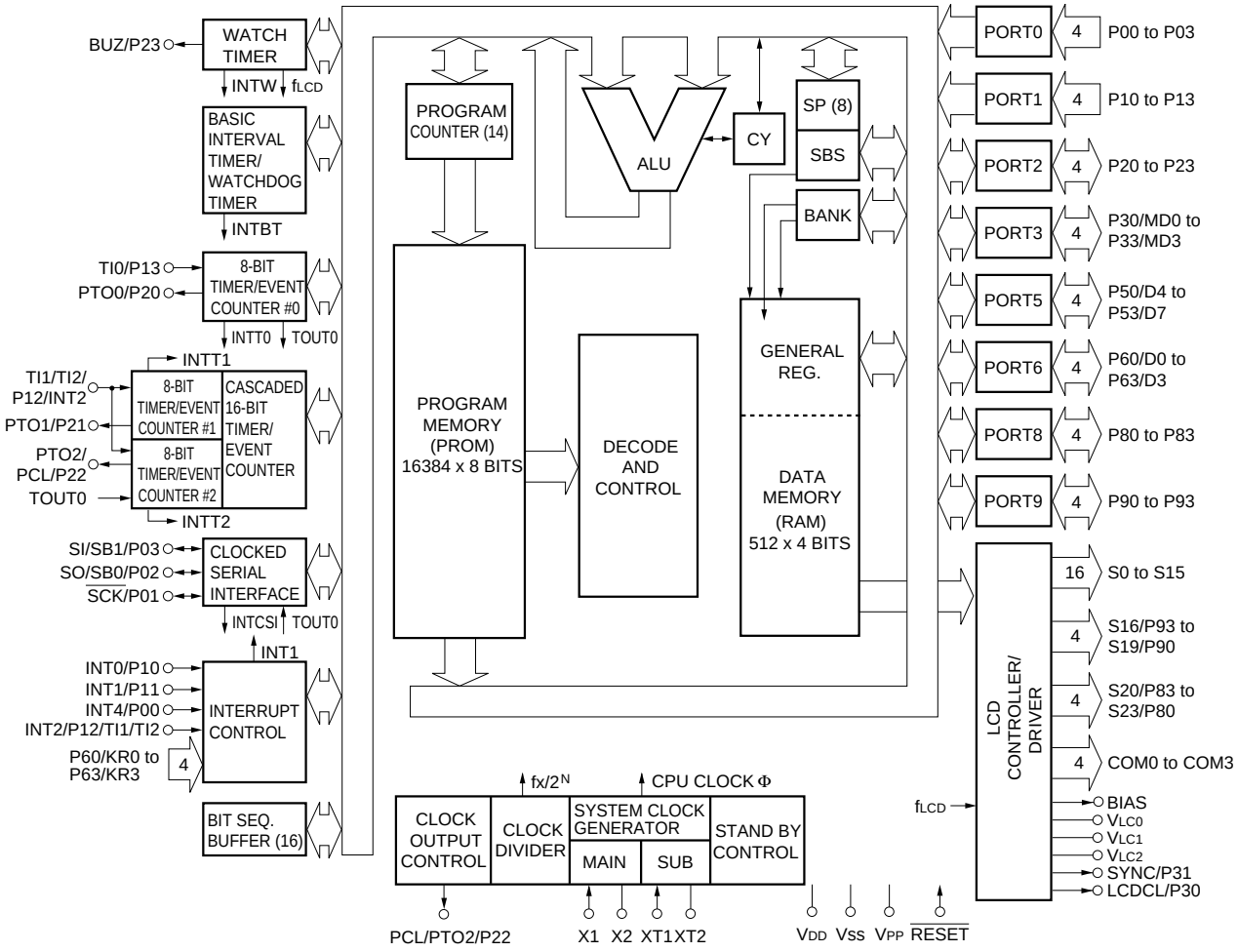


Note Always connect the V_{PP} pin directly to V_{DD} during normal operation.

PIN IDENTIFICATIONS

P00-P03	: Port0	COM0 to COM3	: Common Output 0 to 3
P10-P13	: Port1	V_{LC0} to V_{LC2}	: LCD Power Supply 0 to 2
P20-P23	: Port2	BIAS	: LCD Power Supply Bias Control
P30-P33	: Port3	LCDCL	: LCD Clock
P50-P53	: Port5	SYNC	: LCD Synchronization
P60-P63	: Port6	TI0 to TI2	: Timer Input 0 to 2
P80-P83	: Port8	PTO0 to PTO2	: Programmable Timer Output 0 to 2
P90-P93	: Port9	BUZ	: Buzzer Clock
KR0-KR3	: Key Return 0 to 3	PCL	: Programmable Clock
$\overline{SCK}$	: Serial Clock	INT0, 1, 4	: External Vectored Interrupt 0, 1, 4
SI	: Serial Input	INT2	: External Test Input 2
SO	: Serial Output	X1, X2	: Main System Clock Oscillation 1, 2
SB0, SB1	: Serial Data Bus 0, 1	XT1, XT2	: Subsystem Clock Oscillation 1, 2
$\overline{RESET}$	: Reset	V_{PP}	: Programming Power Supply
MD0 to MD3	: Mode Selection 0 to 3	V_{DD}	: Positive Power Supply
D0 to D7	: Data Bus 0 to 7	Vss	: Ground
S0 to S23	: Segment Output 0 to 23		

2. BLOCK DIAGRAM



3. PIN FUNCTIONS

3.1 Port Pins (1/2)

Pin name	I/O	Alternate function	Function	8-bit I/O	Status after reset	I/O circuit type[Note 1]
P00	Input	INT4	4-bit input port (PORT0) P01 to P03 are 3-bit pins for which connection of an internal pull-up resistor can be specified by software.	X	Input	<B>
P01	I/O	$\overline{\text{SCK}}$				<F>-A
P02	I/O	SO/SB0				<F>-B
P03	I/O	SI/SB1				<M>-C
P10	Input	INT0	4-bit input port (PORT1) Connection of an internal pull-up resistor can be specified by software in 4-bit units. P10/INT0 can select noise elimination circuit.	X	Input	<B>-C
P11		INT1				
P12		TI1/TI2/INT2				
P13		TI0				
P20	I/O	PTO0	4-bit I/O port (PORT2) Connection of an internal pull-up resistor can be specified by software in 4-bit units.	X	Input	E-B
P21		PTO1				
P22		PCL/PTO2				
P23		BUZ				
P30	I/O	LCDCL/MD0	Programmable 4-bit I/O port (PORT3) Input and output in single-bit units can be specified. When set for 4-bit units, connection of an internal pull-up resistor can be specified by software.	X	Input	E-B
P31		SYNC/MD1				
P32		MD2				
P33		MD3				
P50 [Note 2]	I/O	D4	N-ch open-drain 4-bit I/O port (PORT5) When set to open-drain, voltage is 13 V.	X	High impedance	M-E
P51 [Note 2]		D5				
P52 [Note 2]		D6				
P53 [Note 2]		D7				

Notes 1. Circuit types enclosed in brackets indicate Schmitt trigger input.

2. Low-level input leakage current increases when input instructions or bit manipulation instructions are executed.

3.1 Port Pins (2/2)

Pin name	I/O	Alternate function	Function	8-bit I/O	Status after reset	I/O circuit type Note 1
P60	I/O	KR0/D0	Programmable 4-bit I/O port (PORT6) Input and output in single-bit units can be specified. When set for 4-bit units, connection of an internal pull-up resistor can be specified by software.	X	Input	<F>-A
P61		KR1/D1				
P62		KR2/D2				
P63		KR3/D3				
P80	I/O	S23	4-bit I/O port (PORT8) When set for 4-bit units, connection of an internal pull-up resistor can be specified by software Note 3.	○	Input	H
P81		S22				
P82		S21				
P83		S20				
P90	I/O	S19	Programmable 4-bit I/O port (PORT9) When set for 4-bit units, connection of an internal pull-up resistor can be specified by software Note 3.	○	Input	H
P91		S18				
P92		S17				
P93		S16				

Notes 1. Circuit types enclosed in brackets indicate Schmitt trigger input.

2. Low-level leak current increases when an input instruction or a bit manipulation instruction is performed.

3. Do not connect an internal pull-up resistor by software when used as the segment signal output.

3.2 Non-port Pins (1/2)

Pin name	I/O	Alternate function	Function		Status after reset	I/O circuit type[Note 1]
TI0	Input	P13	External event pulse input to timer/event counter		Input	<B>-C
TI1		P12/INT2/TI2				
TI2		P12/INT2/TI1				
PTO0	Output	P20	Timer/event counter output		Input	E-B
PTO1		P21				
PTO2		P22/PCL				
PCL		P22/PTO2	Clock output			
BUZ		P23	Frequency output (for buzzer or system clock trimming)			
$\overline{SCK}$	I/O	P01	Serial clock I/O		Input	<F>-A
SO/SB0		P02	Serial data output Serial data bus I/O			<F>-B
SI/SB1		P03	Serial data input Serial data bus I/O			<M>-C
INT4	Input	P00	Edge detection vectored interrupt input (valid for detecting both rising and falling edges)			<B>
INT0	Input	P10	Edge detection vectored interrupt input (detection edge is selectable)	With noise elimination circuit/asynch is selectable	Input	<B>-C
INT1		P11	INT0/P10 can select noise elimination circuit.	Asynch		
INT2	Input	P12/TI1/TI2	Rising edge detection testable input	Asynch		
KR0 to KR3	I/O	P60 to P63	Parallel falling edge detection testable input		Input	<F>-A
X1	Input	—	Ceramic/crystal resonator connection for main system clock oscillation. If using an external clock, input signal to X1 and input inverted phase to X2.		—	—
X2	—					
XT1	Input	—	Crystal resonator connection for subsystem clock oscillation. If using an external clock, input signal to XT1 and input inverted phase to XT2. XT1 can be used as a 1-bit (test) input.		—	—
XT2	—					
$\overline{RESET}$	Input	—	System reset input (low-level active)		—	<B>
MD0 to MD3	Input	P30 to P33	Mode selection for program memory (PROM) write/verify		Input	E-B
★ D0 to D3	I/O	P60/KR0 to P63/KR3	Data bus for program memory (PROM) write/verify		Input	<F>-A
★ D4 to D7		P50 to P53				M-E
V_{PP} [Note 2]	—	—	Programmable power supply voltage applied for program memory (PROM) write/verify. For normal operation, connect directly to V_{DD}. Apply +12.5 V for PROM write/verify.		—	—
V_{DD}	—	—	Positive power supply		—	—
Vss	—	—	Ground potential		—	—

Notes 1. Circuit types enclosed in brackets indicate Schmitt trigger input.

2. The V_{PP} pin does not operate correctly when it is not connected to the V_{DD} pin during normal operation.

3.2 Non-port Pins (2/2)

Pin name	I/O	Alternate function	Function	Status after reset	I/O circuit type
S0 to S15	Output	—	Segment signal output	**Note 1**	G-A
S16 to S19	Output	P93 to P90	Segment signal output	Input	H
S20 to S23	Output	P83 to P80	Segment signal output	Input	H
COM0 to COM3	Output	—	Common signal output	**Note 1**	G-B
V_{LC0} to V_{LC2}	—	—	Power supply for driving LCD	—	—
BIAS	Output	—	Output for external split resistor cut	**Note 2**	—
LCDCL Note 3	I/O	P30/MD0	Clock output for driving external expansion driver	Input	E-B
SYNC Note 3	I/O	P31/MD1	Clock output for synchronization of external expansion driver	Input	E-B

Notes 1. The V_{PP} pin does not operate normally if it is not connected with V_{DD} pin when normal operation.

2. The V_{LCX} (X = 0, 1, 2) shown below are selected as the input source for the display outputs.
S0 to S23: V_{LC1}, COM0 to COM2: V_{LC2}, COM3: V_{LC0}

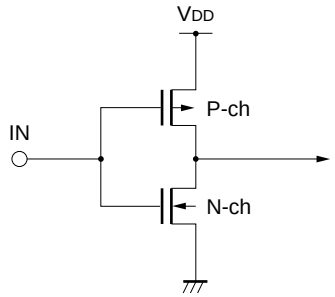
3. When the split resistor is incorporated : Low level
When the split resistor is not incorporated : High impedance

4. These pins are provided for future system expansion. Currently, only P30 and P31 are used.

3.3 Equivalent Circuits for Pins

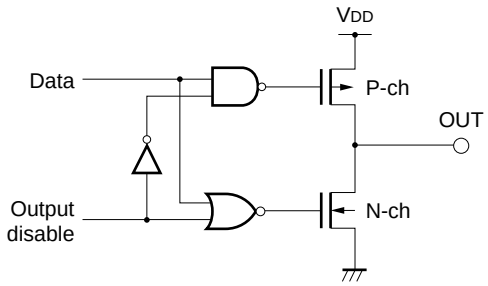
The equivalent circuits for the μPD75P3116's pins are shown in abbreviated form below.

TYPE A



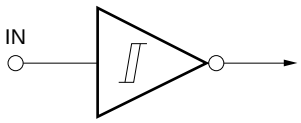
CMOS standard input buffer

TYPE D



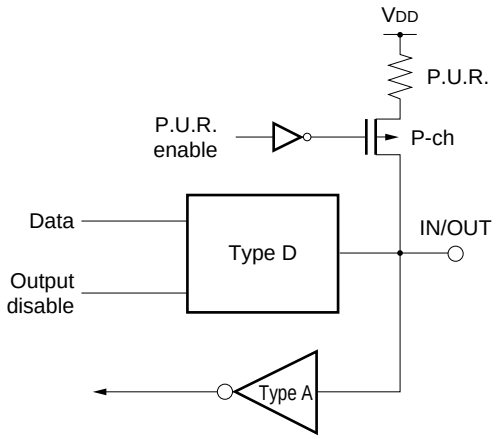
Push-pull output that can be set to high impedance output (with both P-ch and N-ch OFF).

TYPE B



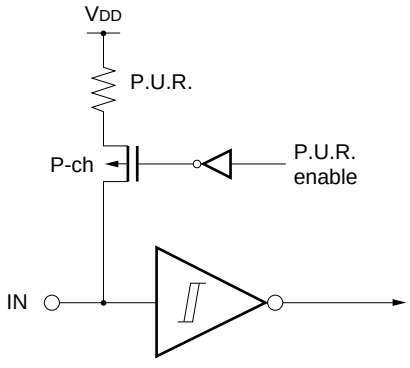
Schmitt trigger input with hysteresis characteristics.

TYPE E-B



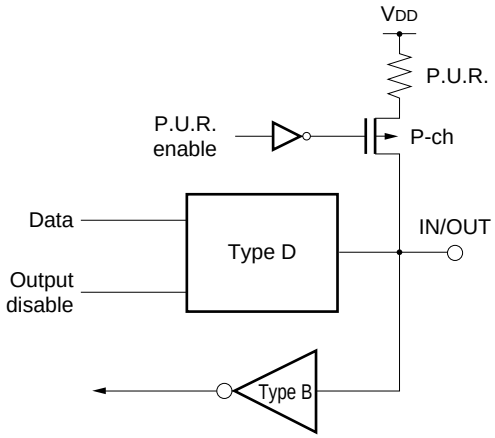
P.U.R. : Pull-Up Resistor

TYPE B-C



P.U.R. : Pull-Up Resistor

TYPE F-A

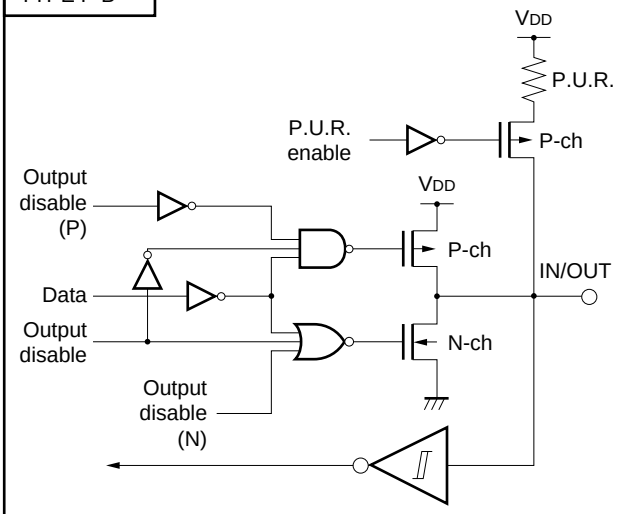


P.U.R. : Pull-Up Resistor

(Continued)

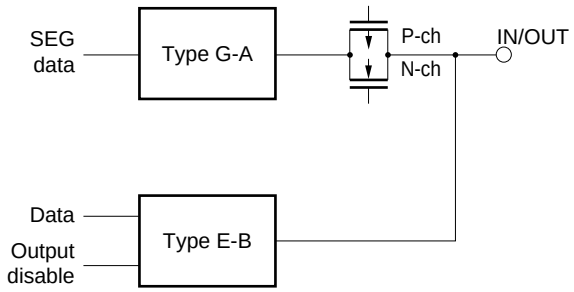
(Continued)

TYPE F-B

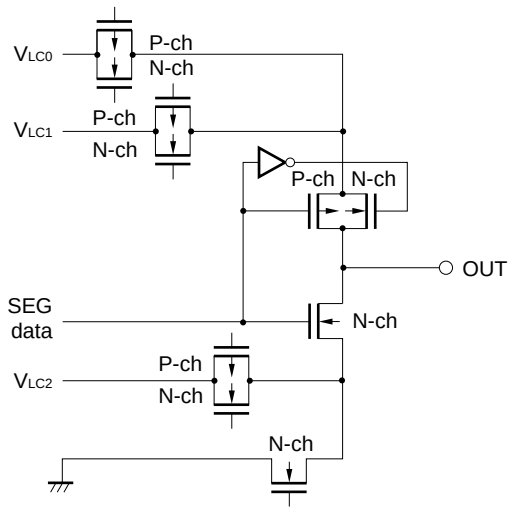


P.U.R. : Pull-Up Resistor

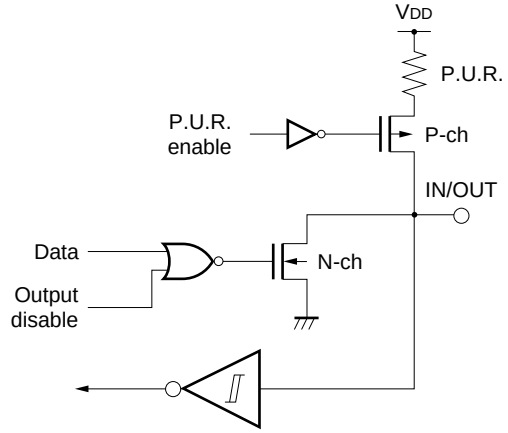
TYPE H



★ TYPE G-A

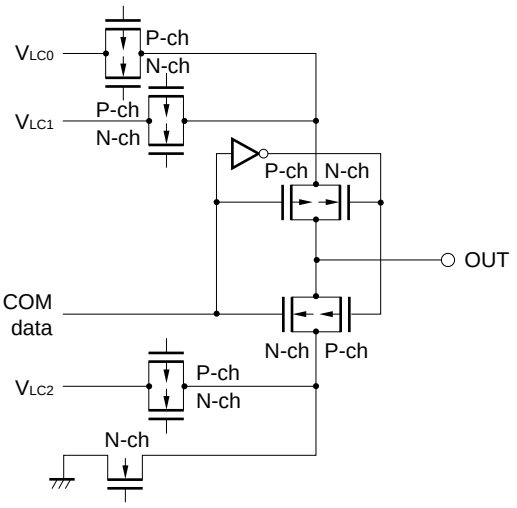


TYPE M-C

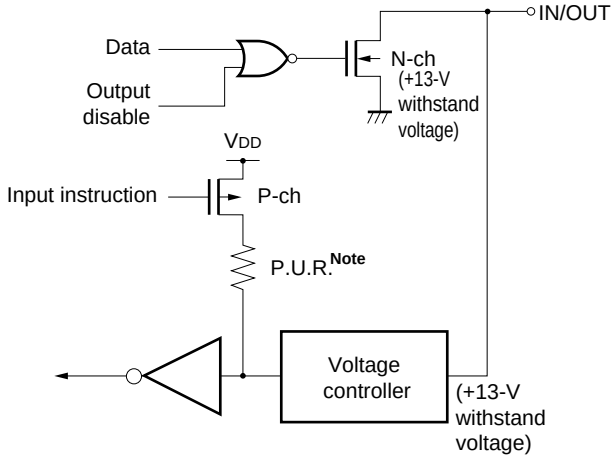


P.U.R. : Pull-Up Resistor

TYPE G-B



★ TYPE M-E



Note Pull-up resistor that operates only when an input instruction is executed. (The current flows from V_{DD} to a pin when the pin is at low level.)

3.4 Recommended Connection of Unused Pins

★ **Table 3-1. List of Unused Pin Connection**

Pin	Recommended connection
P00/INT4	Connect to Vss or V_{DD}
P01/$\overline{SCK}$	Individually connect to Vss or V_{DD} through a resistor.
P02/SO/SB0	
P03/SI/SB1	Connect to Vss
P10/INT0 and P11/INT1	Connect to Vss or V_{DD}
P12/TI1/TI2/INT2	
P13/TI0	
P20/PTO0	Input status : Individually connect to Vss or V_{DD} through a resistor Output status : Leave open
P21/PTO1	
P22/PTO2/PCL	
P23/BUZ	
P30/LCDCL/MD0	
P31/SYNC/MD1	
P32/MD2	
P33/MD3	
P50/D4 to P53/D7	Connect to Vss
P60/KR0/D0 to P63/KR3/D3	Input status : Individually connect to Vss or V_{DD} through a resistor Output status : Leave open
S0 to S15	Leave open
COM0 to COM3	
S16/P93 to S19/P90	Input status : Individually connect to Vss or V_{DD} through a resistor
S20/P83 to S23/P80	Output status : Leave open
V_{LC0} to V_{LC2}	Connect to Vss
BIAS	Connect to Vss only when neither of V_{LC0}, V_{LC1} and V_{LC2} is used. In other cases, leave open.
XT1 Note	Connect to Vss or V_{DD}
XT2 Note	Leave open
V_{PP}	Always connect to V_{DD} directly

Note In case the subsystem clock is not used, set SOS.0 = 1 (on-chip feedback resistor not used).

4. Mk I AND Mk II MODE SELECTION FUNCTION

Setting a stack bank selection (SBS) register for the μPD75P3116 enables the program memory to be switched between the Mk I mode and Mk II mode. This function is applicable when using the μPD75P3116 to evaluate the μPD753104, 753106, or 753108.

When the SBS bit 3 is set to 1 : sets the Mk I mode (supports the Mk I mode for the μPD753104, 753106, and 753108)
When the SBS bit 3 is set to 0 : sets the Mk II mode (supports the Mk II mode for the μPD753104, 753106, and 753108)

4.1 Differences between Mk I Mode and Mk II Mode

Table 4-1 lists differences between the Mk I mode and the Mk II mode for the μPD75P3116.

Table 4-1. Differences between Mk I Mode and Mk II Mode

Item		Mk I mode	Mk II mode
Program counter		PC_{13-0}	
Program memory (bytes)		16384	
Data memory (bits)		512 x 4	
Stack	Stack bank	Selectable via memory banks 0, 1	
	No. of stack bytes	2 bytes	3 bytes
Instruction	BRA !addr1 instruction CALLA !addr1 instruction	Not available	Available
Instruction execution time	CALL !addr instruction	3 machine cycles	4 machine cycles
	CALLF !faddr instruction	2 machine cycles	3 machine cycles
Supported mask ROMs		When set to Mk I mode: μPD753104, 753106, and 753108	When set to Mk II mode: μPD753104, 753106, and 753108

★ **Caution The Mk II mode supports a program area exceeding 16 Kbytes for the 75X and 75XL Series. Therefore, this mode is effective for enhancing software compatibility with products that have a program area of more than 16 Kbytes.**
With regard to the number of stack bytes during execution of subroutine call instructions, the usable area increases by 1 byte per stack compared to the Mk I mode when the Mk II mode is selected.
However, when the CALL !addr and CALLF !faddr instructions are used, the machine cycle becomes longer by 1 machine cycle. Therefore, if more emphasis is placed on RAM use efficiency and processing performance than on software compatibility, the Mk I mode should be used.

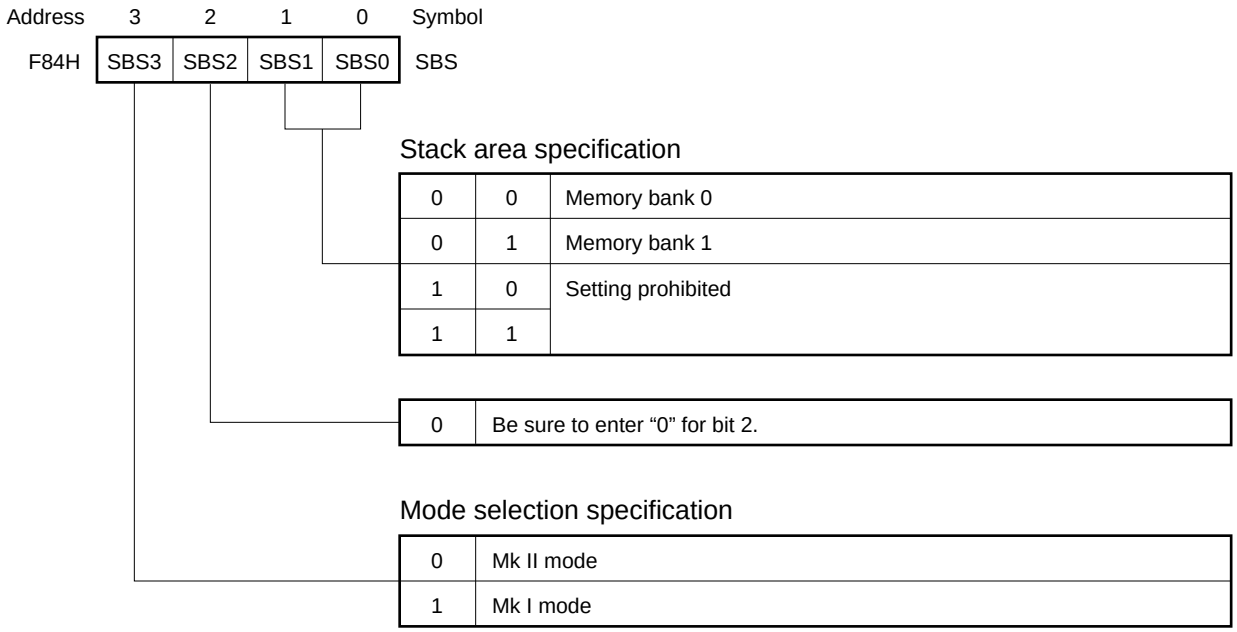
4.2 Setting of Stack Bank Selection (SBS) Register

Use the stack bank selection register to switch between the Mk I mode and Mk II mode. **Figure 4-1** shows the format of the stack bank selection register.

The stack bank selection register is set using a 4-bit memory manipulation instruction. When using the Mk I mode, be sure to initialize the stack bank selection register to 100XB [Note] at the beginning of the program. When using the Mk II mode, be sure to initialize it to 000XB [Note].

Note Set the desired value for X.

Figure 4-1. Format of Stack Bank Selection Register



Caution SBS3 is set to “1” after $\overline{\text{RESET}}$ input, and consequently the CPU operates in the Mk I mode. When using instructions for the Mk II mode, set SBS3 to “0” and set the Mk II mode before using the instructions.

5. DIFFERENCES BETWEEN μPD75P3116 AND μPD753104, 753106, 753108

The μPD75P3116 replaces the internal mask ROM in the μPD753104, 753106, and 753108 with a one-time PROM and features expanded ROM capacity. The μPD75P3116's Mk I mode supports the Mk I mode in the μPD753104, 753106, and 753108 and the μPD75P3116's Mk II mode supports the Mk II mode in the μPD753104, 753106, and 753108.
Table 5-1 lists differences among the μPD75P3116 and the μPD753104, 753106, and 753108. Be sure to check the differences among these products before using them with PROMs for debugging or prototype testing of application systems or, later, when using them with a mask ROM for full-scale production.
For details on the CPU functions and internal hardware, refer to the **User's Manual**.

Table 5-1. Differences between μPD75P3116 and μPD753104, 753106, and 753108

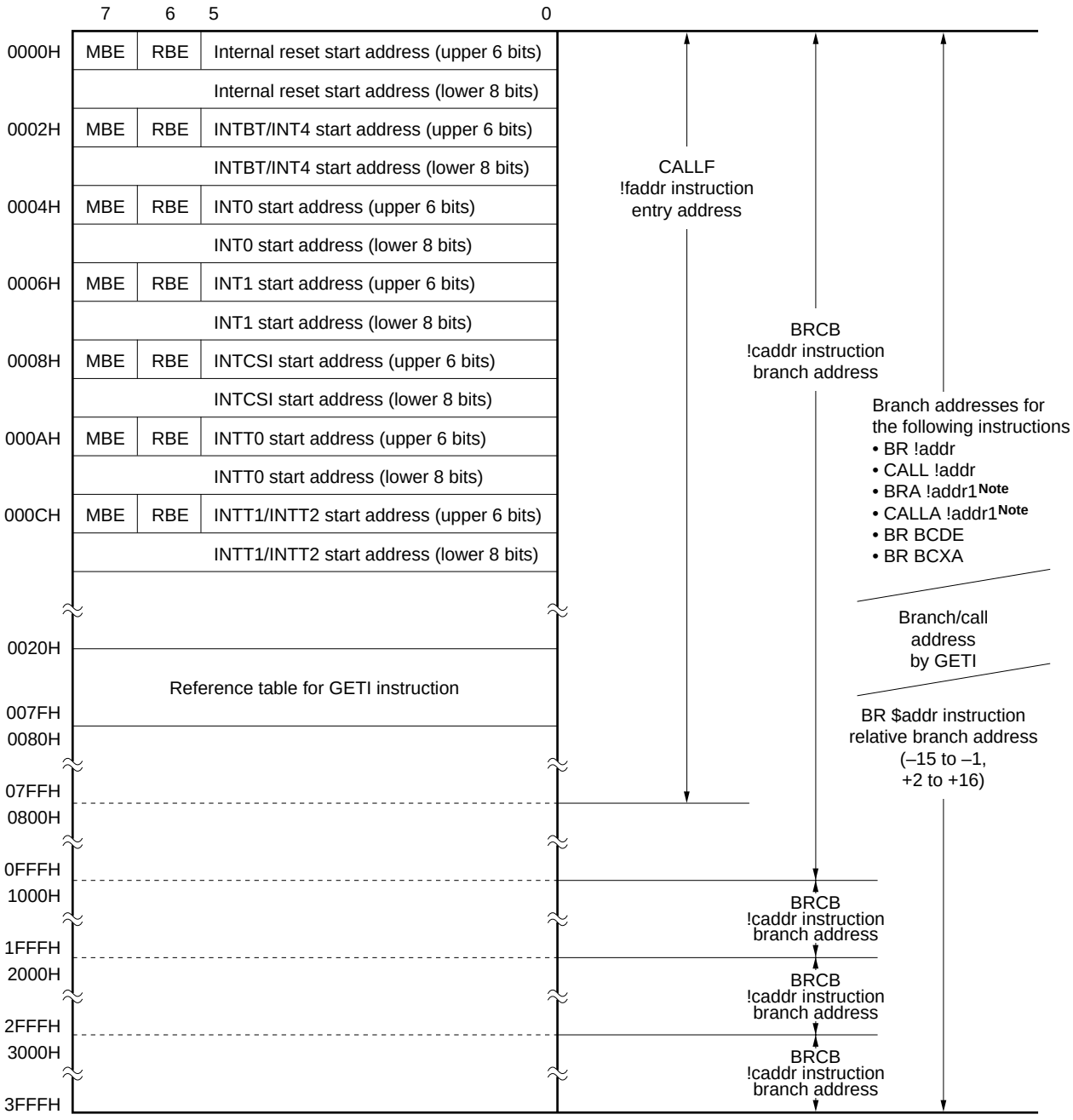
Item		μPD753104	μPD753106	μPD753108	μPD75P3116
Program counter		12 bits	13 bits		14 bits
Program memory (bytes)		Mask ROM 4096	Mask ROM 6144	Mask ROM 8192	One-time PROM 16384
Data memory (x 4 bits)		512			
Mask options	Pull-up resistor for PORT5	Available (On chip/not on chip can be specified.)			Not available (Not on chip)
	Split resistor for LCD driving power supply				
	$\overline{\text{RESET}}$ Wait time after RESET	Available (Selectable between $2^{17}/f_X$ and $2^{15}/f_X$)			Not available (fixed to $2^{15}/f_X$) Note
	Feedback resistor of subsystem clock	Available (Use/not use can be selected.)			Not available (Enable)
Pin configuration	Pin Nos. 5 to 8	P30 to P33			P30/MD0 to P33/MD3
	Pin Nos. 10 to 13	P50 to P53			P50/D4 to P53/D7
	Pin Nos. 14 to 17	P60/KR0 to P63/KR3			P60/KR0/D0 to P63/KR3/D3
	Pin No. 21	IC			V_{PP}
Other		Noise resistance and noise radiation may differ due to the different circuit sizes and mask layouts.			

Note $2^{17}/f_X$: 21.8 ms at 6.0-MHz operation, 31.3 ms at 4.19-MHz operation
$2^{15}/f_X$: 5.46 ms at 6.0-MHz operation, 7.81 ms at 4.19-MHz operation

Caution Noise resistance and noise radiation are different in PROM and mask ROMs. When changing from PROM versions to mask ROM versions when switching from prototype development to full production, be sure to fully evaluate the mask ROM version's CS (not ES).

6. MEMORY CONFIGURATION

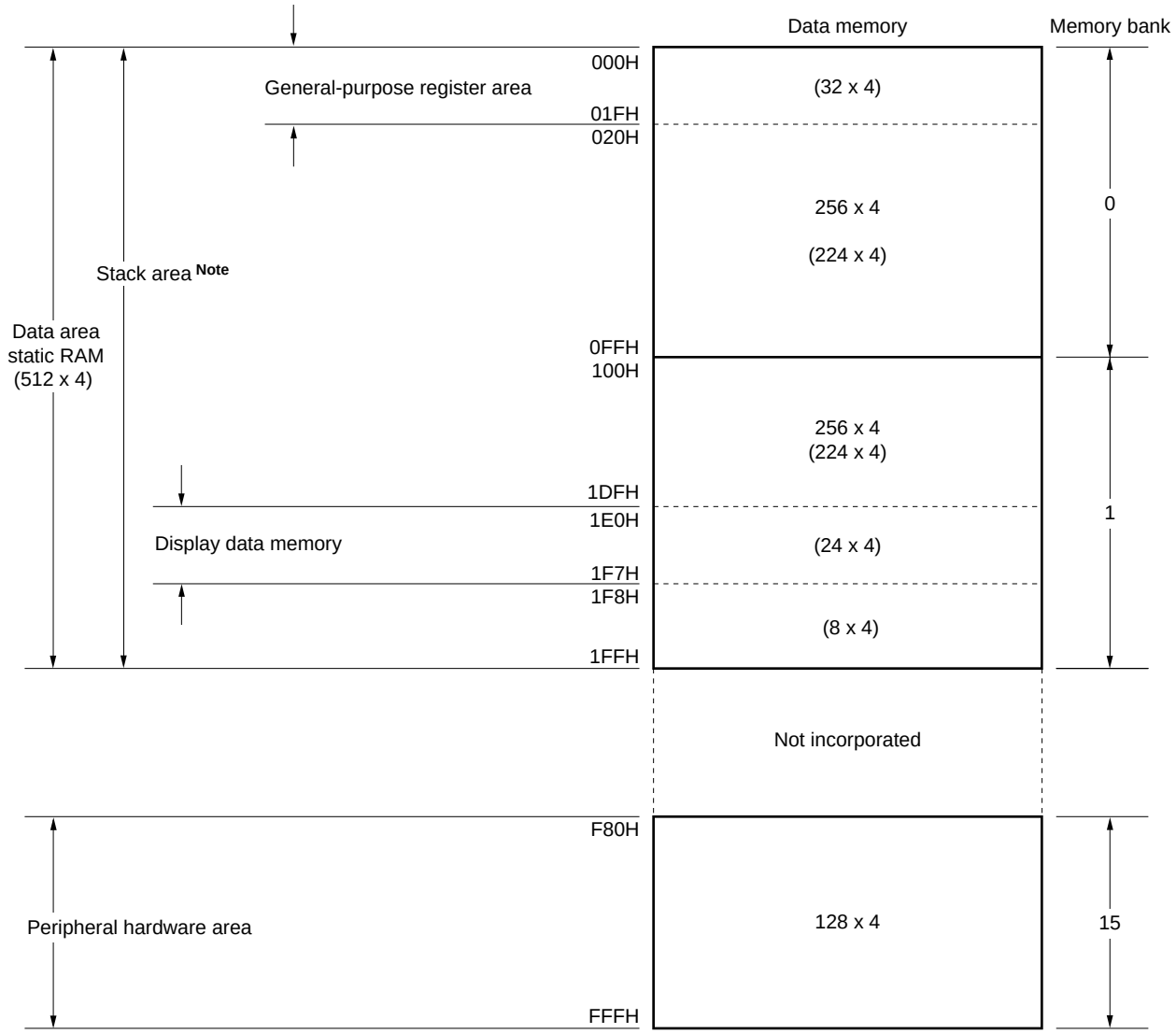
Figure 6-1. Program Memory Map



Note Can be used only in the Mk II mode

Remark For instructions other than those noted above, the BR PCDE and BR PCXA instructions can be used to branch to addresses with changes in the PC's lower 8 bits only.

Figure 6-2. Data Memory Map



Note Memory bank 0 or 1 can be selected as the stack area.

7. INSTRUCTION SET

(1) Representation and coding formats for operands

In the instruction's operand area, use the following coding format to describe operands corresponding to the instruction's operand representations (for further description, refer to the **RA75X Assembler Package User's Manual Language (EEU-1363)**). When there are several codes, select and use just one. Codes that consist of upper-case letters and + or – symbols are key words that should be entered as they are.

For immediate data, enter an appropriate numerical value or label.

Enter register flag symbols as label descriptors instead of mem, fmem, pmem, bit, etc. (for further description, refer to the **User's Manual**). The number of labels that can be entered for fmem and pmem are restricted.

Representation	Coding format
reg	X, A, B, C, D, E, H, L
reg1	X, B, C, D, E, H, L
rp	XA, BC, DE, HL
rp1	BC, DE, HL
rp2	BC, DE
rp'	XA, BC, DE, HL, XA', BC', DE', HL'
rp'1	BC, DE, HL, XA', BC', DE', HL'
rpa	HL, HL+, HL–, DE, DL
rpa1	DE, DL
n4	4-bit immediate data or label
n8	8-bit immediate data or label
mem	8-bit immediate data or label[Note]
bit	2-bit immediate data or label
fmem	FB0H to FBFH, FF0H to FFFH immediate data or label
pmem	FC0H to FFFH immediate data or label
addr	0000H to 3FFFH immediate data or label
addr1	0000H to 3FFFH immediate data or label (Mk II mode only)
caddr	12-bit immediate data or label
faddr	11-bit immediate data or label
taddr	20H to 7FH immediate data (however, bit0 = 0) or label
PORTn	PORT0 to PORT3, PORT5, PORT6, PORT8, PORT9
IEXXX	IEBT, IECSI, IET0 to IET2, IE0 to IE2, IE4, IEW
RBn	RB0 to RB3
MBn	MB0, MB1, MB15

Note When processing 8-bit data, only even-numbered addresses can be specified.

(2) Operation legend

A	: A register; 4-bit accumulator
B	: B register
C	: C register
D	: D register
E	: E register
H	: H register
L	: L register
X	: X register
XA	: Register pair (XA); 8-bit accumulator
BC	: Register pair (BC)
DE	: Register pair (DE)
HL	: Register pair (HL)
XA'	: Expansion register pair (XA')
BC'	: Expansion register pair (BC')
DE'	: Expansion register pair (DE')
HL'	: Expansion register pair (HL')
PC	: Program counter
SP	: Stack pointer
CY	: Carry flag; bit accumulator
PSW	: Program status word
MBE	: Memory bank enable flag
RBE	: Register bank enable flag
PORTn	: Port n (n = 0 to 3, 5, 6, 8, 9)
IME	: Interrupt master enable flag
IPS	: Interrupt priority selection register
IEXXX	: Interrupt enable flag
RBS	: Register bank selection register
MBS	: Memory bank selection register
PCC	: Processor clock control register
.	: Delimiter for address and bit
(XX)	: Addressed data with xx
XXH	: Hexadecimal data

(3) Description of symbols used in addressing area

*1	MB = MBE • MBS MBS = 0, 1, 15	Data memory addressing
*2	MB = 0	
*3	MBE = 0 : MB = 0 (000H to 07FH) MB = 15 (F80H to FFFH) MBE = 1 : MB = MBS MBS = 0, 1, 15	
*4	MB = 15, fmem = FB0H to FBFH, FF0H to FFFH	
*5	MB = 15, pmem = FC0H to FFFH	
*6	addr = 0000H to 3FFFH	Program memory addressing
*7	addr, addr1 = (Current PC) –15 to (Current PC) –1 (Current PC) +2 to (Current PC) +16	
*8	caddr = 0000H to 0FFFH ($PC_{13, 12}$ = 00B) or 1000H to 1FFFH ($PC_{13, 12}$ = 01B) or 2000H to 2FFFH ($PC_{13, 12}$ = 10B) or 3000H to 3FFFH ($PC_{13, 12}$ = 11B)	
*9	faddr = 0000H to 07FFH	
*10	taddr = 0020H to 007FH	
*11	addr1 = 0000H to 3FFFH (Mk II mode only)	

Remarks 1. MB indicates access-enabled memory banks.

2. In area *2, MB = 0 for both MBE and MBS.

3. In areas *4 and *5, MB = 15 for both MBE and MBS.

4. Areas *6 to *11 indicate corresponding address-enabled areas.

(4) Description of machine cycles

S indicates the number of machine cycles required for skipping of skip-specified instructions. The value of S varies as shown below.

- No skip ..... S = 0
- Skipped instruction is 1-byte or 2-byte instruction .... S = 1
- Skipped instruction is 3-byte instruction[Note] ..... S = 2

Note 3-byte instructions: BR !addr, BRA !addr1, CALL !addr, and CALLA !addr1

Caution The GETI instruction is skipped for one machine cycle.

One machine cycle equals one cycle (= t_{CY}) of the CPU clock Φ. Use the PCC setting to select among four cycle times.

Instruction group	Mnemonic	Operand	No. of bytes	Machine cycle	Operation	Addressing area	Skip condition
Transfer	MOV	A, #n4	1	1	A<-n4		String-effect A
		reg1, #n4	2	2	reg1<-n4		
		XA, #n8	2	2	XA<-n8		String-effect A
		HL, #n8	2	2	HL<-n8		String-effect B
		rp2, #n8	2	2	rp2<-n8		
		A, @HL	1	1	A<-(HL)	*1	
		A, @HL+	1	2+S	A<-(HL), then L<-L+1	*1	L=0
		A, @HL–	1	2+S	A<-(HL), then L<-L–1	*1	L=FH
		A, @rpa1	1	1	A<-(rpa1)	*2	
		XA, @HL	2	2	XA<-(HL)	*1	
		@HL, A	1	1	(HL)<-A	*1	
		@HL, XA	2	2	(HL)<-XA	*1	
		A, mem	2	2	A<-(mem)	*3	
		XA, mem	2	2	XA<-(mem)	*3	
		mem, A	2	2	(mem)<-A	*3	
		mem, XA	2	2	(mem)<-XA	*3	
		A, reg	2	2	A<-reg		
		XA, rp’	2	2	XA<-rp’		
		reg1, A	2	2	reg1<-A		
		rp’1, XA	2	2	rp’1<-XA		
	XCH	A, @HL	1	1	A<->(HL)	*1	
		A, @HL+	1	2+S	A<->(HL), then L<-L+1	*1	L=0
		A, @HL–	1	2+S	A<->(HL), then L<-L–1	*1	L=FH
		A, @rpa1	1	1	A<->(rpa1)	*2	
		XA, @HL	2	2	XA<->(HL)	*1	
		A, mem	2	2	A<->(mem)	*3	
		XA, mem	2	2	XA<->(mem)	*3	
		A, reg1	1	1	A<->reg1		
		XA, rp’	2	2	XA<->rp’		
Table reference	MOVT	XA, @PCDE	1	3	$XA\leftarrow(PC_{13\text{-}8}+DE)_{ROM}$		
		XA, @PCXA	1	3	$XA\leftarrow(PC_{13\text{-}8}+XA)_{ROM}$		
		XA, @BCDE[Note]	1	3	$XA\leftarrow(BCDE)_{ROM}$	*6	
		XA, @BCXA[Note]	1	3	$XA\leftarrow(BCXA)_{ROM}$	*6	

Note Only the lower 3 bits in the B register are valid.

Instruction group	Mnemonic	Operand	No. of bytes	Machine cycle	Operation	Addressing area	Skip condition
Bit transfer	MOV1	CY, fmem.bit	2	2	CY<-(fmem.bit)	*4	
		CY, pmem.@L	2	2	CY<-(pmem$_{7-2}$+L$_{3-2}$.bit(L$_{1-0}$))	*5	
		CY, @H+mem.bit	2	2	CY<-(H+mem$_{3-0}$.bit)	*1	
		fmem.bit, CY	2	2	(fmem.bit)<-CY	*4	
		pmem.@L, CY	2	2	(pmem$_{7-2}$+L$_{3-2}$.bit(L$_{1-0}$))<-CY	*5	
		@H+mem.bit, CY	2	2	(H+mem$_{3-0}$.bit)<-CY	*1	
Arithmetic	ADDS	A, #n4	1	1+S	A<-A+n4		carry
		XA, #n8	2	2+S	XA<-XA+n8		carry
		A, @HL	1	1+S	A<-A+(HL)	*1	carry
		XA, rp'	2	2+S	XA<-XA+rp'		carry
		rp'1, XA	2	2+S	rp'1<-rp'1+XA		carry
	ADDC	A, @HL	1	1	A, CY<-A+(HL)+CY	*1	
		XA, rp'	2	2	XA, CY<-XA+rp'+CY		
		rp'1, XA	2	2	rp'1, CY<-rp'1+XA+CY		
	SUBS	A, @HL	1	1+S	A<-A–(HL)	*1	borrow
		XA, rp'	2	2+S	XA<-XA–rp'		borrow
		rp'1, XA	2	2+S	rp'1<-rp'1–XA		borrow
	SUBC	A, @HL	1	1	A, CY<-A–(HL)–CY	*1	
		XA, rp'	2	2	XA, CY<-XA–rp'–CY		
		rp'1, XA	2	2	rp'1, CY<-rp'1–XA–CY		
	AND	A, #n4	2	2	A<-A ∧ n4		
		A, @HL	1	1	A<-A ∧ (HL)	*1	
		XA, rp'	2	2	XA<-XA ∧ rp'		
		rp'1, XA	2	2	rp'1<-rp'1 ∧ XA		
	OR	A, #n4	2	2	A<-A ∨ n4		
		A, @HL	1	1	A<-A ∨ (HL)	*1	
		XA, rp'	2	2	XA<-XA ∨ rp'		
		rp'1, XA	2	2	rp'1<-rp'1 ∨ XA		
	XOR	A, #n4	2	2	A<-A ∀ n4		
		A, @HL	1	1	A<-A ∀ (HL)	*1	
		XA, rp'	2	2	XA<-XA ∀ rp'		
		rp'1, XA	2	2	rp'1<-rp'1 ∀ XA		
Accumulator manipulation	RORC	A	1	1	CY<-A$_0$, A$_3$<-CY, A$_{n-1}$<-A$_n$		
	NOT	A	2	2	A<-$\overline{A}$		
Increment/ decrement	INCS	reg	1	1+S	reg<-reg+1		reg=0
		rp1	1	1+S	rp1<-rp1+1		rp1=00H
		@HL	2	2+S	(HL)<-(HL)+1	*1	(HL)=0
		mem	2	2+S	(mem)<-(mem)+1	*3	(mem)=0
	DECS	reg	1	1+S	reg<-reg–1		reg=FH
		rp'	2	2+S	rp'<-rp'–1		rp'=FFH

Instruction group	Mnemonic	Operand	No. of bytes	Machine cycle	Operation	Addressing area	Skip condition
Comparison	SKE	reg, #n4	2	2+S	Skip if reg=n4		reg=n4
		@HL, #n4	2	2+S	Skip if (HL)=n4	*1	(HL)=n4
		A, @HL	1	1+S	Skip if A=(HL)	*1	A=(HL)
		XA, @HL	2	2+S	Skip if XA=(HL)	*1	XA=(HL)
		A, reg	2	2+S	Skip if A=reg		A=reg
		XA, rp'	2	2+S	Skip if XA=rp'		XA=rp'
Carry flag manipulation	SET1	CY	1	1	CY<-1		
	CLR1	CY	1	1	CY<-0		
	SKT	CY	1	1+S	Skip if CY=1		CY=1
	NOT1	CY	1	1	CY<-$\overline{CY}$		
Memory bit manipulation	SET1	mem.bit	2	2	(mem.bit)<-1	*3	
		fmem.bit	2	2	(fmem.bit)<-1	*4	
		pmem.@L	2	2	($pmem_{7-2}$+L_{3-2}.bit(L_{1-0}))<-1	*5	
		@H+mem.bit	2	2	(H+mem_{3-0}.bit)<-1	*1	
	CLR1	mem.bit	2	2	(mem.bit)<-0	*3	
		fmem.bit	2	2	(fmem.bit)<-0	*4	
		pmem.@L	2	2	($pmem_{7-2}$+L_{3-2}.bit(L_{1-0}))<-0	*5	
		@H+mem.bit	2	2	(H+mem_{3-0}.bit)<-0	*1	
	SKT	mem.bit	2	2+S	Skip if(mem.bit)=1	*3	(mem.bit)=1
		fmem.bit	2	2+S	Skip if(fmem.bit)=1	*4	(fmem.bit)=1
		pmem.@L	2	2+S	Skip if($pmem_{7-2}$+L_{3-2}.bit(L_{1-0}))=1	*5	(pmem.@L)=1
		@H+mem.bit	2	2+S	Skip if(H+mem_{3-0}.bit)=1	*1	(@H+mem.bit)=1
	SKF	mem.bit	2	2+S	Skip if(mem.bit)=0	*3	(mem.bit)=0
		fmem.bit	2	2+S	Skip if(fmem.bit)=0	*4	(fmem.bit)=0
		pmem.@L	2	2+S	Skip if($pmem_{7-2}$+L_{3-2}.bit(L_{1-0}))=0	*5	(pmem.@L)=0
		@H+mem.bit	2	2+S	Skip if(H+mem_{3-0}.bit)=0	*1	(@H+mem.bit)=0
	SKTCLR	fmem.bit	2	2+S	Skip if(fmem.bit)=1 and clear	*4	(fmem.bit)=1
		pmem.@L	2	2+S	Skip if($pmem_{7-2}$+L_{3-2}.bit(L_{1-0}))=1 and clear	*5	(pmem.@L)=1
		@H+mem.bit	2	2+S	Skip if(H+mem_{3-0}.bit)=1 and clear	*1	(@H+mem.bit)=1
	AND1	CY, fmem.bit	2	2	CY<-CY ∧ (fmem.bit)	*4	
		CY, pmem.@L	2	2	CY<-CY ∧ ($pmem_{7-2}$+L_{3-2}.bit(L_{1-0}))	*5	
		CY, @H+mem.bit	2	2	CY<-CY ∧ (H+mem_{3-0}.bit)	*1	
	OR1	CY, fmem.bit	2	2	CY<-CY v (fmem.bit)	*4	
		CY, pmem.@L	2	2	CY<-CY v ($pmem_{7-2}$+L_{3-2}.bit(L_{1-0}))	*5	
		CY, @H+mem.bit	2	2	CY<-CY v (H+mem_{3-0}.bit)	*1	
	XOR1	CY, fmem.bit	2	2	CY<-CY ∀ (fmem.bit)	*4	
		CY, pmem.@L	2	2	CY<- CY ∀ ($pmem_{7-2}$+L_{3-2}.bit(L_{1-0}))	*5	
		CY, @H+mem.bit	2	2	CY<-CY ∀ (H+mem_{3-0}.bit)	*1	

Instruction group	Mnemonic	Operand	No. of bytes	Machine cycle	Operation	Addressing area	Skip condition
Branch	BR[Note 1]	addr	—	—	PC_{13-0}<-addr (Use the assembler to select the most appropriate instruction among the following. • BR !addr • BRCB !caddr • BR $addr)	*6	
		addr1	—	—	PC_{13-0}<-addr1 (Use the assembler to select the most appropriate instruction among the following. • BRA !addr1 • BR !addr • BRCB !caddr • BR $addr1)	*11	
		!addr	3	3	PC_{13-0}<-addr	*6	
		$addr	1	2	PC_{13-0}<-addr	*7	
		$addr1	1	2	PC_{13-0}<-addr1		
		PCDE	2	3	PC_{13-0}<-PC_{13-8}+DE		
		PCXA	2	3	PC_{13-0}<-PC_{13-8}+XA		
		BCDE	2	3	PC_{13-0}<-BCDE[Note 2]	*6	
		BCXA	2	3	PC_{13-0}<-BCXA[Note 2]	*6	
	BRA[Note 1]	!addr1	3	3	PC_{13-0}<-addr1	*11	
	BRCB	!caddr	2	2	PC_{13-0}<-$PC_{13, 12}$+$caddr_{11-0}$	*8	

Notes 1. The portion in a double box can be supported only in the Mk II mode. The others can be supported only in the MK I mode.

2. The B register is valid only for the lower two bits.

Instruction group	Mnemonic	Operand	No. of bytes	Machine cycle	Operation	Addressing area	Skip condition
Subroutine stack control	CALLA[Note]	!addr1	3	3	(SP–6)(SP–3)(SP–4)<-PC11-0 (SP–5)<-0, 0, PC13, 12 (SP–2)<-X, X, MBE, RBE PC13-0<-addr1, SP<-SP–6	*11	
	CALL[Note]	!addr	3	3	(SP–4)(SP–1)(SP–2)<-PC11-0 (SP–3)<-MBE, RBE, PC13, 12 PC13-0<-addr, SP<-SP–4	*6	
				4	(SP–6)(SP–3)(SP–4)<-PC11-0 (SP–5)<-0, 0, PC13, 12 (SP–2)<-X, X, MBE, RBE PC13-0<-addr, SP<-SP–6		
	CALLF[Note]	!faddr	2	2	(SP–4)(SP–1)(SP–2)<-PC11-0 (SP–3)<-MBE, RBE, PC13, 12 PC13-0<-000+faddr, SP<-SP–4	*9	
				3	(SP–6)(SP–3)(SP–4)<-PC11-0 (SP–5)<-0, 0, PC13, 12 (SP–2)<-X, X, MBE, RBE PC13-0<-000+faddr, SP<-SP–6		
	RET[Note]		1	3	MBE, RBE, PC13, 12<-(SP+1) PC11-0<-(SP)(SP+3)(SP+2) SP<-SP+4		
					X, X, MBE, RBE<-(SP+4) PC11-0<-(SP)(SP+3)(SP+2) 0, 0, PC13, 12<-(SP+1) SP<-SP+6		
	RETS[Note]		1	3+S	MBE, RBE, PC13, 12<-(SP+1) PC11-0<-(SP)(SP+3)(SP+2) SP<-SP+4 then skip unconditionally		Unconditional
					X, X, MBE, RBE<-(SP+4) PC11-0<-(SP)(SP+3)(SP+2) 0, 0, PC13, 12<-(SP+1) SP<-SP+6 then skip unconditionally		
	RETI [Note]		1	3	MBE, RBE, PC13, 12<-(SP+1) PC11-0<-(SP)(SP+3)(SP+2) PSW<-(SP+4)(SP+5) SP<-SP+6		
					0, 0, PC13, 12<-(SP+1) PC11-0<-(SP)(SP+3)(SP+2) PSW<-(SP+4)(SP+5), SP<-SP+6		

Note The portion in a double box can be supported only in the Mk II mode. Other portions can be supported only in the Mk I mode.

Instruction group	Mnemonic	Operand	No. of bytes	Machine cycle	Operation	Addressing area	Skip condition
Subroutine stack control	PUSH	rp	1	1	(SP–1)(SP–2)<-rp, SP<-SP–2		
		BS	2	2	(SP–1)<-MBS, (SP–2)<-RBS, SP<-SP–2		
	POP	rp	1	1	rp<-(SP+1)(SP), SP<-SP+2		
		BS	2	2	MBS<-(SP+1), RBS<-(SP), SP<-SP+2		
Interrupt control	EI		2	2	IME(IPS.3)<-1		
		IEXXX	2	2	IEXXX<-1		
	DI		2	2	IME(IPS.3)<-0		
		IEXXX	2	2	IEXXX<-0		
I/O	IN Note 1	A, PORTn	2	2	A<-PORTn (n=0 to 3, 5, 6, 8, 9)		
		XA, PORTn	2	2	XA<-PORTn+1, PORTn (n=8)		
	OUT Note 1	PORTn, A	2	2	PORTn<-A (n=2 to 3, 5, 6, 8, 9)		
		PORTn, XA	2	2	PORTn+1, PORTn<-XA (n=8)		
CPU control	HALT		2	2	Set HALT Mode(PCC.2<-1)		
	STOP		2	2	Set STOP Mode(PCC.3<-1)		
	NOP		1	1	No Operation		
Special	SEL	RBn	2	2	RBS<-n (n=0 to 3)		
		MBn	2	2	MBS<-n (n=0, 1, 15)		
	GETI Note 2, 3	taddr	1	3	• When using TBR instruction PC13-0<-(taddr)5-0+(taddr+1)	*10	
					• When using TCALL instruction (SP–4)(SP–1)(SP–2)<-PC11-0 (SP–3)<-MBE, RBE, PC13, 12 PC13-0<-(taddr)5-0+(taddr+1) SP<-SP–4		
					• When using instruction other than TBR or TCALL Execute (taddr)(taddr+1) instructions		Determined by referenced instruction
			1	3	• When using TBR instruction PC13-0<-(taddr)5-0+(taddr+1)	*10	
				4	• When using TCALL instruction (SP–6)(SP–3)(SP–4)<-PC11-0 (SP–5)<-0, 0, PC13, 12 (SP–2)<-X, X, MBE, RBE PC13-0<-(taddr)5-0+(taddr+1) SP<-SP–6		
				3	• When using instruction other than TBR or TCALL Execute (taddr)(taddr+1) instructions		Determined by referenced instruction

Notes 1. Setting MBE=0 or MBE=1, MBS=15 is required during the execution of IN or OUT instruction.

2. TBR and TCALL instructions are assembler pseudo-instructions for the GETI instruction table definitions.

3. The portion in a double box can be supported only in the Mk II mode. Other portions can be supported only in the Mk I mode.

8. ONE-TIME PROM (PROGRAM MEMORY) WRITE AND VERIFY

The program memory contained in the μPD75P3116 is a 16384 x 8-bit one-time PROM that can be electrically written one time only. The pins listed in the table below are used for this PROM's write/verify operations. Clock input from the X1 pin is used instead of address input as a method for updating addresses.

Pin	Function
V_{PP}	Pin where program voltage is applied during program memory write/verify (usually V_{DD} potential)
X1, X2	Clock input pins for address updating during program memory write/verify. Input the X1 pin's inverted signal to the X2 pin.
MD0 to MD3	Operation mode selection pin for program memory write/verify
D0/P60 to D3/P63 (lower 4 bits) D4/P50 to D7/P53 (upper 4 bits)	8-bit data I/O pins for program memory write/verify
V_{DD}	Pin where power supply voltage is applied. Applies 1.8 to 5.5 V in normal operation mode and +6 V for program memory write/verify.

Caution Pins not used for program memory write/verify should be connected to Vss.

8.1 Operation Modes for Program Memory Write/Verify

When +6 V is applied to the V_{DD} pin and +12.5 V to the V_{PP} pin, the μPD75P3116 enters the program memory write/verify mode. The following operation modes can be specified by setting pins MD0 to MD3 as shown below.

Operation mode specification						Operation mode
V_{PP}	V_{DD}	MD0	MD1	MD2	MD3	
+12.5 V	+6 V	H	L	H	L	Zero-clear program memory address
		L	H	H	H	Write mode
		L	L	H	H	Verify mode
		H	X	H	H	Program inhibit mode

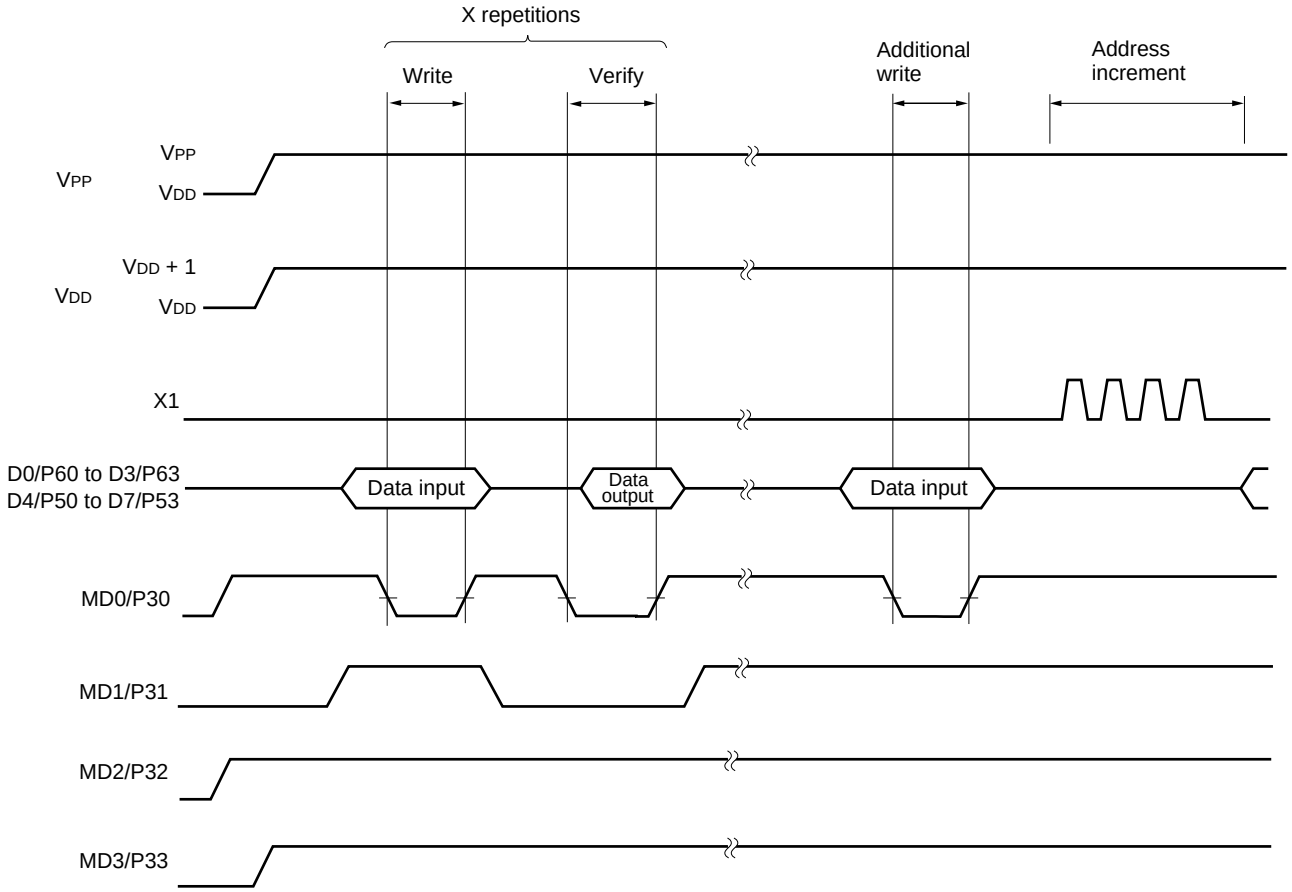
X: L or H

★ **8.2 Program Memory Write Procedure**

Program memory can be written at high speed using the following procedure.

(1) Pull down unused pins to Vss through resistors. Set the X1 pin low.
(2) Supply 5 V to the V_{DD} and V_{PP} pins.
(3) Wait 10 μs.
(4) Select the program memory address zero-clear mode.
(5) Supply 6 V to V_{DD} and 12.5 V to V_{PP} pins.
(6) Write data in the 1-ms write mode.
(7) Select the verify mode. If the data is written, go to (8) and if not, repeat (6) and (7).
(8) Additional write. (X: number of write operations from (6) and (7)) x 1 ms
(9) Apply four pulses to the X1 pin to increment the program memory address by one.
(10) Repeat (6) to (9) until the end address is reached.
(11) Select the program memory address zero-clear mode.
(12) Return the V_{DD}- and V_{PP}-pin voltages to 5 V.
(13) Turn off the power.

The following figure shows steps (2) to (9).

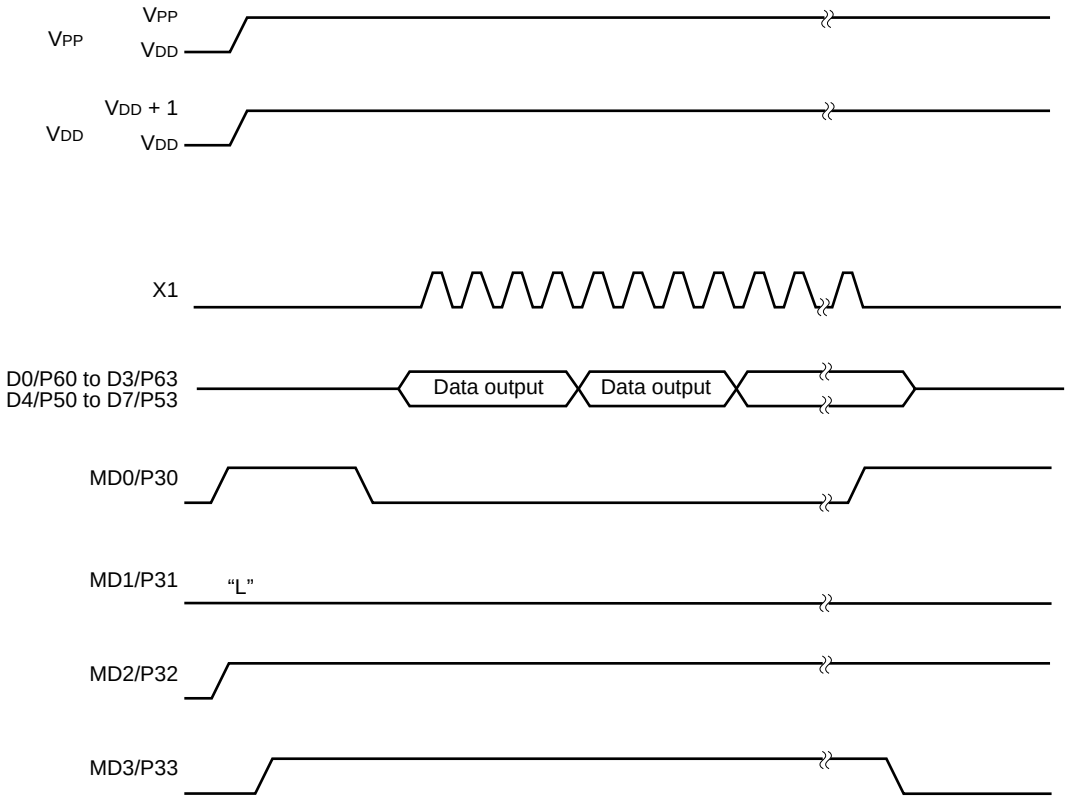


★ **8.3 Program Memory Read Procedure**

The μPD75P3116 can read program memory contents using the following procedure.

(1) Pull down unused pins to V_{SS} through resistors. Set the X1 pin low.
(2) Supply 5 V to the V_{DD} and V_{PP} pins.
(3) Wait 10 μs.
(4) Select the program memory address zero-clear mode.
(5) Supply 6 V to the V_{DD} and 12.5 to the V_{PP} pins.
(6) Select the verify mode. Apply four pulses to the X1 pin. Every four clock pulses will output the data stored in one address.
(7) Select the program memory address zero-clear mode.
(8) Return the V_{DD}- and V_{PP}-pin voltages to 5V.
(9) Turn off the power.

The following figure shows steps (2) to (7).



8.4 One-time PROM Screening

Due to its structure, the one-time PROM cannot be fully tested before shipment by NEC. Therefore, NEC recommends that after the required data is written and the PROM is stored under the temperature and time conditions shown below, the PROM should be verified via a screening.

Storage temperature	Storage time
125˚C	24 hours

★ NEC offers QTOP microcontrollers for which one-time PROM writing, marking, screening, and verification are provided at additional cost. For more detailed information, contact an NEC sales representative.

9. ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C)

Parameter	Symbol	Test Conditions	Rating	Unit
Power supply voltage	V_{DD}		–0.3 to +7.0	V
PROM power supply voltage	V_{PP}		–0.3 to +13.5	V
Input voltage	V_{I1}	Except port 5	–0.3 to V_{DD} +0.3	V
	V_{I2}	Port 5 (N-ch open drain)	–0.3 to +14	V
Output voltage	V_O		–0.3 to V_{DD} +0.3	V
Output current high	I_{OH}	Per pin	–10	mA
		Total of all pins	–30	mA
Output current low	I_{OL}	Per pin	30	mA
		Total of all pins	220	mA
Operating ambient temperature	T_A		–40 to +85 Note	°C
Storage temperature	T_{stg}		–65 to +150	°C

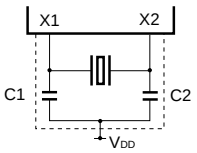
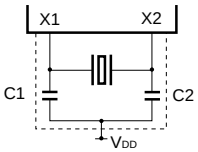
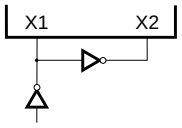
Note When LCD is driven in normal mode: T_A = –10 to +85°C

Caution If any of the parameters exceeds the absolute maximum ratings, even momentarily, the reliability of the product may be impaired. The absolute maximum ratings are values that may physically damage the products. Be sure to use the products within the ratings.

CAPACITANCE (T_A = 25°C, V_{DD} = 0 V)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Input capacitance	C_{IN}	f = 1 MHz			15	pF
Output capacitance	C_{OUT}	Unmeasured pins returned to 0 V.			15	pF
I/O capacitance	C_{IO}				15	pF

MAIN SYSTEM CLOCK OSCILLATOR CHARACTERISTICS (T_A = –40 to +85°C, V_{DD} = 1.8 to 5.5 V)

Resonator	Recommended constant	Parameter	Test conditions	MIN.	TYP.	MAX.	Unit
Ceramic resonator		Oscillation frequency (fx) Note 1		1.0		6.0 Note 2	MHz
		Oscillation stabilization time Note 3	After V_{DD} reaches oscillation voltage range MIN.			4	ms
Crystal resonator		Oscillation frequency (fx) Note 1		1.0		6.0 Note 2	MHz
		Oscillation stabilization time Note 3	V_{DD} = 4.5 to 5.5 V			10	ms
						30	
External clock		X1 input frequency (fx) Note 1		1.0		6.0 Note 2	MHz
★		X1 input high-/low-level width (t_{XH}, t_{XL})		83.3		500	ns

Notes 1. The oscillation frequency and X1 input frequency indicate characteristics of the oscillator only. For the instruction execution time, refer to AC Characteristics.

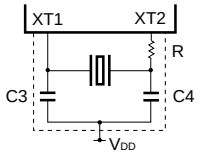
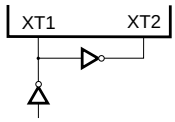
2. When the power supply voltage is 1.8 V ≤ V_{DD} < 2.7 V and the oscillation frequency is 4.19 MHz < fx ≤ 6.0 MHz, setting the processor clock control register (PCC) to 0011 results in 1 machine cycle being less than the required 0.95 μs. Therefore, set PCC to a value other than 0011.

3. The oscillation stabilization time is necessary for oscillation to stabilize after applying V_{DD} or releasing the STOP mode.

Caution When using the main system clock oscillator, wiring in the area enclosed with the dotted line should be carried out as follows to avoid an adverse effect from wiring capacitance.

- **Wiring should be as short as possible.**
- **Wiring should not cross other signal lines.**
- **Wiring should not be placed close to a varying high current.**
- **The potential of the oscillator capacitor ground should be the same as V_{DD}.**
- **Do not ground to a ground pattern in which a high current flows.**
- **Do not fetch a signal from the oscillator.**

SUBSYSTEM CLOCK OSCILLATOR CHARACTERISTICS (T_A = –40 to +85°C, V_{DD} = 1.8 to 5.5 V)

Resonator	Recommended constant	Parameter	Test conditions	MIN.	TYP.	MAX.	Unit
Crystal resonator		Oscillation frequency (f_{XT}) Note 1		32	32.768	35	kHz
		Oscillation stabilization time Note 2	V_{DD} = 4.5 to 5.5 V		1.0	2	s
						10	
External clock		XT1 input frequency (f_{XT}) Note 1		32		100	kHz
		XT1 input high-/low-level width (t_{XTH}, t_{XTL})		5		15	μs

Notes 1. Indicates only oscillator characteristics. Refer to AC Characteristics for instruction execution time.

2. The oscillation stabilization time is necessary for oscillation to stabilize after applying V_{DD}.

Caution When using the subsystem clock oscillator, wiring in the area enclosed with the dotted line should be carried out as follows to avoid an adverse effect from wiring capacitance.

- **Wiring should be as short as possible.**
- **Wiring should not cross other signal lines.**
- **Wiring should not be placed close to a varying high current.**
- **The potential of the oscillator capacitor ground should be the same as V_{DD}.**
- **Do not ground to a ground pattern in which a high current flows.**
- **Do not fetch a signal from the oscillator.**

The subsystem clock oscillator is designed as a low amplification circuit to provide low consumption current, and is more liable to misoperation by noise than the main system clock oscillation circuit. Special care should therefore be taken regarding the wiring method when the subsystem clock is used.

DC CHARACTERISTICS (T_A = –40 to +85°C, V_{DD} = 1.8 to 5.5 V)

Parameter	Symbol	Test conditions		MIN.	TYP.	MAX.	Unit
Output current low	I_{OL}	Per pin				15	mA
		Total of all pins				150	mA
Input voltage high	V_{IH1}	Ports 2, 3, 8, and 9	2.7 ≤ V_{DD} ≤ 5.5 V	0.7V_{DD}		V_{DD}	V
			1.8 ≤ V_{DD} < 2.7 V	0.9V_{DD}		V_{DD}	V
	V_{IH2}	Ports 0, 1, 6, $\overline{\text{RESET}}$	2.7 ≤ V_{DD} ≤ 5.5 V	0.8V_{DD}		V_{DD}	V
			1.8 ≤ V_{DD} < 2.7 V	0.9V_{DD}		V_{DD}	V
	V_{IH3}	Port 5	2.7 ≤ V_{DD} ≤ 5.5 V	0.7V_{DD}		13	V
		(N-ch open-drain)	1.8 ≤ V_{DD} < 2.7 V	0.9V_{DD}		13	V
	V_{IH4}	X1, XT1		V_{DD} – 0.1		V_{DD}	V
Input voltage low	V_{IL1}	Ports 2, 3, 5, 8, and 9	2.7 ≤ V_{DD} ≤ 5.5 V	0		0.3V_{DD}	V
			1.8 ≤ V_{DD} < 2.7 V	0		0.1V_{DD}	V
	V_{IL2}	Ports 0, 1, 6, $\overline{\text{RESET}}$	2.7 ≤ V_{DD} ≤ 5.5 V	0		0.2V_{DD}	V
			1.8 ≤ V_{DD} < 2.7 V	0		0.1V_{DD}	V
	V_{IL3}	X1, XT1		0		0.1	V
Output voltage high	V_{OH}	$\overline{\text{SCK}}$, SO, Ports 2, 3, 6, 8, and 9	I_{OH} = –1.0 mA	V_{DD} – 0.5			V
Output voltage low	V_{OL1}	$\overline{\text{SCK}}$, SO, Ports 2, 3, 5, 6, 8, and 9	I_{OL} = 15 mA, V_{DD} = 4.5 to 5.5 V		0.2	2.0	V
			I_{OL} = 1.6 mA			0.4	V
	V_{OL2}	SB0, SB1	When N-ch open-drain pull-up resistor ≥ 1 kΩ			0.2V_{DD}	V
Input leakage current high	I_{LIH1}	V_{IN} = V_{DD}	Pins other than X1, XT1			3	μA
	I_{LIH2}		X1, XT1			20	μA
	I_{LIH3}	V_{IN} = 13 V	Port 5 (N-ch open-drain)			20	μA
Input leakage current low	I_{LIL1}	V_{IN} = 0 V	Pins other than X1, XT1, and Port 5			–3	μA
	I_{LIL2}		X1, XT1			–20	μA
★	I_{LIL3}		Port 5 (N-ch open-drain) When another instruction than input instruction is executed			–3	μA
			Port 5 (N-ch open-drain)			–30	μA
			When input instruction is executed, V_{DD} = 5.0 V		–10	–27	μA
			When input instruction is executed, V_{DD} = 3.0 V		–3	–8	μA
Output leakage current high	I_{LOH1}	V_{OUT} = V_{DD}	$\overline{\text{SCK}}$, SO/SB0, SB1, Ports 2, 3, 6, 8, and 9			3	μA
	I_{LOH2}	V_{OUT} = 13 V	Port 5 (N-ch open-drain)			20	μA
Output leakage current low	I_{LOL}	V_{OUT} = 0 V				–3	μA
On-chip pull-up resistor	R_L	V_{IN} = 0 V	Ports 0, 1, 2, 3, 6, 8, and 9 (Excluding P00 pin)	50	100	200	kΩ

DC CHARACTERISTICS (T_A = –40 to +85°C, V_{DD} = 1.8 to 5.5 V)

Parameter	Symbol	Test conditions			MIN.	TYP.	MAX.	Unit
★ LCD drive voltage	V_{LCD}	VAC0 = 0	T_A = –40 to +85°C		2.7		V_{DD}	V
			T_A = –10 to +85°C		2.2		V_{DD}	V
		VAC0 = 1			1.8		V_{DD}	V
VAC current Note 1	I_{VAC}	VAC0 = 1, V_{DD} = 2.0 V ± 10%				1	4	μA
LCD output voltage deviation Note 2 (common)	V_{ODC}	Io = ±1.0 μA	$V_{LCD0} = V_{LCD}$ $V_{LCD1} = V_{LCD}$ x 2/3		0		±0.2	V
LCD output voltage deviation Note 2 (segment)	V_{ODS}	Io = ±0.5 μA	$V_{LCD2} = V_{LCD}$ x 1/3 1.8 V ≤ V_{LCD} ≤ V_{DD}		0		±0.2	V
Supply current Note 3	I_{DD1}	6.00 MHz Note 4	V_{DD} = 5.0 V ± 10% Note 5			3.2	9.5	mA
		Crystal oscillation	V_{DD} = 3.0 V ± 10% Note 6			0.55	1.6	mA
	I_{DD2}	C1 = C2 = 22 pF	HALT mode	V_{DD} = 5.0 V ± 10%		0.7	2.0	mA
				V_{DD} = 3.0 V ± 10%		0.25	0.8	mA
	I_{DD1}	4.19 MHz Note 4	V_{DD} = 5.0 V ± 10% Note 5			2.5	7.5	mA
		Crystal oscillation	V_{DD} = 3.0 V ± 10% Note 6			0.45	1.35	mA
	I_{DD2}	C1 = C2 = 22 pF	HALT mode	V_{DD} = 5.0 V ± 10%		0.65	1.8	mA
				V_{DD} = 3.0 V ± 10%		0.22	0.7	mA
	I_{DD3}	32.768 kHz Note 7	Low-voltage mode Note 8	V_{DD} = 3.0 V ± 10%		45	130	μA
		Crystal oscillation		V_{DD} = 2.0 V ± 10%		20	55	μA
				V_{DD} = 3.0 V, T_A = 25°C		45	90	μA
			Low power consumption mode Note 9	V_{DD} = 3.0 V ± 10%		42	120	μA
				V_{DD} = 3.0 V, T_A = 25°C		42	85	μA
	I_{DD4}		HALT mode	Low-voltage mode Note 8: V_{DD} = 3.0 V ± 10%		5.5	18	μA
				Low-voltage mode Note 8: V_{DD} = 2.0 V ± 10%		2.2	7	μA
				Low-voltage mode Note 8: V_{DD} = 3.0 V, T_A = 25°C		5.5	12	μA
				Low power consumption mode Note 9: V_{DD} = 3.0 V ± 10%		4.0	12	μA
				Low power consumption mode Note 9: V_{DD} = 3.0 V, T_A = 25°C		4.0	8	μA
	I_{DD5}	XT1 = 0 V Note 10	V_{DD} = 5.0 V ± 10%			0.05	10	μA
		STOP mode	V_{DD} = 3.0 V			0.02	5	μA
			± 10%	T_A = 25°C		0.02	3	μA

★ **Notes 1.** Set to VAC0 = 0 when the low power consumption mode and the stop mode are used. If VAC0 = 1 is set, the current increases for approx. 1 μA.

2. The voltage deviation is the difference from the output voltage corresponding to the ideal value of the segment and common outputs (V_{LCDn}; n = 0, 1, 2).

3. Not including currents flowing in on-chip pull-up resistors.

4. Including oscillation of the subsystem clock.

5. When the processor clock control register (PCC) is set to 0011 and the device is operated in the high-speed mode.

6. When PCC is set to 0000 and the device is operated in the low-speed mode.

7. When the system clock control register (SCC) is set to 1001 and the device is operated on the subsystem clock, with main system clock oscillation stopped.

★ **8.** When the sub-oscillation circuit control register (SOS) is set to 0000.

★ **9.** When SOS is set to 0010.

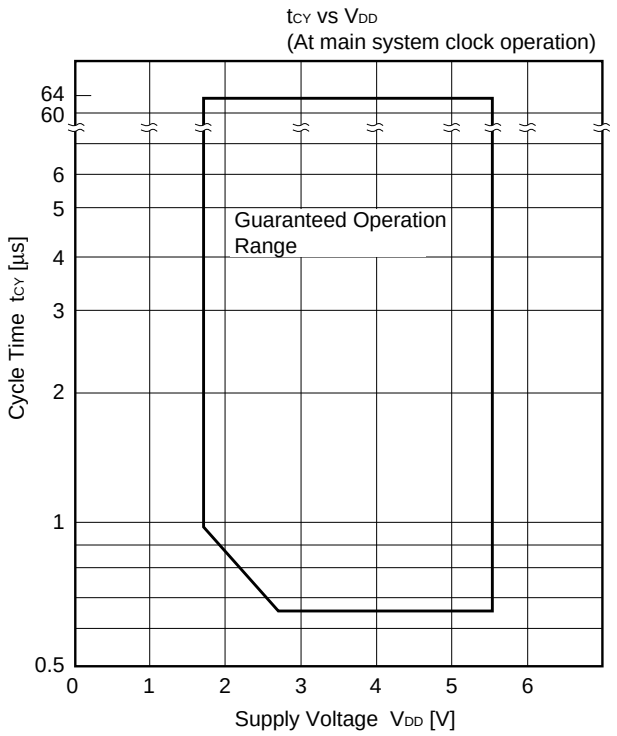
★ **10.** When SOS is set to 00×1 and the feedback resistor of the sub-oscillation circuit is not used.

AC CHARACTERISTICS (T_A = –40 to +85°C, V_{DD} = 1.8 to 5.5 V)

Parameter	Symbol	Test conditions		MIN.	TYP.	MAX.	Unit
CPU clock cycle time Note 1 (Min. instruction execution time = 1 machine cycle)	t_{CY}	Operating on main system clock	V_{DD} = 2.7 to 5.5 V	0.67		64	μs
				0.95		64	μs
		Operating on subsystem clock		114	122	125	μs
TI0, TI1, TI2 input frequency	f_{TI}	V_{DD} = 2.7 to 5.5 V		0		1.0	MHz
				0		275	kHz
TI0, TI1, TI2 input high-/low-level width	t_{TIH}, t_{TIL}	V_{DD} = 2.7 to 5.5 V		0.48			μs
				1.8			μs
Interrupt input high-/low-level width	t_{INTH}, t_{INTL}	INT0	IM02 = 0	**Note 2**			μs
			IM02 = 1	10			μs
		INT1, 2, 4		10			μs
		KR0 to KR7		10			μs
$\overline{\text{RESET}}$ low-level width	t_{RSL}			10			μs

Notes 1. The cycle time (minimum instruction execution time) of the CPU clock (Φ) is determined by the oscillation frequency of the connected resonator (and external clock), the system clock control register (SCC) and the processor clock control register (PCC). The figure at the right indicates the cycle time t_{CY} versus supply voltage V_{DD} characteristic with the main system clock operating.

2. $2t_{CY}$ or 128/fx is set by setting the interrupt mode register (IM0).



SERIAL TRANSFER OPERATION

2-Wire and 3-Wire Serial I/O Mode ($\overline{SCK}$...Internal clock output): (T_A = –40 to +85°C, V_{DD} = 1.8 to 5.5 V)

Parameter	Symbol	Test conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK}$ cycle time	t_{KCY1}	V_{DD} = 2.7 to 5.5 V		1300			ns
				3800			ns
$\overline{SCK}$ high-/low-level width	t_{KL1}, t_{KH1}	V_{DD} = 2.7 to 5.5 V		t_{KCY1}/2–50			ns
				t_{KCY1}/2–150			ns
SI Note 1 setup time (to $\overline{SCK}$↑)	t_{SIK1}	V_{DD} = 2.7 to 5.5 V		150			ns
				500			ns
SI Note 1 hold time (from $\overline{SCK}$↑)	t_{KSI1}	V_{DD} = 2.7 to 5.5 V		400			ns
				600			ns
$\overline{SCK}$↓→SO Note 1 output delay time	t_{KSO1}	R_L = 1 kΩ,	V_{DD} = 2.7 to 5.5 V	0		250	ns
		C_L = 100 pF Note 2		0		1000	ns

Notes 1. In 2-wire serial I/O mode, read this parameter as SB0 or SB1 instead.

2. R_L and C_L are the load resistance and load capacitance of the SO output lines, respectively.

2-Wire and 3-Wire Serial I/O Mode ($\overline{SCK}$...External clock input): (T_A = –40 to +85°C, V_{DD} = 1.8 to 5.5 V)

Parameter	Symbol	Test conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK}$ cycle time	t_{KCY2}	V_{DD} = 2.7 to 5.5 V		800			ns
				3200			ns
$\overline{SCK}$ high-/low-level width	t_{KL2}, t_{KH2}	V_{DD} = 2.7 to 5.5 V		400			ns
				1600			ns
SI Note 1 setup time (to $\overline{SCK}$↑)	t_{SIK2}	V_{DD} = 2.7 to 5.5 V		100			ns
				150			ns
SI Note 1 hold time (from $\overline{SCK}$↑)	t_{KSI2}	V_{DD} = 2.7 to 5.5 V		400			ns
				600			ns
$\overline{SCK}$↓→SO Note 1 output delay time	t_{KSO2}	R_L = 1 kΩ,	V_{DD} = 2.7 to 5.5 V	0		300	ns
		C_L = 100 pF Note 2		0		1000	ns

Notes 1. In 2-wire serial I/O mode, read this parameter as SB0 or SB1 instead.

2. R_L and C_L are the load resistance and load capacitance of the SO output lines, respectively.

SBI Mode ($\overline{SCK}$...Internal clock output (master)): (T_A = –40 to +85°C, V_{DD} = 1.8 to 5.5 V)

Parameter	Symbol	Test conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK}$ cycle time	t_{KCY3}	V_{DD} = 2.7 to 5.5 V		1300			ns
				3800			ns
$\overline{SCK}$ high-/low-level width	t_{KL3}, t_{KH3}	V_{DD} = 2.7 to 5.5 V		t_{KCY3}/2–50			ns
				t_{KCY3}/2–150			ns
SB0, 1 setup time (to $\overline{SCK}$↑)	t_{SIK3}	V_{DD} = 2.7 to 5.5 V		150			ns
				500			ns
SB0, 1 hold time (from $\overline{SCK}$↑)	t_{KSI3}			t_{KCY3}/2			ns
$\overline{SCK}$↓→ SB0, 1 output delay time	t_{KSO3}	R_L = 1 kΩ, C_L = 100 pF Note	V_{DD} = 2.7 to 5.5 V	0		250	ns
				0		1000	ns
$\overline{SCK}$↑→ SB0, 1↓	t_{KSB}			t_{KCY3}			ns
SB0, 1 ↓→$\overline{SCK}$↓	t_{SBK}			t_{KCY3}			ns
SB0, 1 low-level width	t_{SBL}			t_{KCY3}			ns
SB0, 1 high-level width	t_{SBH}			t_{KCY3}			ns

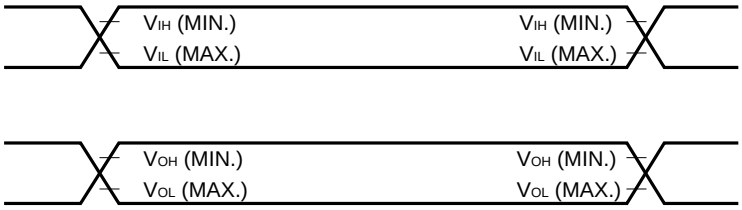
Note R_L and C_L are the load resistance and load capacitance of the SB0 and SB1 output lines, respectively.

SBI Mode ($\overline{SCK}$...External clock input (slave)): (T_A = –40 to +85°C, V_{DD} = 1.8 to 5.5 V)

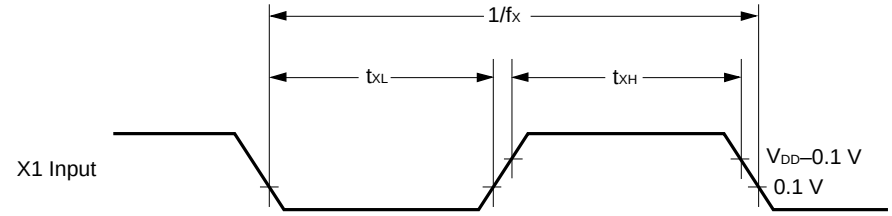
Parameter	Symbol	Test conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK}$ cycle time	t_{KCY4}	V_{DD} = 2.7 to 5.5 V		800			ns
				3200			ns
$\overline{SCK}$ high-/low-level width	t_{KL4}, t_{KH4}	V_{DD} = 2.7 to 5.5 V		400			ns
				1600			ns
SB0, 1 setup time (to $\overline{SCK}$↑)	t_{SIK4}	V_{DD} = 2.7 to 5.5 V		100			ns
				150			ns
SB0, 1 hold time (from $\overline{SCK}$↑)	t_{KSI4}			t_{KCY4}/2			ns
$\overline{SCK}$↓→SB0, 1 output delay time	t_{KSO4}	R_L = 1 kΩ, C_L = 100 pF Note	V_{DD} = 2.7 to 5.5 V	0		300	ns
				0		1000	ns
$\overline{SCK}$↑→ SB0, 1↓	t_{KSB}			t_{KCY4}			ns
SB0, 1↓→ $\overline{SCK}$↓	t_{SBK}			t_{KCY4}			ns
SB0, 1 low-level width	t_{SBL}			t_{KCY4}			ns
SB0, 1 high-level width	t_{SBH}			t_{KCY4}			ns

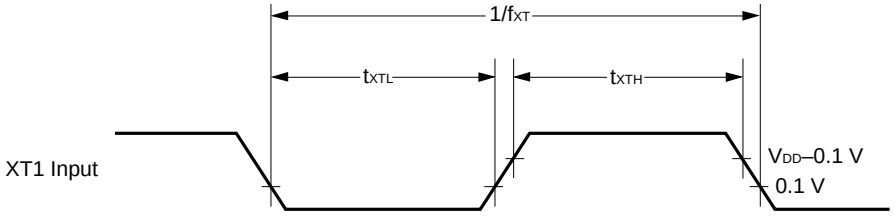
Note R_L and C_L are the load resistance and load capacitance of the SB0 and SB1 output lines, respectively.

★ **AC Timing Test Point (Excluding X1, XT1 Input)**

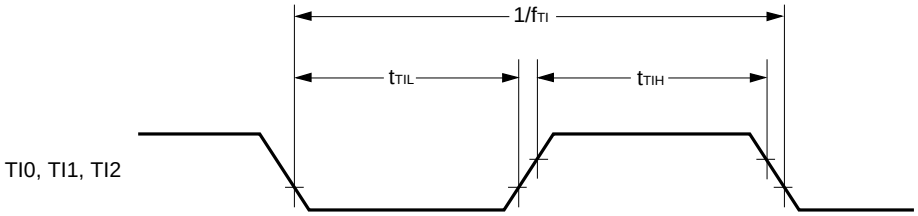


★ **Clock Timing**



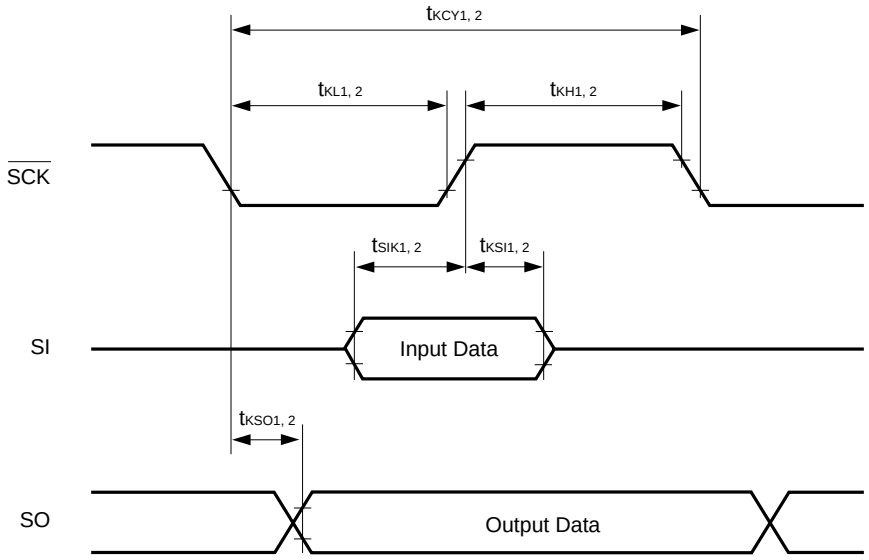


TI0, TI1, TI2 Timing

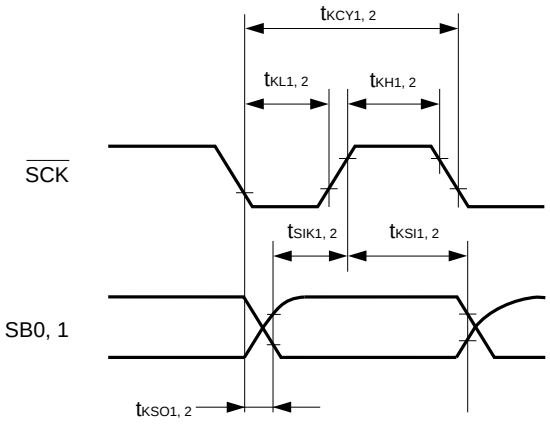


Serial Transfer Timing

3-wire serial I/O mode

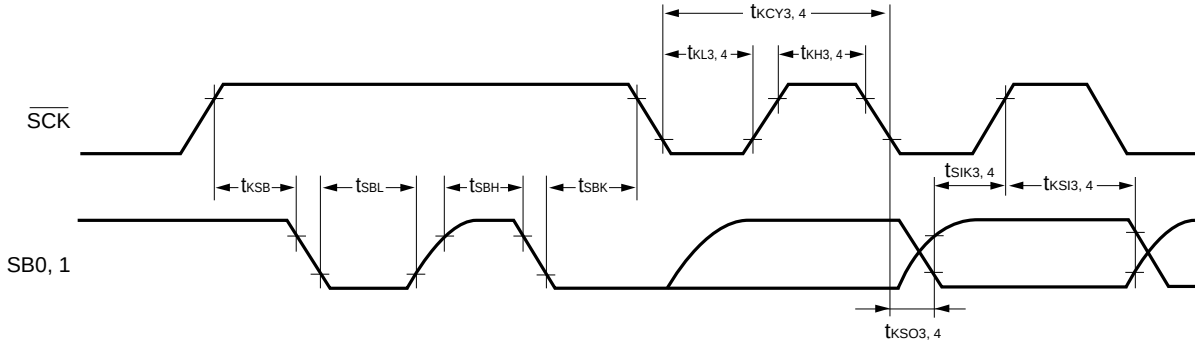


2-wire serial I/O mode

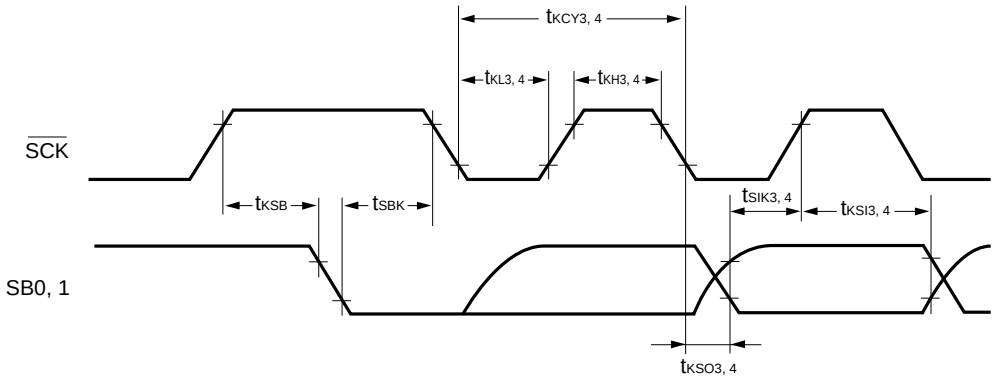


Serial Transfer Timing

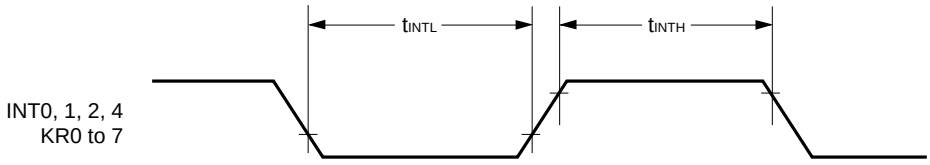
Bus release signal transfer



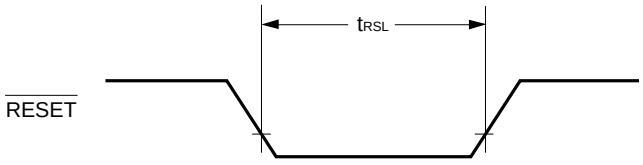
Command signal transfer



Interrupt input timing



$\overline{\text{RESET}}$ input timing



DATA MEMORY STOP MODE LOW SUPPLY VOLTAGE DATA RETENTION CHARACTERISTICS

(T_A = –40 to +85°C)

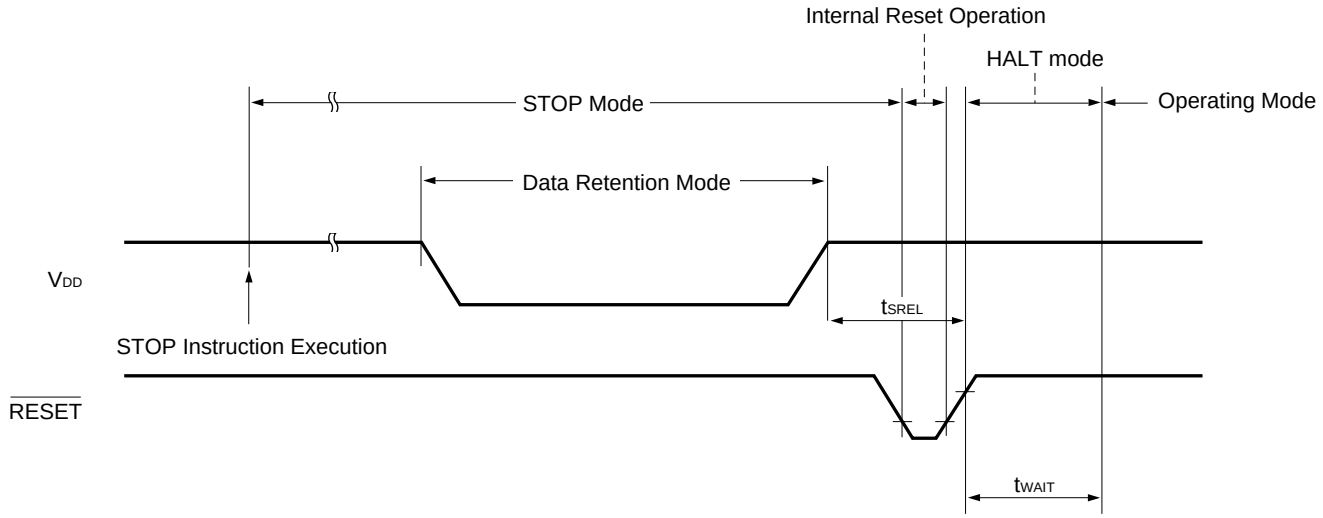
Parameter	Symbol	Test conditions	MIN.	TYP.	MAX.	Unit
Release signal set time	t_{SREL}		0			μs
Oscillation stabilization wait time Note 1	t_{WAIT}	Release by $\overline{\text{RESET}}$		$2^{15}/f_X$		ms
		Release by interrupt request		**Note 2**		ms

Notes 1. The oscillation stabilization wait time is the time during which the CPU operation is stopped to prevent unstable operation at the oscillation start.

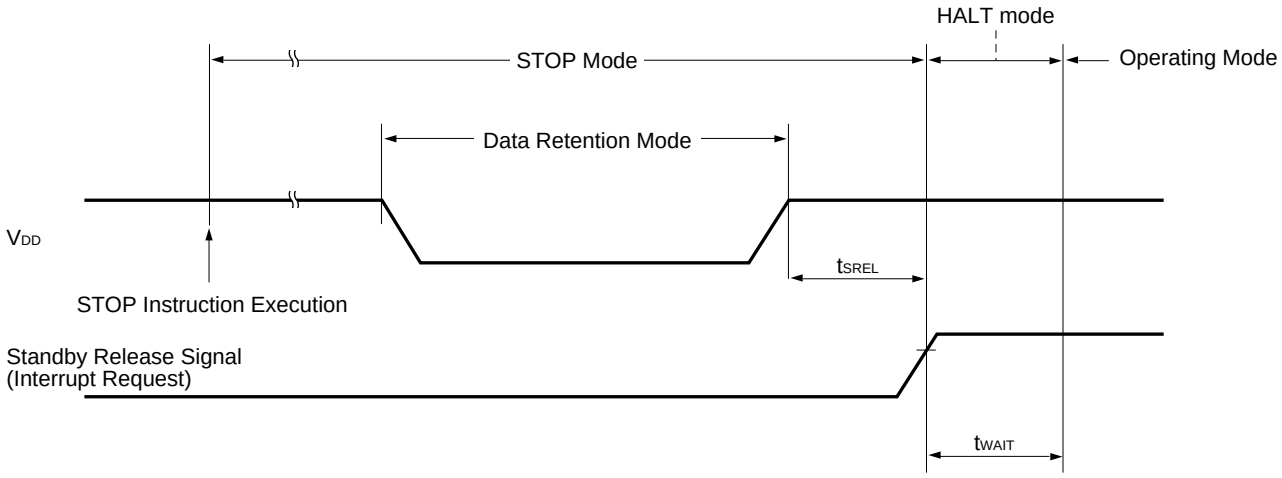
2. Depends on the basic interval timer mode register (BTM) settings (See the table below).

BTM3	BTM2	BTM1	BTM0	Wait time	
				fx = at 4.19 MHz	fx = at 6.0 MHz
—	0	0	0	2^{20}/fx (approx. 250 ms)	2^{20}/fx (approx. 175 ms)
—	0	1	1	2^{17}/fx (approx. 31.3 ms)	2^{17}/fx (approx. 21.8 ms)
—	1	0	1	2^{15}/fx (approx. 7.81 ms)	2^{15}/fx (approx. 5.46 ms)
—	1	1	1	2^{13}/fx (approx. 1.95 ms)	2^{13}/fx (approx. 1.37 ms)

Data Retention Timing (STOP Mode Release by $\overline{\text{RESET}}$)



Data Retention Timing (Standby Release Signal: STOP Mode Release by Interrupt Signal)



DC PROGRAMMING CHARACTERISTICS (T_A = 25 ± 5°C, V_{DD} = 6.0 ± 0.25 V, V_{PP} = 12.5 ± 0.3 V, V_{SS} = 0 V)

Parameter	Symbol	Test conditions	MIN.	TYP.	MAX.	Unit
Input voltage high	V_{IH1}	Except X1 and X2 pins	0.7V_{DD}		V_{DD}	V
	V_{IH2}	X1, X2	V_{DD}–0.5		V_{DD}	V
Input voltage low	V_{IL1}	Except X1 and X2 pins	0		0.3V_{DD}	V
	V_{IL2}	X1, X2	0		0.4	V
Input leakage current	I_{LI}	V_{IN} = V_{IL} or V_{IH}			10	μA
Output voltage high	V_{OH}	I_{OH} = –1 mA	V_{DD}–1.0			V
Output voltage low	V_{OL}	I_{OL} = 1.6 mA			0.4	V
V_{DD} power supply current	I_{DD}				30	mA
V_{PP} power supply current	I_{PP}	MD0 = V_{IL}, MD1 = V_{IH}			30	mA

Cautions 1. Avoid exceeding +13.5 V for V_{PP} including the overshoot.

2. V_{DD} must be applied before V_{PP}, and cut after V_{PP}.

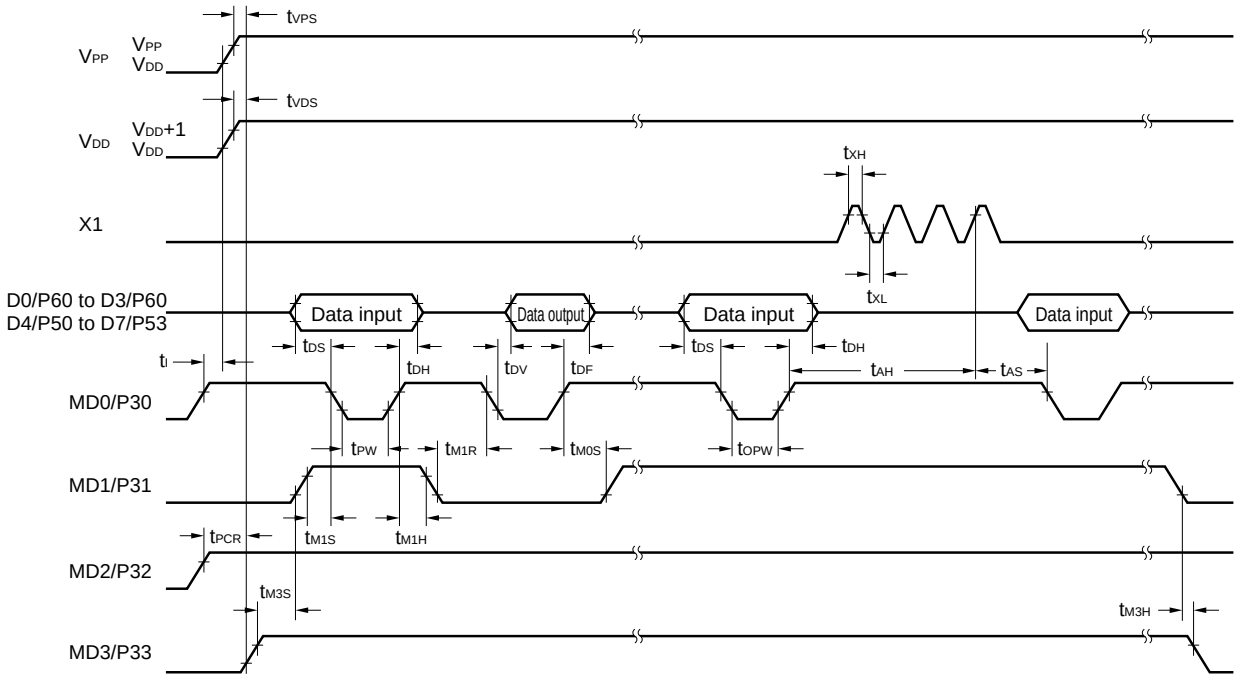
AC PROGRAMMING CHARACTERISTICS (T_A = 25 ±5°C, V_{DD} = 6.0 ±0.25 V, V_{PP} = 12.5 ±0.3 V, V_{SS} = 0 V)

Parameter	Symbol	**Note 1**	Test conditions	MIN.	TYP.	MAX.	Unit
Address setup time Note 2 (to MD0↓)	t_{AS}	t_{AS}		2			μs
MD1 setup time (to MD0↓)	t_{M1S}	t_{OES}		2			μs
Data setup time (to MD0↓)	t_{DS}	t_{DS}		2			μs
Address hold time Note 2 (from MD0↑)	t_{AH}	t_{AH}		2			μs
Data hold time (from MD0↑)	t_{DH}	t_{DH}		2			μs
MD0↑→data output float delay time	t_{DF}	t_{DF}		0		130	ns
V_{PP} setup time (to MD3↑)	t_{VPS}	t_{VPS}		2			μs
V_{DD} setup time (to MD3↑)	t_{VDS}	t_{VCS}		2			μs
Initial program pulse width	t_{PW}	t_{PW}		0.95	1.0	1.05	ms
Additional program pulse width	t_{OPW}	t_{OPW}		0.95		21.0	ms
MD0 setup time (to MD1↑)	t_{M0S}	t_{CES}		2			μs
MD0↓→data output delay time	t_{DV}	t_{DV}	MD0 = MD1 = V_{IL}			1	μs
MD1 hold time (from MD0↑)	t_{M1H}	t_{OEH}	t_{M1H}+t_{M1R} ≥ 50 μs	2			μs
MD1 recovery time (from MD0↓)	t_{M1R}	t_{OR}		2			μs
Program counter reset time	t_{PCR}	–		10			μs
X1 input high-/low-level width	t_{XH}, t_{XL}	–		0.125			μs
X1 input frequency	f_X	–				4.19	MHz
Initial mode set time	t_I	–		2			μs
MD3 setup time (to MD1↑)	t_{M3S}	–		2			μs
MD3 hold time (from MD1↓)	t_{M3H}	–		2			μs
MD3 setup time (to MD0↓)	t_{M3SR}	–	During program memory read	2			μs
Address Note 2 →data output delay time	t_{DAD}	t_{ACC}	During program memory read			2	μs
★ Address Note 2 →data output hold time	t_{HAD}	t_{OH}	During program memory read	0		130	ns
MD3 hold time (from MD0↑)	t_{M3HR}	–	During program memory read	2			μs
MD3↓→data output float delay time	t_{DFR}	–	During program memory read			2	μs

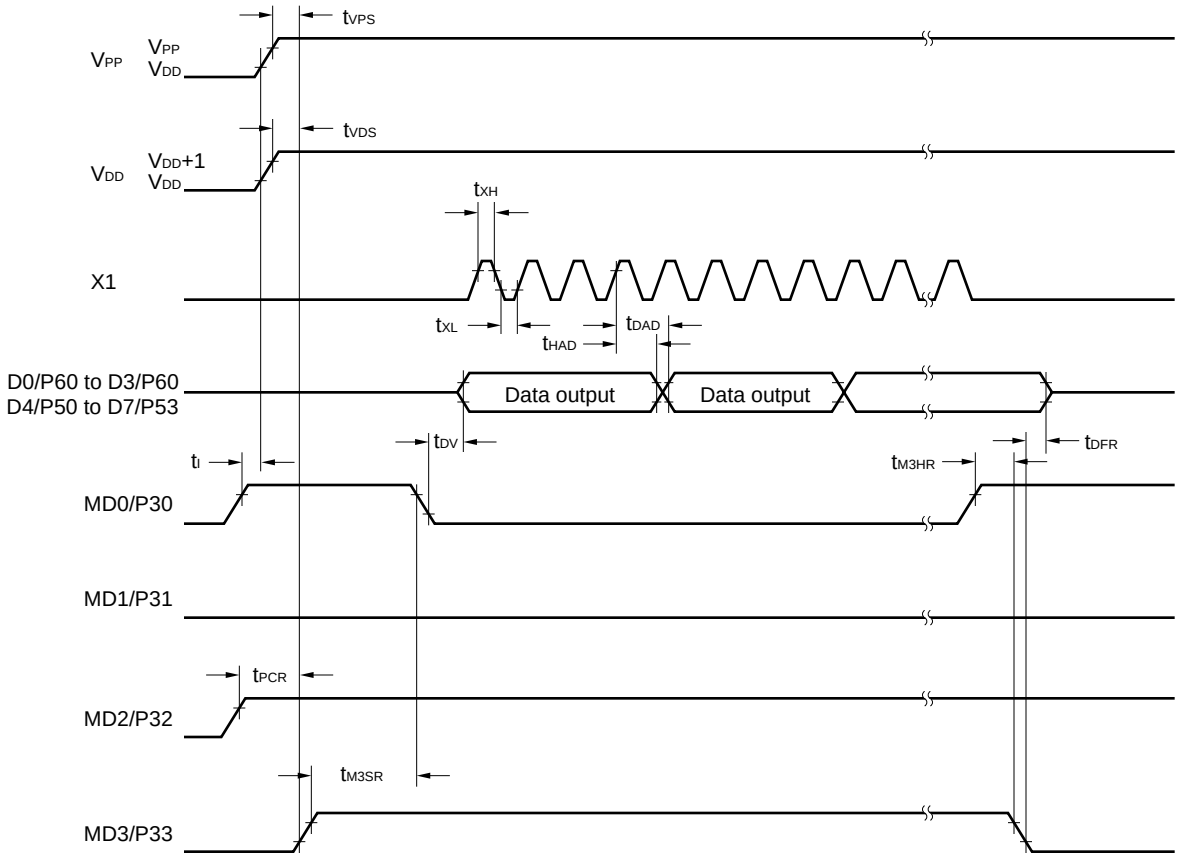
Notes 1. Corresponding symbol of μPD27C256A

2. The internal address signal is incremented by 1 at the rising edge of the fourth X1 input and is not connected to a pin.

Program Memory Write Timing

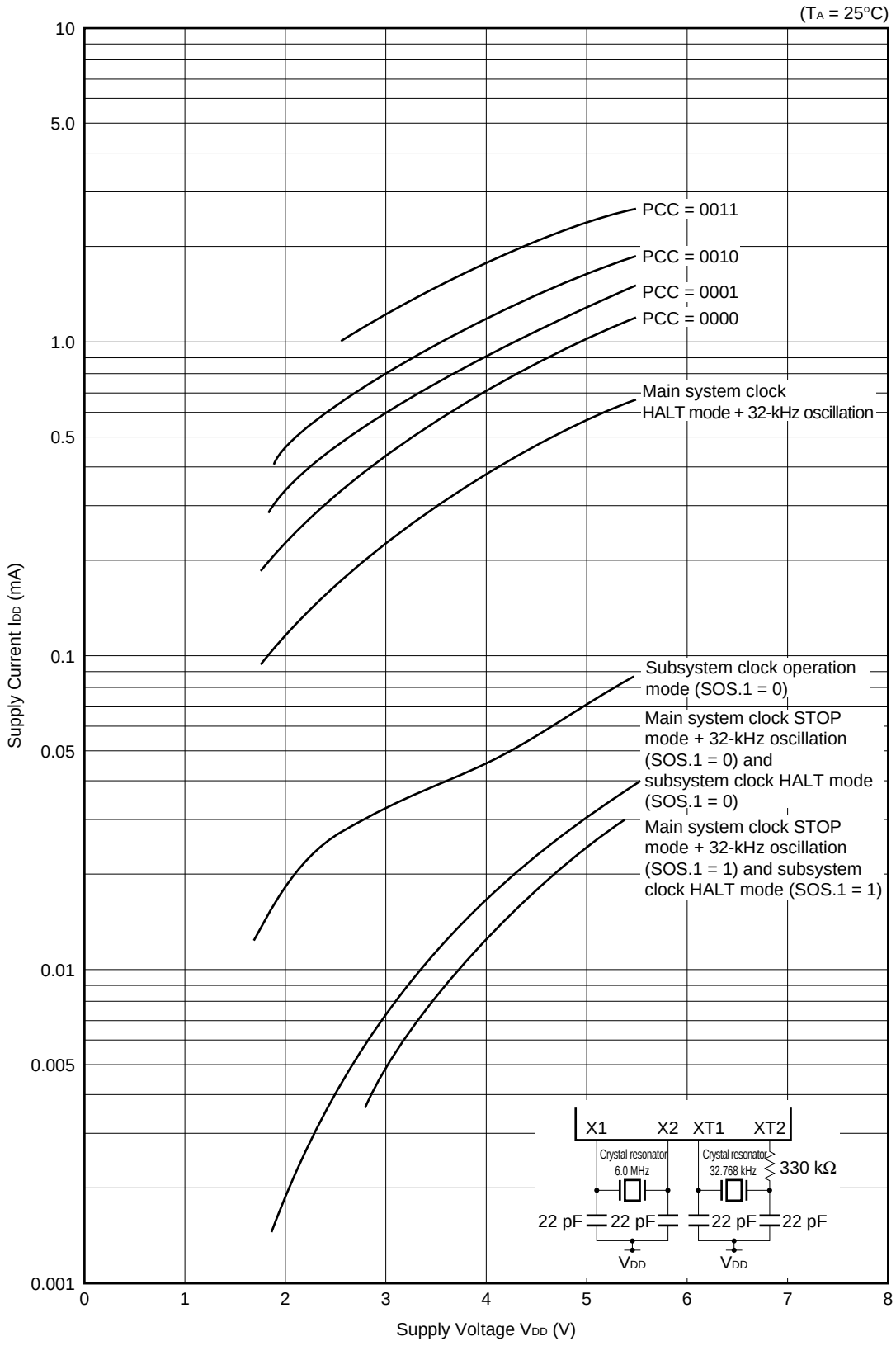


Program Memory Read Timing

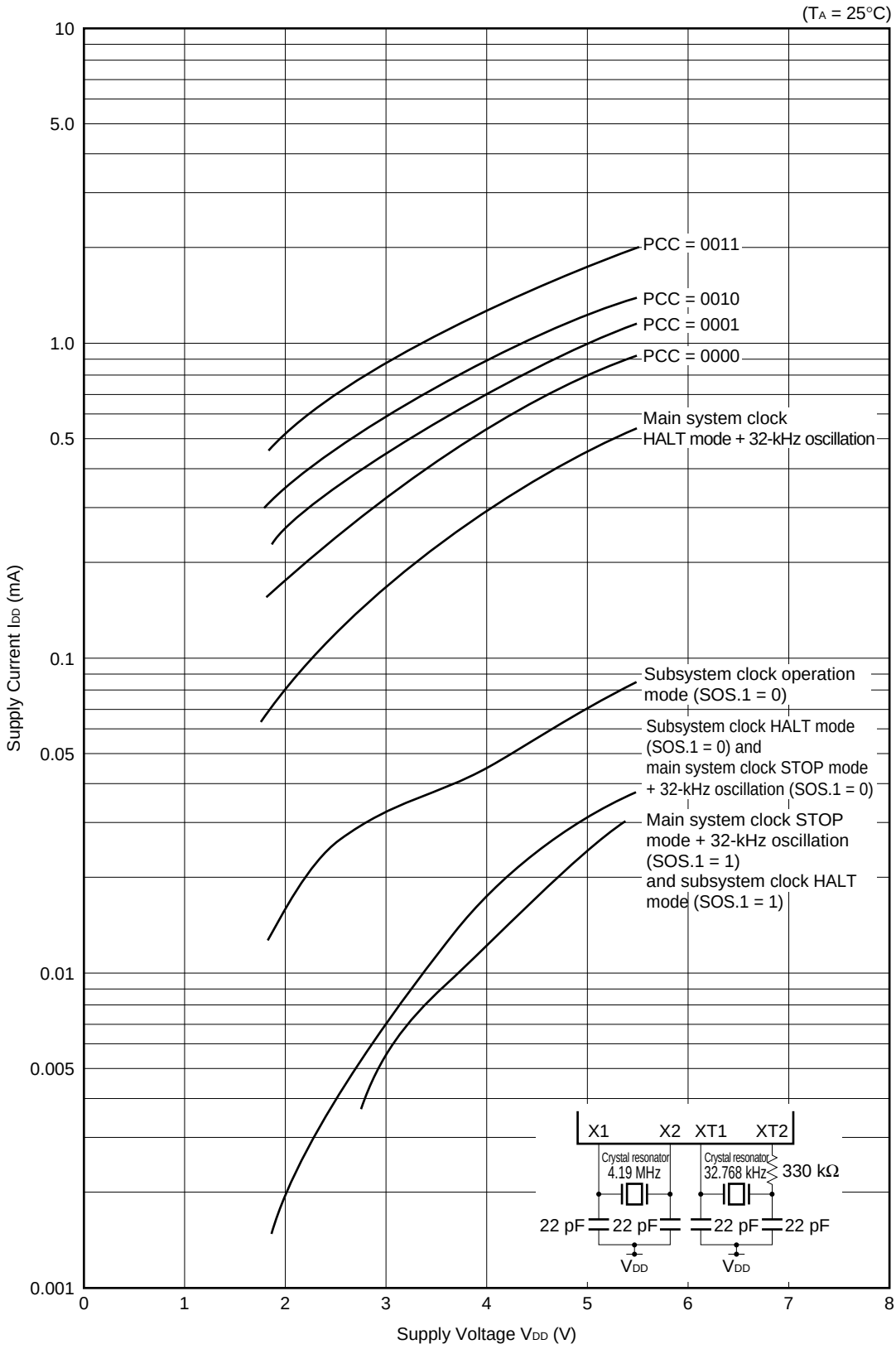


10. CHARACTERISTIC CURVES (REFERENCE VALUES)

I_{DD} vs V_{DD} (Main System Clock: 6.0-MHz Crystal Resonator)

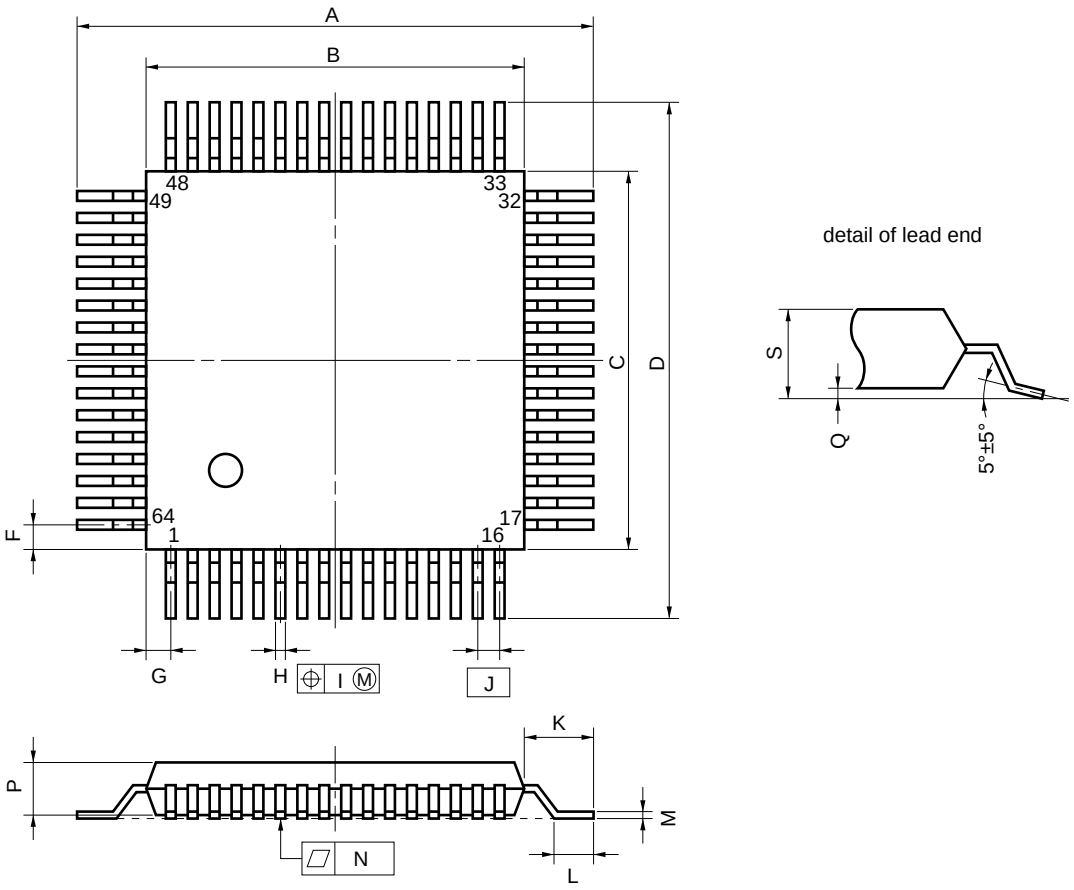


I_{DD} vs V_{DD} (Main System Clock: 4.19-MHz Crystal Resonator)



11. PACKAGE DRAWINGS

64 PIN PLASTIC QFP (□14)



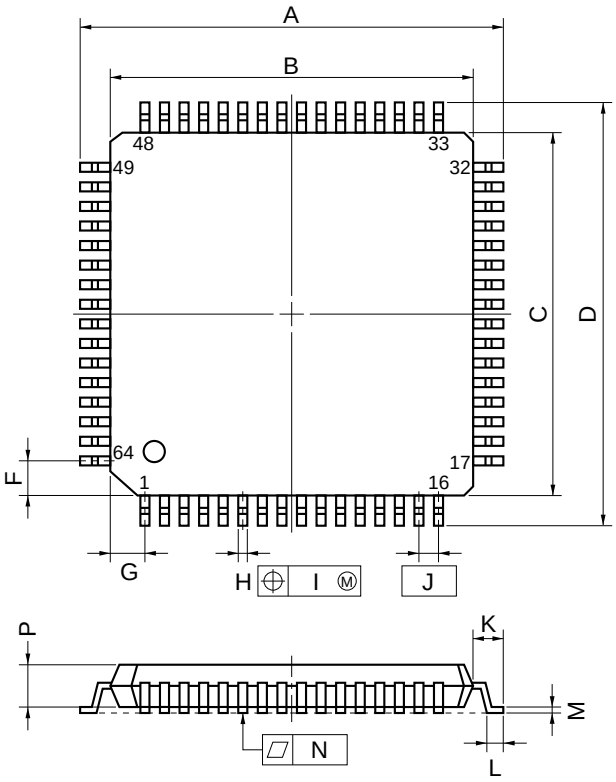
P64GC-80-AB8-3

NOTE

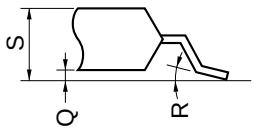
Each lead centerline is located within 0.15 mm (0.006 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	17.6±0.4	0.693±0.016
B	14.0±0.2	$0.551^{+0.009}_{-0.008}$
C	14.0±0.2	$0.551^{+0.009}_{-0.008}$
D	17.6±0.4	0.693±0.016
F	1.0	0.039
G	1.0	0.039
H	0.35±0.10	$0.014^{+0.004}_{-0.005}$
I	0.15	0.006
J	0.8 (T.P.)	0.031 (T.P.)
K	1.8±0.2	0.071±0.008
L	0.8±0.2	$0.031^{+0.009}_{-0.008}$
M	$0.15^{+0.10}_{-0.05}$	$0.006^{+0.004}_{-0.003}$
N	0.10	0.004
P	2.55	0.100
Q	0.1±0.1	0.004±0.004
S	2.85 MAX.	0.112 MAX.

64 PIN PLASTIC LQFP (□12)



detail of lead end



NOTE

Each lead centerline is located within 0.13 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	14.8±0.4	0.583±0.016
B	12.0±0.2	$0.472^{+0.009}_{-0.008}$
C	12.0±0.2	$0.472^{+0.009}_{-0.008}$
D	14.8±0.4	0.583±0.016
F	1.125	0.044
G	1.125	0.044
H	0.30±0.10	$0.012^{+0.004}_{-0.005}$
I	0.13	0.005
J	0.65 (T.P.)	0.026 (T.P.)
K	1.4±0.2	0.055±0.008
L	0.6±0.2	$0.024^{+0.008}_{-0.009}$
M	$0.15^{+0.10}_{-0.05}$	$0.006^{+0.004}_{-0.003}$
N	0.10	0.004
P	1.4	0.055
Q	0.125±0.075	0.005±0.003
R	5°±5°	5°±5°
S	1.7 MAX.	0.067 MAX.

P64GK-65-8A8-1

12. RECOMMENDED SOLDERING CONDITIONS

The μPD75P3116 should be soldered and mounted under the conditions recommended in the table below.

For details of recommended soldering conditions, refer to the information document **Semiconductor Device Mounting Technology Manual (C10535E).**

For soldering methods and conditions other than those recommended below, contact an NEC Sales representative.

★ **Table 12-1. Surface Mounting Type Soldering Conditions**

(1) μPD75P3116GC-AB8: 64-pin plastic QFP (14 x 14 mm, 0.8-mm pitch)

Soldering Method	Soldering Conditions	Symbol
Infrared reflow	Package peak temperature: 235°C, Time: 30 seconds max. (at 210°C min.), Number of times: Three times max.	IR35-00-3
VPS	Package peak temperature: 215°C, Time: 40 seconds max. (at 200°C min.), Number of times: Three times max.	VP15-00-3
Wave soldering	Solder temperature: 260°C max., Flow time: 10 seconds max., Number of times: Once, Preheating temperature: 120°C max. (Package surface temperature)	WS60-00-1
Partial heating	Pin temperature: 300°C max., Time : 3 seconds max. (per device)	—

Caution Use of more than one soldering method should be avoided (except for partial heating).

(2) μPD75P3116GK-8A8: 64-pin plastic QFP (12 x 12 mm, 0.65-mm pitch)

Soldering Method	Soldering Conditions	Recommended Conditions Reference Code
Infrared reflow	Package peak temperature: 235°C, Time: 30 seconds max. (at 210°C min.), Number of times: Twice max., Number of days: 7[Note] (after that, prebaking is necessary at 125°C for 10 hours) <Precaution> Products other than those supplied in thermal-resistant tray (magazine, taping, and non-thermal-resistant tray) cannot be baked in their packs.	IR35-107-2
VPS	Package peak temperature: 215°C, Time: 40 seconds max. (at 200°C min.), Number of times: Twice max., Number of days: 7[Note] (after that, prebaking is necessary at 125°C for 10 hours) <Precaution> Products other than those supplied in thermal-resistant tray (magazine, taping, and non-thermal-resistant tray) cannot be baked in their packs.	VP15-107-2
Wave soldering	Soldering bath temperature: 260°C max., Time: 10 seconds max., Number of times: Once Preheating temperature: 120°C max. (package surface temperature) Number of days: 7[Note] (after that, prebaking is necessary at 125°C for 10 hours)	WS 60-107-1
Partial heating	Pin temperature: 300°C max., Time: 3 seconds max. (per pin row)	—

Note Number of days after unpacking the dry pack. Storage conditions are 25°C and 65%RH max.

Caution Do not use different soldering methods together (however, partial heating can be performed with other soldering methods.)

APPENDIX A. FUNCTION LIST OF μPD75308B, 753108 AND 75P3116

Parameter		μPD75308B	μPD753108	μPD75P3116
Program memory		Mask ROM 0000H to 1F7FH (8064 x 8 bits)	Mask ROM 0000H to 1FFFH (8192 x 8 bits)	One-time PROM 0000H to 3FFFH (16384 x 8 bits)
Data memory			000H to 1FFH (512 x 4 bits)	
CPU		75X Standard	75XL CPU	
Instruction execution time	When main system clock is selected	0.95, 1.91, 15.3 μs (during 4.19-MHz operation)	• 0.95, 1.91, 3.81, 15.3 μs (during 4.19-MHz operation) • 0.67, 1.33, 2.67, 10.7 μs (during 6.0-MHz operation)	
	When subsystem clock is selected	122 μs (during 32.768-kHz operation)		
Stack	SBS register	None	SBS.3 = 1: Mk I mode selection SBS.3 = 0: Mk II mode selection	
	Stack area	000H to 0FFH	000H to 1FFH	
	Subroutine call instruction stack operation	2-byte stack	When Mk I mode : 2-byte stack When Mk II mode : 3-byte stack	
Instruction	BRA !addr1 CALLA !addr1	Unavailable	When Mk I mode : unavailable When Mk II mode : available	

	MOVT XA, @BCDE
	MOVT XA, @BCXA
	BR BCDE
	BR BCXA
			Available	

	CALL !addr	3 machine cycles	Mk I mode : 3 machine cycles Mk II mode : 4 machine cycles	
	CALLF !faddr	2 machine cycles	Mk I mode : 2 machine cycles Mk II mode : 3 machine cycles	
I/O port	CMOS input	8	8	
	CMOS input/output	16	20	
	Bit port output	8	0	
	N-ch open-drain input/output	8	4	
	Total	40	32	
LCD controller/driver		Segment selection: 24/28/32 (can be changed to CMOS input/output port in 4-unit; max. 8)	Segment selection: 16/20/24 segments (can be changed to CMOS input/output port in 4-unit; max. 8)	
		Display mode selection: static, 1/2 duty (1/2 bias), 1/3 duty (1/2 bias), 1/3 duty (1/3 bias), 1/4 duty (1/3 bias)		
		On-chip split resistor for LCD driver can be specified by using mask option.		No on-chip split resistor for LCD driver
Timer		3 channels • Basic interval timer: 1 channel • 8-bit timer/event counter: 1 channel • Watch timer: 1 channel	5 channels • Basic interval timer/watchdog timer: 1 channel • 8-bit timer/event counter: 3 channels (can be used as 16-bit timer/event counter) • Watch timer: 1 channel	

Parameter		μPD75308B	μPD753108	μPD75P3116
Clock output (PCL)		• Φ, 524, 262, 65.5 kHz (Main system clock: during 4.19-MHz operation)	• Φ, 524, 262, 65.5 kHz (Main system clock: during 4.19-MHz operation) • Φ, 750, 375, 93.8 kHz (Main system clock: during 6.0-MHz operation)	
BUZ output (BUZ)		2 kHz (Main system clock: during 4.19-MHz operation)	• 2, 4, 32 kHz (Main system clock: during 4.19-MHz operation or subsystem clock: during 32.768-kHz operation) • 2.93, 5.86, 46.9 kHz (Main system clock: 6.0-MHz operation)	
Serial interface		3 modes are available • 3-wire serial I/O mode ⋯ MSB/LSB can be selected for transfer first bit • 2-wire serial I/O mode • SBI mode		
SOS register	Feedback resistor cut flag (SOS.0)	None	Contained	
	Sub-oscillation circuit current cut flag (SOS.1)	None	Contained	
Register bank selection register (RBS)		None	Yes	
Standby release by INT0		No	Yes	
Vectored interrupt		External: 3, Internal: 3	External: 3, Internal: 5	
Supply voltage		V_{DD} = 2.0 to 6.0 V	V_{DD} = 1.8 to 5.5 V	
Operating ambient temperature		T_A = –40 to +85°C		
Package		• 80-pin plastic QFP (14 x 20 mm) • 80-pin plastic QFP (14 x 14 mm) • 80-pin plastic TQFP (Fine pitch) (12 x 12 mm)	• 84-pin plastic QFP (14 x 14 mm, 0.8-mm pitch) • 64-pin plastic QFP (12 x 12 mm, 0.65-mm pitch)	

APPENDIX B. DEVELOPMENT TOOLS

The following development tools have been provided for system development using the μPD75P3116.
In the 75XL series, a common relocatable assembler is used in combination with a device file dedicated to each model.

RA75X relocatable assembler	Host machine			Part No. (name)
		OS	Supply medium	
	PC-9800 Series	MS-DOS™ (Ver.3.30 to Ver.6.2 Note)	3.5" 2HD	μS5A13RA75X
			5" 2HD	μS5A10RA75X
	IBM PC/AT™ or compatibles	Refer to **OS for IBM PCs**	3.5" 2HC	μS7B13RA75X
			5" 2HC	μS7B10RA75X

Device file	Host machine			Part No. (name)
		OS	Supply medium	
	PC-9800 Series	MS-DOS (Ver.3.30 to Ver.6.2 Note)	3.5" 2HD	μS5A13DF753108
			5" 2HD	μS5A10DF753108
	IBM PC/AT or compatibles	Refer to **OS for IBM PCs**	3.5" 2HC	μS7B13DF753108
			5" 2HC	μS7B10DF753108

Note Ver. 5.00 and later include a task swapping function, but this function cannot be used in this software.

Remark Operation of the assembler and device file is guaranteed only when using the host machine and OS described above.

PROM Write Tools

Hardware	PG-1500	This is a PROM writer that can program single-chip microcontroller with PROM in stand-alone mode or under control of host machine when connected with supplied accessory board and optional programmer adapter. It can also program typical PROMs in capacities ranging from 256 K to 4 M bits.			
	PA-75P3116BGC	This is a PROM programmer adapter for the μPD75P3116GC. It can be used when connected to a PG-1500.			
	PA-75P3116BGK	This is a PROM programmer adapter for the μPD75P3116GK. It can be used when connected to a PG-1500.			
Software	PG-1500 controller	Connects PG-1500 to host machine with serial and parallel interface and controls PG-1500 on host machine.			
		Host machine			Part No. (name)
			OS	Supply medium	
		PC-9800 Series	MS-DOS (Ver.3.30 to Ver.6.2 Note)	3.5" 2HD	μS5A13PG1500
				5" 2HD	μS5A10PG1500
		IBM PC/AT or compatible	Refer to **OS for IBM PCs**	3.5" 2HD	μS7B13PG1500
				5" 2HC	μS7B10PG1500

Note Ver. 5.00 and later include a task swapping function, but this function cannot be used in this software.

Remark Operation of the PG-1500 controller is guaranteed only when using the host machine and OS described above.

Debugging Tools

In-circuit emulators (IE-75000-R and IE-75001-R) are provided as program debugging tools for the μPD75P3116. Various system configurations using these in-circuit emulators are listed below.

Hardware	IE-75000-R[Note 1]	The IE-75000-R is an in-circuit emulator to be used for hardware and software debugging during development of application systems using the 75X or 75XL Series products. For development of the μPD753108 Subseries, the IE-75000-R is used with optional emulation board (IE-75300-R-EM) and emulation probe (EP-753108GC-R or EP-753108GK-R). Highly efficient debugging can be performed when connected to host machine and PROM programmer. The IE-75000-R includes a connected emulation board (IE-75000-R-EM).			
	IE-75001-R	The IE-75001-R is an in-circuit emulator to be used for hardware and software debugging during development of application systems using the 75X or 75XL Series products. The IE-75001-R is used in combination with optional emulation board (IE-75300-R-EM) and emulation probe (EP-753108GC-R or EP-753108GK-R). Highly efficient debugging can be performed when connected to host machine and PROM programmer.			
	IE-75300-R-EM	This is an emulation board for evaluating application systems using the μPD75P3116. It is used in combination with the IE-75000-R or IE-75001-R.			
	EP-753108GC-R	This is an emulation probe for the μPD75P3116GC. When being used, it is connected with the IE-75000-R or IE-75001-R and the IE-75300-R-EM.			
	EV-9200GC-64	It includes a 64-pin conversion socket (EV-9200GC-64) to facilitate connections with target system.			
	EP-753108GK-R	This is an emulation probe for the μPD75P3116GK. When being used, it is connected with the IE-75000-R or IE-75001-R and the IE-75300-R-EM.			
★	TGK-064SBW [Note 2]	It includes a 64-pin conversion adapter (TGK-064SBW) to facilitate connections with target system.			
Software	IE control program	This program can control the IE-75000-R or IE-75001-R on a host machine when connected to the IE-75000-R or IE-75001-R via an RS-232C or Centronics interface.			
		Host machine			Part No. (name)
			OS	Supply medium	
		PC-9800 Series	MS-DOS (Ver.3.30 to Ver.6.2 [Note 3])	3.5" 2HD	μS5A13IE75X
				5" 2HD	μS5A10IE75X
		IBM PC/AT or compatible	Refer to **OS for IBM PCs**	3.5" 2HC	μS7B13IE75X
				5" 2HC	μS7B10IE75X

Notes 1. This is a maintenance product.

★ **2.** Made by TOKYO ELETECH Corporation (Tokyo, 03-5295-1661).
Contact to an NEC sales representative for detailed information.

3. Ver. 5.00 and later include a task swapping function, but this function cannot be used in this software.

Remarks 1. Operation of the IE control program is guaranteed only when using the host machine and OS described above.

2. The μPD753104, 753106, 753108, and 75P3116 are generically called the μPD753108 Subseries.

OS for IBM PCs

The following operating systems for the IBM PC are supported.

OS	Version
PC DOS™	Ver.3.1 to 6.3, J6.1/V Note to J6.3/V Note
MS-DOS	Ver.5.0 to 6.2 5.0/V Note to 6.2/V Note
IBM DOS™	J5.02/V Note

Note Only English mode is supported.

Caution Ver. 5.0 and later include a task swapping function, but this function cannot be used in this software.

APPENDIX C. RELATED DOCUMENTS

The related documents indicated in this publication may include preliminary versions. However, preliminary versions are not marked as such.

Device Related Documents

Document Name	Document No.	
	English	Japanese
μPD753104, 753106, and 753108 Data Sheet	U10086E	U10086J
μPD75P3116 Data Sheet	U11369E (This document)	U11369J
μPD753108 User's Manual	U10890E	U10890J
μPD753108 Instruction Table	–	IEM-5600
75XL Series Selection Guide	U10453E	U10453J

Development Tool Related Documents

Document Name			Document No.	
			English	Japanese
Hardware	IE-75000-R/IE-75001-R User's Manual		EEU-1416	EEU-846
	IE-75300-R-EM User's Manual		U11354E	U11354J
	EP-753108GC/GK-R User's Manual		EEU-1495	EEU-968
	PG-1500 User's Manual		EEU-1335	U11940J
Software	RA75X Assembler Package	Operation	EEU-1346	EEU-731
	User's Manual	Language	EEU-1363	EEU-730
	PG-1500 Controller User's Manual	PC-9800 series (MS-DOS) base	EEU-1291	EEU-704
		IBM PC series (PC DOS) base	U10540E	EEU-5008

Other Related Documents

Document Name	Document No.	
	English	Japanese
IC Package Manual	C10943X	
Semiconductor Device Mounting Technology Manual	C10535E	C10535J
Quality Grades on NEC Semiconductor Devices	C11531E	C11531J
NEC Semiconductor Device Reliability/Quality Control System	C10983E	C10983J
Electrostatic Discharge (ESD) Test	–	MEM-539
Guide to Quality Assurance for Semiconductor Devices	MEI-1202	C11893J
Microcontroller-related Product Guide Third Party's Product	–	U11416J

Caution The above related documents are subject to change without notice. For design purposes, etc., be sure to use the latest versions.

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note: Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note: No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note: Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

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Some information contained in this document may vary from country to country. Before using any NEC product in your application, please contact the NEC office in your country to obtain a list of authorized representatives and distributors. They will verify:

- Device availability
- Ordering information
- Product release schedule
- Availability of related technical literature
- Development environment specifications (for example, specifications for third-party tools and components, host computers, power plugs, AC supply voltages, and so forth)
- Network requirements

In addition, trademarks, registered trademarks, export restrictions, and other legal issues may also vary from country to country.

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