A/D Type Full Speed USB 8-Bit MCU with SPI

Technical Document

- Application Note
  - HA0075E MCU Reset and Oscillator Circuits Application Note

Features

- Operating voltage:
  - VDD (MCU)
    f_{SYS} = 6MHz: 2.2V~5.5V
    f_{SYS} = 12MHz: 3.0V~5.5V
  - UBUS (USB BUS Voltage): 4.5V~5.5V
  - VCC (HT82A6208 & HT82A6216 for Flash): 2.8V~3.6V
- 4K×15 bits Program Memory
- 160×8 bits Data Memory RAM
- HT82A6208: 8M×1 bits Flash memory structure
- HT82A6216: 16M×1 bits or 8Mx2 bits Flash memory structure
- 32 bidirectional I/O lines
- USB 2.0 Full Speed Compatible
- One external interrupt input shared with I/O line
- Two 16-bit programmable Timer/Event Counters with overflow interrupt
- Two SPI interfaces (master and slave mode) shared with PA0~PA3, PB0~PB3
- Total of 6 Interrupts - EXT, Timer0, Timer1, SPIA, SPIB, USB
- Flash Serial Peripheral Interface compatible - Mode0 and Mode3
- 8288608×1bit Flash memory structure - HT82A6208
- 16777216×1bit or 8388608x2bit Flash memory structure - HT82A6216
- 256 Equal Sector with 4K byte each for Flash memory structure- HT82A6208
- 512 Equal Sector with 4K byte each for Flash memory structure- HT82A6216
- Flash Memory Input Data Format: 1-byte Command code
- Flash Memory Block Lock protection
- Single Power Supply Operation
- Watchdog Timer function
- 32768Hz Real time clock
- Power down and wake-up functions to reduce power consumption
- 16 channel 12-bit resolution A/D converter
- 2-channel 8-bit PWM output shared with two I/O lines
- Up to 0.33μs instruction cycle with 12MHz system clock at V_{DD}=5V
- Max. 4 endpoints supported - endpoint 0 included
- All endpoints support Interrupt, & bulk transfer
- Endpoint 0 supports control, interrupt and bulk transfer
- All endpoints except endpoint 0 can be configured as 8, 16, 32, 64 FIFO size
- Endpoint 0 has 8 byte FIFO
- Total FIFO size: 64+8 bytes (RAM0: 48 bytes; RAM1:16 bytes, 8 bytes for endpoint0)
- 2.2V ± 5% LVD
- 6-level subroutine nesting
- Bit manipulation instruction
- Table read instructions
- 63 powerful instructions
- All instructions executed in one or two instruction cycles
- Low voltage reset function
- Wide range of available package types

General Description

The HT82A623R, HT82A6208 and HT82A6216 are 8-bit high performance RISC-like microcontrollers designed for USB keyboard, mouse and joystick product applications. The devices are also suitable for use in home appliances, particularly for use in high-level household appliances such as microwave ovens, washing instructions and air conditioner products.

The HT82A6208 and HT82A6216 devices also possess an internal 8M or 16M Flash Memory further enhancing and expanding their application possibilities.

The advantages of low power consumption, I/O flexibility, programmable frequency divider, timer functions, oscillator options, multi-channel A/D Converter, Pulse Width Modulation function, USB Interface, Watchdog timer, SPI interfaces, Power Down and wake-up functions, enhance the versatility of these devices to suit a wide range of application possibilities.

The HT82A6208 contains a 8,388,608 bit serial Flash memory, which is configured as 1,048,576×8 internally. The HT82A6216 contains a 16,777,216 bit serial Flash memory, which is configured as 2,097,152×8 internally. The HT82A6208/HT82A6216 feature a serial peripheral interface and software protocol allowing operation on a simple 3-wire bus. The three bus signals are a clock input (SCLK), a serial data input (SI), and a serial data output (SO). SPI access to the device is enabled by the FHCS# input.

The device provides a sequential read operation on the whole chip.

After a program/erase command is issued, auto program/ erase algorithms are executed which program/erase and verify the specified page or byte/sector/block locations. A program command is executed on a page (256 bytes) basis, and an erase command is executed on a chip or sector (4K-bytes) or block (64K-bytes) basis.

To provide the user with ease of interface, a status register is included to indicate the status of the device. The status read command can be issued to detect completion status of a program or erase operation via the WIP bit.

When the HT82A6208/HT82A6216 is not operating and FHCS# is high, it can be put into the standby mode where it will draw less than 10μA/20μA DC current.

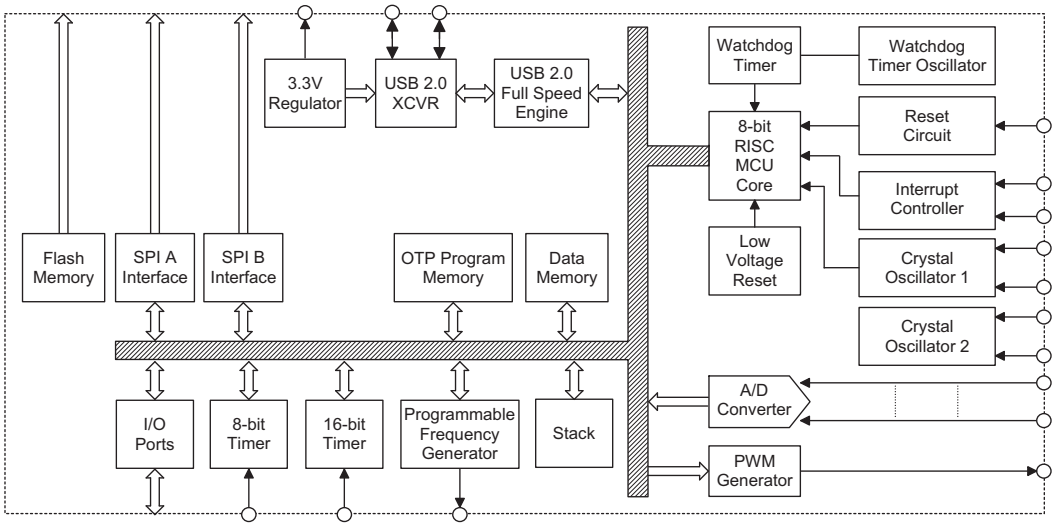
The HT82A6208/HT82A6216 contains proprietary memory cells, which reliably store memory contents even after 100,000 program and erase cycles.

Selection Table

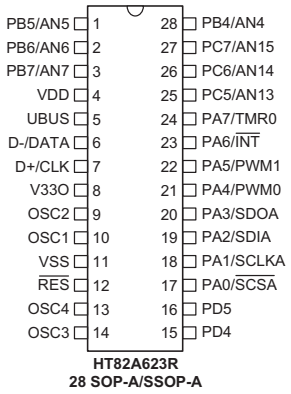
The following table summarises the main features of each device.

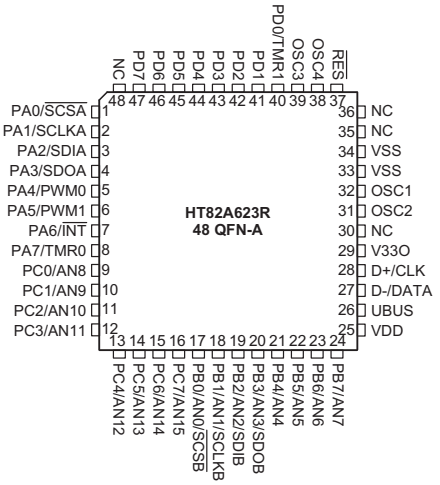
Part No.	VDD	VCC	Program Memory	Data Memory	Flash Memory	I/O	Timer		A/D	PWM	SPI	Stack	Package
							16-bit	RTC					
HT82A623R	2.2V~5.5V	—	4K×15	160×8	—	32	2	√	12-bit×16	8-bit×2	2	6	28SOP, 28SSOP, 48QFN
HT82A6208	2.2V~5.5V	2.8V~3.6V	4K×15	160×8	8M	32	2	√	12-bit×16	8-bit×2	2	6	44/52QFP
HT82A6216					16M								

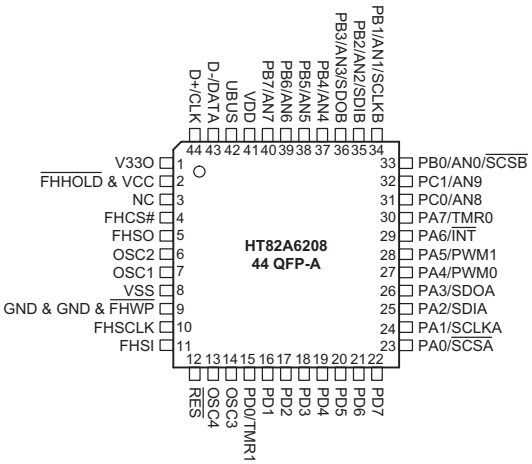
Block Diagram

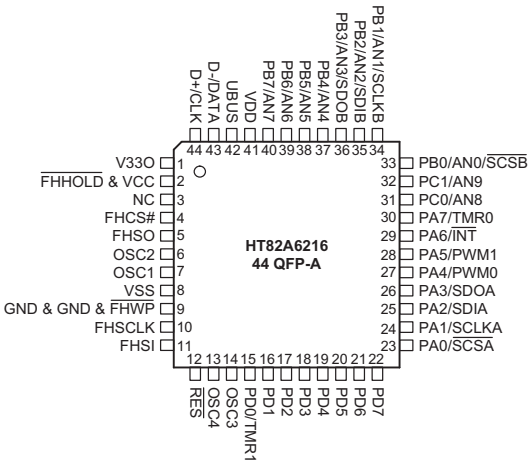


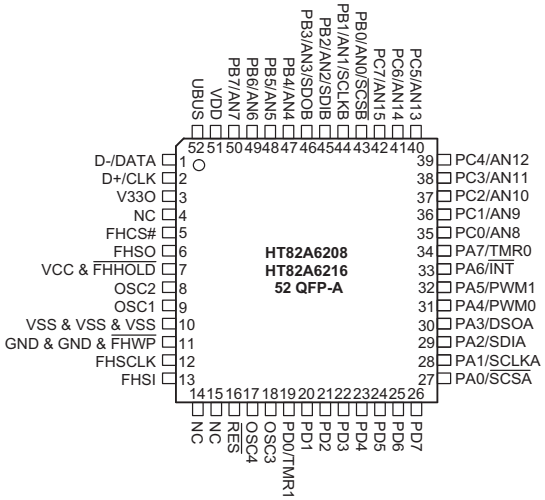
Pin Assignment











Pin Description

Pin Name	I/O	Options	Description
PA0/$\overline{SCSA}$ PA1/SCLKA PA2/SDIA PA3/SDOA PA4/PWM0 PA5/PWM1 PA6/$\overline{INT}$ PA7/TMR0	I/O	Pull-high Wake-up NMOS or CMOS	Bidirectional 8-bit input/output port. Each pin can be configured as a wake-up input by a configuration option. Software instructions determine if the pin is a CMOS output or Schmitt Trigger input. Configuration options determine if the pins have pull-high resistors. The INTB and TMR0 pins are pin-shared with PA6 and PA7 respectively. PA0~PA3 are shared with the SPIA function. PA4~PA5 are shared with PWM0 and PWM1.
PB0/AN0/$\overline{SCSB}$ PB1/AN1/SCLKB PB2/AN2/SDIB PB3/AN3/SDOB PB4/AN4 PB5/AN5 PB6/AN6 PB7/AN7/VDDIO	I/O	Pull-high Wake-up PB7/VDDIO PB0~PB6 with VDDIO	Bidirectional 8-bit input/output port. Each nibble, PB0~PB3 and PB4~PB7 pin can be configured as a wake-up input by a configuration option. Software instructions determine if the pin is a CMOS output or Schmitt Trigger input. Configuration options determine if the pins have pull-high resistors. PB is pin shared with the A/D inputs. Once a PB line is selected as an A/D input using software control, the I/O function and pull-high resistor are disabled automatically. PB7 can be configured as a normal I/O or a VDDIO pin by configuration option. The power supply for pins PB0~PB6 can be set to either VDD or VDDIO by configuration options. PB0~PB3 are shared with SPIB.
PC0/AN8~ PC7/AN15	I/O	Pull-high Wake-up	Bidirectional 8-bit input/output port. Each nibble, PC0~PC3 and PC4~PC7 pin can be configured as a wake-up input by a configuration option. Software instructions determine if the pin is a CMOS output or Schmitt Trigger input. Configuration options determine if the pins have pull-high resistors. PC is pin shared with the A/D inputs. Once a PC line is selected as an A/D input using software control, the I/O function and pull-high resistor are disabled automatically.
PD0/TMR1 PD1~PD7	I/O	Pull-high Wake-up	Bi-directional 8-bit input/output port. Each nibble, PD0~PD3 and PD4~PD7 pin can be configured as a wake-up input by a configuration option. Software instructions determine if the pin is a CMOS output or Schmitt Trigger input. Configuration options determine if the pins have pull-high resistors. The TMR1 pin is shared with PD0.
D-/DATA	I/O	—	USBD- line
D+/CLK	I/O	—	USBD+ line
V33O	O	—	3.3V regulator output
UBUS	—	—	USB SIE VDD
OSC1 OSC2	I O	—	OSC1, OSC2 are connected to an external 6MHz or 12MHz Crystal/resonator, determined by software instructions, for the internal system clock
OSC3 OSC4	I O	—	Real time clock oscillator. OSC3, OSC4 are connected to a 32768Hz crystal oscillator for timing purposes or to a system clock source (depending on the options). No built-in capacitor.
$\overline{RES}$	I	—	Schmitt trigger reset input. Active low
VDD	—	—	Positive power supply of MCU except for USBSIE
FHCS#	I	—	Flash Memory chip select
FHSI	I	—	Flash Memory Serial data input
FHSO	O	—	Flash Memory Serial data output
FHSCLK	I	—	Flash Memory Clock input
$\overline{FHHOLD}$	I	—	Flash Memory HOLD, to pause the device without deselecting the device
$\overline{FHWP}$	I	—	Flash Memory Write protection
VCC	—	—	HT82A6208 and HT82A6216 Flash Memory Positive Power Supply

Note: The Pin Description reflects the situation of the largest package, smaller package types may not contain all pins described in the table.

Absolute Maximum Ratings

Supply Voltage ..... V_{SS}–0.3V to V_{SS}+6.0V
Input Voltage ..... V_{SS}–0.3V to V_{DD}+0.3V
I_{OL} Total 150mA
Total Power Dissipation 500mW

Storage Temperature ..... –50°C to 125°C
Operating Temperature ..... 0°C to 70°C
I_{OH} Total ..... –100mA

Note: These are stress ratings only. Stresses exceeding the range specified under "Absolute Maximum Ratings" may cause substantial damage to the device. Functional operation of this device at other conditions beyond those listed in the specification is not implied and prolonged exposure to extreme conditions may affect device reliability.

D.C. Characteristics

Ta=25°C

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V_{DD}	Conditions				
V_{DD}	MCU Operating Voltage	—	f_{SYS}=6MHz	2.2	—	5.5	V
			f_{SYS}=12MHz	3.0	—	5.5	V
V_{CC}	HT82A6208 and HT82A6216 Flash Memory Operating Voltage	—	—	2.8	3.3	3.6	V
UBUS	USB SIE Operating Voltage	—	—	4.5	—	5.5	V
I_{DD1}	Operating Current	5V	No load, f_{SYS}=12MHz, ADC Off, DAC Off	—	8	—	mA
I_{DD2}	Operating Current	5V	No load, f_{SYS}=12MHz, ADC On, DAC On	—	12	—	mA
I_{SUS}	Suspend Current	5V	No load, system HALT, USB transceiver and 3.3V regulator on	—	330	500	μA
I_{STB}	Standby Current (WDT Disabled)	5V	No load ,system HALT, PS MODE, Set SUSP2 [UCC.4]	—	—	10	μA
V_{IL1}	Input Low Voltage for I/O Ports	5V	—	0	—	0.3V_{DD}	V
V_{IH1}	Input High Voltage for I/O Ports	5V	—	0.7V_{DD}	—	V_{DD}	V
V_{IL2}	Input Low Voltage ($\overline{RES}$)	5V	—	0	—	0.4V_{DD}	V
V_{IH2}	Input High Voltage ($\overline{RES}$)	5V	—	0.8V_{DD}	—	V_{DD}	V
V_{LVR0}	Low Voltage Reset	5V	—	1.9	2.0	2.1	V
V_{V33O}	3.3V Regulator Output	5V	I_{V33O}=–5mA	3.0	3.3	3.6	V
V_{AD}	12-bit A/D Input Voltage	—	—	0	—	V_{DD}	V
V_{OS}	Offset Error	—	—	–2	—	2	mV
V_{LVD}	Low Voltage Detect	—	—	2.1	2.2	2.3	V
I_{OL}	I/O Port Sink Current	5V	V_{OL}=0.1V_{DD}	10	20	—	mA
I_{OH}	I/O Port Source Current	5V	V_{OH}=0.9V_{DD}	–5	–10	—	mA
R_{PH}	Pull-high Resistance	5V	—	10	30	50	kΩ
R_{PH1}	Pull-high Resistance for DATA	5V	—	—	4.5	—	kΩ
R_{PH2}	Pull-high Resistance for CLK	5V	—	—	4.5	—	kΩ
I_{ADC}	Additional Power Consumption if A/D Converter is Used	5V	No load	—	1.5	3.0	mA
DNL	A/D Differential Non-Linearity	—	—	—	—	±2	LSB
INL	A/D Integral Non-Linearity	—	—		±2.5	±4.0	LSB
RESOLU	Resolution	—	—			12	Bits

A.C. Characteristics

Ta=25°C

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V_{DD}	Conditions				
f_{SYS}	System Clock	—	2.2V~5.5V	—	6000	—	kHz
		—	3.0V~5.5V	—	12000	—	kHz
f_{TIMER}	Timer I/P Frequency (TMR0/TMR1)	—	f_{SYS}=6MHz	0	—	6000	kHz
			f_{SYS}=12MHz	0	—	12000	kHz
t_{WDTOSC}	Watchdog Oscillator Period	5V	—	—	65	—	μs
t_{RES}	External Reset Low Pulse Width	—	—	1	—	—	ms
t_{SST}	System Start-up Timer Period	—	Wake-up from HALT	—	1024	—	t_{SYS}
t_{OPD}	Option Load Timer Period	5V	—	33	70	140	ms
t_{INT}	Interrupt Pulse Width	—	—	1	—	—	μs
t_{AD}	A/D Clock Period	—	—	1	—	—	μs
t_{ADC}	A/D Conversion Time	—	—	—	16	—	t_{AD}
t_{ADCS}	A/D Sample Time	—	—	—	8	—	t_{AD}
t_{CS_SK}	SPI $\overline{SCSA}$ or $\overline{SCSB}$ to SCLKA or SCLKB Time	—	—	50	—	—	ns
t_{SPICK}	SPI Clock Time	—	—	166	—	—	ns

Note: $t_{SYS}=1/f_{SYS}$

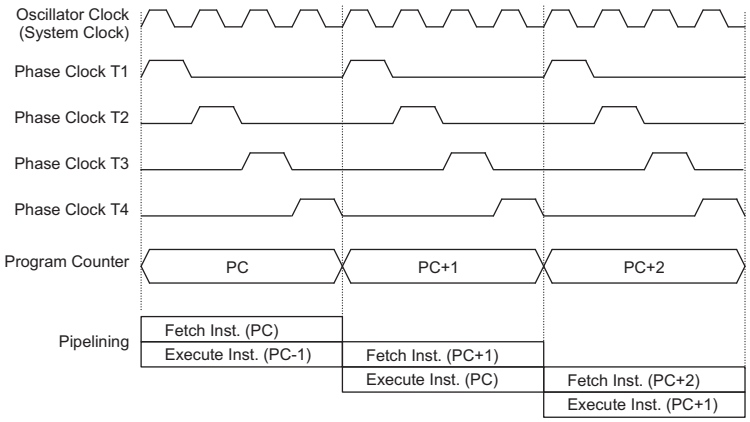
System Architecture

A key factor in the high-performance features of the Holtek range of microcontrollers is attributed to the internal system architecture. The range of devices take advantage of the usual features found within RISC microcontrollers providing increased speed of operation and enhanced performance. The pipelining scheme is implemented in such a way that instruction fetching and instruction execution are overlapped, hence instructions are effectively executed in one cycle, with the exception of branch or call instructions. An 8-bit wide ALU is used in practically all operations of the instruction set. It carries out arithmetic operations, logic operations, rotation, increment, decrement, branch decisions, etc. The internal data path is simplified by moving data through the Accumulator and the ALU. Certain internal registers are implemented in the Data Memory and can be directly or indirectly addressed. The simple addressing methods of these registers along with additional architectural features ensure that a minimum of external components is required to provide a functional I/O and A/D control system with maximum reliability and flexibility.

Clocking and Pipelining

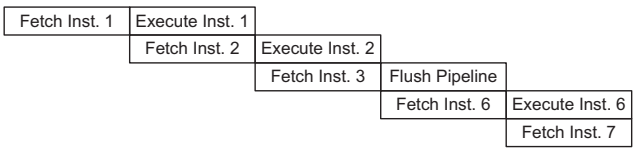
The main system clock, derived from a Crystal/Resonator is subdivided into four internally generated non-overlapping clocks, T1~T4. The Program Counter is incremented at the beginning of the T1 clock during which time a new instruction is fetched. The remaining T2~T4 clocks carry out the decoding and execution functions. In this way, one T1~T4 clock cycle forms one instruction cycle. Although the fetching and execution of instructions takes place in consecutive instruction cycles, the pipelining structure of the microcontroller ensures that instructions are effectively executed in one instruction cycle. The exception to this are instructions where the contents of the Program Counter are changed, such as subroutine calls or jumps, in which case the instruction will take one more instruction cycle to execute.

For instructions involving branches, such as jump or call instructions, two instruction cycles are required to complete instruction execution. An extra cycle is required as the program takes one cycle to first obtain the actual jump or call address and then another cycle to actually execute the branch. The requirement for this extra cycle should be taken into account by programmers in timing sensitive applications.



System Clocking and Pipelining

```
1            MOV A,[12H]
2            CALL DELAY
3            CPL [12H]
4            :
5            :
6  DELAY:    NOP
```



Instruction Fetching

Program Counter

During program execution, the Program Counter is used to keep track of the address of the next instruction to be executed. It is automatically incremented by one each time an instruction is executed except for instructions, such as "JMP" or "CALL" that demand a jump to a non-consecutive Program Memory address. It must be noted that only the lower 8 bits, known as the Program Counter Low Register, are directly addressable by user.

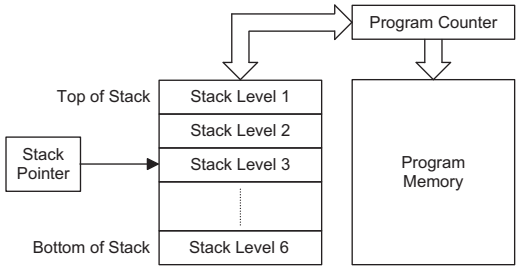
When executing instructions requiring jumps to non-consecutive addresses such as a jump instruction, a subroutine call, interrupt or reset, etc., the microcontroller manages program control by loading the required address into the Program Counter. For conditional skip instructions, once the condition has been met, the next instruction, which has already been fetched during the present instruction execution, is discarded and a dummy cycle takes its place while the correct instruction is obtained.

The lower byte of the Program Counter, known as the Program Counter Low register or PCL, is available for program control and is a readable and writeable register. By transferring data directly into this register, a short program jump can be executed directly, however, as only this low byte is available for manipulation, the jumps are limited to the present page of memory, that is 256 locations. When such program jumps are executed it should also be noted that a dummy cycle will be inserted.

The lower byte of the Program Counter is fully accessible under program control. Manipulating the PCL might cause program branching, so an extra cycle is needed to pre-fetch. Further information on the PCL register can be found in the Special Function Register section.

Stack

This is a special part of the memory which is used to save the contents of the Program Counter only. The stack has 6 levels and is neither part of the data nor part of the program space, and is neither readable nor writeable. The activated level is indexed by the Stack Pointer, SP, and is neither readable nor writeable. At a subroutine call or interrupt acknowledge signal, the contents of the Program Counter are pushed onto the stack. At the end of a subroutine or an interrupt routine, signaled by a return instruction, RET or RETI, the Program Counter is restored to its previous value from the stack. After a device reset, the Stack Pointer will point to the top of the stack.



Mode	Program Counter Bits											
	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Initial Reset	0	0	0	0	0	0	0	0	0	0	0	0
USB Interrupt	0	0	0	0	0	0	0	0	0	1	0	0
External Interrupt	0	0	0	0	0	0	0	0	1	0	0	0
Timer/Event Counter 0 Overflow	0	0	0	0	0	0	0	0	1	1	0	0
SPIA Interrupt	0	0	0	0	0	0	0	1	0	0	0	0
SPIB Interrupt	0	0	0	0	0	0	0	1	0	1	0	0
Timer/Event Counter 1 Overflow	0	0	0	0	0	0	0	1	1	0	0	0
Skip	Program Counter + 2											
Loading PCL	PC11	PC10	PC9	PC8	@7	@6	@5	@4	@3	@2	@1	@0
Jump, Call Branch	#11	#10	#9	#8	#7	#6	#5	#4	#3	#2	#1	#0
Return from Subroutine	S11	S10	S9	S8	S7	S6	S5	S4	S3	S2	S1	S0

Program Counter

Note: PC11~PC8: Current Program Counter bits
#11~#0: Instruction code address bits
@7~@0: PCL bits
S11~S0: Stack register bits

If the stack is full and an enabled interrupt takes place, the interrupt request flag will be recorded but the acknowledge signal will be inhibited. When the Stack Pointer is decremented, by RET or RETI, the interrupt will be serviced. This feature prevents stack overflow allowing the programmer to use the structure more easily. However, when the stack is full, a CALL subroutine instruction can still be executed which will result in a stack overflow. Precautions should be taken to avoid such cases which might cause unpredictable program branching.

Arithmetic and Logic Unit – ALU

The arithmetic-logic unit or ALU is a critical area of the microcontroller that carries out arithmetic and logic operations of the instruction set. Connected to the main microcontroller data bus, the ALU receives related instruction codes and performs the required arithmetic or logical operations after which the result will be placed in the specified register. As these ALU calculation or operations may result in carry, borrow or other status changes, the status register will be correspondingly updated to reflect these changes. The ALU supports the following functions:

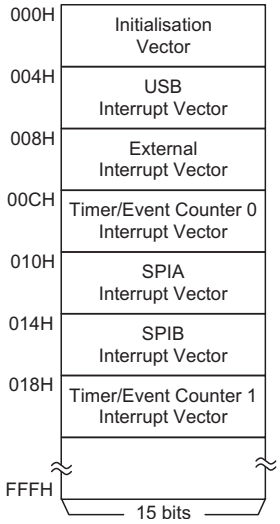
- Arithmetic operations: ADD, ADDM, ADC, ADCM, SUB, SUBM, SBC, SBCM, DAA
- Logic operations: AND, OR, XOR, ANDM, ORM, XORM, CPL, CPLA
- Rotation RRA, RR, RRCA, RRC, RLA, RL, RLCA, RLC
- Increment and Decrement INCA, INC, DECA, DEC
- Branch decision, JMP, SZ, SZA, SNZ, SIZ, SDZ, SIZA, SDZA, CALL, RET, RETI

Program Memory

The Program Memory is the location where the user code or program is stored. The HT82A623R is a One-Time Programmable, OTP, memory type device where users can program their application code into the device. By using the appropriate programming tools, OTP devices offer users the flexibility to freely develop their applications which may be useful during debug or for products requiring frequent upgrades or program changes. OTP devices are also applicable for use in applications that require low or medium volume production runs.

Structure

The Program Memory has a capacity of 4K by 15 bits. The Program Memory is addressed by the Program Counter and also contains data, table information and interrupt entries. Table data, which can be setup in any location within the Program Memory, is addressed by separate table pointer registers.



Program Memory Structure

Special Vectors

Within the Program Memory, certain locations are reserved for special usage such as reset and interrupts.

- Location 000H
  This vector is reserved for use by the device reset for program initialisation. After a device reset is initiated, the program will jump to this location and begin execution.
- Location 004H
  This area is reserved for the USB interrupt service program. If the USB interrupt is activated, the interrupt is enabled and the stack is not full, the program will jump to this location and begin execution.
- Location 008H
  This vector is used by the external interrupt. If the $\overline{INT}$ external input pin on the device receives a high to low transition, the program will jump to this location and begin execution, if the interrupt is enabled and the stack is not full.
- Location 00CH
  This vector is used by the timer0 counter. If a counter overflow occurs, the program will jump to this location and begin execution if the timer interrupt is enabled and the stack is not full.
- Location 010H
  This vector is used by serial interface A . When 8-bits of data have been received or transmitted successfully from serial interface A, the program will jump to this location and begin execution if the interrupt is enabled and the stack is not full.
- Location 014H
  This vector is used by serial interface B . When 8-bits of data have been received or transmitted successfully from serial interface A, the program will jump to this location and begin execution if the interrupt is enabled and the stack is not full

- Location 018H
  This vector is used by the timer1 counter. If a counter overflow occurs, the program will jump to this location and begin execution if the timer interrupt is enabled and the stack is not full.

Look-up Table

Any location within the Program Memory can be defined as a look-up table where programmers can store fixed data. To use the look-up table, one method is to first setup a low byte table pointer by placing the lower order address of the look up data to be retrieved in the low byte table pointer register, TBLP. This register defines the lower 8-bit address of the look-up table.

After setting up the table pointer, the table data can be retrieved from the current Program Memory page or last Program Memory page using the "TABRDC[m]" or "TABRDL [m]" instructions, respectively. When these instructions are executed, the lower order table byte from the Program Memory will be transferred to the user defined Data Memory register [m] as specified in the instruction. The higher order table data byte from the Program Memory will be transferred to the TBLH special register. Any unused bits in this transferred higher order byte will be read as "0".

The following diagram illustrates the addressing/data flow of the look-up table:

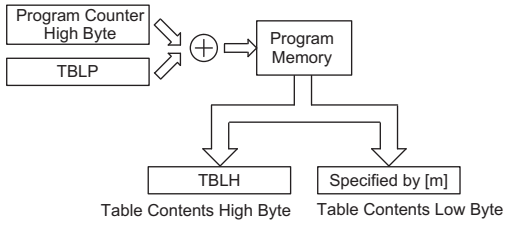


Table Read – TBLP only

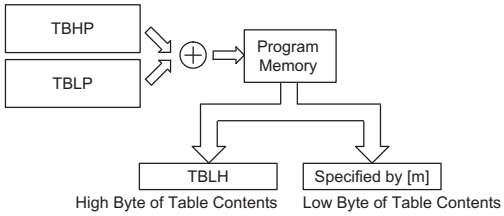


Table Read – TBLP/TBHP

Table Program Example

Another method is to setup the full table address using both the TBLP and TBHP low and high byte table pointer registers to directly address any area in he Program Memory. In this way any page of data can be accessed directly using the TABRDL instruction. If the TBHP high byte table pointer register is to be used, then it must first be enabled with a configuration option.

The following example shows how the table pointer and table data is defined and retrieved from the microcontroller. This example uses raw table data located in the last page which is stored there using the ORG statement. The value at this ORG statement is "F00H" which refers to the start address of the last page within the 4K Program Memory of device. The table pointer is setup here to have an initial value of "06H". This will ensure that the first data read from the data table will be at the Program Memory address "F06H" or 6 locations after the start of the last page. Note that the value for the table pointer is referenced to the first address of the present page if the "TABRDC [m]" instruction is being used. The high byte of the table data which in this case is equal to zero will be transferred to the TBLH register automatically when the "TABRDL [m]" instruction is executed.

Instruction	Table Location Bits											
	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
TABRDC [m]	PC11	PC10	PC9	PC8	@7	@6	@5	@4	@3	@2	@1	@0
TABRDL [m]	1	1	1	1	@7	@6	@5	@4	@3	@2	@1	@0

Table Location

Note: PC11~PC8: Current Program Counter bits
@7~@0: Table Pointer TBLP bits
TBHP register bit3~bit0 when TBHP is enabled

• Table Program Example

```
tempreg1 db    ?    ; temporary register #1
tempreg2 db    ?    ; temporary register #2
     :
     :

mov a,06h           ; initialise table pointer - note that this address
                    ; is referenced

mov tblp,a          ; to the last page or present page
     :
     :

tabrdl   tempreg1   ; transfers value in table referenced by table pointer
                    ; to tempregl
                    ; data at prog. memory address "F06H" transferred to
                    ; tempregl and TBLH

dec tblp            ; reduce value of table pointer by one

tabrdl   tempreg2   ; transfers value in table referenced by table pointer
                    ; to tempreg2
                    ; data at prog.memory address "F05H" transferred to
                    ; tempreg2 and TBLH
                    ; in this example the data "1AH" is transferred to
                    ; tempreg1 and data "0FH" to register tempreg2
                    ; the value "00H" will be transferred to the high byte
                    ; register TBLH
     :
     :

org F00h            ; sets initial address of last page

dc  00Ah, 00Bh, 00Ch, 00Dh, 00Eh, 00Fh, 01Ah, 01Bh
     :
     :
```

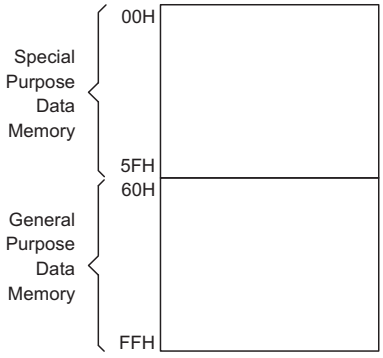
Because the TBLH register is a read-only register and cannot be restored, care should be taken to ensure its protection if both the main routine and Interrupt Service Routine use the table read instructions. If using the table read instructions, the Interrupt Service Routines may change the value of TBLH and subsequently cause errors if used again by the main routine. As a rule it is recommended that simultaneous use of the table read instructions should be avoided. However, in situations where simultaneous use cannot be avoided, the interrupts should be disabled prior to the execution of any main routine table-read instructions. Note that all table related instructions require two instruction cycles to complete their operation.

Data Memory

The Data Memory is a volatile area of 8-bit wide RAM internal memory and is the location where temporary information is stored. Divided into two sections, the first of these is an area of RAM where special function registers are located. These registers have fixed locations and are necessary for correct operation of the device. Many of these registers can be read from and written to directly under program control, however, some remain protected from user manipulation. The second area of Data Memory is reserved for general purpose use. All locations within this area are read and write accessible under program control.

Structure

The two sections of Data Memory, the Special Purpose and General Purpose Data Memory are located at consecutive locations. All are implemented in RAM and are 8 bits wide but the length of each memory section is dictated by the type of microcontroller chosen. The start address of the Data Memory for all devices is the address ″00H″. Registers which are common to all microcontrollers, such as ACC, PCL, etc., have the same Data Memory address.



Data Memory Structure

Note: Most of the Data Memory bits can be directly manipulated using the ″SET [m].i″ and ″CLR [m].i″ with the exception of a few dedicated bits. The Data Memory can also be accessed through the memory pointer register MP.

General Purpose Data Memory

All microcontroller programs require an area of read/write memory where temporary data can be stored and retrieved for use later. It is this area of RAM memory that is known as General Purpose Data Memory. This area of Data Memory is fully accessible by the user program for both read and write operations. By using the ″SET [m].i″ and ″CLR [m].i″ instructions individual bits can be set or reset under program control giving the user a large range of flexibility for bit manipulation in the Data Memory.

00H	IAR0	2EH	
01H	MP0	2FH	
02H	IAR1	30H	UFOEN
03H	MP1	31H	UFC0
04H		32H	
05H	ACC	33H	
06H	PCL	34H	
07H	TBLP	35H	
08H	TBLH	36H	
09H	WDTS	37H	
0AH	STATUS	38H	SBCRA
0BH	INTC0	39A	SBDRA
0CH	TMR1H	3AH	ADRL
0DH	TMR1L	3BH	ADRH
0EH	TMR1C	3CH	ADCR
0FH	TMR0H	3DH	ACSR
10H	TMR0L	3EH	SBCRB
11H	TMR0C	3FH	SBDRB
12H	PA	40H	MODE
13H	PAC	41H	SPI_REG
14H	PB	42H	
15H	PBC	43H	
16H	PC	44H	
17H	PCC	45H	
18H	PD	46H	
19H	PDC	47H	
1AH		48H	
1BH		49H	
1CH	USB_STAT	4AH	
1DH	UINT	4BH	
1EH	INTC1	4CH	
1FH	TBHP	4DH	
20H	USC	4EH	
21H	USR	4FH	
22H	UCC	50H	
23H	AWR	51H	
24H	STALL	52H	
25H	SIES	53H	
26H	MISC	54H	
27H	UFIEN	55H	
28H	FIFO0	56H	PWMBR0
29H	FIFO1	57H	PWM0DR
2AH	FIFO2	58H	PWMBR1
2BH	FIFO3	59H	PWM1DR
2CH		5AH	PWNCTL
2DH			

: Unused Read as "00"

Special Purpose Data Memory

This area of Data Memory is where registers, necessary for the correct operation of the microcontroller, are stored. Most of the registers are both readable and writable but some are protected and are readable only, the details of which are located under the relevant Special Function Register section. Note that for locations that are unused, any read instruction to these addresses will return the value ″00H″.

Special Function Registers

To ensure successful operation of the microcontroller, certain internal registers are implemented in the Data Memory area. These registers ensure correct operation of internal functions such as timers, interrupts, etc., as well as external functions such as I/O data control. The location of these registers within the Data Memory begins at the address 00H. Any unused Data Memory locations between these special function registers and the point where the General Purpose Memory begins is reserved and attempting to read data from these locations will return a value of 00H.

Indirect Addressing Register – IAR0, IAR1

The IAR0 and IAR1 register, although having their locations in normal RAM register space, do not actually physically exist as normal registers. The method of indirect addressing for RAM data manipulation uses these Indirect Addressing Registers and Memory Pointers, in contrast to direct memory addressing, where the actual memory address is specified. Actions on the IAR0 and IAR1 registers will result in no actual read or write operation to these registers but rather to the memory location specified by their corresponding Memory Pointer, MP0 or MP1. Acting as a pair, IAR0 and MP0 can together only access data from Bank 0, while the IAR1 and MP1 register pair can access data from both Bank 0 and Bank 1. As the Indirect Addressing Registers are not physically implemented, reading the Indirect Addressing Registers indirectly will return a result of ″00H″ and writing to the registers indirectly will result in no operation.

Memory Pointer – MP0, MP1

For all devices, two Memory Pointers, known as MP0 and MP1 are provided. These Memory Pointers are physically implemented in the Data Memory and can be manipulated in the same way as normal registers providing a convenient way with which to address and track data. When any operation to the relevant Indirect Addressing Registers is carried out, the actual address that the microcontroller is directed to, is the address specified by the related Memory Pointer.

```
data .section  'data'
adres1    db ?
adres2    db ?
adres3    db ?
adres4    db ?
block     db ?
code .section at 0 'code'
org   00h

start:
    mov a,04h           ; setup size of block
    mov block,a
    mov a,offset adres1; Accumulator loaded with first RAM address
    mov mp0,a           ; setup memory pointer with first RAM address

loop:
    clr IAR0               ; clear the data at address defined by MP0
    inc mp0                ; increment memory pointer
    sdz block           ; check if last memory location has been cleared
    jmp loop

continue:
```

The important point to note here is that in the example shown above, no reference is made to specific Data Memory addresses.

Accumulator – ACC

The Accumulator is central to the operation of any microcontroller and is closely related with operations carried out by the ALU. The Accumulator is the place where all intermediate results from the ALU are stored. Without the Accumulator it would be necessary to write the result of each calculation or logical operation such as addition, subtraction, shift, etc., to the Data Memory resulting in higher programming and timing overheads. Data transfer operations usually involve the temporary storage function of the Accumulator; for example, when transferring data between one user defined register and another, it is necessary to do this by passing the data through the Accumulator as no direct transfer between two registers is permitted.

Program Counter Low Register – PCL

To provide additional program control functions, the low byte of the Program Counter is made accessible to programmers by locating it within the Special Purpose area of the Data Memory. By manipulating this register, direct jumps to other program locations are easily implemented. Loading a value directly into this PCL register will cause a jump to the specified Program Memory location, however, as the register is only 8-bit wide, only jumps within the current Program Memory page are permitted. When such operations are used, note that a dummy cycle will be inserted.

Look-up Table Registers – TBLP, TBHP, TBLH

These three special function registers are used to control operation of the look-up table which is stored in the Program Memory. TBLP and TBHP are the table pointer low and high byte registers and indicate the location where the table data is located. There value must be setup before any table read commands are executed. Their value can be changed, for example using the ″INC″ or ″DEC″ instructions, allowing for easy table data pointing and reading. TBLH is the location where the high order byte of the table data is stored after a table read data instruction has been executed. Note that the lower order table data byte is transferred to a user defined location.

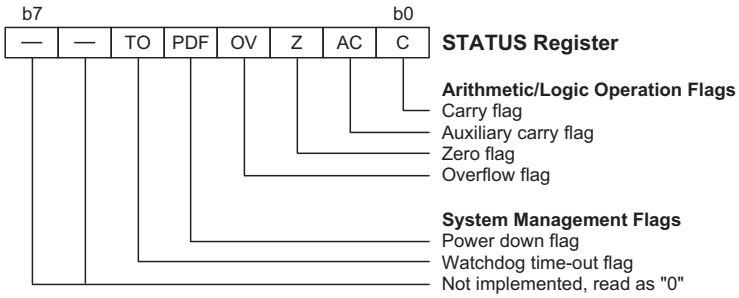
Status Register – STATUS

This 8-bit register contains the zero flag (Z), carry flag (C), auxiliary carry flag (AC), overflow flag (OV), power down flag (PDF), and watchdog time-out flag (TO). These arithmetic/logical operation and system management flags are used to record the status and operation of the microcontroller.

With the exception of the TO and PDF flags, bits in the status register can be altered by instructions like most other registers. Any data written into the status register will not change the TO or PDF flag. In addition, operations related to the status register may give different results due to the different instruction operations. The TO flag can be affected only by a system power-up, a WDT time-out or by executing the ″CLR WDT″ or ″HALT″ instruction. The PDF flag is affected only by executing the ″HALT″ or ″CLR WDT″ instruction or during a system power-up.

The Z, OV, AC and C flags generally reflect the status of the latest operations.

- **C** is set if an operation results in a carry during an addition operation or if a borrow does not take place during a subtraction operation; otherwise C is cleared. C is also affected by a rotate through carry instruction.
- **AC** is set if an operation results in a carry out of the low nibbles in addition, or no borrow from the high nibble into the low nibble in subtraction; otherwise AC is cleared.
- **Z** is set if the result of an arithmetic or logical operation is zero; otherwise Z is cleared.
- **OV** is set if an operation results in a carry into the highest-order bit but not a carry out of the highest-order bit, or vice versa; otherwise OV is cleared.
- **PDF** is cleared by a system power-up or executing the ″CLR WDT″ instruction. PDF is set by executing the ″HALT″ instruction.
- **TO** is cleared by a system power-up or executing the ″CLR WDT″ or ″HALT″ instruction. TO is set by a WDT time-out.



Status Register

In addition, on entering an interrupt sequence or executing a subroutine call, the status register will not be pushed onto the stack automatically. If the contents of the status registers are important and if the interrupt routine can change the status register, precautions must be taken to correctly save it.

Interrupt Control Registers – INTC0, INTC1

The microcontrollers provide one external interrupt, two internal timer/event counter overflow interrupts, two SPI interrupts and one USB interrupt. By setting various bits within these registers using standard bit manipulation instructions, the enable/disable function of each interrupt can be independently controlled. A master interrupt bit within this register, the EMI bit, acts like a global enable/disable and is used to set all of the interrupt enable bits on or off. This bit is cleared when an interrupt routine is entered to disable further interrupt and is set by executing the "RETI" instruction.

Timer/Event Counter Registers – TMR0H/TMR1H, TMR0L/TMR1L,TMR0C/TMR1C

All devices possess two internal 16-bit count-up timer. An associated register pair known as TMR0L/TMR0H and TMR1L/TMR1H are the locations where the timer 16-bit values are located. These registers can also be preloaded with fixed data to allow different time intervals to be setup. Associated control registers, known as TMR0C and TMR1C, contains the setup information for the timers, which determines in what mode the timer is to be used as well as containing the timer on/off control function.

Input/Output Ports and Control Registers

Within the area of Special Function Registers, the I/O registers and their associated control registers play a prominent role. All I/O ports have a designated register correspondingly labeled as PA, PB, PC and PD. These labeled I/O registers are mapped to specific addresses within the Data Memory as shown in the Data Memory table, which are used to transfer the appropriate output or input data on that port. With each I/O port there is an associated control register labeled PAC, PBC, PCC and PDC, also mapped to specific addresses with the Data Memory. The control register specifies which pins of that port are set as inputs and which are set as outputs. To setup a pin as an input, the corresponding bit of the control register must be set high, for an output it must be set low. During program initialisation, it is important to first setup the control registers to specify which pins are outputs and which are inputs before reading data from or writing data to the I/O ports. One flexible feature of these registers is the ability to directly program single bits using the "SET [m].i" and "CLR [m].i" instructions. The ability to change I/O pins from output to input and vice versa by manipulating specific bits of the I/O control registers during normal program operation is a useful feature of these devices.

Flash Memory

The HT82A6208 contains a 8,388,608 bit serial Flash memory, which has an internal configuration of 1,048,576×8. The HT82A6208 internal Flash Memory contains a 16,777,216 bit serial Flash memory, with a 2,097,152×8 internal configuration. The HT82A623R does not contain Flash Memory.

Device	Size	Configuration
HT82A623R	—	—
HT82A6208	8M	1,048,576×8
HT82A6216	16M	2,097,152×8

Flash Memory Description

The HT82A6208/HT82A6216 internal Flash Memory feature a serial peripheral interface and software protocol which permits operation using a simple 3-wire bus. The three bus signals are a clock input, FHSCLK, serial data input, FHSI, and serial data output, FHSO. The SPI access to the device is enabled using the FHCS# input. There is a sequential read operation for the whole device.

After a program/erase command is issued, the auto program/erase algorithms which program/erase and verify the specified page or byte/sector/block locations will be executed. Program command is executed on a page, 256 byte, basis, and an erase command is executed on chip or sector, 4K-bytes, or block, 64K-bytes. To provide the user with a simplistic interface, a status register is included to indicate the status of the device. The status read command can be issued to detect a completion status of a program or erase operation using the WIP bit.

When the HT82A6208/HT82A6216 internal Flash Memory is not in operation and FHCS# is high, the device will be place into a standby mode where it will draw less than 10μA/20μA DC current. The HT82A6208/HT82A6216 internal Flash Memory reliably stores its memory contents even after 100,000 program and erase cycles.

Data Protection

The device is designed to offer protection against accidental erasure or programming caused by spurious system level signals that may exist during power transition. During power up the device automatically resets the state instruction in the Read mode. In addition, with its control register architecture, alteration of the memory contents only occurs after successful completion of specific command sequences. The device also incorpo-

rates several features to prevent inadvertent write cycles during power-on and power-down transitions or due to system noise. These features are:

- Power-on reset and t_{PUW}: to avoid problems due to system power supply transitions, the power-on reset and t_{PUW} (internal timer) may protect the Flash Memory.
- Valid command length checking: The command length will be checked whether it is at byte base and completed on byte boundary.
- Write Enable (WREN) command: The WREN command is required to set the Write Enable Latch bit (WEL) before other commands to change data. The WEL bit will return to its reset condition under the following situations:
  - Power-on
  - Write Disable (WRDI) command completion
  - Write Status Register (WRSR) command completion
  - Page Program (PP) command completion
  - Continuous Program mode (CP) instruction completion - only for HT82A6216 internal Flash Memory
  - Sector Erase (SE) command completion
  - Block Erase (BE) command completion
  - Chip Erase (CE) command completion
  - Write Read-lock Bit (WRLB) instruction completion - only for HT82A6216 internal Flash Memory
- Deep Power Down Mode: By entering the deep power down mode, the flash memory is also under protection from all write commands except for the Release from deep power down mode command (RDP) and Read Electronic Signature command ($\overline{RES}$).
- Software Protection Mode (SPM): by using the BP register bits BP0~BP3, sections of the Flash Memory can be protected.
- Hardware Protection Mode (HPM): keeping WP low will protect the BP0~BP3 bits and the SRWD bit from a state change.

Status Bit			Protect Level	8Mb
BP2	BP1	BP0		
0	0	0	0 (none)	None
0	0	1	1 (1 block)	Block 15
0	1	0	2 (2 blocks)	Block 14~15
0	1	1	3 (4 blocks)	Block 12~15
1	0	0	4 (8 blocks)	Block 8~15
1	0	1	5 (all)	All
1	1	0	6 (all)	All
1	1	1	7 (all)	All

Protected Flash Area - HT82A6208

Status Bit				16Mb
BP3	BP2	BP1	BP0	
0	0	0	0	0 (none)
0	0	0	1	1 (1block, block 31th)
0	0	1	0	2 (2blocks, block 30~31th)
0	0	1	1	3 (4blocks, block 28~31th)
0	1	0	0	4 (8blocks, block 24~31th)
0	1	0	1	5 (16blocks, block 16~31th)
0	1	1	0	6 (32blocks, all)
0	1	1	1	7 (32blocks, all)
1	0	0	0	8 (32blocks, all)
1	0	0	1	9 (32blocks, all)
1	0	1	0	10 (16blocks, block 0~15th)
1	0	1	1	11 (24blocks, block 0~23th)
1	1	0	0	12 (28blocks, block 0~27th)
1	1	0	1	13 (30blocks, block 0~29th)
1	1	1	0	14 (31blocks, block 0~30th)
1	1	1	1	15 (32blocks, all)

Protected Flash Area - HT82A6216

Hold Features

The $\overline{FHHOLD}$ pin signal goes low to hold any serial communications with the device. The HOLD features will not stop the function of the write status register or any programming erase operation in progress.

The HOLD operation requires that the Chip Select, (FHCS#) is kept low and starts on the falling edge of the $\overline{FHHOLD}$ pin signal while the Serial Clock (FHSCLK) signal is low (if Serial Clock signal is not being low. The HOLD operation will not start until the Serial Clock is low). The HOLD condition ends on the rising edge of the $\overline{FHHOLD}$ pin signal white the Serial Clock (FHSCLK)

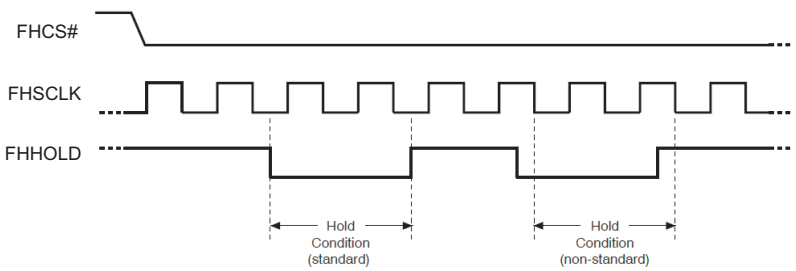


Figure 1. Hold Condition Operation

signal is low. If the Serial Clock signal is low, the HOLD operation will not end until the Serial Clock being is low for the following figure 1.

The Serial Data Output (FHSO) is high impedance, both Serial Data Input (FHSI) and Serial Clock (FHSCLK) are don't care during the HOLD operation. If the Chip Select (FHCS#) is set high during the HOLD operation then it will reset the internal logic of the device. To re-start communication with the device, the $\overline{\text{FHHOLD}}$ pin must be high and FHCS# must be low.

For the HT82A6208/HT82A6216, the internal Flash Memory $\overline{\text{FHHOLD}}$ pin must is bound to the VCC pin.

Memory Organisation

The internal memory blocks of the Flash Memory including the sector and address range is shown in the following tables.

Block	Sector	Address Range	
15	255	0FF000h	0FFFFFh
	⋮	⋮	⋮
	240	0F0000h	0F0FFFh
14	239	0EF000h	0EFFFFh
	⋮	⋮	⋮
	224	0E0000h	0E0FFFh
13	223	0DF000h	0DFFFFh
	⋮	⋮	⋮
	208	0D0000h	0D0FFFh
12	207	0CF000h	0CFFFFh
	⋮	⋮	⋮
	192	0C0000h	0C0FFFh
11	191	0BF000h	0BFFFFh
	⋮	⋮	⋮
	176	0B0000h	0B0FFFh
10	175	0AF000h	0AFFFFh
	⋮	⋮	⋮
	160	0A0000h	0A0FFFh
9	159	09F000h	09FFFFh
	⋮	⋮	⋮
	144	090000h	090FFFh
8	143	08F000h	08FFFFh
	⋮	⋮	⋮
	128	080000h	080FFFh
7	127	07F000h	07FFFFh
	⋮	⋮	⋮
	112	070000h	070FFFh
6	111	06F000h	06FFFFh
	⋮	⋮	⋮
	96	060000h	060FFFh
5	95	05F000h	05FFFFh
	⋮	⋮	⋮
	80	050000h	050FFFh
4	79	04F000h	04FFFFh
	⋮	⋮	⋮
	64	040000h	040FFFh
3	63	03F000h	03FFFFh
	⋮	⋮	⋮
	48	030000h	030FFFh
2	47	02F000h	02FFFFh
	⋮	⋮	⋮
	32	020000h	020FFFh
1	31	01F000h	01FFFFh
	⋮	⋮	⋮
	16	010000h	010FFFh
0	15	00F000h	00FFFFh
	⋮	⋮	⋮
	4	004000h	004FFFh
	3	003000h	003FFFh
	2	002000h	002FFFh
	1	001000h	001FFFh
	0	000000h	000FFFh

Table 1. Flash Memory Organisation – HT82A6208

Block	Sector	Address Range	
31	511	1FF000h	1FFFFFh
	⋮	⋮	⋮
	496	1F0000h	1F0FFFh
30	495	1EF000h	1EFFFFh
	⋮	⋮	⋮
	480	1E0000h	1E0FFFh
29	479	1DF000h	1DFFFFh
	⋮	⋮	⋮
	464	1D0000h	1D0FFFh
28	463	1CF000h	1CFFFFh
	⋮	⋮	⋮
	448	1C0000h	1C0FFFh
27	447	1BF000h	1BFFFFh
	⋮	⋮	⋮
	432	1B0000h	1B0FFFh
26	431	1AF000h	1AFFFFh
	⋮	⋮	⋮
	416	1A0000h	1A0FFFh
25	415	19F000h	19FFFFh
	⋮	⋮	⋮
	400	190000h	190FFFh
24	399	18F000h	18FFFFh
	⋮	⋮	⋮
	384	180000h	180FFFh
23	383	17F000h	17FFFFh
	⋮	⋮	⋮
	368	170000h	170FFFh
22	367	16F000h	16FFFFh
	⋮	⋮	⋮
	352	160000h	160FFFh
21	351	15F000h	15FFFFh
	⋮	⋮	⋮
	336	150000h	150FFFh
20	335	14F000h	14FFFFh
	⋮	⋮	⋮
	320	140000h	140FFFh
19	319	13F000h	13FFFFh
	⋮	⋮	⋮
	304	130000h	130FFFh
18	303	12F000h	12FFFFh
	⋮	⋮	⋮
	288	120000h	120FFFh
17	287	11F000h	11FFFFh
	⋮	⋮	⋮
	272	110000h	110FFFh
16	271	10F000h	10FFFFh
	⋮	⋮	⋮
	256	100000h	100FFFh

Table 2. 16Mb Flash Memory Organisation - HT82A6216

Block	Sector	Address Range	
15	255	0FF000h	0FFFFFh
	⋮	⋮	⋮
	240	0F0000h	0F0FFFh
14	239	0EF000h	0EFFFFh
	⋮	⋮	⋮
	224	0E0000h	0E0FFFh
13	223	0DF000h	0DFFFFh
	⋮	⋮	⋮
	208	0D0000h	0D0FFFh
12	207	0CF000h	0CFFFFh
	⋮	⋮	⋮
	192	0C0000h	0C0FFFh
11	191	0BF000h	0BFFFFh
	⋮	⋮	⋮
	176	0B0000h	0B0FFFh
10	175	0AF000h	0AFFFFh
	⋮	⋮	⋮
	160	0A0000h	0A0FFFh
9	159	09F000h	09FFFFh
	⋮	⋮	⋮
	144	090000h	090FFFh
8	143	08F000h	08FFFFh
	⋮	⋮	⋮
	128	080000h	080FFFh
7	127	07F000h	07FFFFh
	⋮	⋮	⋮
	112	070000h	070FFFh
6	111	06F000h	06FFFFh
	⋮	⋮	⋮
	96	060000h	060FFFh
5	95	05F000h	05FFFFh
	⋮	⋮	⋮
	80	050000h	050FFFh
4	79	04F000h	04FFFFh
	⋮	⋮	⋮
	64	040000h	040FFFh
3	63	03F000h	03FFFFh
	⋮	⋮	⋮
	48	030000h	030FFFh
2	47	02F000h	02FFFFh
	⋮	⋮	⋮
	32	020000h	020FFFh
1	31	01F000h	01FFFFh
	⋮	⋮	⋮
	16	010000h	010FFFh
0	15	00F000h	00FFFFh
	⋮	⋮	⋮
	4	004000h	004FFFh
	3	003000h	003FFFh
	2	002000h	002FFFh
	1	001000h	001FFFh
	0	000000h	000FFFh

Table 2. 16Mb Flah Memory Organisation - HT82A6216

Command Definitions

The internal Flash Memory operates using a range of commands issued serially by the microcontroller to the Flash Memory. These commands are summarised in the accompanying table.

COMMAND (byte)	WREN (write Enable)	WRDI (write disable)	RDID (read ident-ification)	RDSR (read status register)	WRSR (write status register)	READ (read data)	Fast Read (fast read data)
1st	06 Hex	04 Hex	9F Hex	05 Hex	01 Hex	03 Hex	0B Hex
2nd						AD1	AD1
3rd						AD2	AD2
4th						AD3	AD3
5th							x
Action	sets the (WEL) write enable latch bit	reset the (WEL) write enable latch bit	output the manufacturer ID and 2-byte device ID	to read out the status register	to write new values to the status register	n bytes read out until **FHCS# goes high**	

COMMAND (byte)	SE (Sector Erase)	BE (Block Erase)	CE (Chip Erase)	PP (Page Program)	DP (Deep Power Down)	RDP (Release from Deep Power-down)	RES (Read Electronic ID)	REMS (Read Electronic Manufacturer & Device ID)
1st	20 Hex	52 or D8 Hex	60 or C7 Hex	02 Hex	B9 Hex	AB Hex	AB Hex	90 Hex
2nd	AD1	AD1		AD1			x	x
3rd	AD2	AD2		AD2			x	x
4th	AD3	AD3		AD3			x	ADD(1)
5th								
Action								Output the manufacturer ID and device ID

(1) ADD=00H will output the manufacturer's ID first and ADD=01H will output device ID first.

(2) It is not recommended to adopt any other code which is not in the above command definition table.

Flash Memory Command Definition - HT82A6208

COMMAND (byte)	WREN (write enable)	WRDI (write disable)	RDID (read identification)	RDSR (read status register)	WRSR (write status register)	READ (read data)	FAST READ (fast read data)	2READ (2 x I/O read command) note1	SE (sector erase)
1st byte	06 (hex)	04 (hex)	9F (hex)	05 (hex)	01 (hex)	03 (hex)	0B (hex)	BB (hex)	20 (hex)
2nd byte						AD1	AD1	ADD(2)	AD1
3rd byte						AD2	AD2	ADD(2) & Dummy(2)	AD2
4th byte						AD3	AD3		AD3
5th byte							Dummy		
Action	sets the (WEL) write enable latch bit	resets the (WEL) write enable latch bit	outputs JEDEC ID: 1-byte manufacturer ID & 2-byte device ID	to read out the values of the status register	to write new values to the status register	n bytes read out until FHCS# goes high	n bytes read out until FHCS# goes high	n bytes read out by 2 x I/O until FHCS# goes high	to erase the selected sector

Note 1: The count base is 4-bit for ADD(2) and Dummy(2) because of 2 x I/O. And the MSB is on SI/SIO0 which is different from 1 x I/O condition

COMMAND (byte)	BE (block erase)	CE (chip erase)	PP (Page program)	CP (Continuously program mode)	DP (Deep power down)	RDP (Release from deep power down)	RES (read electronic ID)	REMS (read electronic manufacturer & device ID)	REMS2 (read ID for 2x I/O mode)
1st byte	D8 (hex)	60 or C7 (hex)	02 (hex)	AD (hex)	B9 (hex)	AB (hex)	AB (hex)	90 (hex)	EF (hex)
2nd byte	AD1		AD1	AD1			x	x	x
3rd byte	AD2		AD2	AD2			x	x	x
4th byte	AD3		AD3	AD3			x	ADD(note 2)	ADD(note 2)
5th byte									
Action	to erase the selected block	to erase whole chip	to program the selected page	continously program whole chip, the address is automatically increase	enters deep power down mode	release from deep power down mode	to read out 1-byte device ID	outout the manufacturer ID & device ID	output the manufacturer ID & device ID

Note 2: ADD=00H will output the manufacturer ID first and ADD=01H will output device ID first

COMMAND (byte)	ENSO (enter secured OTP)	EXSO (exit secured OTP)	RDSCUR (read security register)	WRSCUR (write security register)	ESRY (enable SO to output RY/BY#)	DSRY (disable SO to output RY/BY#)
1st byte	B1 (hex)	C1 (hex)	2B (hex)	2F (hex)	70 (hex)	80 (hex)
2nd byte						
3rd byte						
4th byte						
5th byte						
Action	to enter the 512-bit secured OTP mode	to exit the 512-bit secured OTP mode	to read value of security register	to set the lock-down bit as "1" (once lock-down, cannot be updated)	to enable SO to output RY/BY# during CP mode	to disable SO to output RY/BY# during CP mode

Note 3: It is not recommoded to adopt any other code not in the command definition table, which will potentially enter the hidden mode.

Flash Memory Command Definition - HT82A6216

Flash Memory Operation

The following statements show the basic protocol behind each Flash Memory command execution.

- Before a command is issued, the status register should be checked to ensure that the device is ready for the intended operation.
- When a correct command is input to the device, it will enter the standby mode and remain in the standby mode until the next FHCS# falling edge. In the standby mode, the device FHSO pin should be High-Z.
- When a correct command is input to the device, it will enter the active mode and remain in the active mode until the next FHCS# rising edge.
- The input data is latched on the rising edge of the Serial Clock, FHSCLK, and the data is shifted out on the falling edge of FHSCLK. The difference between SPI mode 0 and mode 3 is shown in Figure 2.
- For the following instructions: RDID, RDSR, READ, FAST_READ, RES and REMS the shifted-in instruction sequence is followed by a data-out sequence. After any data bit is shifted out, FSCS# can be high. For the following instructions: WREN, WRDI, WRSR, SE, BE, CE, PP, RDP and DP, CS must go high exactly at the byte boundary; otherwise the instruction will be rejected and not executed.
- During the progress of Write Status Register, Program, Erase operations, the memory array access is neglected and therefore does not affect the current operation of the Write Status Register, Program, Erase.

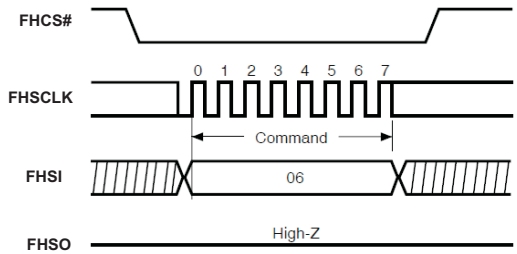
Command Description

The following provides a detailed description of each Flash Memory Command.

- Write Enable - WREN

  The Write Enable, WREN, instruction is used to set the Write Enable Latch, WEL, bit. For instructions like PP, SE, BE, CE, and WRSR, which are intended to change the device contents, it should be set every time after the WREN instruction sets the WEL bit.

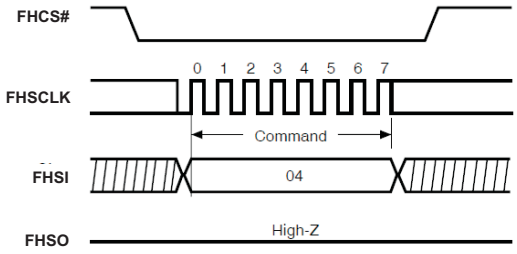
  The sequence to execute the WREN instruction is: FHCS# goes low → send WREN instruction code → FHCS# goes high.



Write Enable (WREN) Sequence (Command 06)

- Write Disable - WRDI

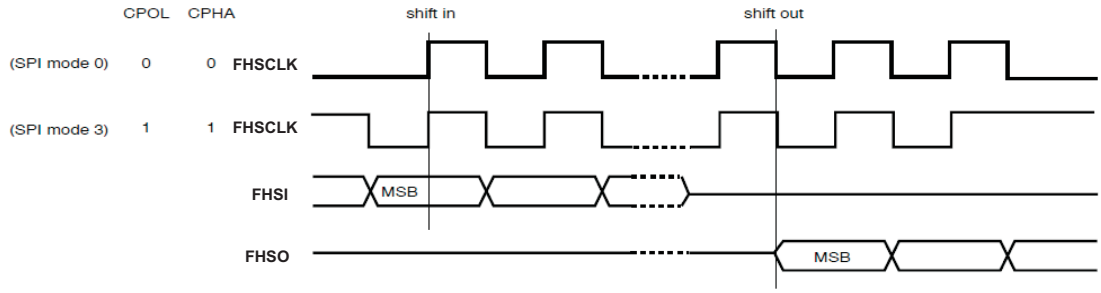
  The Write Disable, WRDI, instruction is for resetting the Write Enable Latch, WEL, bit. The sequence of issuing the WRDI instruction is: FHCS# goes low → send WRDI instruction code → FHCS# goes high.



Write Disable (WRDI) Sequence (Command 04)

The WEL bit is reset by following conditions:

- Power-up
- Write Disable, WRDI, instruction completion
- Write Status Register (WRSR) instruction completion
- Page Program (PP) instruction completion
- Sector Erase (SE) instruction completion
- Block Erase (BE) instruction completion
- Chip Erase (CE) instruction completion



Note: CPOL indicates clock polarity of the SPI master, CPOL=1 for SCLK high while idle, CPOL=0 for SCLK low while not transmitting. CPHA indicates clock phase. The combination of the CPOL bit and CPHA bit decides which SPI mode is supported.

Figure 2. Supported SPI Modes

- Read Identification - RDID

  The RDID instruction is for reading the manufacturer 1-byte ID followed by the 2-byte Device ID. The device Manufacturer ID is C2(hex), the memory type ID is 20(hex) as the first-byte device ID, and the individual device ID of second-byte ID is as follows: 14(hex) for the HT82A6208/HT82A6216 internal Flash Memory. The sequence for issuing the RDID instruction is: FHCS# goes low → sending RDID instruction code → 24-bits ID data out on SO → to end RDID operation can use FHCS# high at any time during data out. While the Program/Erase operation is in progress, it will not decode the RDID instruction, so there is no effect on the cycle of program/erase operation which is currently in progress. When FHCS# goes high, the device is in the standby stage.

- Read Status Register - RDSR

  The instruction is for reading the Status Register Bits. The Read Status Register can be read at any time (even in the program/erase/write status register condition) and continuously. It is recommended to check the Write in Progress (WIP) bit before sending a new instruction when a program, erase, or write status register operation is in progress. The sequence to issue the RDSR instruction is: FHCS# goes low → sending RDSR instruction code → Status Register data out on SO.

The definition of the status register bits is shown below:

- WIP bit

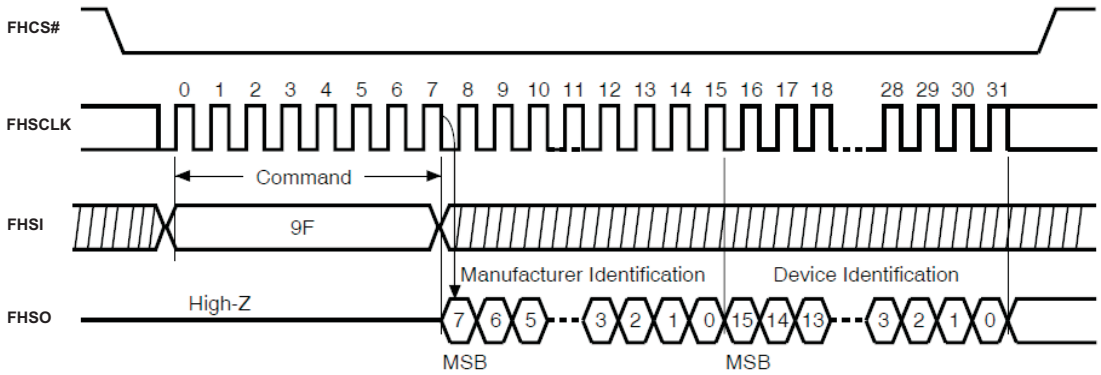
  The Write in Progress (WIP) bit, a volatile bit, indicates whether the device is busy in program/erase/write status register progress. When the WIP bit is set to ″1″, this means the device is busy in program/erase/write status register progress. When the WIP bit is set to ″0″, this means the device is not in progress of program/erase/write status register cycle.

- WEL bit

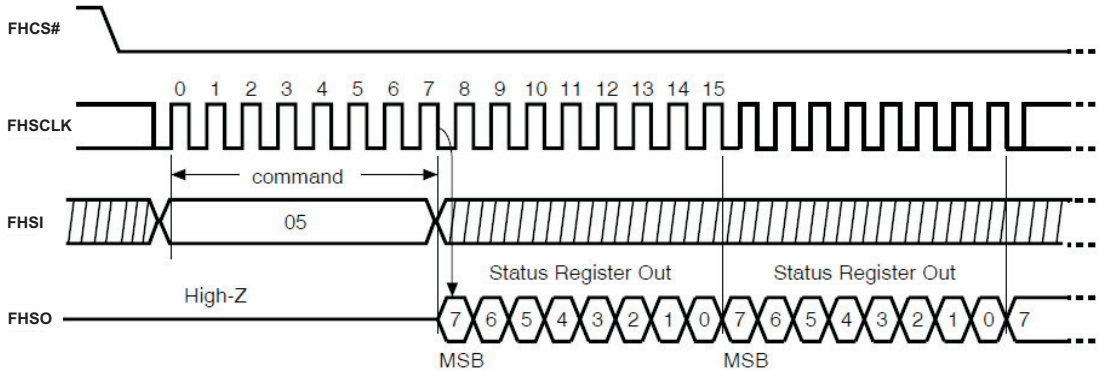
  The Write Enable Latch (WEL) bit, a volatile bit, indicates whether the device is set to internal write enable latch. When the WEL bit is set to ″1″, which means the internal write enable latch is set, the device can accept program/erase/write status register instructions. When the WEL bit is cleared to ″0″, which means no internal write enable latch; the device will not accept program/erase/write status register instructions.

- BP0~BP3 Bits

  The Block Protect bits BP0~BP3, are non-volatile bits, which indicate the protected area (as defined in the table) of the device against the program/erase instruction without the hardware protection mode being set. To write the Block Protect bits requires the Write Status Register (WRSR) instruction to be executed. Those bits define the protected area of



Read Identification (RDID) Sequence (Command 9F)



Read Status Register (RDSR) Sequence (Command 05)

the memory against Page Program (PP), Sector Erase (SE), Block Erase (BE) and Chip Erase(CE) instructions (only if all Block Protect bits are set to ″0″, can the CE instruction be executed).

- SRWD bit

  The Status Register Write Disable (SRWD) bit, non-volatile bit, is operated together with the Write Protection ($\overline{FHWP}$) pin to provide the hardware protection mode. The hardware protection mode requires that SRWD is set to ″1″ and the WP# pin signal is low . In the hardware protection mode, the Write Status Register (WRSR) instruction is no longer accepted for execution and the SRWD bit and Block Protect bits (BP0~BP3) are read only.

  For the HT82A6208/HT82A6216 internal Flash memory, the Write Protection ($\overline{FHWP}$) pin is always bonded with the GND pin

- Write Status Register - WRSR

  The WRSR instruction is used to change the values of the Status Register Bits. Before sending an WRSR instruction, the Write Enable (WREN) instruction must be decoded and executed to set the Write Enable Latch (WEL) bit in advance. The WRSR instruction can change the value of the Block Protect (BP0~BP3) bits to define the protected area of memory (as shown in the table). The WRSR also can set or reset the Status Register Write Disable (SRWD) bit in accordance with the Write Protection (WP#) pin signal. The WRSR instruction cannot be executed once the Hardware Protected Mode is entered.

  The sequence to issue WRSR instruction is: FHCS# goes low → sending WRSR instruction code → Status Register data on SI → FHCS# goes high. (see Figure 3). The WRSR instruction has no effect on b6, b5, b1, b0 of the status register.

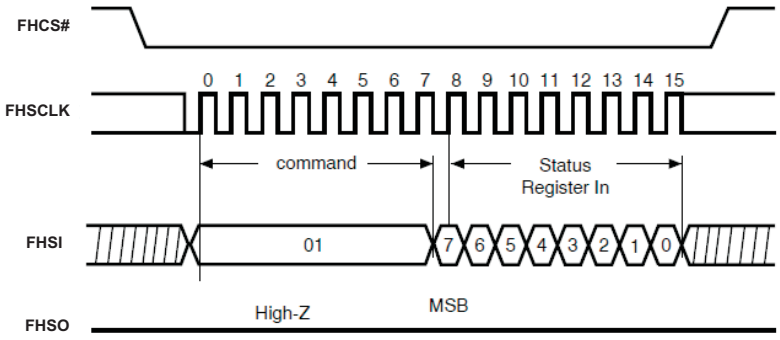


Figure 3. Write Status Register (WRSR) Sequence (Command 01)

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
SRWD Status Register Write Protect	0	0	BP2 the level of protected block	BP1 the level of protected block	BP0 the level of protected block	WEL (write enable latch)	WIP (write in progress bit)
1= status register write disable			(note 1)	(note 1)	(note 1)	1=write enable 0=not write enable	1=write operation 0=not in write operation

Note: 1. See the table ″Protected Flash Area ″.

2. The endurance cycles for the protect bits are 100,000 cycles; however, the tW time out spec for the protect bits is relaxed to $t_W = N \times 15ms$ (N is a multiple of 10,000 cycles, ex. N = 2 for 20,000 cycles) after 10,000 cycles on those bits.

Status Register - HT82A6208 Internal Flash Memory

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
SRWD (status register write protect)	Continuously program mode (CP mode)	BP3 (level of protected block)	BP2 (level of protected block)	BP1 (level of protected block)	BP0 (level of protected block)	WEL (write enable latch)	WIP (write in progress bit)
1= status register write disable	0 = normal program mode 1 = CP mode(default 0)	(note1)	(note1)	(note1)	(note1)	1= write enable 0= not write enable	1= write operation 0= not in write operation
Non- volatile bit	volatile bit	Non- volatile bit	Non- volatile bit	Non- volatile bit	Non- volatile bit	volatile bit	volatile bit

Note: See the table ″Protected Flash Area ″

Status Register - HT82A6216 Internal Flash Memory

Mode	Status register condition	$\overline{FHWP}$ and SRWD bit status	Memory
Software protection mode(SPM)	Status register can be written in (WEL bit is set to "1") and the SRWD, BP0-BP2 bits can be changed	$\overline{FHWP}$ =1 and SRWD bit=0, or $\overline{FHWP}$ =0 and SRWD bit=0, or $\overline{FHWP}$ =1 and SRWD=1	The protected area cannot be program or erase.
Hardware protection mode (HPM)	The SRWD, BP0-BP2 of status register bits cannot be changed	$\overline{FHWP}$ =0, SRWD bit=1	The protected area cannot be program or erase.

Note: As defined by the values in the Block Protect (BP2, BP1, BP0) bits of the Status Register, as shown in Table 1.

The above table shows the summary of the Software Protected Mode, SPM, and Hardware Protected Mode, HPM.

Software Protected Mode - SPM:

- When the SRWD bit=0, no matter if $\overline{FHWP}$ is low or high, the WREN instruction may set the WEL bit and can change the values of SRWD, BP2, BP1, BP0. The protected area, which is defined by bits BP2, BP1, BP0, is in the software protected mode.
- When the SRWD bit=1 and $\overline{FHWP}$ is high, the WREN instruction may set the WEL bit and can change the values of SRWD, BP2, BP1, BP0. The protected area, which is defined by BP2, BP1, BP0, is in the software protected mode.

Note: If SRWD bit=1 but $\overline{FHWP}$ is low, it is impossible to write to the Status Register even if the WEL bit has previously been set.

Hardware Protected Mode - HPM:

- When the SRWD bit=1, and then $\overline{FHWP}$ is low (or $\overline{FHWP}$ is low before SRWD bit=1), the device enters the hardware protected mode. The protected area data, defined by bits BP2, BP1, BP0 and hardware protected mode using $\overline{FHWP}$ is protected against data modification.

Note: to exit the hardware protected mode requires that $\overline{FHWP}$ is set high once the hardware protected mode is entered. If the $\overline{FHWP}$ pin is permanently connected high, the hardware protected mode can never be entered; only software can be used to enter the protected mode via bits BP2, BP1, BP0.

Protection Modes - HT82A6208 Internal Flash Memory

Mode	Status register condition	$\overline{\text{FHWP}}$ and SRWD bit status	Memory
Software protection mode(SPM)	Status register can be written in (WEL bit is set to "1") and the SRWD, BP0-BP3 bits can be changed	$\overline{\text{FHWP}}$ =1 and SRWD bit=0, or $\overline{\text{FHWP}}$ =0 and SRWD bit=0, or $\overline{\text{FHWP}}$ =1 and SRWD=1	The protected area cannot be program or erase.
Hardware protection mode (HPM)	The SRWD, BP0-BP3 of status register bits cannot be changed	$\overline{\text{FHWP}}$ =0, SRWD bit=1	The protected area cannot be program or erase.

Note: As defined by the values in the Block Protect (BP3, BP2, BP1, BP0) bits of the Status Register, as shown in Table 1.

The above table shows the summary of the Software Protected Mode (SPM) and Hardware Protected Mode (HPM).

Software Protected Mode - SPM:

- When the SRWD bit=0, no matter if $\overline{\text{FHWP}}$/ACC is low or high, the WREN instruction may set the WEL bit and can change the values of SRWD, BP3, BP2, BP1, BP0. The protected area, which is defined by BP3, BP2, BP1, BP0, is in the software protected mode (SPM).
- When the SRWD bit=1 and $\overline{\text{FHWP}}$/ACC is high, the WREN instruction may set the WEL bit and can change the values of SRWD, BP3, BP2, BP1, BP0. The protected area, which is defined by BP3, BP2, BP1, BP0, is in the software protected mode (SPM)

Note: If the SRWD bit=1 but $\overline{\text{FHWP}}$/ACC is low, it is impossible to write to the Status Register even if the WEL bit has previously been set. It is rejected to write to the Status Register and not be executed.

Hardware Protected Mode - HPM:

- When the SRWD bit=1, and then $\overline{\text{FHWP}}$/ACC is low (or $\overline{\text{FHWP}}$/ACC is low before SRWD bit=1), it enters the hardware protected mode. The data of the protected area is protected by the software protected mode by BP3, BP2, BP1, BP0 and the hardware protected mode by the $\overline{\text{FHWP}}$/ACC against data modification.

Note: to exit the hardware protected mode requires $\overline{\text{FHWP}}$/ACC is driven high once the hardware protected mode is entered. If the $\overline{\text{FHWP}}$/ACC pin is permanently connected high, the hardware protected mode can never be entered; only the software protected mode can be used via BP3, BP2, BP1, BP0.

Protection Modes - HT82A6216 Internal Flash Memory

CS must go high exactly at the byte boundary; otherwise, the instruction will be rejected and not executed. The self-timed Write Status Register cycle time (t_W) is initiated as soon as the Chip Select (FHCS#) goes high. The Write in Progress (WIP) bit can still be checked when the Write Status Register cycle is in progress. The WIP is set to "1" during the t_W timing, and cleared "0" when the Write Status Register Cycle has completed, and the Write Enable Latch (WEL) bit is reset.

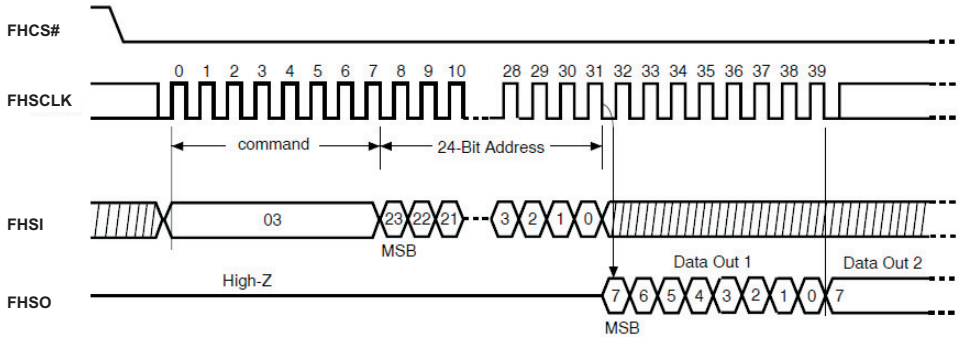
- Read Data Bytes - READ

  The read instruction is for reading data out. The address is latched on the rising edge of FHSCLK, and data shifts out on the falling edge of FHSCLK at a maximum frequency f_R. The first address byte can be at any location. The address is automatically increased to the next higher address after each data byte is shifted out, so the whole memory can be read out with a single READ instruction. The address counter rolls over to "0" when the highest address has been reached.

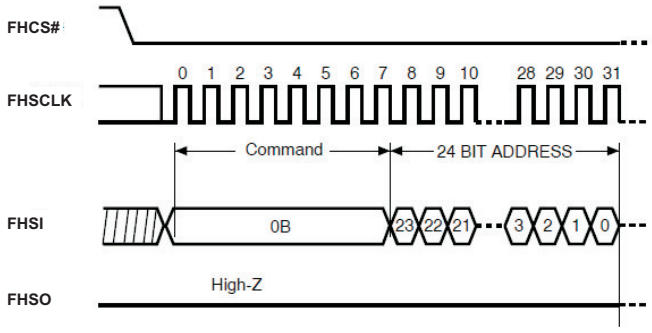
  The sequence to issue a READ instruction is: FHCS# goes low → sending READ instruction code → 3-byte address on SI → data out on SO → to end a READ operation, FHCS# going high can be used at any time during data out.

- Read Data Bytes at Higher Speed - FAST_READ

  The FAST_READ instruction is to read data out quickly. The address is latched on the rising edge of SCLK, and each bit of data is shifted out on the falling edge of SCLK at a maximum frequency f_C. The first address byte can be at any location. The address is automatically increased to the next higher address after each data byte is shifted out, so the whole memory



Read Data Bytes (READ) Sequence (Command 03)



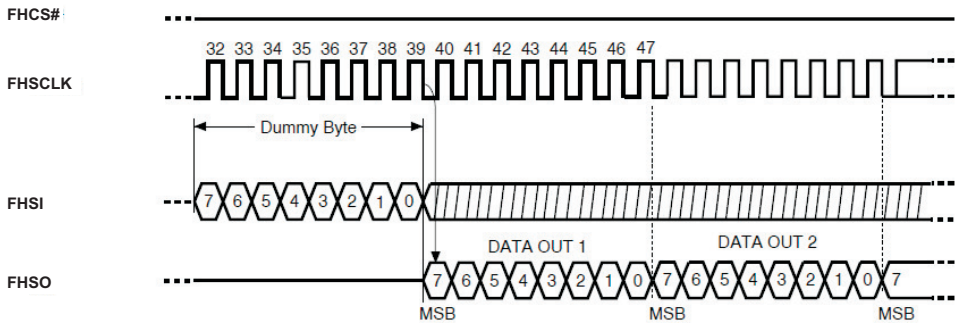


Figure 4. Read at Higher Speed (FAST_READ) Sequence (Command 0B)

can be read out with a single FAST_READ instruction. The address counter rolls over to ″0″ when the highest address has been reached.

The sequence to issue a FAST_READ instruction is: FHCS# goes low → sending FAST_READ instruction code → 3-byte address on SI → 1-dummy byte address on SI → data out on SO → to end FAST_READ operation can use FHCS# going high at any time during data out. (see Figure 4) While Program/Erase/Write Status Register cycle is in progress, FAST_READ instruction is rejected without any impact on the Program/Erase/Write Status Register current cycle.

- Sector Erase - SE

  The Sector Erase (SE) instruction is used to erase the data of the chosen sector to ″1″. A Write Enable (WREN) instruction must be executed to set the Write Enable Latch (WEL) bit before sending the Sector Erase (SE). Any address in the sector (see Table 1 or Table 2) is a valid address for a Sector Erase (SE) instruction. CS must go high exactly at the byte boundary (when the latest eighth address byte has been latched-in); otherwise, the instruction will be rejected and not executed.

  Address bits [Am-A12] (Am is the most significant address) select the sector address. The sequence to issue a SE instruction is: FHCS# goes low → sending SE instruction code → 3-byte address on SI → FHCS# goes high.

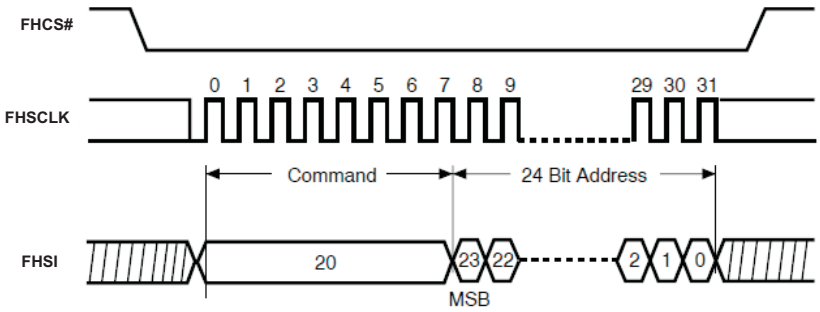
  The self-timed Sector Erase Cycle time (tSE) is initiated as soon as the Chip Select (CS) goes high. The Write in Progress (WIP) bit can still be checked when a Sector Erase cycle is in progress. WIP is set to ″1″ during the tSE timing, and cleared to ″0″ when the Sector Erase Cycle is completed, and the Write Enable Latch (WEL) bit is reset. If the page is protected by BP2, BP1, BP0 or BP3, BP2, BP1, BP0 bitts, the Sector Erase (SE) instruction will not be executed on the page.

- Block Erase - BE

  The Block Erase (BE) instruction erases data of the chosen block to ″1″. A Write Enable (WREN) instruction must executed to set the Write Enable Latch (WEL) bit before sending the Block Erase (BE). Any addresses of the block (see Table 1 or Table 2) are valid addressed for a Block Erase (BE) instruction. CS must go high exactly at the byte boundary (when the latest eighth address byte been latched-in); otherwise, the instruction will be rejected and not executed.

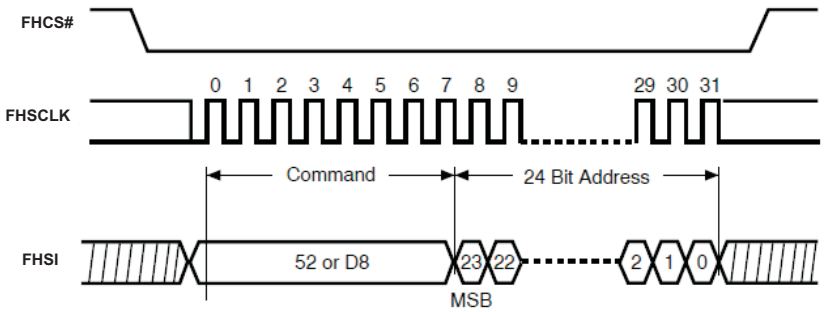
  The sequence of issuing BE instruction is: FHCS# goes low → sending BE instruction code → 3-byte address on SI → FHCS# goes high.

  The self-timed Block Erase Cycle time (tBE) is initiated as soon as Chip Select (FHCS#) goes high. The Write in Progress (WIP) bit still can be checked out when the Sector Erase cycle is in progress. The WIP is set to ″1″ during the tBE timing, and cleared to ″0″ when the Sector Erase Cycle has completed, and the Write Enable Latch (WEL) bit is reset. If the page is protected by BP0~BP3 bits, the Block Erase (BE) instruction will not be executed on the page.



Note: SE command is 20(hex).

Sector Erase (SE) Sequence (Command 20)



Note: BE command is 52 or D8(hex).

Block Erase (BE) Sequence (Command 52 or D8)

- Chip Erase - CE

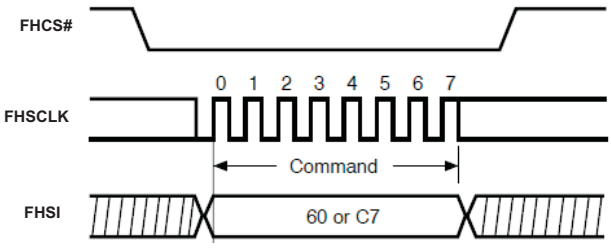
  The Chip Erase (CE) instruction is used to erase the data of the whole chip to "1". A Write Enable (WREN) instruction must be executed to set the Write Enable Latch (WEL) bit before sending the Chip Erase (CE). Any address of the sector (see Table 1 or Table 2) is a valid address for the Chip Erase (CE) instruction. FHCS# must go high exactly at the byte boundary (when the latest eighth address byte has been latched-in); otherwise, the instruction will be rejected and not executed.

  The sequence of issuing CE instruction is: FHCS# goes low → sending CE instruction code → FHCS# goes high. (see Figure 5).

  The self-timed Chip Erase Cycle time (tCE) is initiated as soon as the Chip Select (FHCS#) goes high. The Write in Progress (WIP) bit still can be checked when the Chip Erase cycle is in progress. The WIP is set to "1" during the tCE timing, and cleared to "0" when the Chip Erase Cycle has completed, and the Write Enable Latch (WEL) bit is reset. If the chip is protected by the BP0~BP3 bits, the Chip Erase (CE) instruction will not be executed. It will be only executed when BP0~BP3 are all set to "0".

- Page Program - PP

  The Page Program (PP) instruction is used to programming the memory to "0". A Write Enable (WREN) instruction must executed to set the Write Enable Latch (WEL) bit before sending the Page Program (PP). If the eighth least significant address bits (A7~A0) are not all 0, all transmitted data which goes beyond the end of the current page are programmed from the start address if the same page (from the address whose 8 least significant address bits (A7~A0) are all 0). FHCS# must go high exactly at the byte boundary (when the latest eighth address byte been latched-in); otherwise, the instruction will be rejected and not executed. If more than 256 bytes are sent to the device, the data of the last 256-bytes are programmed at the request page and previous data will be disregarded. If less than 256 bytes are sent to the device, the data is programmed at the request address of the page without effect on other address of the same page.



Note: CE command is 60(hex) or C7(hex).

Figure 5. Chip Erase (CE) Sequence (Command 60 or C7)

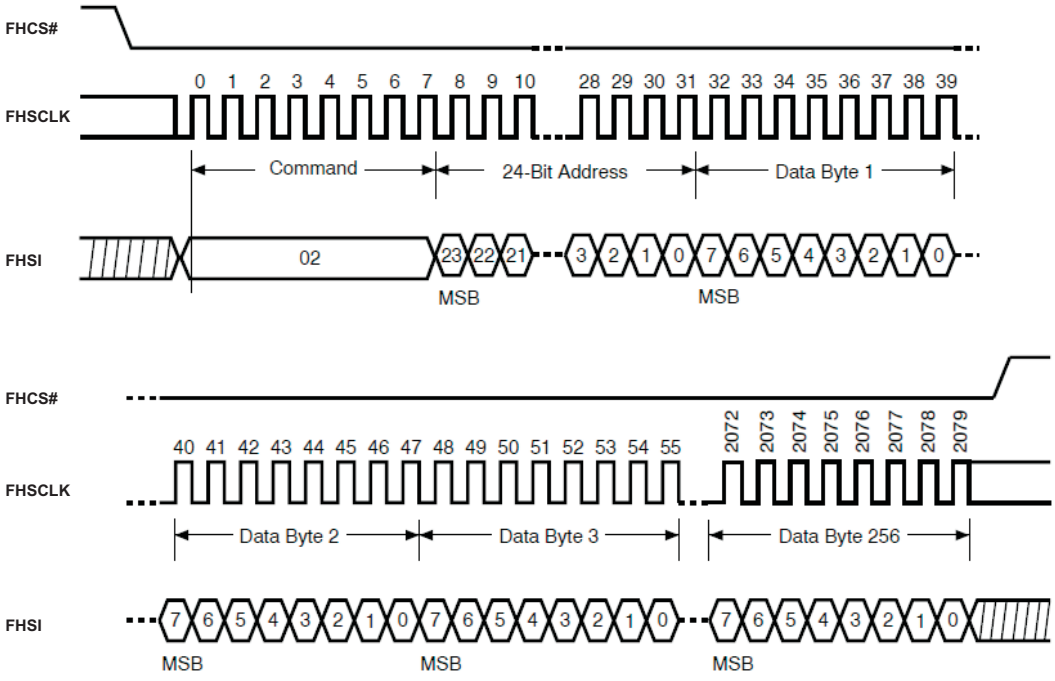


Figure 6. Page Program (PP) Sequence (Command 02)

The sequence to issue a PP instruction is: FHCS# goes low → sending PP instruction code → 3-byte address on SI → at least 1-byte on data on SI → FHCS# goes high (see Figure 6).

The self-timed Page Program Cycle time(tPP) is initiated as soon as the Chip Select (FHCS#) goes high. The Write in Progress (WIP) bit still can still be checked when the Page Program cycle is in progress. WIP is set to ″1″ during the tPP timing, and cleared to ″0″ when the Page Program Cycle has completed, and the Write Enable Latch (WEL) bit is reset. If the page is protected by the BP0~BP3 bits, the Page Program (PP) instruction will not be executed.

- Deep Power-down - DP

  The Deep Power-down (DP) instruction is used to set the device to a condition of minimum power consumption. The standby current is reduced from ISB1 to ISB2). The Deep Power-down mode requires the Deep Power-down (DP) instruction to be executed. During the Deep Power-down mode, the device is not active and all Write/ Program/Erase instructions are ignored. When FHCS# goes high, it will only be in standby mode and not in deep power-down mode.

  The sequence to issue a DP instruction is: FHCS# goes low → sending DP instruction code → FHCS# goes high. (see Figure 7) Once the DP instruction is executed, all instructions will be ignored except the Release from Deep Power-down mode (RDP) and Read Electronic Signature ($\overline{RES}$) instruction. ($\overline{RES}$ instruction to allow the ID been read out). During Power-down, the deep power-down mode automatically stops, and when powered-up, the device automatically is in standby mode. For the RDP instruction FHCS# must go high exactly at the byte boundary (when the latest eighth bit of the instruction code has been latched-in); otherwise, the instruction will not be executed. As soon as the Chip Select (FHCS#) goes high, a delay of tDP is required before entering the Deep Power-down mode and reducing the current to ISB2.

- Release from Deep Power-down (RDP), Read Electronic Signature (RES)

  The Release from Deep Power-down (RDP) instruction is terminated by driving Chip Select (FHCS#) High. When Chip Select (FHCS#) is driven High, the device is put into the Stand-by Power mode. If the device was not previously in the Deep Power-down mode, the transition to the Stand-by Power mode is immediate. If the device was previously in the Deep Power-down mode, though, the transition to the Stand-by Power mode is delayed by tRES2, and Chip Select (FHCS#) must remain High for at least tRES2(max), as specified in the Table. Once in the Stand-by Power mode, the device waits to be selected, so that it can receive, decode and execute instructions. The RES instruction reads out the old style of 8-bit Electronic Signature, whose values are shown in the table of ID Definitions. This is not the same as the RDID instruction. It is not recommended to use

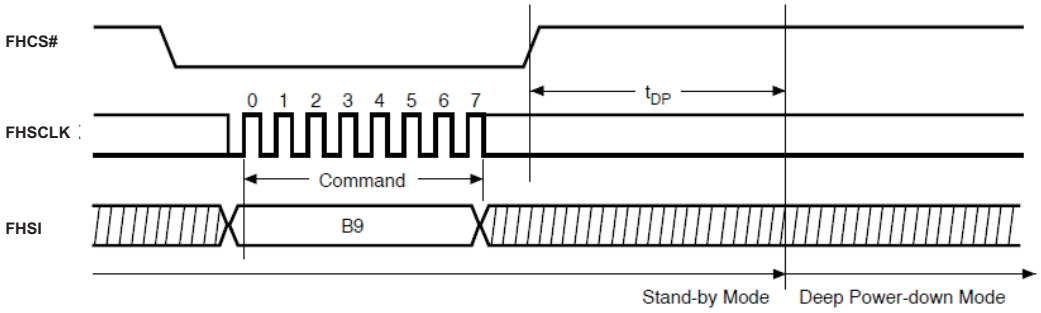
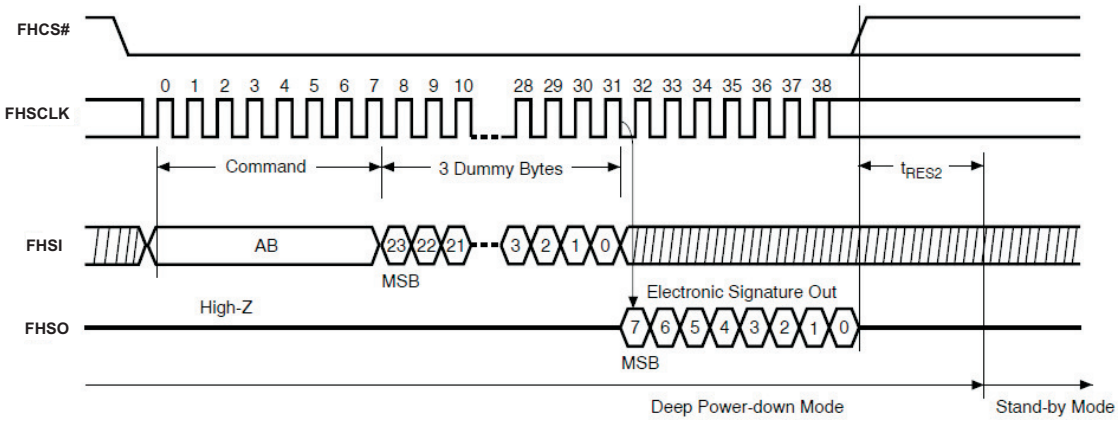


Figure 7. Deep Power-down (DP) Sequence (Command B9)



Release from Deep Power-down and Read Electronic Signature (RES) Sequence (Command AB)

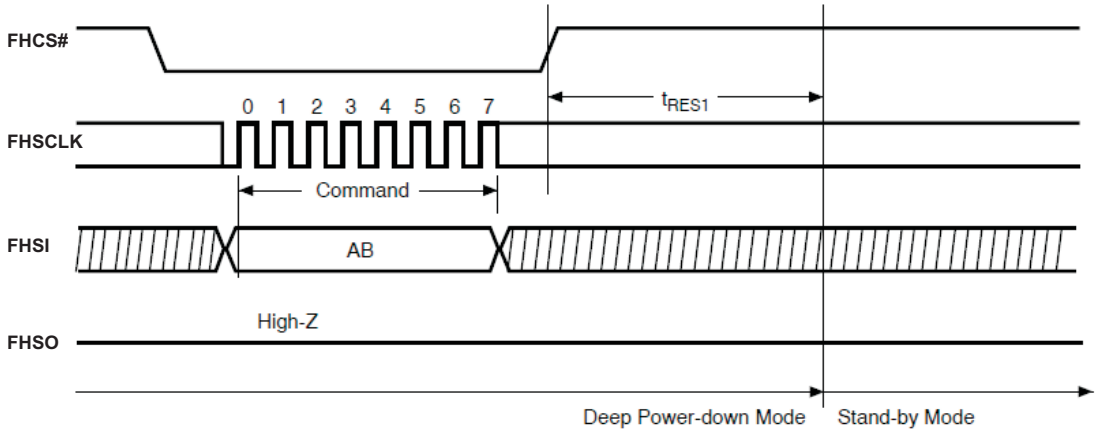


Figure 8. Release from Deep Power-down (RDP) Sequence (Command AB)

this for new designs. For new designs, use the RDID instruction. Even in Deep power-down mode, the RDP and RES are also allowed to be executed, except when the device is in the program/erase/write cycle; here there is no effect on the current program/erase/write cycle in progress.

The sequence is shown as figure 8.

The $\overline{RES}$ instruction is ended when FHCS# goes high after the ID has been read out at least once. The ID outputs repeatedly if additional clock cycles on FHSCLK are repeatedly sent while FHCS# is low. If the device was not previously in the Deep Power-down mode, the device transition to standby mode is immediate. If the device was previously in the Deep Power-down mode, there is a delay of tRES2 to transition to the standby mode, and FHCS# must remain high for at least tRES2(max). Once in the standby mode, the device waits to be selected, so it can be receive, decode, and execute instruction.

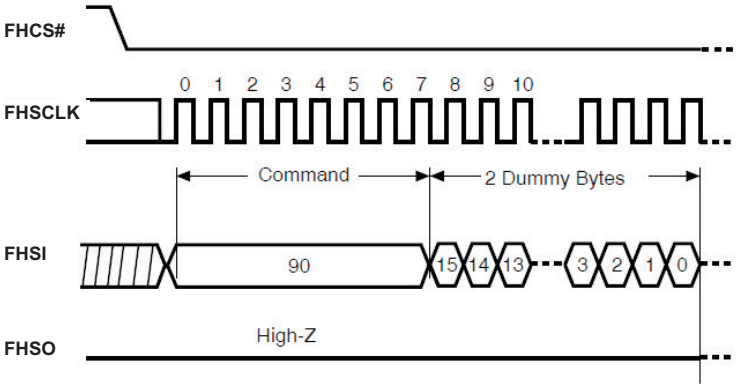
The RDP instruction is to release the device from the Deep Power-down Mode.

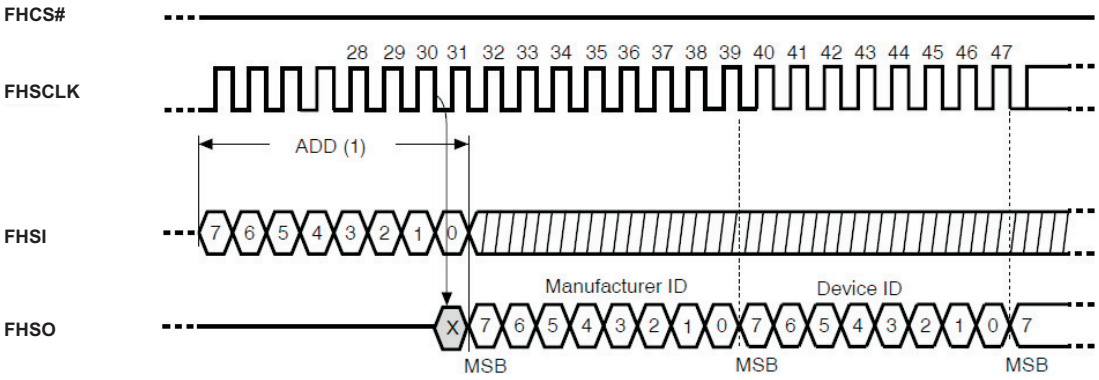
- Read Electronic Manufacturer ID & Device ID (REMS) - for the HT82A6208 internal Flash Memory

  The REMS instruction is an alternative to the Release from Power-down/Device ID instruction that provides both the JEDEC assigned manufacturer ID and the specific device ID.

  The REMS instruction is very similar to the Release from Power-down/Device ID instruction. The instruction is initiated by driving the FHCS# pin low and shifting the instruction code "90h" followed by two dummy bytes and one bytes address (A7~A0). After this, the Manufacturer ID for the device (C2h) and the Device ID are shifted out on the falling edge of FHSCLK with the most significant bit (MSB) first as shown in figure 9. The Device ID values are listed in the ID Definition table. If the one-byte address is initially set to 01h, then the device ID will be read first and then followed by the Manufacturer ID. The Manufacturer and Device IDs can be read continuously, alternating from one to the other. The instruction is completed by driving FHCS# high.

Command Type	HT82A6208 Internal Flash Memory		
RDID	Manufacture ID	Memory Type	Memory Density
	C2	20	14
RES	Electronic ID		
	13		
REMS	Manufacture ID		Device ID
	C2		13





Notes: ADD=00H will output the manufacturer's ID first and ADD=01H will output device ID first

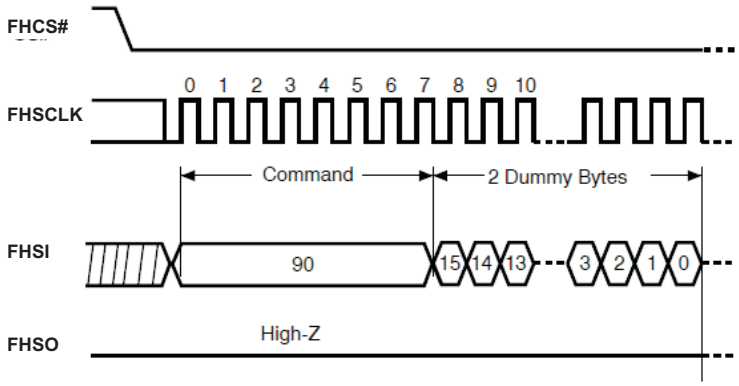
Figure 9. Read Electronic Manufacturer & Device ID (REMS) Sequence (Command 90)

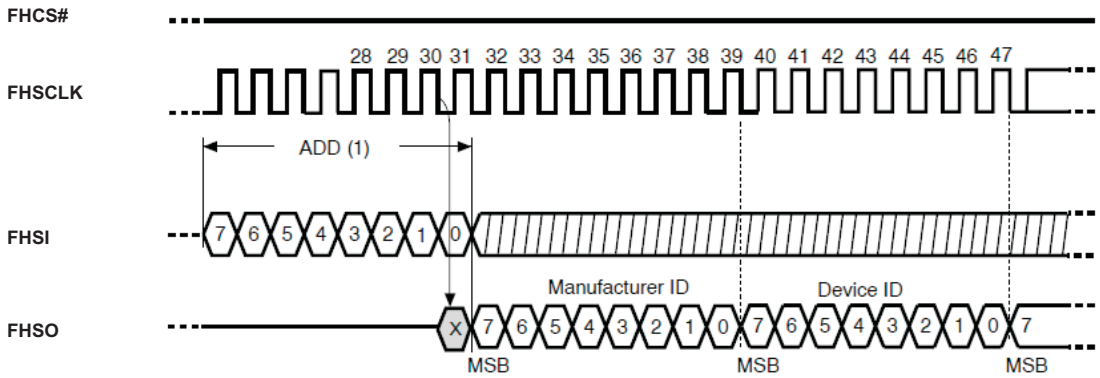
- Read Electronic Manufacturer ID & Device ID (REMS), (REMS2) - HT82A6216 internal Flash Memory

  The REMS & REMS2 instruction is an alternative to the Release from Power-down/Device ID instruction that provides both the JEDEC assigned manufacturer ID and the specific device ID.

  The REMS & REMS2 instruction is very similar to the Release from Power-down/Device ID instruction. The instruction is initiated by driving the FHCS# pin low and shifting the instruction code "90H" or "EFh" followed by two dummy bytes and one bytes address (A7~A0). After this, the Manufacturer ID for MXIC (C2h) and the Device ID are shifted out on the falling edge of FHSCLK with most significant bit (MSB) first as shown in figure 10. The Device ID values are listed in Table of ID Definitions. If the one-byte address is initially set to 01h, then the device ID will be read first and then followed by the Manufacturer ID. The Manufacturer and Device IDs can be read continuously, alternating from one to the other. The instruction is completed by driving FHCS# high.

Command Type	HT82A6216 Internal Flash Memory		
RDID (JEDEC ID)	Manufacture ID	Memory Type	Memory Density
	C2	20	15
RES	Electronic ID		
	14		
REMS/REMS2	Manufacture ID		Device ID
	C2		14





Notes: ADD=00H will output the manufacturer's ID first and ADD=01H will output device ID first

Figure 10. Read Electronic Manufacturer & Device ID (REMS) Sequence (Command 90)

Table 5. DC CHARACTERISTICS (Temperature = -40°C to 85°C for Industrial grade, Temperature = 0°C to 70°C for Commercial grade, VCC = 2.7V ~ 3.6V)

SYMBOL	PARAMETER	NOTES	MIN.	TYP	MAX.	UNITS	TEST CONDITIONS
ILI	Input Load Current	1			±2	uA	VCC = VCC Max VIN = VCC or GND
ILO	Output Leakage Current	1			±2	uA	VCC = VCC Max VIN = VCC or GND
ISB1	VCC Standby Current	1			10	uA	VIN = VCC or GND **FHCS# =VCC**
ISB2	Deep Power-down Current				10	uA	VIN = VCC or GND **FHCS# =VCC**
ICC1	VCC Read	1			12	mA	f=86MHz and 70MHz **FHSCLK** =0.1VCC/0.9VCC, SO=Open
					8	mA	f=66MHz **FHSCLK** =0.1VCC/0.9VCC, SO=Open
					4	mA	f=33MHz **FHSCLK** =0.1VCC/0.9VCC, SO=Open
ICC2	VCC Program Current (PP)	1			15	mA	Program in Progress **FHCS# =VCC**
ICC3	VCC Write Status Register (WRSR) Current				15	mA	Program status register in progress **FHCS# =VCC**
ICC4	VCC Sector Erase Current (SE)	1			15	mA	Erase in Progress **FHCS# =VCC**
ICC5	VCC Chip Erase Current (CE)	1			15	mA	Erase in Progress **FHCS# =VCC**
VIL	Input Low Voltage		-0.5		0.3VCC	V	
VIH	Input High Voltage		0.7VCC		VCC+0.4	V	
VOL	Output Low Voltage				0.4	V	IOL = 1.6mA
VOH	Output High Voltage		VCC-0.2			V	IOH = -100uA

Notes :
1. Typical values at VCC = 3.3V, T = 25°C. These currents are valid for all product versions (package and speeds).
2. Typical value is calculated by simulation.

Table 6. AC CHARACTERISTICS (Temperature = -40°C to 85°C for Industrial grade, Temperature = 0°C to 70°C for Commercial grade, VCC = 2.7V ~ 3.6V)

Symbol	Alt.	Parameter		Min.	Typ.	Max.	Unit
fSCLK	fC	Clock Frequency for the following instructions: FAST_READ, PP, SE, BE, CE, DP, RES,RDP WREN, WRDI, RDID, RDSR, WRSR		1KHz		70 & 86 (Condition:15pF) 66 (Condition:30pF)	MHz MHz
fRSCLK	fR	Clock Frequency for READ instructions		1KHz		33	MHz
tCH(1)	tCLH	Clock High Time		7			ns
tCL(1)	tCLL	Clock Low Time		7			ns
tCLCH(2)		Clock Rise Time (3) (peak to peak)		0.1			V/ns
tCHCL(2)		Clock Fall Time (3) (peak to peak)		0.1			V/ns
tSLCH	tCSS	**FHCS# Active Setup Time (relative to FHSCLK)**		5			ns
tCHSL		**FHCS# Not Active Hold Time (relative to FHSCLK)**		5			ns
tDVCH	tDSU	Data In Setup Time		2			ns
tCHDX	tDH	Data In Hold Time		5			ns
tCHSH		**FHCS# Active Hold Time (relative to FHSCLK)**		5			ns
tSHCH		**FHCS# Not Active Setup Time (relative to FHSCLK)**		5			ns
tSHSL	tCSH	**FHCS# Deselect Time**		100			ns
tSHQZ(2)	tDIS	Output Disable Time				6	ns
tCLQV	tV	Clock Low to Output Valid	@33MHz 30pF			8	ns
			@86MHz/70MHz 15pF or @66MHz 30pF			6	ns
tCLQX	tHO	Output Hold Time		0			ns
tHLCH		**$\overline{\text{FHHOLD}}$ Setup Time (relative to FHSCLK)**		5			ns
tCHHH		**$\overline{\text{FHHOLD}}$ Hold Time (relative to FHSCLK)**		5			ns
tHHCH		**$\overline{\text{FHHOLD}}$ Setup Time (relative to FHSCLK)**		5			ns
tCHHL		**$\overline{\text{FHHOLD}}$ Hold Time (relative to FHSCLK)**		5			ns
tHHQX(2)	tLZ	**$\overline{\text{FHHOLD}}$ to Output Low-Z**				6	ns
tHLQZ(2)	tHZ	**$\overline{\text{FHHOLD}}$ to Output High-Z**				6	ns
tWHSL(4)		Write Protect Setup Time		20			ns
tSHWL(4)		Write Protect Hold Time		100			ns
tDP(2)		**FHCS# High to Deep Power-down Mode**				3	us
tRES1(2)		**FHCS# High to Standby Mode without Electronic Signature Read**				3	us
tRES2(2)		**FHCS# High to Standby Mode with Electronic Signature Read**				1.8	us
tW		Write Status Register Cycle Time			5	15	ms
tPP		Page Program Cycle Time			1.4	5	ms
tSE		Sector Erase Cycle Time			60	120	ms
tBE		Block Erase Cycle Time			1	2	s
tCE		Chip Erase Cycle Time			7	15	s

Note:
1. tCH + tCL must be greater than or equal to 1/ fC
2. Value guaranteed by characterization, not 100% tested in production.
3. Expressed as a slew-rate.
4. Only applicable as a constraint for a WRSR instruction when SRWD is set at 1.
5. Test condition is shown as Figure 11.

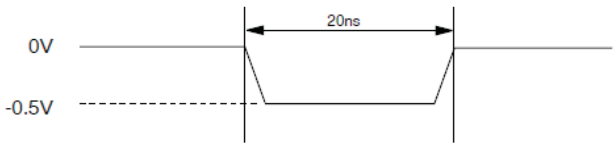
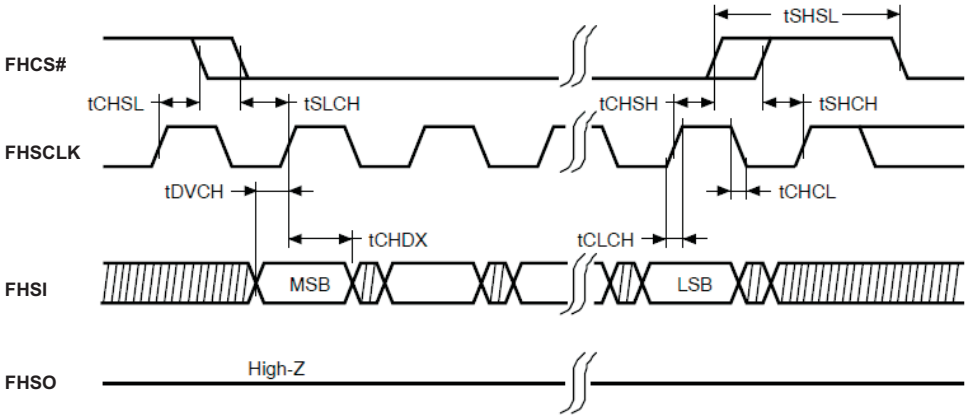
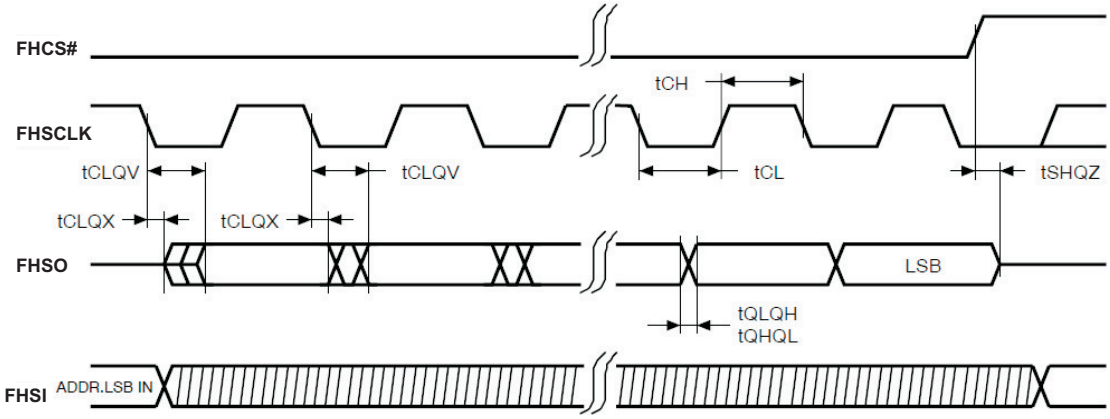


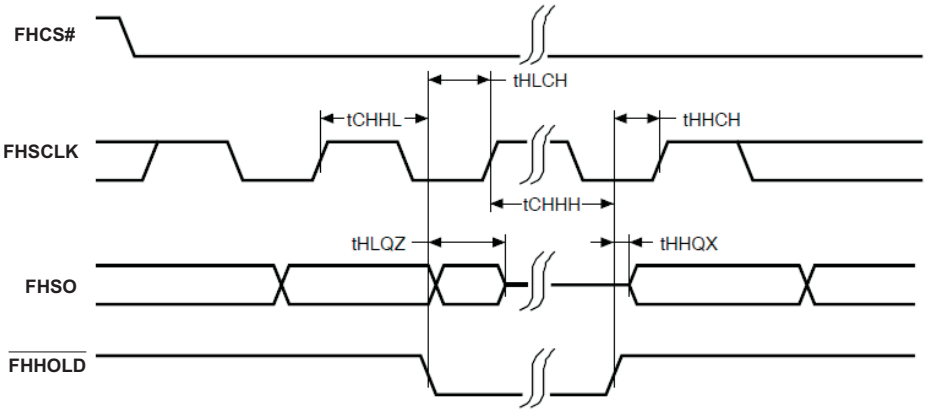
Figure 11. Maximum Negative Overshoot Waveform



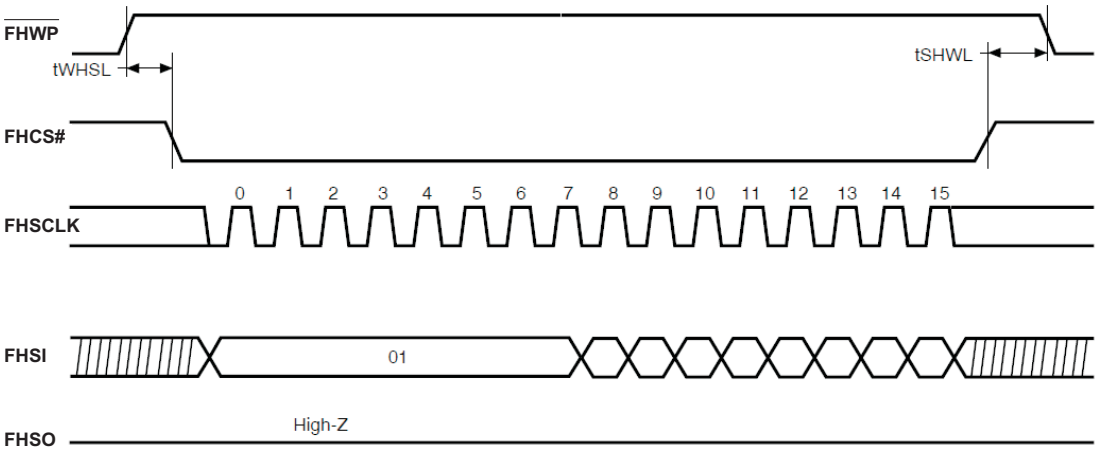
Serial Input Timing



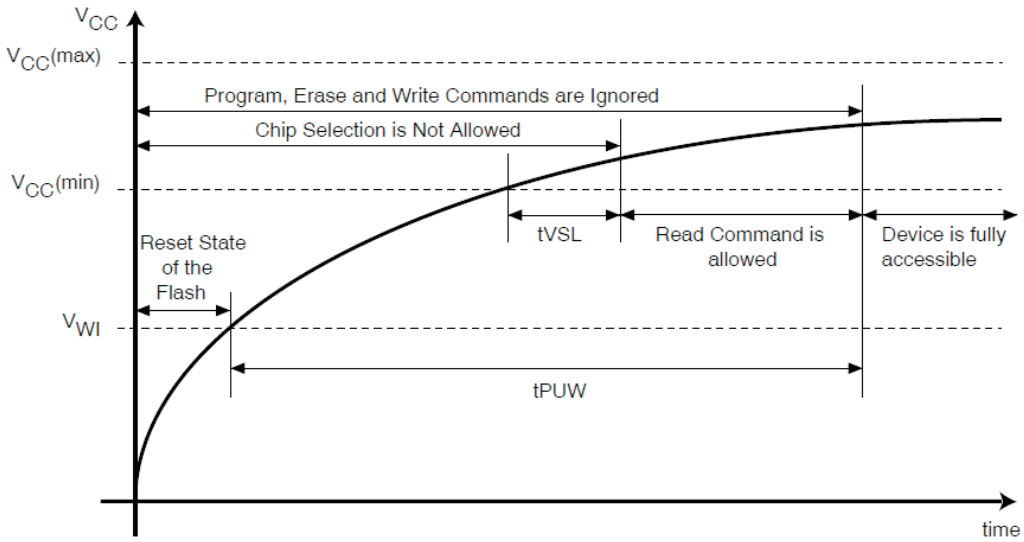
Output Timing



Hold Timing



$\overline{\text{FHWP}}$ Disable Setup and Hold Timing during WRSR when SRWD=1



Power-up Timing

Recommended Operating Conditions

At Device Power-Up

AC timing illustrated in Figure 12 is recommended for the supply voltages and the control signals at device power-up. If the timing in the figure is ignored, the device may not operate correctly.

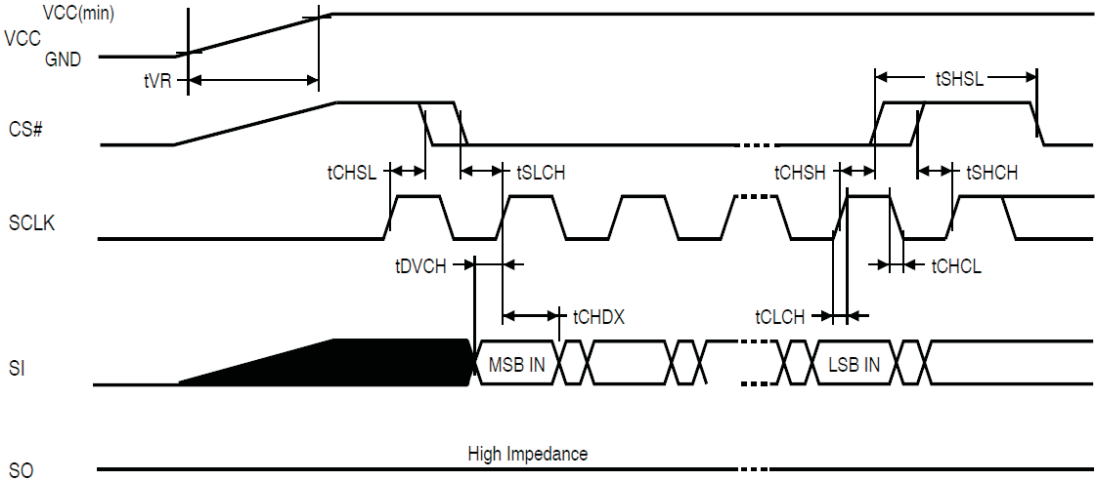


Figure 12. AC Timing at Device Power-Up

Symbol	Parameter	Notes	Min.	Max.	Unit
tVR	VCC Rise Time	1	0.5	500000	us/V

Notes :
1. Sampled, not 100% tested.
2. For AC spec tCHSL, tSLCH, tDVCH, tCHDX, tSHSL, tCHSH, tSHCH, tCHCL, tCLCH in the figure, please refer to "AC CHARACTERISTICS" table.

HT82A6208 Internal Flash Memory

Symbol	Parameter	Notes	Min.	Max.	Unit
tVR	VCC Rise Time	1	20	500000	us/V

Notes :
1. Sampled, not 100% tested.
2. For AC spec tCHSL, tSLCH, tDVCH, tCHDX, tSHSL, tCHSH, tSHCH, tCHCL, tCLCH in the figure, please refer to "AC CHARACTERISTICS" table.

HT82A6216 Internal Flash Memory

Erase and Programming Performance

PARAMETER	Min.	TYP. (1)	Max. (2)	UNIT
Write Status Register Cycle Time		5	15	ms
Sector erase Time		60	120	ms
Block erase Time		1	2	s
Chip Erase Time		7	15	s
Page Program Time		1.4	5	ms
Erase/Program Cycle	100,000			cycles

Note:
1. Typical program and erase time assumes the following conditions: 25°C, 3.3V, and checker board pattern.
2. Under worst conditions of 70°C and 3.0V.
3. System-level overhead is the time required to execute the first-bus-cycle sequence for the programming command.
4. The maximum chip programming time is evaluated under the worst conditions of 0C, VCC=3.0V, and 100K cycle with 90% confidence level.

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PARAMETER		Min.	TYP. (1)	Max. (2)	UNIT
Write Status Register Cycle Time			40	100	ms
Sector Erase Time			90	300	ms
Block Erase Time			0.7	2	s
Chip Erase Time	64Mb		50	80	s
	32Mb		25	50	s
	16Mb		14	30	s
Chip Erase Time (at ACC mode)	64Mb		30	48	s
	32Mb		15	30	s
	16Mb		8	18	s
Byte Program Time (via page program command)			9	300	us
Page Program Time			1.4	5	ms
Page Program Time (at ACC mode)			1.4	5	ms
Erase/Program Cycle			100,000		cycles

Note:
1. Typical program and erase time assumes the following conditions: 25°C, 3.3V, and checker board pattern.
2. Under worst conditions of 85°C and 2.7V.
3. System-level overhead is the time required to execute the first-bus-cycle sequence for the programming command.
4. Erase/Program cycles comply with JEDEC JESD-47E & A117A standard

HT82A6216 Internal Flash Memory

Input/Output Ports

Holtek microcontrollers offer considerable flexibility on their I/O ports. With the input or output designation of every pin fully under user program control, pull-high options for all ports and wake-up options on certain pins, the user is provided with an I/O structure to meet the needs of a wide range of application possibilities.

Depending upon which package is chosen, the microcontroller provides up to 32 bidirectional input/output lines labeled with port names PA, PB, PC and PD.

These registers are mapped to the Data Memory with an addresses as shown in the Special Purpose Data Memory table. For input operation, these ports are non-latching, which means the inputs must be ready at the T2 rising edge of instruction "MOV A,[m]", where m denotes the port address. For output operation, all the data is latched and remains unchanged until the output latch is rewritten.

Pull-high Resistors

Many product applications require pull-high resistors for their switch inputs usually requiring the use of an external resistor. To eliminate the need for these external resistors, I/O pins, when configured as an input have the capability of being connected to an internal pull-high resistor. The pull-high resistors are selectable via configuration options and are implemented using weak PMOS transistors. PA pins have bit select pull-high configuration options. Other ports have nibble select pull-high configuration options.

Port Pin Wake-up

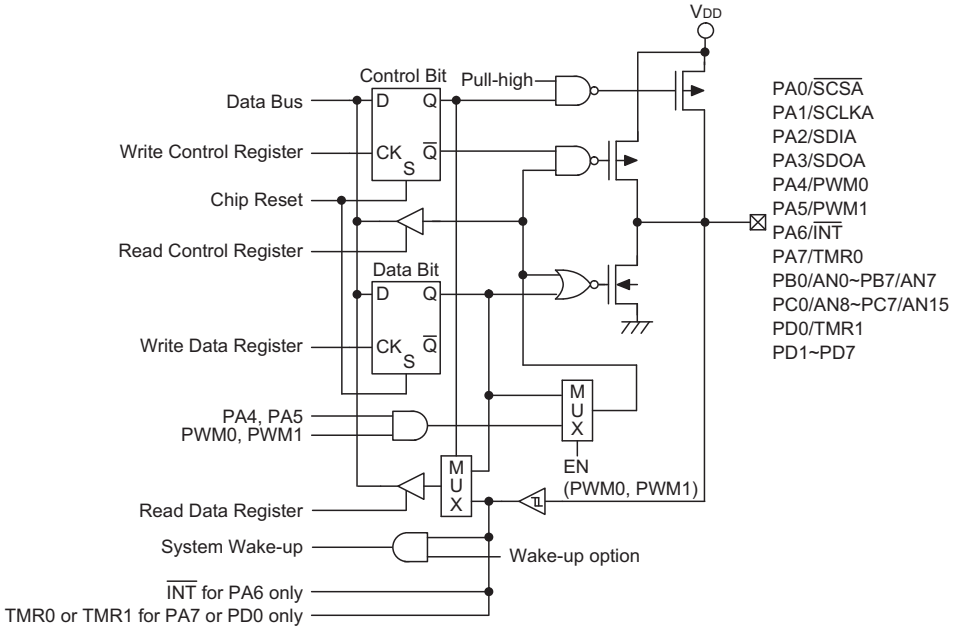
If the HALT instruction is executed, the device will enter the Power Down Mode, where the system clock will stop resulting in power being conserved, a feature that is important for battery and other low-power applications. Various methods exist to wake-up the microcontroller, one of which is to change the logic condition on one of the port pins from high to low. After a HALT instruction forces the microcontroller into entering the Power Down Mode, the processor will remain in a low-power state until the logic condition of the selected wake-up pin on the port pin changes from high to low. This function is especially suitable for applications that can be woken up via external switches.

PA pins have bit select wake-up configuration options. Other ports have nibble select wake-up configuration options. All wake up the MCU on a high to low transition. This means if the pin is low, the I/O cannot wake-up the MCU.

I/O Port Control Registers

Each I/O port has its own control register PAC, PBC, PCC and PDC, to control the input/output configuration. With this control register, each CMOS output or input with or without pull-high resistor structures can be reconfigured dynamically under software control. Each of the I/O ports is directly mapped to a bit in its associated port control register. Note that PA pins can be setup to have NMOS outputs using configuration options.

For the I/O pin to function as an input, the corresponding bit of the control register must be written as a "1". This



Input/Output Ports

will then allow the logic state of the input pin to be directly read by instructions. When the corresponding bit of the control register is written as a "0", the I/O pin will be setup as an output. If the pin is currently setup as an output, instructions can still be used to read the output register. However, it should be noted that the program will in fact only read the status of the output data latch and not the actual logic status of the output pin.

Port B VDDIO Function

The output drivers of most I/O pins use the VDD power supply line as their high voltage level. In this device pins PB0~PB6 can use a different voltage, other than VDD as their high level. This is supplied externally on pin PB7. This function is selected using configuration options.

Pin-shared Functions

The flexibility of the microcontroller range is greatly enhanced by the use of pins that have more than one function. Limited numbers of pins can force serious design constraints on designers but by supplying pins with multi-functions, many of these difficulties can be overcome. For some pins, the chosen function of the multi-function I/O pins is set by configuration options while for others the function is set by application program control.

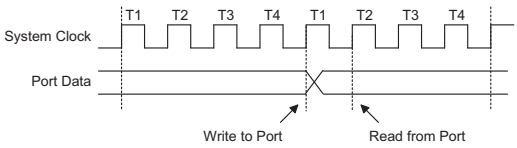
- External interrupt input
  The external interrupt pin $\overline{INT}$ is pin-shared with the I/O pin PA6. For applications not requiring an external interrupt input, the pin-shared external interrupt pin can be used as a normal I/O pin, however to do this, the external interrupt enable bits in the INTC0 register must be disabled.
- External Timer Clock Inputs
  The external timer pins TMR0 and TMR1 are pin-shared with I/O pins. To configure these pins to operate as timer inputs, the corresponding control bits in the timer control register must be correctly set. For applications that do not require external timer inputs, these pins can be used as normal I/O pins. Note that if used as normal I/O pins the timer mode control bits in the timer control register must select the timer mode, which has an internal clock source, to prevent the input pin from interfering with the timer operation.
- PWM outputs
  The device contains two PWM outputs which are pin-shared with I/O pins. The PWM output functions are chosen via configuration options and remain fixed after the device is programmed. Note that the corresponding bit of the port control register, PAC, must setup the pin as an output to enable the PWM output. If the PAC port control register has setup the pin as an input, then the pin will function as a normal logic input with the usual pull-high option, even if the PWM configuration option has been selected.
- A/D inputs
  These devices can have up to 16 A/D converter inputs depending upon which package type is chosen. All of these analog inputs are pin-shared with I/O pins on Port B and Port C. If these pins are to be used as A/D inputs and not as normal I/O pins then the corresponding bits in the A/D Converter Control Register, ADCR, must be properly set. There are no configuration options associated with the A/D function. If used as I/O pins, then full pull-high resistor configuration options remain, however if used as A/D inputs then any pull-high resistor options associated with these pins will be automatically disconnected.

I/O Pin Structures

The vast range of I/O functions and pin-shared options results in a huge variety of I/O pin structure types. For this reason the generic Input/Output Port diagram provided here is for general reference only. As the exact logical construction of the I/O pin will differ from the drawing, they are supplied as a guide only to assist with the functional understanding of the basic I/O pins.

Programming Considerations

Within the user program, one of the first things to consider is port initialisation. After a reset, all of the data and port control register will be set high. This means that all I/O pins will default to an input state, the level of which depends on the other connected circuitry and whether pull-high options have been selected. If the PAC, PBC, PCC and PDC port control register, are then programmed to setup some pins as outputs, these output pins will have an initial high output value unless the associated PA, PB, PC and PD port data registers are first programmed. Selecting which pins are inputs and which are outputs can be achieved byte-wide by loading the correct value into the port control register or by programming individual bits in the port control register using the "SET [m].i" and "CLR [m].i" instructions. Note that when using these bit control instructions, a read-modify-write operation takes place. The microcontroller must first read in the data on the entire port, modify it to the required new bit values and then rewrite this data back to the output ports.



Read/Write Timing

The ports have the additional capability of providing wake-up functions. When the device is in the Power Down Mode, various methods are available to wake the device up. One of these is a high to low transition of any of the port pins. Single or multiple pins on the ports can be setup to have this function.

Timer/Event Counters

The provision of timers form an important part of any microcontroller giving the designer a means of carrying out time related functions. The device contains two internal 16-bit count-up timer which has three operating modes. The timer can be configured to operate as a general timer, external event counter or as a pulse width measurement device. The provision of an internal 16-stage prescaler on one of the timers clock circuitry gives added range to the timer.

There are two types of registers related to the Timer/Event Counters. The first is the register that contain the actual value of the Timer/Event Counter and into which an initial value can be preloaded, and is known as TMR0H, TMR0L, TMR1H or TMR1L. Reading from this register retrieves the contents of the Timer/Event Counter. The second type of associated register is the Timer Control Register, which defines the timer options and determines how the Timer/Event Counter is to be used, and has the name TMR0C or TMR1C. This device can have the timer clocks configured to come from the internal clock sources. In addition, the timer clock sources can also be configured to come from the external timer pins.

Configuring the Timer/Event Counter Input Clock Source

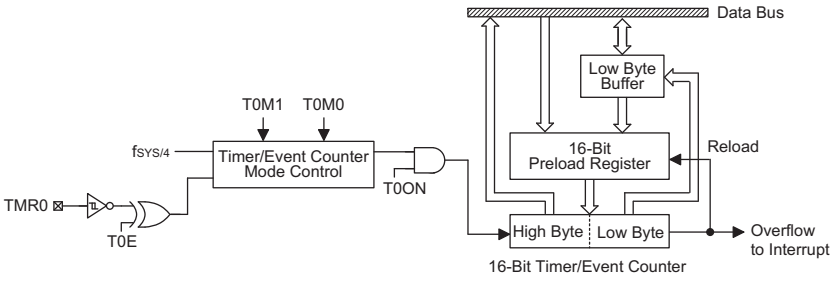
The internal timers clock source can originate from a choice of internal system clocks or from an external clock source. The system clock input timer source is used when the timer is in the timer mode or in the pulse width measurement mode.

The internal clock source of Timer1 passes trough a prescaler or can directly come from fsys/4 using bits T1S and T1PSS0/T1PSS1 in the MODE register. The prescaler clock source can come from either WDT OSC, RTC Oscillator or $f_{SYS}/4$. The prescaler value is conditioned by the bits PS1C0, PS1C1 and PS1C2 in the TMR1C register.

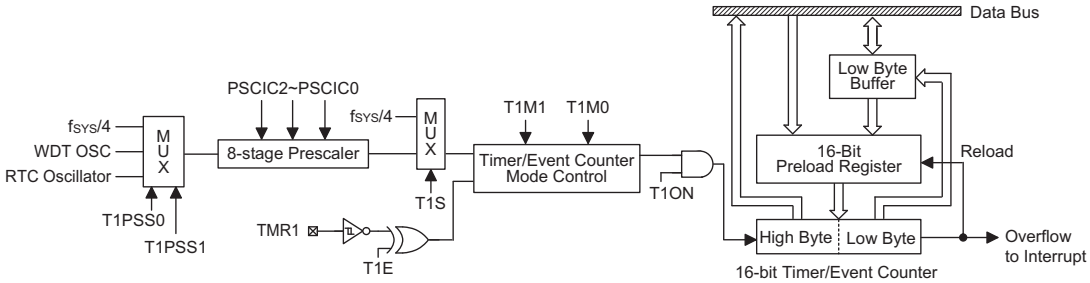
An external clock source is used when the timer is in the event counting mode, the clock source being provided on the shared TMR0 or TMR1 pin. Depending upon the condition of the T0E or T1E bit, each high to low, or low to high transition on the external timer pin will increment the counter by one.

Timer Register – TMR0H/TMR1H, TMR0L/TMR1L

The timer registers are special function registers located in the Special Purpose Data Memory and are the places where the actual timer values are stored. The timer registers are known as TMR0L, TMR0H, TMR1L and TMR1H. The value in the timer registers increases by one each time an internal clock pulse is received or an external transition occurs on the external timer pin. The timer will count from the initial value loaded by the preload register to the full count of FFFFH for the 16-bit timer at which point the timer overflows and an internal interrupt signal is generated. The timer value will then be reset with the initial preload register value and continue counting.



16-bit Timer/Event Counter 0 Structure



16-bit Timer/Event Counter 1 Structure

To achieve a maximum full range count of FFFFH, the preload registers must first be cleared to all zeros. It should be noted that after power-on, the preload register will be in an unknown condition. Note that if the Timer/Event Counter is switched off and data is written to its preload registers, this data will be immediately written into the actual timer registers. However, if the Timer/Event Counter is enabled and counting, any new data written into the preload data registers during this period will remain in the preload registers and will only be written into the timer registers the next time an overflow occurs.

For 16-bit Timer/Event Counters which have both low byte and high byte timer registers, accessing these registers is carried out in a specific way. It must be note when using instructions to preload data into the low byte timer register, namely TMR1L, the data will only be placed in a low byte buffer and not directly into the low byte timer register. The actual transfer of the data into the low byte timer register is only carried out when a write to its associated high byte timer register, namely TMR1H, is executed. On the other hand, using instructions to preload data into the high byte timer register will result in the data being directly written to the high byte timer register. At the same time the data in the low byte buffer will be transferred into its associated low byte timer register. For this reason, the low byte timer register should be written first when preloading data into the 16-bit timer registers. It must also be noted that to read the contents of the low byte timer register, a read to the high byte timer register must be executed first to latch the contents of the low byte timer register into its associated low byte buffer. After this has been done, the low byte timer register can be read in the normal way. Note that reading the low byte timer register will result in reading the previously latched contents of the low byte buffer and not the actual contents of the low byte timer register.

Timer Control Register – TMR0C/TMR1C

The flexible features of the Holtek microcontroller Timer/Event Counters enable them to operate in three different modes, the options of which are determined by the contents of the Timer Control Register TMR0C/TMR1C. Together with the TMR0L/TMR1L and TMR0H/TMR1H registers, these three registers control the full operation of the Timer/Event Counter. Before the timer can be used, it is essential that the TMR0C/TMR1C register is fully programmed with the right data to ensure its correct operation, a process that is normally carried out during program initialisation.

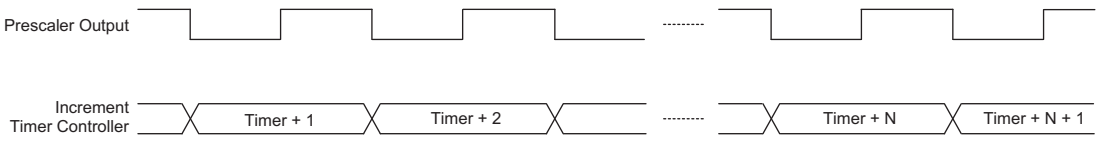
To choose which of the three modes the timer is to operate in, the timer mode, the event counting mode or the pulse width measurement mode, bits T0M0/T1M0 and T0M1/T1M1 must be set to the required logic levels. The timer-on bit T0ON/T1ON or bit 4 of the TMR0C/TMR1C register provides the basic on/off control of the timer, setting the bit high allows the counter to run, clearing the bit stops the counter. If the timer is in the event count or pulse width measurement mode the active transition edge level type is selected by the logic level of the T0E/T1E or bit 3 of the TMR0C/TMR1C register.

Configuring the Timer Mode

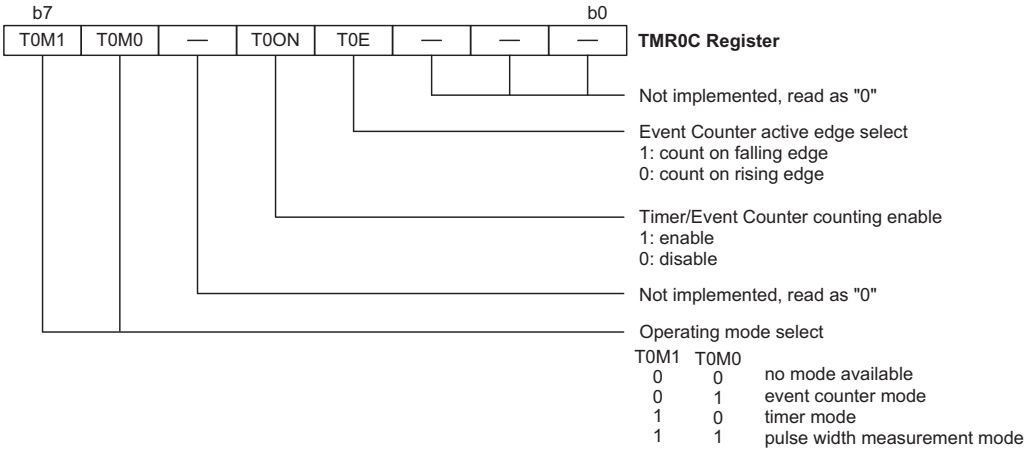
In this mode, the Timer/Event Counter can be utilised to measure fixed time intervals, providing an internal interrupt signal each time the Timer/Event Counter overflows. To operate in this mode, the Operating Mode Select bit pair, T0M1/T0M0 or T1M1/T1M0, in the Timer Control Register must be set to the correct value as shown.

Control Register Operating Mode Select Bits for the Timer Mode	Bit7	Bit6
	1	0

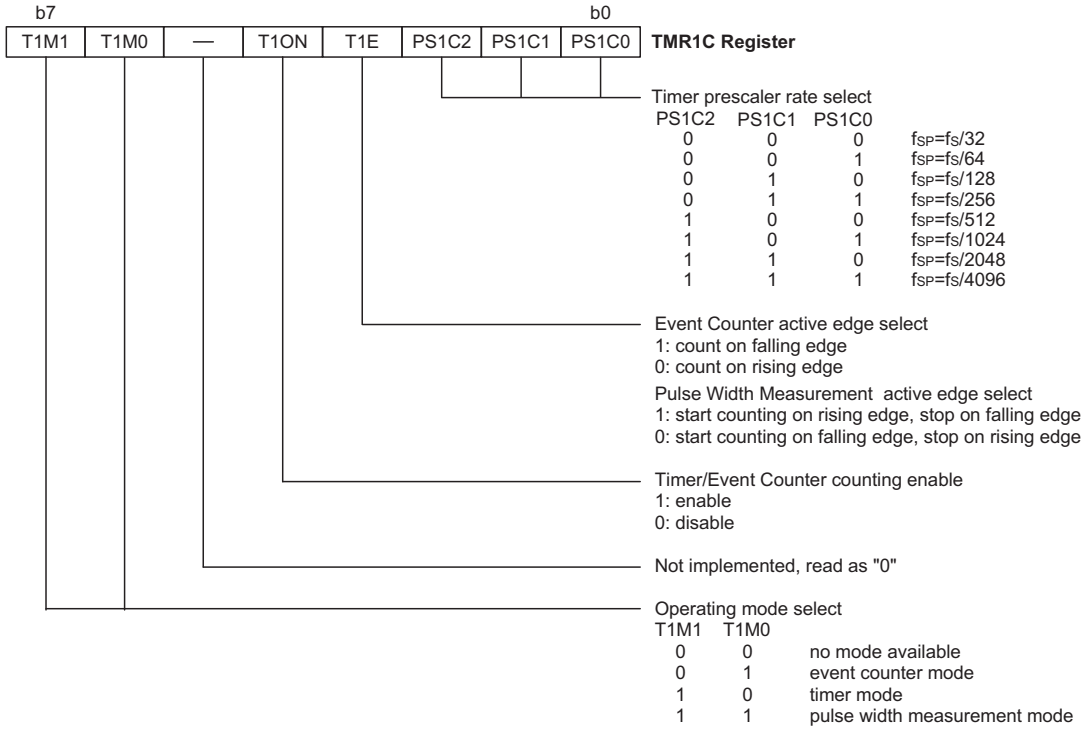
In this mode the internal clock, $f_{SYS}/4$ is used as the internal clock for the Timer/Event Counter. After the other bits in the Timer Control Register have been setup, the enable bit T0ON or T1ON, which is bit 4 of the Timer Control Register, can be set high to enable the Timer/Event Counter to run. Each time an internal clock cycle occurs, the Timer/Event Counter increments by one. When it is full and overflows, an interrupt signal is generated and the Timer/Event Counter will reload the value already loaded into the preload register and continue counting. The interrupt can be disabled by ensuring that the Timer/Event Counter Interrupt Enable bit in the Interrupt Control Register, INTC, is reset to zero.



Timer Mode Timing Chart



Timer/Event Counter 0 Control Register



Timer/Event Counter 1 Control Register

Configuring the Event Counter Mode

In this mode, a number of externally changing logic events, occurring on the external timer pin, can be recorded by the Timer/Event Counter. To operate in this mode, the Operating Mode Select bit pair, T0M1/T0M0 or T1M1/T1M0, in the Timer Control Register must be set to the correct value as shown.

Control Register Operating Mode Select Bits for the Event Counter Mode	Bit7	Bit6
	0	1

In this mode, the external timer pin, TMR0 or TMR1, is used as the Timer/Event Counter clock source, however it is not divided by the internal prescaler. After the other bits in the Timer Control Register have been setup, the enable bit T0ON or T1ON, which is bit 4 of the Timer Control Register, can be set high to enable the Timer/Event Counter to run. If the Active Edge Select bit T0E or T1E, which is bit 3 of the Timer Control Register, is low, the Timer/Event Counter will increment each time the external timer pin receives a low to high transition. If the Active Edge Select bit is high, the counter will increment each time the external timer pin receives a high to low transition. When it is full and overflows, an interrupt signal is generated and the Timer/Event Counter will reload the value already loaded into the preload register and continue counting. The interrupt can be disabled by ensuring that the Timer/Event Counter Interrupt Enable bit in the Interrupt Control Register, INTC, is reset to zero.

As the external timer pin is an independent pin and not shared with an I/O pin, the only thing to ensure the timer operate as an event counter is to ensure that the Operating Mode Select bits in the Timer Control Register place the Timer/Event Counter in the Event Counting Mode. It should be noted that in the event counting mode, even if the microcontroller is in the Power Down Mode, the Timer/Event Counter will continue to record externally changing logic events on the timer input pin. As a result when the timer overflows it will generate a timer interrupt and corresponding wake-up source.

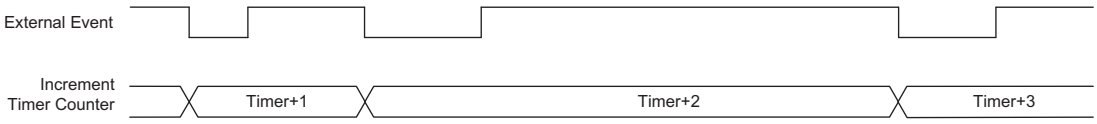
Configuring the Pulse Width Measurement Mode

In this mode, the Timer/Event Counter can be utilised to measure the width of external pulses applied to the external timer pin. To operate in this mode, the Operating Mode Select bit pair, T0M1/T0M0 or T1M1/T1M0, in the Timer Control Register must be set to the correct value as shown.

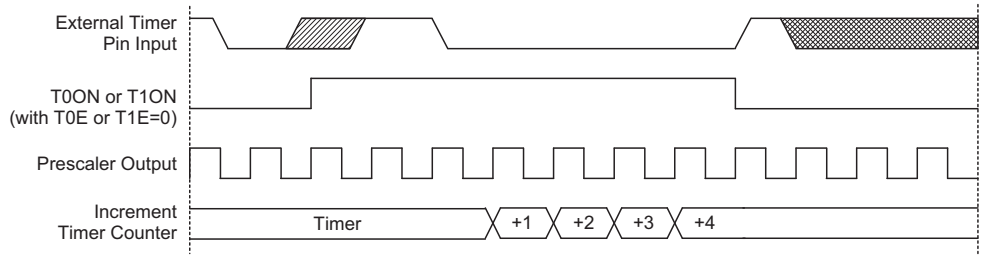
Control Register Operating Mode Select Bits for the Pulse Width Measurement Mode	Bit7	Bit6
	1	1

In this mode the internal clock, $f_{SYS}/4$ is used as the internal clock for the 16-bit Timer/Event Counter 0. The T1S and T1PSS0/T1PSS1 bits select the internal clock for the 16-bit Timer/Event Counter 1. After the other bits in the Timer Control Register have been setup, the enable bit T0ON or T1ON, which is bit 4 of the Timer Control Register, can be set high to enable the Timer/Event Counter, however it will not actually start counting until an active edge is received on the external timer pin.

If the Active Edge Select bit T0E or T1E, which is bit 3 of the Timer Control Register, is low, once a high to low transition has been received on the external timer pin, TMR0 or TMR1, the Timer/Event Counter will start counting until the external timer pin returns to its original high level. At this point the enable bit will be automatically reset to zero and the Timer/Event Counter will stop counting. If the Active Edge Select bit is high, the Timer/Event Counter will begin counting once a low to high transition has been received on the external timer pin and stop counting when the external timer pin returns to its original low level. As before, the enable bit will be automatically reset to zero and the Timer/Event Counter will stop counting. It is important to note that in the Pulse Width Measurement Mode, the enable bit is



Event Counter Mode Timing Chart



Prescaler Output is sampled at every falling edge of T1.

Pulse Width Measure Mode Timing Chart

automatically reset to zero when the external control signal on the external timer pin returns to its original level, whereas in the other two modes the enable bit can only be reset to zero under program control.

The residual value in the Timer/Event Counter, which can now be read by the program, therefore represents the length of the pulse received on the external timer pin. As the enable bit has now been reset, any further transitions on the external timer pin will be ignored. Not until the enable bit is again set high by the program can the timer begin further pulse width measurements. In this way, single shot pulse measurements can be easily made.

It should be noted that in this mode the Timer/Event Counter is controlled by logical transitions on the external timer pin and not by the logic level. When the Timer/Event Counter is full and overflows, an interrupt signal is generated and the Timer/Event Counter will reload the value already loaded into the preload register and continue counting. The interrupt can be disabled by ensuring that the Timer/Event Counter Interrupt Enable bit in the Interrupt Control Register, INTC, is reset to zero.

As the external timer pin is an independent pin and not shared with an I/O pin, the only thing to ensure the timer operate in Pulse Width Measurement mode is to ensure that the Operating Mode Select bits in the Timer Control Register place the Timer/Event Counter in the Pulse Width Measurement Mode.

Prescaler

Bits PS1C0~PS1C2 of the TMR1C register are used to define the pre-scaling stages of the internal clock source of the Timer/Event Counter 1.

I/O Interfacing

The Timer/Event Counter, when configured to run in the event counter or pulse width measurement mode, require the use of external pins for correct operation. As these pins are shared pins they must be configured correctly to ensure they are setup for use as Timer/Event Counter inputs and not as a normal I/O pins. This is implemented by ensuring that the mode select bits in the Timer/Event Counter control register, select either the event counter or pulse width measurement mode. Additionally the relevant Port Control Register for this pin must be set high to ensure that the pin is setup as an input. Any pull-high resistor configuration option on this pin will remain valid even if the pin is used as a Timer/Event Counter input.

Programming Considerations

When configured to run in the timer mode, the internal system clock is used as the timer clock source and is therefore synchronised with the overall operation of the microcontroller. In this mode when the appropriate timer register is full, the microcontroller will generate an internal interrupt signal directing the program flow to the respective internal interrupt vector. For the pulse width measurement mode, the internal system clock is also used as the timer clock source but the timer will only run when the correct logic condition appears on the external timer input pin. As this is an external event and not synchronised with the internal timer clock, the microcontroller will only see this external event when the next timer clock pulse arrives. As a result, there may be small differences in measured values requiring programmers to take this into account during programming. The same applies if the timer is configured to be in the event counting mode, which again is an external event and not synchronised with the internal system or timer clock.

When the Timer/Event Counter is read, or if data is written to the preload register, the clock is inhibited to avoid errors, however as this may result in a counting error, this should be taken into account by the programmer. Care must be taken to ensure that the timers are properly initialised before using them for the first time. The associated timer enable bits in the interrupt control register must be properly set otherwise the internal interrupt associated with the timer will remain inactive. The edge select, timer mode and clock source control bits in timer control register must also be correctly set to ensure the timer is properly configured for the required application. It is also important to ensure that an initial value is first loaded into the timer registers before the timer is switched on; this is because after power-on the initial values of the timer registers are unknown. After the timer has been initialised the timer can be turned on and off by controlling the enable bit in the timer control register. Note that setting the timer enable bit high to turn the timer on, should only be executed after the timer mode bits have been properly setup. Setting the timer enable bit high together with a mode bit modification, may lead to improper timer operation if executed as a single timer control register byte write instruction.

When the Timer/Event counter overflows, its corresponding interrupt request flag in the interrupt control register will be set. If the timer interrupt is enabled this will in turn generate an interrupt signal. However irrespective of whether the interrupts are enabled or not, a Timer/Event counter overflow will also generate a wake-up signal if the device is in a Power-down condition. This situation may occur if the Timer/Event Counter is in the Event Counting Mode and if the external signal continues to change state. In such a case, the Timer/Event Counter will continue to count these external events and if an overflow occurs the device will be woken up from its Power-down condition. To prevent such a wake-up from occurring, the timer interrupt request flag should first be set high before issuing the "HALT" instruction to enter the Power Down Mode.

Timer Program Example

This program example shows how the Timer/Event Counter registers are setup, along with how the interrupts are enabled and managed. Note how the Timer/Event Counter is turned on, by setting bit 4 of the Timer Control Register. The Timer/Event Counter can be turned off in a similar way by clearing the same bit. This example program sets the Timer/Event Counter to be in the timer mode, which uses the internal system clock as the clock source.

```
org 04h             ; USB interrupt vector
reti
org 0ch             ; Timer/Event Counter 0 interrupt vector
jmp tmrint          ; jump here when Timer overflows
:
org 20h             ; main program
;internal Timer/Event Counter 0 interrupt routine
tmrint:
:
; Timer/Event Counter main program placed here
:
reti
:
:
begin:
;setup Timer registers
mov a,09bh          ; setup Timer preload value
mov tmr0l,a;
Mov  a,0ffh         ; setup Timer preload value
Mov  trm0h,a
mov a,080h          ; setup Timer control register
mov tmr0c,a         ; timer mode
; setup interrupt register
mov a,009h          ; enable master interrupt and timer interrupt
mov intc0,a
set tmr0c.4         ; start Timer/Event Counter - note mode bits must be previously setup
```

Interrupts

Interrupts are an important part of any microcontroller system. When an external interrupt pin transition or an internal function such as a Timer/Event Counter overflow, an USB interrupt, or transmission or reception of SPI data occurs, their corresponding interrupt will enforce a temporary suspension of the main program allowing the microcontroller to direct attention to their respective needs. Each device contains two external interrupts and several internal interrupts functions. The external interrupt is controlled by the action of the external interrupt pins, while the internal interrupts are controlled by the Timer/Event Counter overflow, a USB interrupt and SPI data transmission or reception.

Interrupt Registers

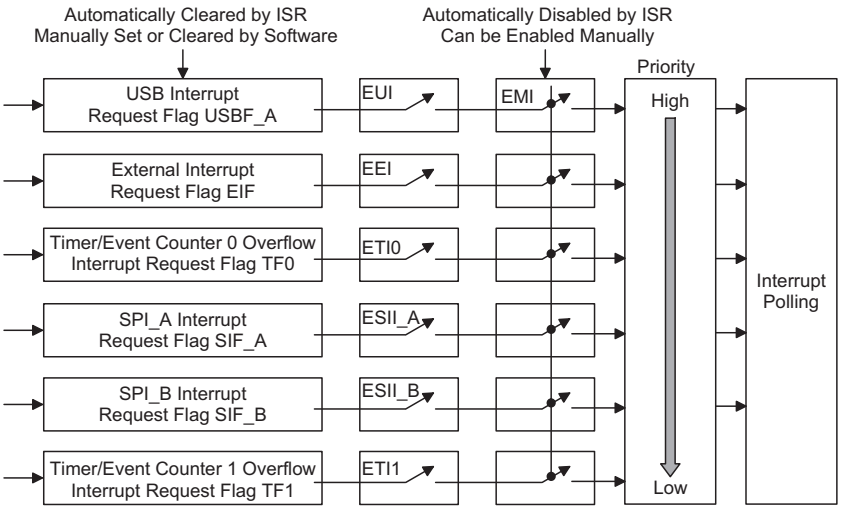
Overall interrupt control, which means interrupt enabling and request flag setting, is controlled by the two interrupt control registers, which are located in the Data Memory. By controlling the appropriate enable bits in these registers each individual interrupt can be enabled or disabled. Also when an interrupt occurs, the corresponding request flag will be set by the microcontroller. The global enable flag if cleared to zero will disable all interrupts.

Interrupt Operation

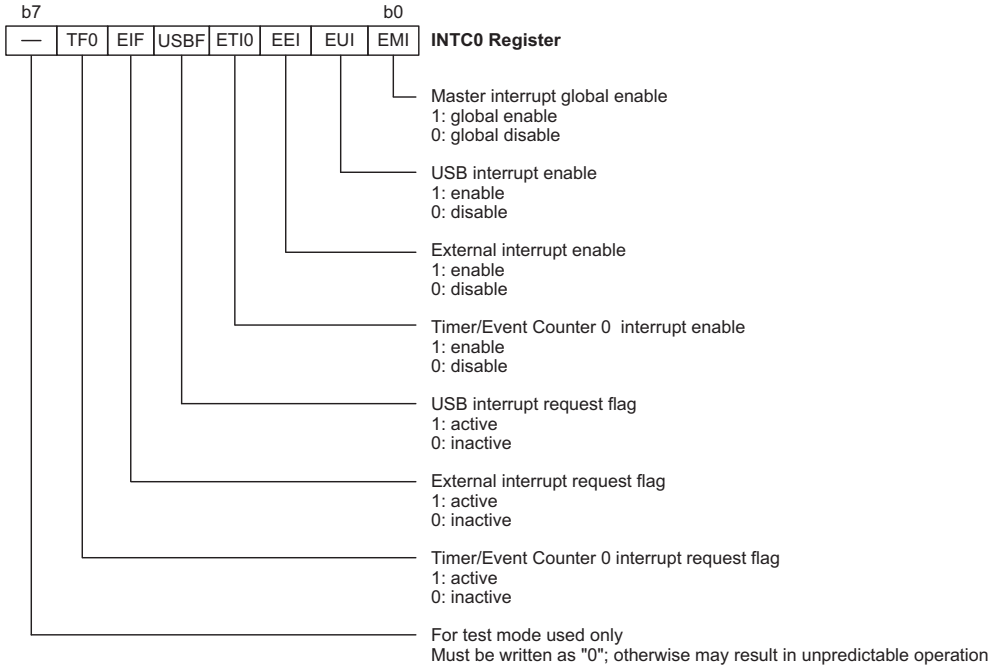
A USB interrupt , a Timer/Event Counter overflow, 8-bits of data transmission or reception on either of the SPI interfaces or an active edge on external interrupt pin will all generate an interrupt request by setting their corresponding request flag, if their appropriate interrupt enable bit is set. When this happens, the Program Counter, which stores the address of the next instruction to be executed, will be transferred onto the stack. The Program Counter will then be loaded with a new address which will be the value of the corresponding interrupt vector. The microcontroller will then fetch its next instruction from this interrupt vector. The instruction at this vector will usually be a JMP statement which will jump to another section of program which is known as the interrupt service routine. Here is located the code to control the appropriate interrupt. The interrupt service routine must be terminated with a RETI statement, which retrieves the original Program Counter address from the stack and allows the microcontroller to continue with normal execution at the point where the interrupt occurred.

The various interrupt enable bits, together with their associated request flags, are shown in the accompanying diagram with their order of priority.

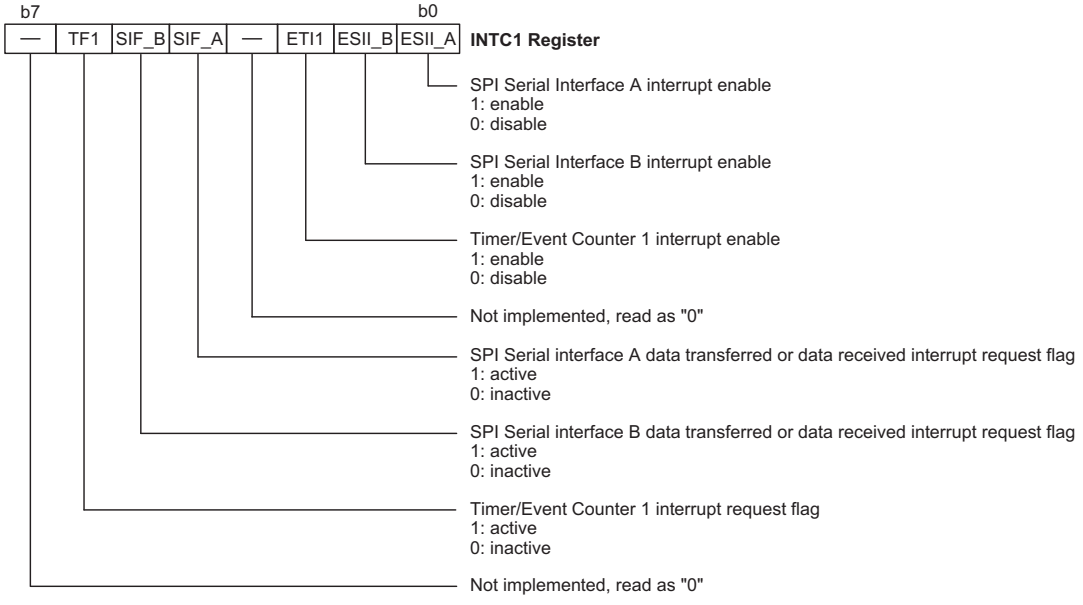
Once an interrupt subroutine is serviced, all the other interrupts will be blocked, as the EMI bit will be cleared automatically. This will prevent any further interrupt nesting from occurring. However, if other interrupt requests occur during this interval, although the interrupt will not be immediately serviced, the request flag will still be recorded. If an interrupt requires immediate servicing while the program is already in another interrupt service routine, the EMI bit should be set after entering the routine, to allow interrupt nesting. If the stack is full, the interrupt request will not be acknowledged, even if the related interrupt is enabled, until the Stack Pointer is decremented. If immediate service is desired, the stack must be prevented from becoming full.



Interrupt Structure



INTC0 Register



INTC1 Register

Interrupt Priority

Interrupts, occurring in the interval between the rising edges of two consecutive T2 pulses, will be serviced on the latter of the two T2 pulses, if the corresponding interrupts are enabled. In case of simultaneous requests, the following table shows the priority that is applied. These can be masked by resetting the EMI bit.

Interrupt Source	Priority	Vector
USB Interrupt	1	0004H
External Interrupt	2	0008H
Timer/Event Counter 0 Overflow Interrupt	3	000CH
SPI_A Interrupt	4	0010H
SPI_B Interrupt	5	0014H
Timer/Event Counter 1 Overflow Interrupt	6	0018H

Suitable masking of the individual interrupts using the interrupt registers can prevent simultaneous occurrences.

External Interrupt

For an external interrupt to occur, the global interrupt enable bit, EMI, and external interrupt enable bit, EEI, must first be set. An actual external interrupt will take place when the external interrupt request flag, EIF is set, a situation that will occur when a high to low transition appears on the interrupt pins. The external interrupt pin is pin-shared with the I/O pins PA6 can only be configured as an external interrupt pin if the corresponding external interrupt enable bits in the interrupt control register INTC0 have been set. The pins must also be setup as inputs by setting the corresponding PAC.6 bits in the port control register. When the interrupt is enabled, the stack is not full and a high to low transition appears on the external interrupt pin, a subroutine call to the external interrupt vector at location 08H will take place. When the interrupt is serviced, the external interrupt request flag, EIF will be automatically reset and the EMI bit will be automatically cleared to disable other interrupts. Note that any pull-high resistor configuration options on these pins will remain valid even if the pins are used as external interrupt inputs.

Timer/Event Counter Interrupt

For a Timer/Event Counter interrupt to occur, the global interrupt enable bit, EMI, and the corresponding timer interrupt enable bit, ETI0 or ETI1, must first be set. An actual Timer/Event Counter interrupt will take place when the Timer/Event Counter interrupt request flag, TF0 or TF1, is set, a situation that will occur when the Timer/Event Counter overflows. When the interrupt is enabled, the stack is not full and a Timer/Event Counter overflow occurs, a subroutine call to the timer interrupt vector at location 0CH or 018H, will take place. When the interrupt is serviced, the timer interrupt request flag, TF0 or TF1, will be automatically reset and the EMI bit will be automatically cleared to disable other interrupts.

SPI Interrupt

For an SPI Interrupt to occur, the global interrupt enable bit, EMI, and the corresponding SPI interrupt enable bit, ESII_A or ESII_B, must be first set. An actual SPI Interrupt will take place when one of the two SPI interrupt request flags, SIF_A or SIF_B, are set, a situation that will occur when 8-bits of data are transferred or received from either of the SPI interfaces. When the interrupt is enabled, the stack is not full and an SPI_A interrupt occurs, a subroutine call to the SPI_A interrupt vector at location 10H, will take place. For an SPI_B interrupt, a subroutine call to the SPI_B interrupt vector at location 14H, will take place. When the interrupt is serviced, the SPI interrupt request flag, SIF_A or SIF_B, will be automatically reset and the EMI bit will be automatically cleared to disable other interrupts.

USB Interrupt

A USB interrupts will be triggered by the following USB events, at which point the the related interrupt request flag, USBF in the INTC0 register, will be set.

- Accessing the corresponding USB FIFO from the PC
- A USB suspend signal from the PC
- A USB resume signal from the PC
- A USB Reset signal

When the interrupt is enabled, the stack is not full and the USB interrupt is active, a subroutine call to location 04H will occur. The interrupt request flag, USBF, and the EMI bit will be cleared to disable other interrupts.

When PC Host accesses the FIFO of the device, the corresponding request USR bit is set, and a USB interrupt is triggered. Therefore it can be determined which FIFO has been accessed. When the interrupt has been served, the corresponding bit should be cleared by the program. When the device receive a USB Suspend signal from the Host PC, the suspend line, bit0 of USC, is set and a USB interrupt is also triggered. Also when device receive a Resume signal from the Host PC, the resume line, bit3 of USC, is set and a USB interrupt is triggered.

Programming Considerations

By disabling the interrupt enable bits, a requested interrupt can be prevented from being serviced, however, once an interrupt request flag is set, it will remain in this condition in the interrupt control register until the corresponding interrupt is serviced or until the request flag is cleared by a software instruction.

It is recommended that programs do not use the "CALL subroutine" instruction within the interrupt subroutine. Interrupts often occur in an unpredictable manner or need to be serviced immediately in some applications. If only one stack is left and the interrupt is not well controlled, the original control sequence will be damaged once a "CALL subroutine" is executed in the interrupt subroutine.

All of these interrupts have the capability of waking up the processor when in the Power Down Mode.

Only the Program Counter is pushed onto the stack. If the contents of the accumulator or status register are altered by the interrupt service program, which may corrupt the desired control sequence, then the contents should be saved in advance.

Reset and Initialisation

A reset function is a fundamental part of any microcontroller ensuring that the device can be set to some predetermined condition irrespective of outside parameters. The most important reset condition is after power is first applied to the microcontroller. In this case, internal circuitry will ensure that the microcontroller, after a short delay, will be in a well defined state and ready to execute the first program instruction. After this power-on reset, certain important internal registers will be set to defined states before the program commences. One of these registers is the Program Counter, which will be reset to zero forcing the microcontroller to begin program execution from the lowest Program Memory address.

In addition to the power-on reset, situations may arise where it is necessary to forcefully apply a reset condition when the microcontroller is running. One example of this is where after power has been applied and the microcontroller is already running, the RES line is forcefully pulled low. In such a case, known as a normal operation reset, some of the microcontroller registers remain unchanged allowing the microcontroller to proceed with normal operation after the reset line is allowed to return high. Another type of reset is when the Watchdog Timer overflows and resets the microcontroller. All types of reset operations result in different register conditions being setup.

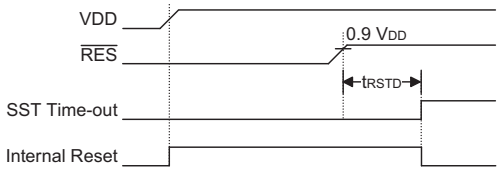
Another reset exists in the form of a Low Voltage Reset, LVR, where a full reset, similar to the RES reset is implemented in situations where the power supply voltage falls below a certain threshold.

Reset Functions

There are five ways in which a microcontroller reset can occur, through events occurring both internally and externally:

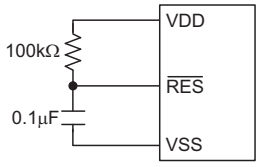
- Power-on Reset
  The most fundamental and unavoidable reset is the one that occurs after power is first applied to the microcontroller. As well as ensuring that the Program Memory begins execution from the first memory address, a power-on reset also ensures that certain other registers are preset to known conditions. All the I/O port and port control registers will power up in a high condition ensuring that all pins will be first set to inputs.

  Although the microcontroller has an internal RC reset function, if the VDD power supply rise time is not fast enough or does not stabilise quickly at power-on, the internal reset function may be incapable of providing a proper reset operation. In such cases it is recommended that an external RC network is connected to the $\overline{RES}$ pin, whose additional time delay will ensure that the $\overline{RES}$ pin remains low for an extended period to allow the power supply to stabilise. During this time delay, normal operation of the microcontroller will be inhibited. After the $\overline{RES}$ line reaches a certain voltage value, the reset delay time t_{RSTD} is invoked to provide an extra delay time after which the microcontroller will begin normal operation. The abbreviation SST in the figures stands for System Start-up Timer.



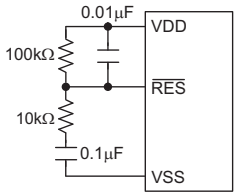
Power-On Reset Timing Chart

For most applications a resistor connected between VDD and the $\overline{RES}$ pin and a capacitor connected between VSS and the $\overline{RES}$ pin will provide a suitable external reset circuit. Any wiring connected to the $\overline{RES}$ pin should be kept as short as possible to minimise any stray noise interference.



Basic Reset Circuit

For applications that operate within an environment where more noise is present the Enhanced Reset Circuit shown is recommended.

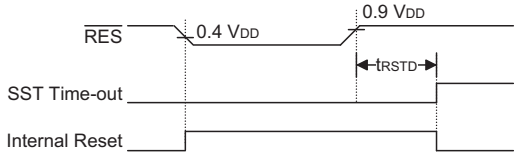


Enhanced Reset Circuit

More information regarding external reset circuits is located in Application Note HA0075E on the Holtek website.

- $\overline{RES}$ Pin Reset

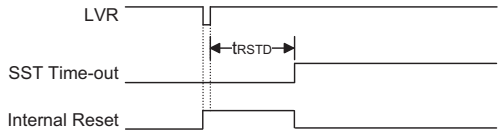
  This type of reset occurs when the microcontroller is already running and the $\overline{RES}$ pin is forcefully pulled low by external hardware such as an external switch. In this case as in the case of other reset, the Program Counter will reset to zero and program execution initiated from this point. Note that as the external reset pin is also pin-shared with PA7, if it is to be used as a reset pin, the correct reset configuration option must be selected.



$\overline{RES}$ Reset Timing Chart

- Low Voltage Reset – LVR

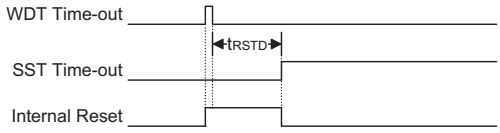
  The microcontroller contains a low voltage reset circuit in order to monitor the supply voltage of the device. The LVR function is selected via a configuration option. If the supply voltage of the device drops to within a range of 0.9V~V_{LVR} such as might occur when changing the battery, the LVR will automatically reset the device internally. For a valid LVR signal, a low supply voltage, i.e., a voltage in the range between 0.9V~V_{LVR} must exist for a time greater than that specified by t_{LVR} in the A.C. characteristics. If the low supply voltage state does not exceed this value, the LVR will ignore the low supply voltage and will not perform a reset function. The actual V_{LVR} value can be selected via configuration options.



Low Voltage Reset Timing Chart

- Watchdog Time-out Reset during Normal Operation

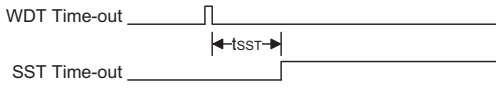
  The Watchdog time-out Reset during normal operation is the same as a hardware $\overline{RES}$ pin reset except that the Watchdog time-out flag TO will be set to "1".



WDT Time-out Reset during Normal Operation Timing Chart

- Watchdog Time-out Reset during Power Down

  The Watchdog time-out Reset during Power Down is a little different from other kinds of reset. Most of the conditions remain unchanged except that the Program Counter and the Stack Pointer will be cleared to "0" and the TO flag will be set to "1". Refer to the A.C. Characteristics for t_{SST} details.



WDT Time-out Reset during Power Down Timing Chart

Reset Initial Conditions

The different types of reset described affect the reset flags in different ways. These flags, known as PDF and TO are located in the status register and are controlled by various microcontroller operations, such as the Power Down function or Watchdog Timer. The reset flags are shown in the table:

TO	PDF	RESET Conditions
0	0	$\overline{RES}$ reset during power-on
0	0	$\overline{RES}$ wake-up during Power Down
0	0	$\overline{RES}$ or LVR reset during normal operation
1	u	WDT time-out reset during normal operation
1	1	WDT time-out reset during Power Down

Note: "u" stands for unchanged

The following table indicates the way in which the various components of the microcontroller are affected after a power-on reset occurs.

Item	Condition After RESET
Program Counter	Reset to zero
Interrupts	All interrupts will be disabled
WDT	Clear after reset, WDT begins counting
Timer/Event Counter	Timer Counter will be turned off
Prescaler	The Timer Counter Prescaler will be cleared
Input/Output Ports	I/O ports will be setup as inputs
Stack Pointer	Stack Pointer will point to the top of the stack

The different kinds of resets all affect the internal registers of the microcontroller in different ways. To ensure reliable continuation of normal program execution after a reset occurs, it is important to know what condition the microcontroller is in after a particular reset occurs. The following table describes how each type of reset affects the microcontroller internal registers.

Register	Reset (Power-on)	WDT Time-out (Normal Operation)	$\overline{RES}$ Reset (Normal Operation)	$\overline{RES}$ Reset (HALT)	WDT Time-out (HALT)*	USB Reset (Normal)	USB Reset (HALT)
MP0	xxxx xxxx	xxxx xxxx	xxxx xxxx	xxxx xxxx	uuuu uuuu	xxxx xxxx	xxxx xxxx
MP1	xxxx xxxx	xxxx xxxx	xxxx xxxx	xxxx xxxx	uuuu uuuu	xxxx xxxx	xxxx xxxx
ACC	xxxx xxxx	uuuu uuuu	uuuu uuuu	uuuu uuuu	uuuu uuuu	uuuu uuuu	uuuu uuuu
PCL	0000 0000	0000 0000	0000 0000	0000 0000	0000 0000	0000 0000	0000 0000
TBLP	xxxx xxxx	uuuu uuuu	uuuu uuuu	uuuu uuuu	uuuu uuuu	uuuu uuuu	uuuu uuuu
TBLH	xxxx xxxx	uuuu uuuu	uuuu uuuu	uuuu uuuu	uuuu uuuu	uuuu uuuu	uuuu uuuu
WDTS	---- -111	---- -111	---- -111	---- -111	---- -111	---- -111	---- -uuu
STATUS	--00 xxxx	--1u uuuu	--00 uuuu	--00 uuuu	--11 uuuu	--uu uuuu	--01 uuuu
INTC0	0000 0000	0000 0000	0000 0000	0000 0000	uuuu uuuu	0000 0000	0000 0000
TMR1H	xxxx xxxx	xxxx xxxx	xxxx xxxx	xxxx xxxx	uuuu uuuu	uuuu uuuu	uuuu uuuu
TMR1L	xxxx xxxx	xxxx xxxx	xxxx xxxx	xxxx xxxx	uuuu uuuu	uuuu uuuu	uuuu uuuu
TMR1C	00-0 1---	00-0 1---	00-0 1---	00-0 1---	uu-u u---	uu-u u---	uu-u u---
TMR0H	xxxx xxxx	xxxx xxxx	xxxx xxxx	xxxx xxxx	uuuu uuuu	xxxx xxxx	xxxx xxxx
TMR0L	xxxx xxxx	xxxx xxxx	xxxx xxxx	xxxx xxxx	uuuu uuuu	xxxx xxxx	xxxx xxxx
TMR0C	00-0 1---	00-0 1---	00-0 1---	00-0 1---	uu-u u---	uu-u u---	uu-u u---
PA	1111 1111	1111 1111	1111 1111	1111 1111	uuuu uuuu	1111 1111	1111 1111
PAC	1111 1111	1111 1111	1111 1111	1111 1111	uuuu uuuu	1111 1111	1111 1111
PB	1111 1111	1111 1111	1111 1111	1111 1111	uuuu uuuu	1111 1111	1111 1111
PBC	1111 1111	1111 1111	1111 1111	1111 1111	uuuu uuuu	1111 1111	1111 1111
PC	1111 1111	1111 1111	1111 1111	1111 1111	uuuu uuuu	1111 1111	1111 1111
PCC	1111 1111	1111 1111	1111 1111	1111 1111	uuuu uuuu	1111 1111	1111 1111
PD	1111 1111	1111 1111	1111 1111	1111 1111	uuuu uuuu	1111 1111	1111 1111
PDC	1111 1111	1111 1111	1111 1111	1111 1111	uuuu uuuu	1111 1111	1111 1111
USB_STAT	--xx 0000	--xx 0000	--xx 0000	--xx 0000	--xx 0000	--xx 0000	--xx 0000
UINT	0000 1111	0000 uuuu	0000 1111	0000 1111	0000 uuuu	0000 1111	0000 1111
INTC1	-000 -000	-000 -000	-000 -000	-000 -000	-uuu -uuu	-000 -000	-000 -000
TBHP	xxxx xxxx	uuuu uuuu	uuuu uuuu	uuuu uuuu	uuuu uuuu	uuuu uuuu	uuuu uuuu
USC	1000 0000	uuuu xuux	1000 0000	1000 0000	uuuu xuux	1uuu 0100	1uuu 0100
USR	---- 0000	---- uuuu	---- 0000	---- 0000	---- uuuu	---- 0000	---- 0000
UCC	0000 0000	uuuu uuuu	0000 0000	0000 0000	uuuu uuuu	0uu0 u000	0uu0 u000
AWR	0000 0000	uuuu uuuu	0000 0000	0000 0000	uuuu uuuu	0000 0000	0000 0000
STALL	---- 0000	---- uuuu	---- 0000	---- 0000	---- uuuu	---- 0000	---- 0000
SIES	00-0 0000	uu-x xuuu	00-0 0000	00-0 0000	uu-x uuuu	00-0 0000	00-0 0000
MISC	0000 0000	xxuu uuuu	0000 0000	0000 0000	xxuu uuuu	0000 0000	0000 0000
UFIEN	---- 0000	---- uuuu	---- 0000	---- 0000	---- uuuu	---- 0000	---- 0000
FIFO0	xxxx xxxx	xxxx xxxx	xxxx xxxx	xxxx xxxx	xxxx xxxx	xxxx xxxx	xxxx xxxx

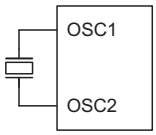
Register	Reset (Power-on)	WDT Time-out (Normal Operation)	$\overline{RES}$ Reset (Normal Operation)	$\overline{RES}$ Reset (HALT)	WDT Time-out (HALT)*	USB Reset (Normal)	USB Reset (HALT)
FIFO1	xxxx xxxx	xxxx xxxx	xxxx xxxx	xxxx xxxx	xxxx xxxx	xxxx xxxx	xxxx xxxx
FIFO2	xxxx xxxx	xxxx xxxx	xxxx xxxx	xxxx xxxx	xxxx xxxx	xxxx xxxx	xxxx xxxx
FIFO3	xxxx xxxx	xxxx xxxx	xxxx xxxx	xxxx xxxx	xxxx xxxx	xxxx xxxx	xxxx xxxx
UFOEN	---- 0000	---- uuuu	---- 0000	---- 0000	---- uuuu	---- 0000	---- 0000
UFC0	0000 0000	uuuu uuuu	0000 0000	0000 0000	uuuu uuuu	0000 0000	0000 0000
SBCRA	0110 0000	0110 0000	0110 0000	0110 0000	uuuu uuuu	uuuu uuuu	uuuu uuuu
SBDRA	uuuu uuuu	uuuu uuuu	uuuu uuuu	uuuu uuuu	uuuu uuuu	uuuu uuuu	uuuu uuuu
ADRL	xxxx ----	xxxx ----	xxxx ----	xxxx ----	uuuu ----	xxxx ----	xxxx ----
ADRH	xxxx xxxx	xxxx xxxx	xxxx xxxx	uuuu uuuu	uuuu uuuu	xxxx xxxx	xxxx xxxx
ADCR	0100 0000	0100 0000	0100 0000	0100 0000	uuuu uuuu	0100 0000	0100 0000
ACSR	0--- --00	0--- --00	0--- --00	---- --00	u--- --uu	1--- --00	---- --00
SBCRB	0110 0000	0110 0000	0110 0000	0110 0000	uuuu uuuu	uuuu uuuu	uuuu uuuu
SBDRB	uuuu uuuu	uuuu uuuu	uuuu uuuu	uuuu uuuu	uuuu uuuu	uuuu uuuu	uuuu uuuu
MODE	xxxx xxxx	xxxx xxxx	xxxx xxxx	xxxx xxxx	xxxx xxxx	xxxx xxxx	xxxx xxxx
SPI_REG	0000 0000	0000 0000	0000 0000	0000 0000	uuuu uuuu	0000 0000	0000 0000
PWMBR0	0000 0000	0000 0000	0000 0000	0000 0000	uuuu uuuu	0000 0000	0000 0000
PWM0DR	0000 0000	0000 0000	0000 0000	0000 0000	uuuu uuuu	0000 0000	0000 0000
PWMBR1	0000 0000	0000 0000	0000 0000	0000 0000	uuuu uuuu	0000 0000	0000 0000
PWM1DR	0000 0000	0000 0000	0000 0000	0000 0000	uuuu uuuu	0000 0000	0000 0000
PWMCTL	0000 0000	0000 0000	0000 0000	0000 0000	uuuu uuuu	0000 0000	0000 0000

Note: "*" means "warm reset", "-" not implemented
"u" means "unchanged", "x" means "unknown"

Oscillator

These devices provide two types of system oscillator circuits, an 6MHz or 12MHz crystal oscillator and a 32768Hz crystal oscillator, the choice of which is determined by software.

To use the 6MHz or 12MHz oscillator, a suitable crystal is connected between OSC1 and OSC2. It is a default option at IC power-on. The other oscillator circuit is designed for the real time clock. For this device, only a 32768Hz crystal oscillator can be used. The crystal should be connected between OSC3 and OSC4. This oscillator is designed for system clocks. The Power-down mode stops the system oscillator to conserve power.



Crystal Oscillator

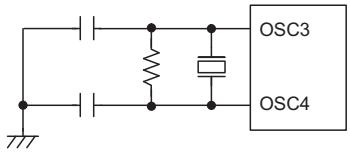
A crystal across OSC1 and OSC2 is needed to provide the feedback and phase shift required for the oscillator. No other external components are required. In stead of a crystal, a resonator can also be connected between OSC1 and OSC2 to get a frequency reference, but two external capacitors in OSC1 and OSC2 may be required.

The devices can operate only with 6MHz or 12MHz system clocks. In order to ensure that the USB SIE functions properly, users should correctly configure the SCLKSEL bit of the SCC Register. The default system clock is 12MHz.

RTC Oscillator

When the device enter a Power-down condition, the internal clocks are normally switched off to stop microcontroller activity and to conserve power. However, in many microcontroller applications it may be necessary to keep some internal functions operational, such as timers, even when the microcontroller is in the Power-down mode. To provide this feature, this device incorporates an RTC oscillator, which will remain active at all times, even when the microcontroller is in the power down condition. This clock source has a fixed frequency of 32768Hz and requires a 32768Hz crystal to be connected between pins OSC3 and OSC4.

The RTC oscillator circuit enable/disable is controlled by the F32K_dis bit in the MODE register. An additional bit F32K_CTRL enables the RTC oscillator to be powered up quickly.



Crystal/Ceramic Oscillator

Watchdog Timer Oscillator

The WDT oscillator is a fully self-contained free running on-chip RC oscillator with a typical period of 65μs at 5V requiring no external components. When the device enters the Power Down Mode, the system clock will stop running but the WDT oscillator continues to free-run and to keep the watchdog active. However, to preserve power in certain applications the WDT oscillator can be disabled via a configuration option.

Operation Mode

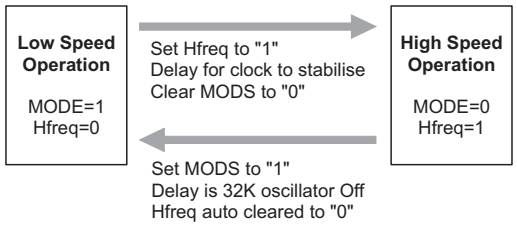
The device supports two system clocks: a high frequency system clock (6MHz, 12MHz) or a low system clock, 32768Hz. There is a single register that determines how to define which system mode is in operation. The system clock is changed as shown in the following procedure.

From high frequency to low frequency:

- Set MODS to ″1″
- Wait a delay time - 400ms if the 32K oscillator is off, no delay if the if the 32K oscillator is on
- The MCU will switch to the low frequency 32768Hz oscillator and turn-off the high frequency system clock

From low frequency to high frequency:

- Set Hfreq_en to ″1″ to turn-on the high frequency oscillator
- Wait a delay time to make sure that the high frequency oscillator is stable - 5ms
- Set MODS to ″0″
- The MCU will switch to the high frequency oscillator but the 32768Hz oscillator will continue to oscillate.



Mode Switching

Bit No.	Label	Function
0	MODS	High/Low frequency system clock select bit 0: High frequency system clock - 6MHz or 12MHz select - default 1: 32768Hz system clock select
1	Hfreq_en	1: Enable High frequency system clock, hardware will automatically clear this bit when MODS switches from low to high
2	F32K_dis	1: Disable 32768Hz oscillator - default enable 0: Enable 32768Hz oscillator
3	2.2LVD	1: V_{DD} < 2.2V 0: V_{DD} > 2.2V
4 5	T1PSS0 T1PSS1	Timer/Event Counter 1 clock source select 00: RTC (default) 01: $f_{SYS}/4$ 10: WDT OSC 11: no source
6	T1S	Timer/Event Counter 1 clock source select 0: $f_{SYS}/4$ (default) 1: Timer1 Prescaler output
7	F32K_ctrl	RTC oscillator quick start function 1: Quick start enabled 0: Quick start disabled - lower operating current This bit will set by the hardware during power on, once the 32K oscillator is stable the bit can be cleared by the application program to reduce power consumption.

MODE (40H) Register

Power Down Mode and Wake-up

Power Down Mode

All of the Holtek microcontrollers have the ability to enter a Power Down Mode. When the device enters this mode, the normal operating current, will be reduced to an extremely low standby current level. This occurs because when the device enters the Power Down Mode, the system oscillator is stopped which reduces the power consumption to extremely low levels, however, as the device maintains its present internal condition, it can be woken up at a later stage and continue running, without requiring a full reset. This feature is extremely important in application areas where the microcontroller must have its power supply constantly maintained to keep the device in a known condition but where the power supply capacity is limited such as in battery applications.

Entering the Power Down Mode

There is only one way for the device to enter the Power Down Mode and that is to execute the "HALT" instruction in the application program. When this instruction is executed, the following will occur:

- The system oscillator will stop running and the application program will stop at the "HALT" instruction.
- If the RTC oscillator configuration option is enabled then the RTC clock will keep running.
- The Data Memory contents and registers will maintain their present condition.
- The WDT will be cleared and resume counting if the WDT clock source is selected to come from the WDT or RTC oscillator. The WDT will stop if its clock source originates from the system clock.
- The I/O ports will maintain their present condition.
- In the status register, the Power Down flag, PDF, will be set and the Watchdog time-out flag, TO, will be cleared.

Standby Current Considerations

As the main reason for entering the Power Down Mode is to keep the current consumption of the microcontroller to as low a value as possible, perhaps only in the order of several micro-amps, there are other considerations which must also be taken into account by the circuit designer if the power consumption is to be minimised.

Special attention must be made to the I/O pins on the device. All high-impedance input pins must be connected to either a fixed high or low level as any floating input pins could create internal oscillations and result in increased current consumption. Care must also be taken with the loads, which are connected to I/O pins, which are setup as outputs. These should be placed in a condition in which minimum current is drawn or connected only to external circuits that do not draw current, such as other CMOS inputs.

If the configuration options have enabled the Watchdog Timer internal oscillator then this will continue to run when in the Power Down Mode and will thus consume some power. For power sensitive applications it may be therefore preferable to use the system clock source for the Watchdog Timer. If any I/O pins are configured as A/D analog inputs using the channel configuration bits in the ADCR register, then the A/D converter will be turned on and a certain amount of power will be consumed. It may be therefore desirable before entering te Power Down Mode to ensure that the A/D converter is powered down by ensuring that any A/D input pins are setup as normal logic inputs with pull-high resistors.

Wake-up

After the system enters the Power Down Mode, it can be woken up from one of various sources listed as follows:

- An external reset
- An external falling edge on any of the I/O pins
- A system interrupt
- A WDT overflow

If the system is woken up by an external reset, the device will experience a full system reset, however, if the device is woken up by a WDT overflow, a Watchdog Timer reset will be initiated. Although both of these wake-up methods will initiate a reset operation, the actual source of the wake-up can be determined by examining the TO and PDF flags. The PDF flag is cleared by a system power-up or executing the clear Watchdog Timer instructions and is set when executing the ″HALT″ instruction. The TO flag is set if a WDT time-out occurs, and causes a wake-up that only resets the Program Counter and Stack Pointer, the other flags remain in their original status.

Each pins on Port A or any nibble on the other ports can be setup via an individual configuration option to permit a negative transition on the pin to wake-up the system. When a Port pins wake-up occurs, the program will resume execution at the instruction following the ″HALT″ instruction.

If the system is woken up by an interrupt, then two possible situations may occur. The first is where the related interrupt is disabled or the interrupt is enabled but the stack is full, in which case the program will resume execution at the instruction following the ″HALT″ instruction. In this situation, the interrupt which woke-up the device will not be immediately serviced, but will rather be serviced later when the related interrupt is finally enabled or when a stack level becomes free. The other situation is where the related interrupt is enabled and the stack is not full, in which case the regular interrupt response takes place. If an interrupt request flag is set to ″1″ before entering the Power Down Mode, the wake-up function of the related interrupt will be disabled.

No matter what the source of the wake-up event is, once a wake-up situation occurs, a time period equal to 1024 system clock periods will be required before normal system operation resumes. However, if the wake-up has originated due to an interrupt, the actual interrupt subroutine execution will be delayed by an additional one or more cycles. If the wake-up results in the execution of the next instruction following the ″HALT″ instruction, this will be executed immediately after the 1024 system clock period delay has ended.

Low Voltage Detector – LVD

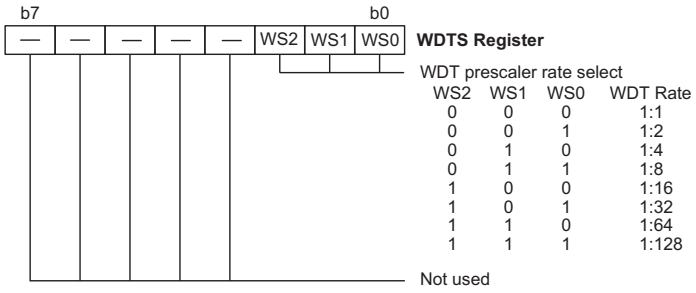
This Low Voltage Detect internal function provides a means for the user to monitor when the power supply voltage falls below a certain fixed level as specified in the DC characteristics. The LVD is enabled using a configuration option. Bit 3 of the MODE register is used to monitor the overall function of the LVD. Under normal operation, and when the power supply voltage is above the specified VLVD value in the DC characteristic section, the 2.2LVD bit will remain at a zero value. If the power supply voltage should fall below this VLVD value then the 2.2LVD bit will change to a high value indicating a low voltage condition. Note that the LVDO bit is a read-only bit. By polling the 2.2LVD bit in the MODE register, the application program can therefore determine the presence of a low voltage condition.

It is important not to confuse the LVD with the LVR function. In the LVR function an automatic reset will be generated by the microcontroller, whereas in the LVD function only the 2.2LVD bit will be affected with no influence on other microcontroller functions.

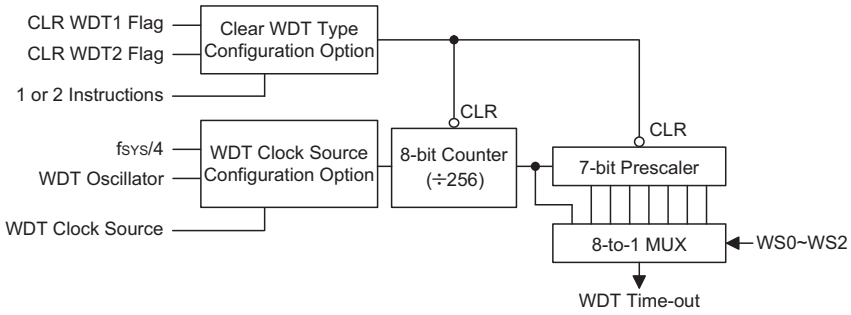
Watchdog Timer

The Watchdog Timer is provided to prevent program malfunctions or sequences from jumping to unknown locations, due to certain uncontrollable external events such as electrical noise. It operates by providing a device reset when the WDT counter overflows. The WDT clock is supplied by one of two sources selected by configuration option: its own self-contained dedicated internal WDT oscillator, or the instruction clock which is the system clock divided by 4. Note that if the WDT configuration option has been disabled, then any instruction relating to its operation will result in no operation.

The internal WDT oscillator has an approximate period of 32μs at a supply voltage of 5V. If selected, it is first divided by 256 via an 8-stage counter to give a nominal period of 8ms. Note that this period can vary with VDD, temperature and process variations. For longer WDT time-out periods the WDT prescaler can be utilized. By writing the required value to bits 0, 1 and 2 of the WDTS register, known as WS0, WS1 and WS2, longer time-out periods can be achieved. With WS0, WS1 and WS2 all



Watchdog Timer Register



Watchdog Timer

equal to ″1″, the division ratio is 1:128 which gives a maximum time-out period of about 1.0s.

A configuration option can select the instruction clock, which is the system clock divided by 4, as the WDT clock source instead of the internal WDT oscillator. If the instruction clock is used as the clock source, it must be noted that when the system enters the Power Down Mode, as the system clock is stopped, then the WDT clock source will also be stopped. Therefore the WDT will lose its protecting purposes. In such cases the system cannot be restarted by the WDT and can only be restarted using external signals. For systems that operate in noisy environments, using the internal WDT oscillator is therefore the recommended choice.

Under normal program operation, a WDT time-out will initialise a device reset and set the status bit TO. However, if the system is in the Power Down Mode, when a WDT time-out occurs, only the Program Counter and Stack Pointer will be reset. Three methods can be adopted to clear the contents of the WDT and the WDT prescaler. The first is an external hardware reset, which means a low level on the $\overline{RES}$ pin, the second is using the watchdog software instructions and the third is via a ″HALT″ instruction.

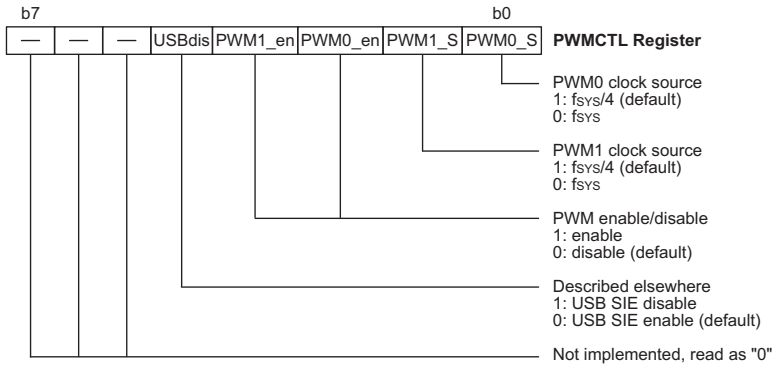
There are two methods of using software instructions to clear the Watchdog Timer, one of which must be chosen by configuration option. The first option is to use the single ″CLR WDT″ instruction while the second is to use the two commands ″CLR WDT1″ and ″CLR WDT2″. For the first option, a simple execution of ″CLR WDT″ will clear the WDT while for the second option, both ″CLR WDT1″ and ″CLR WDT2″ must both be executed to successfully clear the WDT. Note that for this second option, if ″CLR WDT1″ is used to clear the WDT, successive executions of this instruction will have no effect, only the execution of a ″CLR WDT2″ instruction will clear the WDT. Similarly, after the ″CLR WDT2″ instruction has been executed, only a successive ″CLR WDT1″ instruction can clear the Watchdog Timer.

Pulse Width Modulator

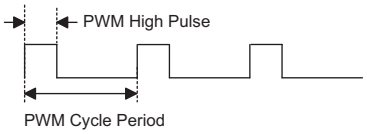
The device is provided with two Pulse Width Modulator, PWM, outputs. The internal PWM function within the device is useful for applications which require functions such as motor control, heating control, illumination control etc. By providing a signal of fixed frequency but of varying duty cycle on the PWM output pins, a square wave AC waveform can be generated with varying equivalent DC RMS values. As both the period and duty cycle of the PWM waveform can be controlled the choice of generated waveform is extremely flexible.

PWM Registers

There are a total of five registers to control the PWM function. Each PWM output has a pair of registers, one to control the waveform period, and another to control the duty cycle. The period control registers are known as PWMBR0 and PWMBR1 while the duty cycle registers have the name PWM0DR and PWM1DR. An addition register, the PWMCTL register, is the control register for both outputs and contains the output enable/disable bits and also select the PWM clock source to be either f_{SYS} or $f_{SYS}/4$.



Pulse Width Modulator Control Register



PWM Operation

The clock source for the PWM output is selected to be either f_{SYS} or $f_{SYS}/4$ using bits in the PWMCTL register. The period of the PWM waveform for each PWM output is setup by programming the required value into the PWMBR0 or PWMBR1 register using the following formula:

PWM waveform period = $256\times(1/f_{SYS})\times$(PWMBRn+1), or $256 \times (4/f_{SYS}) \times$ (PWMBRn+1) depending upon which clock source is selected.

For example if the system frequency is 6MHz, if $f_{SYS}/4$ is selected as the PWM source clock and a decimal value of 17 is in the PWMBRn register, then the PWM waveform will have a period of $\{256\times(4/(6\times10^{-6})\times18\}= 3072\mu s$ which is equivalent to a frequency of 0.325kHz.

The duty cycle for each PWM output can be by configured using the PWM0DR and PWM1DR registers. The value in these registers represents the ratio of the high to low pulse in each waveform period. Therefore the ratio of the high pulse to the low pulse, which is in fact just the duty cycle, is given by (PWMnDR+1)/256.

The PWM output can now be controlled using the enable/disable bits in the CTRL register. As the PWM outputs are pin shared with normal I/O pins they must first be setup as outputs for correct operation. When the PWM output is disabled using the enable/disable bit in the CTRL register it can still be used as a normal I/O pin.

Analog to Digital Converter

The need to interface to real world analog signals is a common requirement for many electronic systems. However, to properly process these signals by a microcontroller, they must first be converted into digital signals by A/D converters. By integrating the A/D conversion electronic circuitry into the microcontroller, the need for external components is reduced significantly with the corresponding follow-on benefits of lower costs and reduced component space requirements.

A/D Overview

The device contains a multi-channel channel analog to digital converter which can directly interface to external analog signals, such as that from sensors or other control signals and convert these signals directly into an 12-bit digital value. The number of available channels depends upon which package type is chosen.

Package	Channels	Resolution	Input Pins
28-pin	7	12-bit	PB4~PB7 PC5~PC7
32-pin	8	12-bit	PB0~PB7
44-pin	16	12-bit	PB0~PB7 PC0~PC7

The A/D block diagram shows the overall internal structure of the A/D converter, together with its associated registers.

A/D Converter Data Registers – ADRL, ADRH

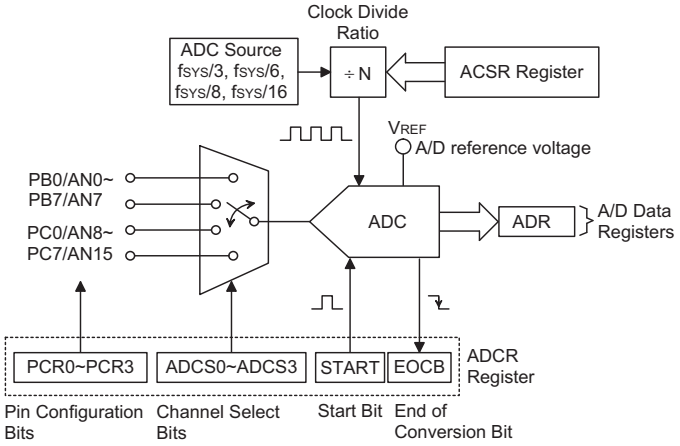
The devices, which contain a single12-bit A/D converter, require two data registers, known as ADRL and ADRH . After the conversion process takes place, these registers can be directly read by the microcontroller to obtain the digitised conversion value.

In the following tables, D0~D7 are the A/D conversion data result bits.

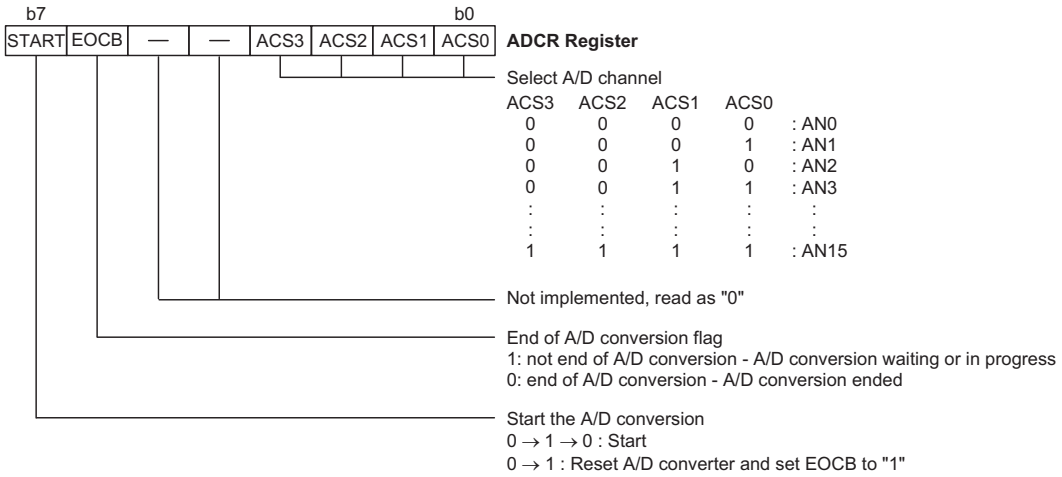
Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ADRL	D3	D2	D1	D0	—	—	—	—
ADRH	D11	D10	D9	D8	D7	D6	D5	D4

Note: D11~D0 is the A/D conversion result data bit MSB~LSB.

A/D Data Register



A/D Converter Structure



A/D Converter Control Register

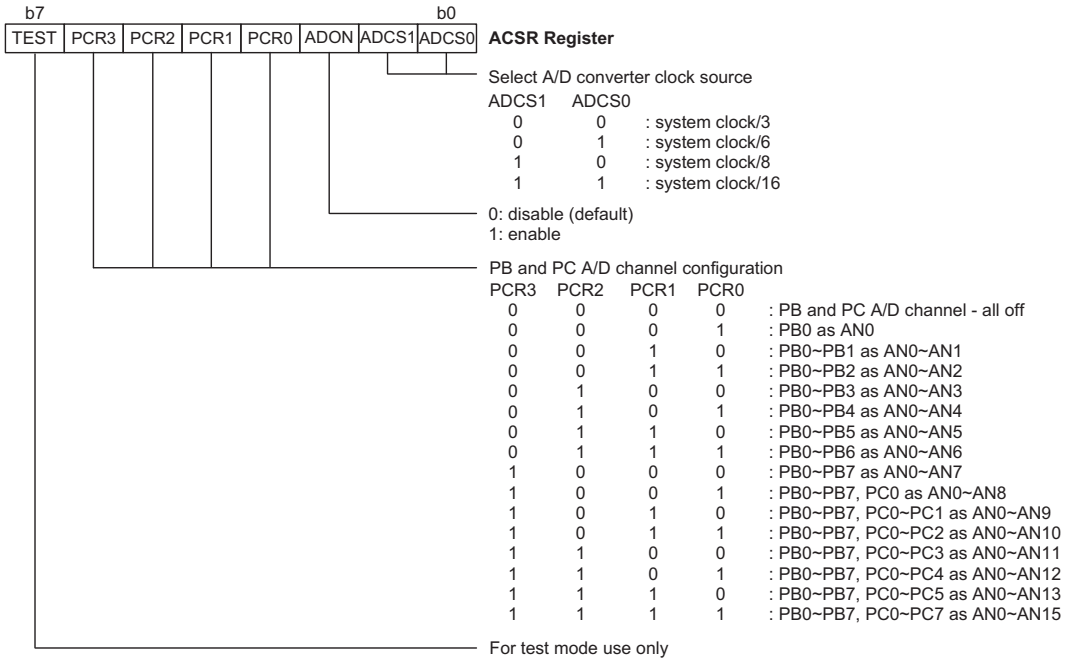
A/D Converter Control Register – ADCR

To control the function and operation of the A/D converter, control registers known as ADCR and ADSR are provided. These 8-bit registers define functions such as the selection of which analog channel is connected to the internal A/D converter, which pins are used as analog inputs and which are used as normal I/Os as well as controlling the start function and monitoring the A/D converter end of conversion status.

One section of this register contains the bits ACS3~ACS0 which define the channel number. As each of the devices contains only one actual analog to digital converter circuit, each of the individual analog inputs must be routed to the converter. It is the function of the ACS3~ACS0 bits in the ADCR register to determine which analog channel is actually connected to the internal A/D converter.

The START bit in the ADCR register is used to start and reset the A/D converter. When the microcontroller sets this bit from low to high and then low again, an analog to digital conversion cycle will be initiated. When the START bit is brought from low to high but not low again, the EOCB bit in the ADCR register will be set to a ″1″ and the analog to digital converter will be reset. It is the START bit that is used to control the overall on/off operation of the internal analog to digital converter.

The EOCB bit in the ADCR register is used to indicate when the analog to digital conversion process is complete. This bit will be automatically set to ″0″ by the microcontroller after a conversion cycle has ended. In addition, the corresponding A/D interrupt request flag will be set in the interrupt control register, and if the interrupts are enabled, an appropriate internal interrupt signal will be generated. This A/D internal interrupt signal will direct the program flow to the associated A/D internal interrupt address for processing. If the A/D internal interrupt is disabled, the microcontroller can be used to poll the EOCB bit in the ADCR register to check whether it has been cleared as an alternative method of detecting the end of an A/D conversion cycle.



A/D Converter Clock Source Register

A/D Converter Clock Source Register – ACSR

The clock source for the A/D converter, which originates from the system clock f_{SYS}, is first divided by a division ratio, the value of which is determined by the ADCS1 and ADCS0 bits in the ACSR register.

The ACSR control register also contains the PCR3~PCR0 bits which determine which pins on Port B and Port C are used as analog inputs for the A/D converter and which pins are to be used as normal I/O pins. If the 4-bit address on PCR3~PCR0 has a value of "1111" or higher, then all 16 pins, namely AN0~ AN15 will all be set as analog inputs. Note that if the PCR3~PCR0 bits are all set to zero, then all the Port B and Port C pins will be setup as normal I/Os and the internal A/D converter circuitry will be powered off to reduce the power consumption.

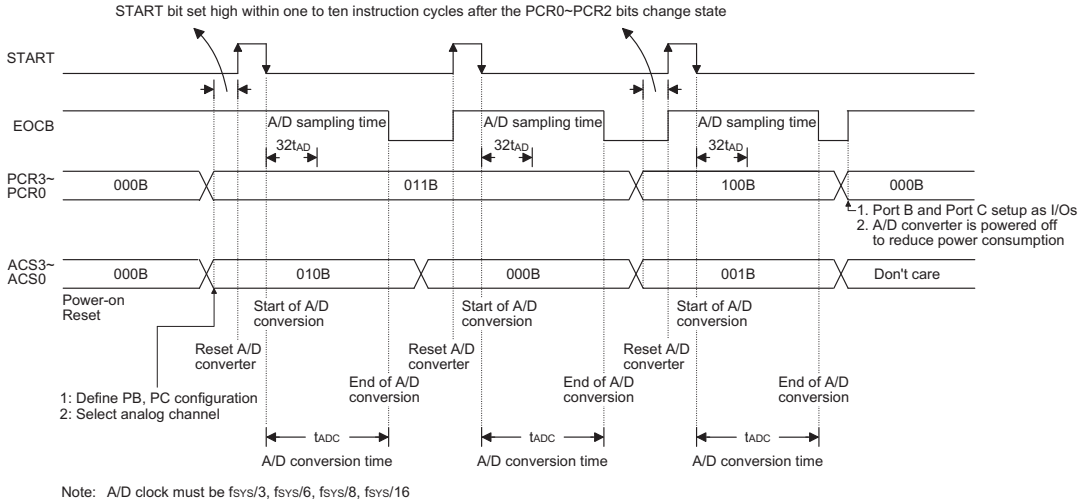
Although the A/D clock source is determined by the system clock f_{SYS}, and by bits ADCS1 and ADCS0, there are some limitations on the maximum A/D clock source speed that can be selected. As the minimum value of permissible A/D clock period, t_{AD}, is 0.5μs, care must be taken for system clock speeds in excess of 4MHz. For system clock speeds in excess of 4MHz, the ADCS1 and ADCS0 bits should not be set to "00". Doing so will give A/D clock periods that are less than the minimum A/D clock period which may result in inaccurate A/D conversion values. Refer to the following table for examples, where values marked with an asterisk * show where, depending upon the device, special care must be taken, as the values may be less than the specified minimum A/D Clock Period.

A/D Input Pins

All of the A/D analog input pins are pin-shared with the I/O pins on Port B and Port C. Bits PCR3~PCR0 in the ACSR register, not configuration options, determine whether the input pins are setup as normal Port B and Port C input/output pins or whether they are setup as analog inputs. In this way, pins can be changed under program control to change their function from normal I/O operation to analog inputs and vice versa. Pull-high resistors, which are setup through configuration options, apply to the input pins only when they are used as normal I/O pins, if setup as A/D inputs the pull-high resistors will be automatically disconnected. Note that it is not necessary to first setup the A/D pin as an input in the PBC or PCC port control register to enable the A/D input as when the PCR3~PCR0 bits enable an A/D input, the status of the port control register will be overridden.

Initialising the A/D Converter

The internal A/D converter must be initialised in a special way. Each time the Port B and Port C A/D channel selection bits are modified by the program, the A/D converter must be re-initialised. If the A/D converter is not initialised after the channel selection bits are changed, the EOCB flag may have an undefined value, which may produce a false end of conversion signal. To initialise the A/D converter after the channel selection bits have changed, then, within a time frame of one to ten instruction cycles, the START bit in the ADCR register must first be set high and then immediately cleared to zero. This will ensure that the EOCB flag is correctly set to a high condition.



A/D Conversion Timing

Summary of A/D Conversion Steps

The following summarises the individual steps that should be executed in order to implement an A/D conversion process.

- Step 1
  Select the required A/D conversion clock by correctly programming bits ADCS1 and ADCS0 in the ACSR register.
- Step 2
  Select which channel is to be connected to the internal A/D converter by correctly programming the ACS3~ ACS0 bits which are also contained in the ADCR register.
- Step 3
  Select which pins on Port B and Port C are to be used as A/D inputs and configure them as A/D input pins by correctly programming the PCR3~PCR0 bits in the ACSR register.
- Step 4
  If the interrupts are to be used, the interrupt control registers must be correctly configured to ensure the A/D converter interrupt function is active. The master interrupt control bit, EMI, in the INTC interrupt control register must be set to ″1″ and the A/D converter interrupt bit, EADI, in the INTC register must also be set to ″1″.
- Step 5
  The analog to digital conversion process can now be initialised by setting the START bit in the ADCR register from ″0″ to ″1″ and then to ″0″ again. Note that this bit should have been originally set to ″0″.
- Step 6
  To check when the analog to digital conversion process is complete, the EOCB bit in the ADCR register can be polled. The conversion process is complete when this bit goes low. When this occurs the A/D data registers ADR can be read to obtain the conversion value. As an alternative method if the interrupts are enabled and the stack is not full, the program can wait for an A/D interrupt to occur.

  Note: When checking for the end of the conversion process, if the method of polling the EOCB bit in the ADCR register is used, the interrupt enable step above can be omitted.

The A/D conversion timing diagram shows graphically the various stages involved in an analog to digital conversion process and its associated timing.

The setting up and operation of the A/D converter function is fully under the control of the application program as there are no configuration options associated with the A/D converter. After an A/D conversion process has been initiated by the application program, the microcontroller internal hardware will begin to carry out the conversion, during which time the program can continue with other functions. The time taken for the A/D conversion is $76t_{AD}$ where t_{AD} is equal to the A/D clock period.

Programming Considerations

When programming, special attention must be given to the A/D channel selection bits in the ADSR register. If these bits are all cleared to zero no external pins will be selected for use as A/D input pins allowing the pins to be used as normal I/O pins. When this happens the power supplied to the internal A/D circuitry will be reduced resulting in a reduction of supply current. This ability to reduce power by turning off the internal A/D function by clearing the A/D channel selection bits may be an important consideration in battery powered applications.

Another important programming consideration is that when the A/D channel selection bits change value, the A/D converter must be re-initialised. This is achieved by pulsing the START bit in the ADCR register immediately after the channel selection bits have changed state. The exception to this is where the channel selection bits are all cleared, in which case the A/D converter is not required to be re-initialised.

A/D Programming Example

The following two programming examples illustrate how to setup and implement an A/D conversion. In the first example, the method of polling the EOCB bit in the ADCR register is used to detect when the conversion cycle is complete, whereas in the second example, the A/D interrupt is used to determine when the conversion is complete.

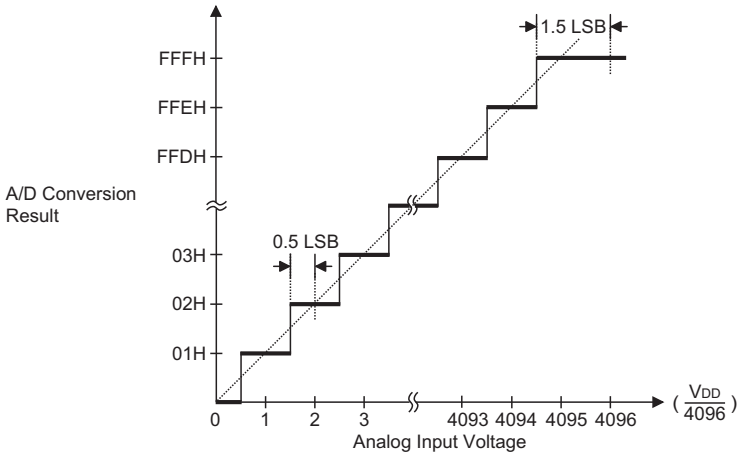
Example: using an EOCB polling method to detect the end of conversion

```
    clr  EADI                  ; disable ADC interrupt
    mov  a,00011001
    mov  acsr,a                ; setup the ACSR register to select fsys/6 as the A/D clock
                               ; setup the ACSR register to configure Port PB0~PB2 as A/D
                               ; Inputs
    mov  a,00000000
    mov  adcr,a                ; setup the ADCR register and select AN0 to be connected to
                               ; the A/D converter
                               ; As the Port B and Port C channel bits have changed the
                               ; following START signal (0→1→0) must be issued within
                               ; 10 instruction cycles
         :
Start_conversion:
    clr  START
    set  START                 ; reset A/D
    clr  START                 ; start A/D
Polling_:
    sz   EOCB                  ; poll the ADCR register EOCB bit to detect end
                               ; of A/D conversion
    jmp  polling_EOC           ; continue polling
    mov  a,ADR                 ; read conversion result value
    mov  adrl_buffer,a         ; save result to user defined register
         :
    jmp  start_conversion      ; start next A/D conversion
```

Example: using the interrupt method to detect the end of conversion

```
    clr  EADI                  ; disable ADC interrupt
    mov  a,00011001B
    mov  ACSR,a                ; setup the ACSR register to select fSYS/6 as the A/D clock

    mov  a,00000000B           ; setup ADCR register to configure Port PB0~PB2
                               ; as A/D inputs
    mov  ADCR,a                ; and select AN0 to be connected to the A/D
         :
                               ; As the Port B channel bits have changed the
                               ; following START signal(0→1→0) must be issued
                               ; within 10 instruction cycles
         :
Start_conversion:
    clr  START
    set  START                 ; reset A/D
    clr  START                 ; start A/D
    clr  ADF                   ; clear ADC interrupt request flag
    set  EADI                  ; enable ADC interrupt
    set  EMI                   ; enable global interrupt
         :
         :
         :
; ADC interrupt service routine
ADC_:
    mov  acc_stack,a           ; save ACC to user defined memory
         a,STATUS
    mov  status_stack,a        ; save STATUS to user defined memory
         :
         :
    mov  a,ADR                 ; read conversion result value
    mov  adrl_buffer,a         ; save result to user defined register
         :
         :
EXIT_INT_ISR:
    mov  a,status_stack
    mov  STATUS,a              ; restore STATUS from user defined memory
    mov  a,acc_stack           ; restore ACC from user defined memory
```



Ideal A/D Transfer Function

A/D Transfer Function

As the device contain a 12-bit A/D converter, its full-scale converted digitised value is equal to FFFH. Since the full-scale analog input value is equal to the VDD voltage, this gives a single bit analog input value of V_{DD}/4096. The diagram show the ideal transfer function between the analog input value and the digitised output value for the A/D converter.

Note that to reduce the quantisation error, a 2.5 LSB offset is added to the A/D Converter input. Except for the digitised zero value, the subsequent digitised values will change at a point 2.5 LSB below where they would change without the offset, and the last full scale digitised value will change at a point 2.5 LSB below the V_{DD} level.

SPI Serial Interface

The device includes two SPI Serial Interfaces. The SPI interface is a full duplex serial data link, originally designed by Motorola, which allows multiple devices connected to the same SPI bus to communicate with each other. The devices communicate using a master/slave technique where only the single master device can initiate a data transfer. A simple four line signal bus is used for all communication.

SPI Interface Communication

Four lines are used for each SPI function. These are, SDIA/B - Serial Data Input, SDOA/B - Serial Data Output, SCLKA/B - Serial Clock and $\overline{\text{SCSA/B}}$ - Slave Select. Note that the condition of the Slave Select line is conditioned by the CSENA/B bit in the SBCRA/B control register. If the CSENA/B bit is high then the $\overline{\text{SCSA/B}}$ line is active while if the bit is low then the $\overline{\text{SCSA/B}}$ line will be in a floating condition. The accompanying timing diagram depicts the basic timing protocol of the SPI bus.

SPI Registers

There are two registers for control of the SPI Interface. These are the SBCRA/B register which is the control register and the SBDRA/B which is the data register. The SBCRA/B register is used to setup the required setup parameters for the SPI bus and also used to store associated operating flags, while the SBDRA/B register is used for data storage.

After Power on, the contents of the SBDRA/B register will be in an unknown condition while the SBCRA/B register will default to the condition below:

CKSn	M1n	M0n	SBENn	MLSn	CSENn	WCOLn	TRFn
0	1	1	0	0	0	0	0

Note: ″n″ where n=A~B

Note that data written to the SBDRA/B register will only be written to the TXRX buffer, whereas data read from the SBDRA/B register will actual be read from the register.

SPI Bus Enable/Disable

To enable the SPI bus, the SBENA/B bit should be set high, then the SCLKA/B, SDIA/B, SDOA/B and $\overline{\text{SCSA/B}}$ lines should all be zero, then wait for data to be written to the SBDRA/B (TXRX buffer) register. For the Master Mode, after data has been written to the SBDRA/B (TXRX buffer) register then transmission or reception will start automatically. When all the data has been transferred, the TRFA/B bit should be set. For the Slave Mode, when clock pulses are received on SCLKA/B, data in the TXRX buffer will be shifted out or data on SDIA/B will be shifted in.

To Disable the SPI bus SCLKA/B, SDIA/B, SDOA/B, $\overline{\text{SCSA/B}}$ should be floating.

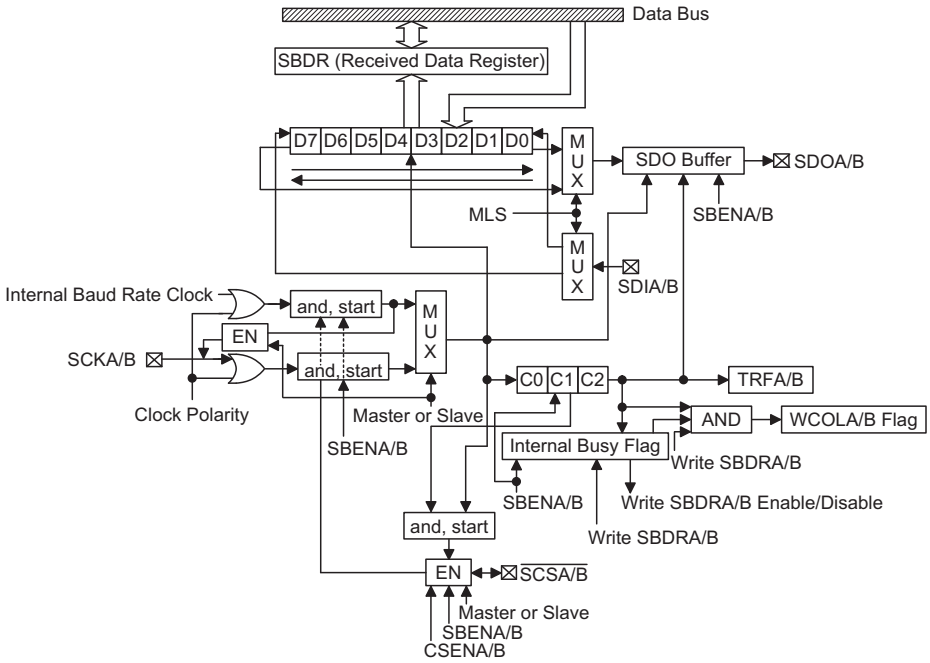
SPI Operation

All communication is carried out using the 4-line interface for both Master or Slave Mode. The timing diagram shows the basic operation of the bus.

The CSENA/B bit in the SBCRA/B register controls the overall function of the SPI interface. Setting this bit high, will enable the SPI interface by allowing the $\overline{SCSA/B}$ line to be active, which can then be used to control the SPI interface. If the CSENA/B bit is low, the SPI interface will be disabled and the $\overline{SCSA/B}$ line will be in a floating condition and can therefore not be used for control of the SPI interface. The SBENA/B bit in the SBCRA/B register must also be high which will place the SDIA/B line in a floating condition and the SDOA/B line high. If in the Master Mode the SCLKA/B line will be either high or low depending upon the clock polarity configuration option. If in the Slave Mode the SCLKA/B line will be in a floating condition. If SBENA/B is low then the bus will be disabled and $\overline{SCSA/B}$, SDIA/B, SDOA/B and SCLKA/B will all be in a floating condition.

In the Master Mode, the Master will always generate the clock signal. The clock and data transmission will be initiated after data has been written to the SBDRA/B register. In the Slave Mode, the clock signal will be received from an external master device for both data transmission or reception. The following sequences show the order to be followed for data transfer in both Master and Slave Mode:

- Master Mode
  - Step 1. Select the clock source using the CKSA/B bit in the SBCRA/B control register
  - Step 2. Setup the M0A/B and M1A/B bits in the SBCRA/B control register to select the Master Mode and the required Baud rate. Values of 00, 01 or 10 can be selected.
  - Step 3. Setup the CSENA/B bit and setup the MLSA/B bit to choose if the data is MSB or LSB first, this must be same as the Slave device.
  - Step 4. Setup the SBENA/B bit in the SBCRA/B control register to enable the SPI interface.



SPI Block Diagram

Note: WCOLA/B: set by SPI cleared by users

CSENA/B: enable/disable chip selection function pin
master mode: 1/0 = with/without $\overline{SCSA/B}$ output function
Slave mode: 1/0 = with/without $\overline{SCSA/B}$ input control function

SBENA/B: enable/disable serial bus (0: initialise all status flags)
when SBENA/B=0, all status flags should be initialised
when SBENA/B=1, all SPI related function pins should stay at floating state

TRFA/B: 1 = data transmitted or received, 0= data is transmitting or still not received

CPOL: I/O = clock polarity rising/falling edge : mask option

If clock polarity set to rising edge (SPIA_CPOL/SPIB_CPOL=1), serial clock timing follow $\overline{CLK}$, otherwise (SPIA_CPOL/SPIB_CPOL=0) CLK is the serial clock timing.

Step 5. For write operations: write the data to the SBDRA/B register, which will actually place the data into the TXRX buffer. Then use the SCLKA/B and $\overline{SCSA/B}$ lines to output the data.
Goto to step 6.For read operations: the data transferred in on the SDIA/B line will be stored in the TXRX buffer until all the data has been received at which point it will be latched into the SBDRA/B register.
Step 6. Check the WCOLA/B bit, if set high then a collision error has occurred so return to step5. If equal to zero then go to the following step.
Step 7. Check the TRFA/B bit or wait for an SPI serial bus interrupt.
Step 8. Read data from the SBDRA/B register.
Step 9. Clear TRFA/B.
Step10. Goto step 5.

- Slave Mode:
Step 1. The CKSA/B bit has a don't care value in the slave mode.
Step 2. Setup the M0A/B and M1A/B bits to 00 to select the Slave Mode. The CKSA/B bit is don't care.
Step 3. Setup the CSENA/B bit and setup the MLSA/B bit to choose if the data is MSB or LSB first, this must be same as the Master device.
Step 4. Setup the SBENA/B bit in the SBCRA/B control register to enable the SPI interface.
Step 5. For write operations: write data to the SBCRA/B register, which will actually place the data into the TXRX register, then wait for the master clock and $\overline{SCSA/B}$ signal. After this goto step 6.
For read operations: the data transferred in on the SDIA/B line will be stored in the TXRX buffer until all the data has been received at which point it will be latched into the SBDRA/B register.
Step 6. Check the WCOLA/B bit, if set high then a collision error has occurred so return to step5. If equal to zero then goto the following step.
Step 7. Check the TRFA/B bit or wait for an SPI serial bus interrupt.
Step 8. Read data from the SBDRA/B register.
Step 9. Clear TRFA/B
Step10. step 5

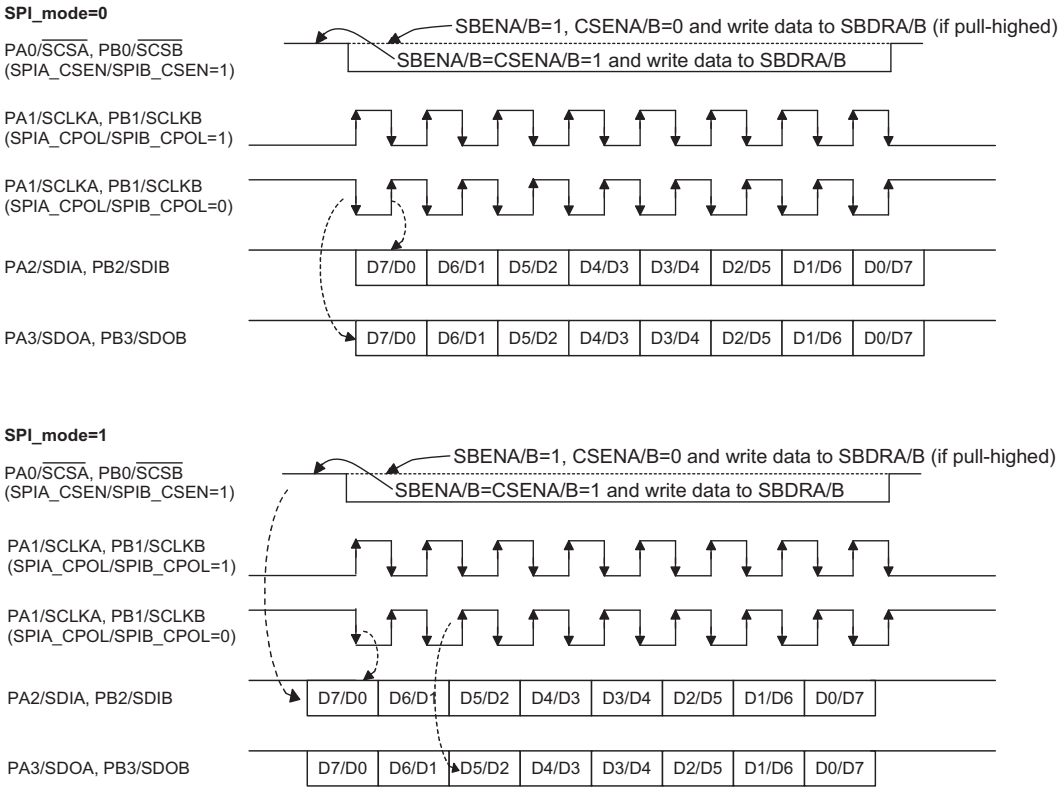
SPI Configuration Options and Status Control

One option is to enable the operation of the WCOLA/B, write collision bit, in the SBCRA/B register. Some control in SPIR register. The SPIA_CPOL/ SPIB_CPOL select the clock polarity of the SCK line. The SPIA_MODE/ SPIB_MODE select SPI data output mode.

SPI include four pins , can share I/O mode status . The status control combine with four bits for SPI and SBCRA/B register. Include SPIA_CSEN/SPIB_CSEN, SPIA_IO/SPIB_IO for SPI register and CSENA/B, SBENA/B for SBCRA/B register.

Control Bit for Register				SPI Share Function Pins Status			
SPIn_IO	SPIn_CSEN	SBENn	CSENn	$\overline{SCSn}$	SCKn	SDOn	SDIn
0	x	x	x	I/O Mode	I/O Mode	I/O Mode	I/O Mode
1	0	0	x	I/O Mode	I/O Mode	I/O Mode	I/O Mode
1	0	1	x	I/O Mode	SPI Mode	SPI Mode	SPI Mode(Z)
1	1	0	x	I/O Mode	I/O Mode	I/O Mode	I/O Mode
1	1	1	0	SPI Mode (Z)	SPI Mode	SPI Mode	SPI Mode(Z)
1	1	1	1	SPI Mode	SPI Mode	SPI Mode	SPI Mode(Z)

Note: "n" where n=A~B
X: don't care
(Z) floating



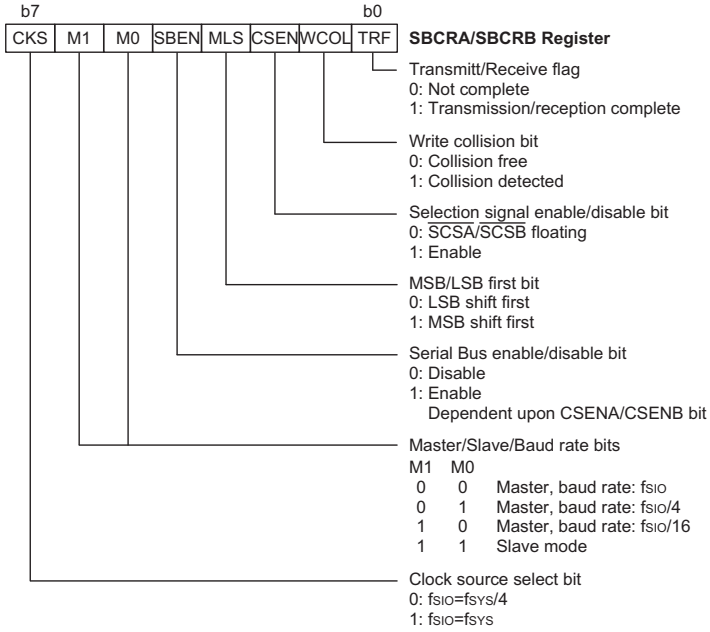
	D7	D6	D5	D4	D3	D2	D1	D0	
SBCRn	CKSn	M1n	M0n	SBENn	MLSn	CSENn	WCOLn	TRFn	SBCRn : Serial Bus
Default	0	1	1	0	0	0	0	0	Control Register
SBDRn	D7	D6	D5	D4	D3	D2	D1	D0	SBDRn : Sserial Bus
Default	U	U	U	U	U	U	U	U	DATA Register

Note: "n" where n=A~B
"U" means unchanged.

SPI Bus Timing

Error Detection

The WCOLA/B bit in the SBCRA/B register is provided to indicate errors during data transfer. The bit is set by the Serial Interface but must be cleared by the application program. This bit indicates a data collision has occurred which happens if a write to the SBDRA/B register takes place during a data transfer operation and will prevent the write operation from continuing. The bit will be set high by the Serial Interface but has to be cleared by the user application program. The overall function of the WCOLA/B bit can be disabled or enabled by a configuration option.

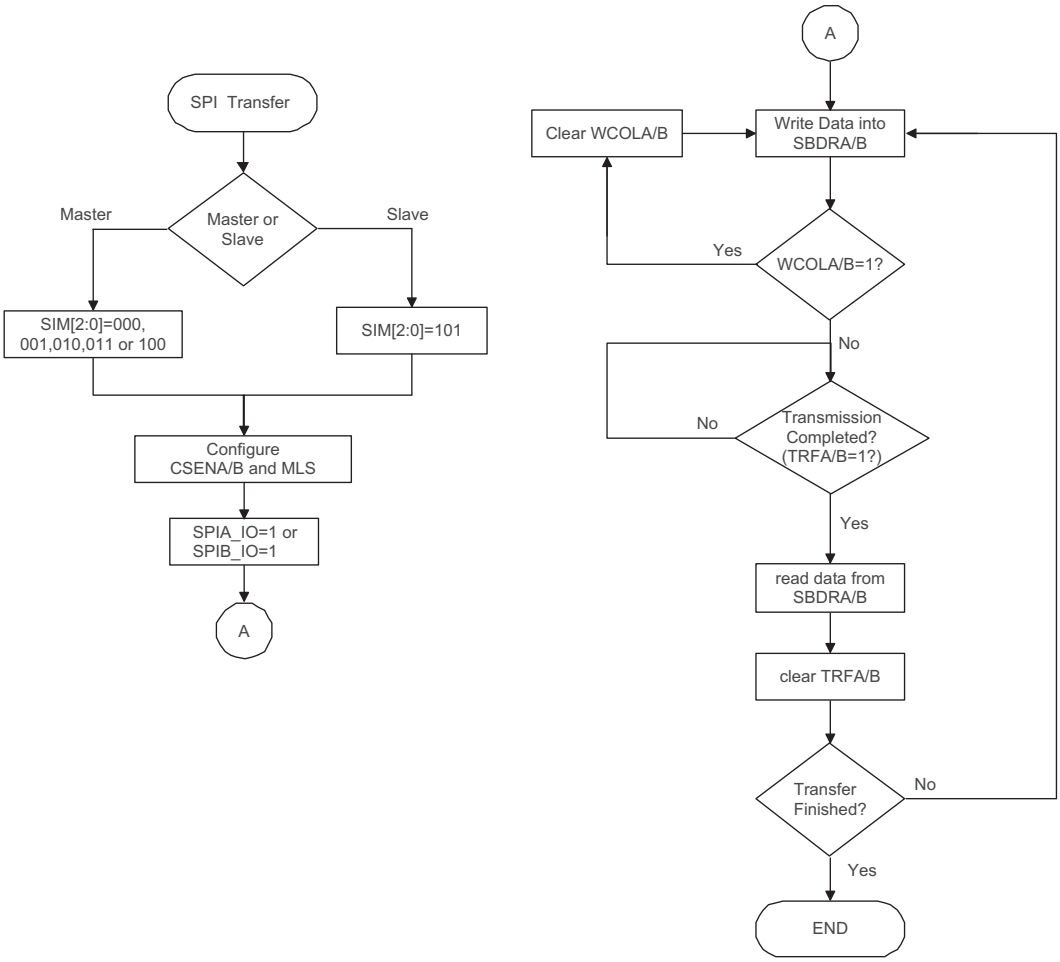


SPI Interface Control Register

Programming Considerations

When the device is placed into the Power Down Mode note that data reception and transmission will continue. The TRFA/B bit is used to generate an interrupt when the data has been transferred or received.

SPI Transfer Control Flowchart



Bit No.	Label	Function
0	SPIA_IO	1: IO, 0: SPI (default)
1	SPIA_MODE	1: SPI first output the data immediately after the SPI is enable. And SPI output the data in the falling edge (polarity=1) or rising edge (polarity=0); SPI read data in the in the rising edge (polarity=1) or falling edge (polarity=0) 0: SPI output the data in the rising edge (polarity=1) or falling edge (polarity=0); SPI read data in the in the falling edge (polarity=1) or rising edge (polarity=0); (default)
2	SPIA_CPOL	1: clock polarity rising 0: clock polarity falling (default falling)
3	SPIA_CSEN	1: SPI_CSEN: Enable , this bit is used to enable/disable software CSEN function (default enable) 0: SPI_CSEN disable, $\overline{SCSA}$ define as GPIO
4	SPIB_IO	1: IO, 0: SPI (default)
5	SPIB_MODE	1: SPI first output the data immediately after the SPI is enable. And SPI output the data in the falling edge (polarity=1) or rising edge (polarity=0); SPI read data in the in the rising edge (polarity=1) or falling edge (polarity=0) 0: SPI output the data in the rising edge (polarity=1) or falling edge (polarity=0); SPI read data in the in the falling edge (polarity=1) or rising edge (polarity=0); (default)
6	SPIB_CPOL	1: clock polarity rising 0: clock polarity falling (default falling)
7	SPIB_CSEN	1: SPI_CSEN: Enable, this bit is used to enable/disable software CSEN function (default enable) 0: SPI_CSEN disable, $\overline{SCSB}$ define as GPIO

SPI Register

USB Interface

The device includes a USB interface function allowing for the convenient design of USB peripheral products. The USB disable/enable control bit ″USBdis″ is in the PWMCTL Register. If the USB is disabled, then V33O and the D+/D- lines will be floating and the USB SIE will be disabled.

Power Plane

There are four power planes for the device: USB SIE VDD, VDDIO and the MCU VDD and Flash memory power for the HT82A6208/HT82A6216. For the USB SIE VDD will supply all circuits related to the USB SIE and be sourced from pin ″UBUS″. Once the USB is removed from the USB and there is no power in the USB BUS, the USB SIE circuit is no longer operational.

For the PB port, it can be configured using a configuration option to define the if the pins PB0~PB7 are supplied by either the MCU VDD, or if pins PB0~PB6 are supplied by the power pin VDDIO, in which case power will be supplied on pin PB7. In the latter configuration, PB7 will be configured as a power pin VDDIO and not a normal I/O pin.

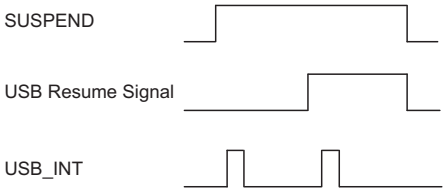
For the MCU VDD, it supplies all the HT82A623R circuit except the USB SIE which is supply by UBUS.

For the HT82A6208 and HT82A6216 the internal Flash memory is supplied by VCC.

USB Suspend Wake-Up Remote Wake-Up

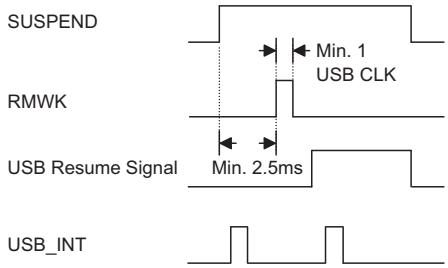
If there is no signal on the USB bus for over 3ms, the device will enter a suspend mode. The Suspend flag, SUSP, in the USC register, will then be set high and a USB interrupt will be generated to indicate that the device should jump to the suspend state to meet the requirements of the USB suspend current spec. In order to meet the requirements of the suspend current, the firmware should disable the USB clock by clearing the USBCKEN bit to zero.

The suspend current can be further decreased by setting the SUSP2 bit in the UCC register. When the resume signal is sent out by the host, the device will be woken up the by the USB interrupt and the Resume bit in the USC register will be set. To ensure correct device operation, the program must set the USBCKEN bit in the UCC register high and clear the SUSP2 bit in the UCC register. The Resume signal will be cleared before the Idle signal is sent out by the host and the Suspend line in the USC register will change to zero. So when the MCU



detects the Suspend bit in the USC register, the condition of the Resume line should be noted and taken into consideration.

The device has a remote wake up function which can wake-up the USB Host by sending a wake-up pulse through RMWK in the USC register. Once the USB Host receives a wake-up signal from the device it will send a Resume signal to the device.



USB Interface Operation

The device has 8 Endpoints, EP0~EP3. EP0 supports Control transfer. All EP1~EP3 support Interrupt or Bulk transfer.

All endpoints except EP0 can be configured as 8, 16, 32 or 64 FIFO size using the register UFC0 and UFC1. EP0 has an 8-byte FIFO size. The Total FIFO size is 64+8 bytes. The URD in the USC register is the USB reset signal control function definition bit.

Bit No.	Label	Function
0	ESD	This bit will set to ″1″ when there are ESD issue. This bit is set by SIE and clear by F/W.
1	PUB	Bit3=1, D+, and D- have a 500kΩ pull-high Bit3=0, no pull-high (default on MCU reset)
2	SE0	This bit is used to indicate the SIE has detect a SE0 noise in the USB bus. This bit is set by SIE and clear by F/W.
3	SE1	This bit is used to indicate the SIE has detect a SE1 noise in the USB bus. This bit is set by SIE and clear by F/W.
4	PS2/DAI	USBD-/DATA input.
5	PS2/CKI	USBD+/CLK input.
6	PS2/DAO	Output for driving USBD-/DATA pin, when work under 3D PS2 mouse function. Default value is ″1″.
7	PS2/CKO	Output for driving USBD+/CLK pin, when work under 3D PS2 mouse function. Default value is ″1″.

USB_STAT Register

Bit No.	Label	Function
0	EP0EN	Control the USB endpoint0 interrupt (1=enabled; 0=disabled)
1	EP1EN	Control the USB endpoint1 interrupt (1=enabled; 0=disabled)
2	EP2EN	Control the USB endpoint2 interrupt (1=enabled; 0=disabled)
3	EP3EN	Control the USB endpoint3 interrupt (1=enabled; 0=disabled)
4~7	—	Unused bit, read as ″0″

UINT1 Register

Bit No.	Label	Function
0	SUSP	Read only, USB suspend indication. When this bit is set to ″1″ (set by SIE), it indicates that the USB bus has entered the suspend mode. The USB interrupt is also triggered when this bit changes from low to high.
1	RMWK	USB remote wake-up command. It is set by MCU to leave the USB host leaving the suspend mode.
2	URST	USB reset indication. This bit is set/cleared by the USB SIE. This bit is used to detect a USB reset event on the USB bus. When this bit is set to ″1″, this indicates that a USB reset has occurred and that a USB interrupt will be initialized.
3	RESUME	USB resume indication. When the USB leaves the suspend mode, this bit is set to ″1″ (set by SIE). When the RESUME is set by SIE, an interrupt will be generated to wake-up the MCU. In order to detect the suspend state, the MCU should set USBCKEN and clear SUSP2 (in the UCC register) to enable the SIE detect function. RESUME will be cleared when the SUSP goes to ″0″. When the MCU is detecting the SUSP, the condition of RESUME (causes the MCU to wake-up) should be noted and taken into consideration.
4	V33O	0/1: Turn-off/on V33O output.
5	PLL	0: Turn-on PLL (default), 1: turn off PLL.
6	SELPS2	When set to ′1′, indicated the chip work under PS2 mode. Default value is ″0″.
7	URD	USB reset signal control function definition. 1: USB reset signal will reset MCU. 0: USB reset signal cannot reset MCU.

USC Register

The USR register which is the endpoint interrupt status register, is used to indicate which endpoint is accessed and to select the USB bus. The endpoint request flags, EP0F, EP1F, EP2F and EP3F, are used to indicate which endpoints are accessed. If an endpoint is accessed, the related endpoint request flag will be set high and a USB interrupt will be generated, if the USB interrupt is enabled and the stack is not full. When the active endpoint request flag is serviced, the endpoint request flag has to be cleared to zero using the program.

Bit No.	Label	Function
0	EP0F	When this bit is set to ″1″ (set by SIE), it indicates that endpoint 0 has been accessed and a USB interrupt will occur. When the interrupt has been serviced, this bit should be cleared by software.
1	EP1F	When this bit is set to ″1″ (set by SIE), it indicates that endpoint 1 has been accessed and a USB interrupt will occur. When the interrupt has been serviced, this bit should be cleared by software.
2	EP2F	When this bit is set to ″1″ (set by SIE), it indicates that endpoint 2 has been accessed and a USB interrupt will occur. When the interrupt has been serviced, this bit should be cleared by software.
3	EP3F	When this bit is set to ″1″ (set by SIE), it indicates that endpoint 3 has been accessed and a USB interrupt will occur. When the interrupt has been serviced, this bit should be cleared by software.
4~7	—	Unused bit, read as ″0″

USR Register

There is a system clock control register to select the clock used in the MCU. This register consists of a USB clock control bit, USBCKEN, a second suspend mode control bit, SUSP2, and a system clock selection bit, SYSCLK.

The endpoint selection is determined by EPS2, EPS1 and EPS0.

Bit No.	Label	Function
0 1 2	EPS0 EPS1 EPS2	Accessing endpoint FIFO selection. EPS2, EPS1, EPS0: 000: Select endpoint 0 FIFO (control) 001: Select endpoint 1 FIFO 010: Select endpoint 2 FIFO 011: Select endpoint 3 FIFO If the selected endpoints do not exist, the related functions will be absent.
3	USBCKEN	USB clock control bit. When this bit is set to ″1″, it indicates that the USB clock is enabled. Otherwise, the USB clock is turned-off.
4	SUSP2	This bit is used for reducing power consumption in suspend mode. In normal mode, clean this bit to ″0″. In halt mode, set this bit to ″1″ for reducing power consumption.
5	FSYS16MHz	This bit is used to define if the MCU system clock comes form an external OSC or comes from the PLL output 16MHz clock. 0: system clock sourced from OSC. 1: system clock sourced from the PLL output 16MHz.
6	SYSCLK	This bit is used to specify the MCU system clock oscillator frequency. For a 6MHz crystal oscillator or resonator, set this bit to ″1″. For a 12MHz crystal oscillator or resonator, clear this bit to ″0″.
7	RCTRL	This bit is used to control whether there is 7.5kΩ resistor between D+ and Vbus. 0: no 7.5kΩ between D+ and Vbus (default) 1: has 7.5kΩ between D+ and Vbus

UCC Register

The AWR register contains the current address and a remote wake up function control bit. The initial value of AWR is ″00H″. The address value extracted from the USB command has not to be loaded into this register until the SETUP stage has finished.

Bit No.	Label	Function
0	WKEN	USB remote-wake-up enable/disable (1/0)
1~7	AD0~AD6	USB device address

AWR Register

The STALL register shows if the corresponding endpoint has worked properly or not. As soon as endpoint improper operation occurs, the related bit in the STALL register has to be set high. The STALL register bits will be cleared by a USB reset signal and a setup token event.

Bit No.	Label	Function
0~3	STL0~ STL3	Set by the users when related USB endpoints were stalled. Cleared by a USB reset. The STL0 is also cleared by a Setup Token event.
4~7	—	Unused bit, read as ″0″

STALL Register

The SIES register is only used for EP0 except for the NMI bit, which can control all endpoints

Bit No.	Label	Function
0	ASET	This bit is used to configure the SIE to automatically change the device address by the value stored in the AWR register. When this bit is set to ″1″ by firmware, the SIE will update the device address by the value stored in the AWR register after the PC host has successfully read the data from he device by an IN operation. Otherwise, when this bit is cleared to ″0″, the SIE will update the device address immediately after an address is written to the AWR register. So, in order to work properly, the firmware has to clear this bit after a next valid SETUP token is received.
1	ERR	This bit is used to indicate that some errors have occurred when the FIFO is accessed. This bit is set by SIE and should be cleared by firmware. This bit is used for all endpoint
2	OUT	This bit is used to indicate the OUT token (except the OUT zero length token) has been received. The firmware clears this bit after the OUT data has been read. Also, this bit will be cleared by SIE after the next valid SETUP token is received.
3	IN	This bit is used to indicate the current USB receiving signal from PC host is IN token.
4	NO ACK	This bit will set to ″1″ once SIE discover ther are some error condition so the SIE is not response (NAK or ACK or DATA) for the USB token. This bit is set by SIE and clear by F/W.
5	—	Unused bit, read as ″0″
6	CRCF	This bit will set to ″1″ when there are the following three condition is happened: CRC error, PID error, Bit stuffing error. This bit is set by SIE and clear by F/W.
7	NMI	NAK token interrupt mask flag. If this bit set, when the device sent a NAK token to the host, an interrupt will be disabled. Otherwise if this bit is cleared, when the device sends a NAK token to the host, it will enter the interrupt sub-routine. This bit is used for all endpoint.

SIES Register

The MISC register combines command and status to control the desired endpoint FIFO action and to show the status of the desired endpoint FIFO. MISC will be cleared by a USB reset signal.

Bit No.	Label	Function
0	REQUEST	After setting the status of the desired one, FIFO can be requested by setting this bit high. After finishing, this bit must be set low.
1	TX	To represent the direction and transition end MCU access. When set to logic 1, the MCU desires to write data to the FIFO. After finishing, this bit must be set to logic 0 before terminating request to represent transition end. For an MCU read operation, this bit must be set to logic 0 and set to logic 1 after finishing.
2	CLEAR	MCU requests to clear the FIFO, even if the FIFO is not ready. After clearing the FIFO, the USB interface will send force_tx_err to tell the Host that data under-run if the Host wants to read data.
3~4	—	Unused bit, read as ″0″
5	SETCMD	To show that the data in the FIFO is a setup command. This bit is set by Hardware and clear by Firmware.
6	READY	To show that the desired FIFO is ready.
7	LEN0	To show that the host sent a 0-sized packet to the MCU. This bit must be cleared by a read action to the corresponding FIFO.

MISC Register

Bit No.	Label	Function
0	FIFO_def	Once this bit set to "1" by Firmware, The SIE should redefine the FIFO configuration. This bit is automatically cleared by SIE
1	SETI1*	Input FIFO for EP1 eanble 1/disable 0; default disable
2	SETI2*	Input FIFO for EP2 eanble 1/disable 0; default disable
3	SETI3*	Input FIFO for EP3 eanble 1/disable 0; default disable
4~7	—	Unused bit, read as "0"

Note: "*" It is only required to set the data pipe as an input pipe or output pipe. The purpose of this function is to avoid the host sending an abnormal IN or OUT token and disabling the endpoint.

UFIEN Register, USB Endpoint 1~Endpoint 3 set IN Pipe Enable Register

Bit No.	Label	Function
0	—	Unused bit, read as "0"
1	SETO1**	Output FIFO for EP1 eanble 1/disable 0; default disable
2	SETO2**	Output FIFO for EP2 eanble 1/disable 0; default disable
3	SETO3**	Output FIFO for EP3 eanble 1/disable 0; default disable
4~7	—	Unused bit, read as "0"

Note: "*" USB definition: when the host sends a "set Configuration", the Data pipe should send the DATA0 (about the Data toggle) first. So, when the Device receives a "set configuration" setup command, the user needs to toggle this bit as the following data will send a Data0 first.

"**" It is only required to set the data pipe as an input pipe or output pipe. The purpose of this function is to avoid the host sending a abnormal IN or OUT token and disabling the endpoint.

UFOEN Register, USB Endpoint 1~Endpoint 3 set OUT Pipe Enable Register

Bit No.	Label	Function
0 1	RAM_def0 RAM_def1	00: RAM0 input FIFO, RAM1 output FIFO 01: Both RAM0 and RAM1 are output FIFO 10: Both RAM0 and RAM1 are input FIFO 11: RAM0 output FIFO, RAM1 input FIFO
2 3	E1FS0 E1FS1	Define endpoint 1 FIFO size E1FS1, E1FS0: 00: 8-byte 01: 16-byte 10: 32-byte 11: 64-byte
4 5	E2FS0 E2FS1	Define endpoint 2 FIFO size E2FS1, E2FS0: 00: 8-byte 01: 16-byte 10: 32-byte 11: 64-byte
6 7	E3FS0 E3FS1	Define endpoint 3 FIFO size E3FS1, E3FS0: 00: 8-byte 01: 16-byte 10: 32-byte 11: 64-byte

UFC0 USB FIFO Size Control Register 0

The total FIFO size is 64+8 bytes. All endpoints except EP0 can be defined by registers UFOEN, UFIEN, UFC0 and UFC. There are three FIFO mapped as follow:

8 bytes FIFO for Endpoint0

RAM0 FIFO for other input Endpoint (1~3)

RAM1 FIFO for other output Endpoint (1~3)

Bit No.	Label	Function
0~3	FIFO0~ FIFO3	EPi accessing register (i=0~3). When an endpoint is disabled, the corresponding accessing register should be disabled.
4~7	—	Unused bit, read as ″0″

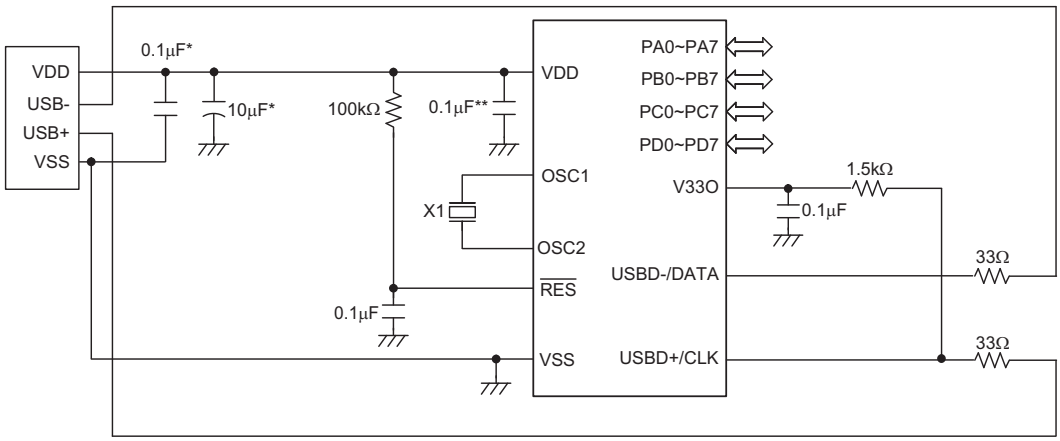
FIFO0~FIFO3 USB endpoint accessing registers definitions

Configuration Options

No.	Options
1	PA pull-high enable/disable (1/0) (default: enable)
2	PB pull-high enable/disable (1/0) by nibble (default: enable)
3	PC pull-high enable/disable (1/0) by nibble (default: enable)
4	PC, wake-up enable/disable (1/0) by nibble (default: disable)
5	SPIA WCOL: Enable/Disable (default disable)
6	Built-in 1.5K (default no built-in)
7	Has 7.5kΩ resistor enable bit (default no)
8	TBHP enable or disable (default disable)
9	Low voltage reset: enable/disable (default: enable)
10	WDT enable/disable (0/1) (default: enable)
11	WDT clock source: $f_{SYS}/4$ or RC (default T1)
12	CLR WDT instructions: one or two clear WDT instruction(s) (0/1) (default: 1 inst.)
13	PA NMOS or CMOS output type (default CMOS)
14	Port A wake-up enable/disable (1/0) by bit (default: enable)
15	PB0~PB3 NMOS or CMOS output type (default CMOS)
16	Port B wake-up enable/disable (1/0) by bit (default: disable)
17	0: PB7 used as GPIO 1: PB7 used as VDDIO pin
18	0: PB0~PB6 use power=V_{DD} 1: PB0~PB6 use power=V_{DDIO}
19	PD NMOS or CMOS output type (default CMOS)
20	PD pull-high enable/disable (1/0) by nibble (default: enable)
21	PD, wake-up enable/disable (1/0) by nibble (default: disable)
22	SPIB WCOL: enable/disable (default disable)

Application Circuits

Crystal or Ceramic Resonator for Multiple I/O Applications



Note: The resistance and capacitance for the reset circuit should be designed in such a way as to ensure that VDD is stable and remains within a valid operating voltage range before bringing $\overline{RES}$ high.

X1 can be 6MHz or 12MHz, and should be located as close to the OSC1/OSC2 pins as possible.

* These capacitors should be placed close to the USB connector.

** This capacitor should be placed close to the MCU.

Instruction Set

Introduction

Central to the successful operation of any microcontroller is its instruction set, which is a set of program instruction codes that directs the microcontroller to perform certain operations. In the case of Holtek microcontrollers, a comprehensive and flexible set of over 60 instructions is provided to enable programmers to implement their application with the minimum of programming overheads.

For easier understanding of the various instruction codes, they have been subdivided into several functional groupings.

Instruction Timing

Most instructions are implemented within one instruction cycle. The exceptions to this are branch, call, or table read instructions where two instruction cycles are required. One instruction cycle is equal to 4 system clock cycles, therefore in the case of an 8MHz system oscillator, most instructions would be implemented within 0.5μs and branch or call instructions would be implemented within 1μs. Although instructions which require one more cycle to implement are generally limited to the JMP, CALL, RET, RETI and table read instructions, it is important to realize that any other instructions which involve manipulation of the Program Counter Low register or PCL will also take one more cycle to implement. As instructions which change the contents of the PCL will imply a direct jump to that new address, one more cycle will be required. Examples of such instructions would be ″CLR PCL″ or ″MOV PCL, A″. For the case of skip instructions, it must be noted that if the result of the comparison involves a skip operation then this will also take one more cycle, if no skip is involved then only one cycle is required.

Moving and Transferring Data

The transfer of data within the microcontroller program is one of the most frequently used operations. Making use of three kinds of MOV instructions, data can be transferred from registers to the Accumulator and vice-versa as well as being able to move specific immediate data directly into the Accumulator. One of the most important data transfer applications is to receive data from the input ports and transfer data to the output ports.

Arithmetic Operations

The ability to perform certain arithmetic operations and data manipulation is a necessary feature of most microcontroller applications. Within the Holtek microcontroller instruction set are a range of add and subtract instruction mnemonics to enable the necessary arithmetic to be carried out. Care must be taken to ensure correct handling of carry and borrow data when results exceed 255 for addition and less than 0 for subtraction. The increment and decrement instructions INC, INCA, DEC and DECA provide a simple means of increasing or decreasing by a value of one of the values in the destination specified.

Logical and Rotate Operations

The standard logical operations such as AND, OR, XOR and CPL all have their own instruction within the Holtek microcontroller instruction set. As with the case of most instructions involving data manipulation, data must pass through the Accumulator which may involve additional programming steps. In all logical data operations, the zero flag may be set if the result of the operation is zero. Another form of logical data manipulation comes from the rotate instructions such as RR, RL, RRC and RLC which provide a simple means of rotating one bit right or left. Different rotate instructions exist depending on program requirements. Rotate instructions are useful for serial port programming applications where data can be rotated from an internal register into the Carry bit from where it can be examined and the necessary serial bit set high or low. Another application where rotate data operations are used is to implement multiplication and division calculations.

Branches and Control Transfer

Program branching takes the form of either jumps to specified locations using the JMP instruction or to a subroutine using the CALL instruction. They differ in the sense that in the case of a subroutine call, the program must return to the instruction immediately when the subroutine has been carried out. This is done by placing a return instruction RET in the subroutine which will cause the program to jump back to the address right after the CALL instruction. In the case of a JMP instruction, the program simply jumps to the desired location. There is no requirement to jump back to the original jumping off point as in the case of the CALL instruction. One special and extremely useful set of branch instructions are the conditional branches. Here a decision is first made regarding the condition of a certain data memory or individual bits. Depending upon the conditions, the program will continue with the next instruction or skip over it and jump to the following instruction. These instructions are the key to decision making and branching within the program perhaps determined by the condition of certain input switches or by the condition of internal data bits.

Bit Operations

The ability to provide single bit operations on Data Memory is an extremely flexible feature of all Holtek microcontrollers. This feature is especially useful for output port bit programming where individual bits or port pins can be directly set high or low using either the "SET [m].i" or "CLR [m].i" instructions respectively. The feature removes the need for programmers to first read the 8-bit output port, manipulate the input data to ensure that other bits are not changed and then output the port with the correct new data. This read-modify-write process is taken care of automatically when these bit operation instructions are used.

Table Read Operations

Data storage is normally implemented by using registers. However, when working with large amounts of fixed data, the volume involved often makes it inconvenient to store the fixed data in the Data Memory. To overcome this problem, Holtek microcontrollers allow an area of Program Memory to be setup as a table where data can be directly stored. A set of easy to use instructions provides the means by which this fixed data can be referenced and retrieved from the Program Memory.

Other Operations

In addition to the above functional instructions, a range of other instructions also exist such as the "HALT" instruction for Power-down operations and instructions to control the operation of the Watchdog Timer for reliable program operations under extreme electric or electromagnetic environments. For their relevant operations, refer to the functional related sections.

Instruction Set Summary

The following table depicts a summary of the instruction set categorised according to function and can be consulted as a basic instruction reference using the following listed conventions.

Table conventions:

x: Bits immediate data

m: Data Memory address

A: Accumulator

i: 0~7 number of bits

addr: Program memory address

Mnemonic	Description	Cycles	Flag Affected
Arithmetic			
ADD A,[m]	Add Data Memory to ACC	1	Z, C, AC, OV
ADDM A,[m]	Add ACC to Data Memory	1Note	Z, C, AC, OV
ADD A,x	Add immediate data to ACC	1	Z, C, AC, OV
ADC A,[m]	Add Data Memory to ACC with Carry	1	Z, C, AC, OV
ADCM A,[m]	Add ACC to Data memory with Carry	1Note	Z, C, AC, OV
SUB A,x	Subtract immediate data from the ACC	1	Z, C, AC, OV
SUB A,[m]	Subtract Data Memory from ACC	1	Z, C, AC, OV
SUBM A,[m]	Subtract Data Memory from ACC with result in Data Memory	1Note	Z, C, AC, OV
SBC A,[m]	Subtract Data Memory from ACC with Carry	1	Z, C, AC, OV
SBCM A,[m]	Subtract Data Memory from ACC with Carry, result in Data Memory	1Note	Z, C, AC, OV
DAA [m]	Decimal adjust ACC for Addition with result in Data Memory	1Note	C
Logic Operation			
AND A,[m]	Logical AND Data Memory to ACC	1	Z
OR A,[m]	Logical OR Data Memory to ACC	1	Z
XOR A,[m]	Logical XOR Data Memory to ACC	1	Z
ANDM A,[m]	Logical AND ACC to Data Memory	1Note	Z
ORM A,[m]	Logical OR ACC to Data Memory	1Note	Z
XORM A,[m]	Logical XOR ACC to Data Memory	1Note	Z
AND A,x	Logical AND immediate Data to ACC	1	Z
OR A,x	Logical OR immediate Data to ACC	1	Z
XOR A,x	Logical XOR immediate Data to ACC	1	Z
CPL [m]	Complement Data Memory	1Note	Z
CPLA [m]	Complement Data Memory with result in ACC	1	Z
Increment & Decrement			
INCA [m]	Increment Data Memory with result in ACC	1	Z
INC [m]	Increment Data Memory	1Note	Z
DECA [m]	Decrement Data Memory with result in ACC	1	Z
DEC [m]	Decrement Data Memory	1Note	Z

Mnemonic	Description	Cycles	Flag Affected
Rotate			
RRA [m]	Rotate Data Memory right with result in ACC	1	None
RR [m]	Rotate Data Memory right	1Note	None
RRCA [m]	Rotate Data Memory right through Carry with result in ACC	1	C
RRC [m]	Rotate Data Memory right through Carry	1Note	C
RLA [m]	Rotate Data Memory left with result in ACC	1	None
RL [m]	Rotate Data Memory left	1Note	None
RLCA [m]	Rotate Data Memory left through Carry with result in ACC	1	C
RLC [m]	Rotate Data Memory left through Carry	1Note	C
Data Move			
MOV A,[m]	Move Data Memory to ACC	1	None
MOV [m],A	Move ACC to Data Memory	1Note	None
MOV A,x	Move immediate data to ACC	1	None
Bit Operation			
CLR [m].i	Clear bit of Data Memory	1Note	None
SET [m].i	Set bit of Data Memory	1Note	None
Branch			
JMP addr	Jump unconditionally	2	None
SZ [m]	Skip if Data Memory is zero	1Note	None
SZA [m]	Skip if Data Memory is zero with data movement to ACC	1note	None
SZ [m].i	Skip if bit i of Data Memory is zero	1Note	None
SNZ [m].i	Skip if bit i of Data Memory is not zero	1Note	None
SIZ [m]	Skip if increment Data Memory is zero	1Note	None
SDZ [m]	Skip if decrement Data Memory is zero	1Note	None
SIZA [m]	Skip if increment Data Memory is zero with result in ACC	1Note	None
SDZA [m]	Skip if decrement Data Memory is zero with result in ACC	1Note	None
CALL addr	Subroutine call	2	None
RET	Return from subroutine	2	None
RET A,x	Return from subroutine and load immediate data to ACC	2	None
RETI	Return from interrupt	2	None
Table Read			
TABRDC [m]	Read table (current page) to TBLH and Data Memory	2Note	None
TABRDL [m]	Read table (last page) to TBLH and Data Memory	2Note	None
Miscellaneous			
NOP	No operation	1	None
CLR [m]	Clear Data Memory	1Note	None
SET [m]	Set Data Memory	1Note	None
CLR WDT	Clear Watchdog Timer	1	TO, PDF
CLR WDT1	Pre-clear Watchdog Timer	1	TO, PDF
CLR WDT2	Pre-clear Watchdog Timer	1	TO, PDF
SWAP [m]	Swap nibbles of Data Memory	1Note	None
SWAPA [m]	Swap nibbles of Data Memory with result in ACC	1	None
HALT	Enter power down mode	1	TO, PDF

Note: 1. For skip instructions, if the result of the comparison involves a skip then two cycles are required, if no skip takes place only one cycle is required.
2. Any instruction which changes the contents of the PCL will also require 2 cycles for execution.
3. For the ″CLR WDT1″ and ″CLR WDT2″ instructions the TO and PDF flags may be affected by the execution status. The TO and PDF flags are cleared after both ″CLR WDT1″ and ″CLR WDT2″ instructions are consecutively executed. Otherwise the TO and PDF flags remain unchanged.

Instruction Definition

ADC A,[m]	Add Data Memory to ACC with Carry
Description	The contents of the specified Data Memory, Accumulator and the carry flag are added. The result is stored in the Accumulator.
Operation	ACC ← ACC + [m] + C
Affected flag(s)	OV, Z, AC, C
ADCM A,[m]	Add ACC to Data Memory with Carry
Description	The contents of the specified Data Memory, Accumulator and the carry flag are added. The result is stored in the specified Data Memory.
Operation	[m] ← ACC + [m] + C
Affected flag(s)	OV, Z, AC, C
ADD A,[m]	Add Data Memory to ACC
Description	The contents of the specified Data Memory and the Accumulator are added. The result is stored in the Accumulator.
Operation	ACC ← ACC + [m]
Affected flag(s)	OV, Z, AC, C
ADD A,x	Add immediate data to ACC
Description	The contents of the Accumulator and the specified immediate data are added. The result is stored in the Accumulator.
Operation	ACC ← ACC + x
Affected flag(s)	OV, Z, AC, C
ADDM A,[m]	Add ACC to Data Memory
Description	The contents of the specified Data Memory and the Accumulator are added. The result is stored in the specified Data Memory.
Operation	[m] ← ACC + [m]
Affected flag(s)	OV, Z, AC, C
AND A,[m]	Logical AND Data Memory to ACC
Description	Data in the Accumulator and the specified Data Memory perform a bitwise logical AND operation. The result is stored in the Accumulator.
Operation	ACC ← ACC ″AND″ [m]
Affected flag(s)	Z
AND A,x	Logical AND immediate data to ACC
Description	Data in the Accumulator and the specified immediate data perform a bitwise logical AND operation. The result is stored in the Accumulator.
Operation	ACC ← ACC ″AND″ x
Affected flag(s)	Z
ANDM A,[m]	Logical AND ACC to Data Memory
Description	Data in the specified Data Memory and the Accumulator perform a bitwise logical AND operation. The result is stored in the Data Memory.
Operation	[m] ← ACC ″AND″ [m]
Affected flag(s)	Z

CALL addr	Subroutine call
Description	Unconditionally calls a subroutine at the specified address. The Program Counter then increments by 1 to obtain the address of the next instruction which is then pushed onto the stack. The specified address is then loaded and the program continues execution from this new address. As this instruction requires an additional operation, it is a two cycle instruction.
Operation	Stack ← Program Counter + 1 Program Counter ← addr
Affected flag(s)	None
CLR [m]	Clear Data Memory
Description	Each bit of the specified Data Memory is cleared to 0.
Operation	[m] ← 00H
Affected flag(s)	None
CLR [m].i	Clear bit of Data Memory
Description	Bit i of the specified Data Memory is cleared to 0.
Operation	[m].i ← 0
Affected flag(s)	None
CLR WDT	Clear Watchdog Timer
Description	The TO, PDF flags and the WDT are all cleared.
Operation	WDT cleared TO ← 0 PDF ← 0
Affected flag(s)	TO, PDF
CLR WDT1	Pre-clear Watchdog Timer
Description	The TO, PDF flags and the WDT are all cleared. Note that this instruction works in conjunction with CLR WDT2 and must be executed alternately with CLR WDT2 to have effect. Repetitively executing this instruction without alternately executing CLR WDT2 will have no effect.
Operation	WDT cleared TO ← 0 PDF ← 0
Affected flag(s)	TO, PDF
CLR WDT2	Pre-clear Watchdog Timer
Description	The TO, PDF flags and the WDT are all cleared. Note that this instruction works in conjunction with CLR WDT1 and must be executed alternately with CLR WDT1 to have effect. Repetitively executing this instruction without alternately executing CLR WDT1 will have no effect.
Operation	WDT cleared TO ← 0 PDF ← 0
Affected flag(s)	TO, PDF

CPL [m] Complement Data Memory

Description Each bit of the specified Data Memory is logically complemented (1′s complement). Bits which previously contained a 1 are changed to 0 and vice versa.

Operation $[m] \leftarrow \overline{[m]}$

Affected flag(s) Z

CPLA [m] Complement Data Memory with result in ACC

Description Each bit of the specified Data Memory is logically complemented (1′s complement). Bits which previously contained a 1 are changed to 0 and vice versa. The complemented result is stored in the Accumulator and the contents of the Data Memory remain unchanged.

Operation $ACC \leftarrow \overline{[m]}$

Affected flag(s) Z

DAA [m] Decimal-Adjust ACC for addition with result in Data Memory

Description Convert the contents of the Accumulator value to a BCD (Binary Coded Decimal) value resulting from the previous addition of two BCD variables. If the low nibble is greater than 9 or if AC flag is set, then a value of 6 will be added to the low nibble. Otherwise the low nibble remains unchanged. If the high nibble is greater than 9 or if the C flag is set, then a value of 6 will be added to the high nibble. Essentially, the decimal conversion is performed by adding 00H, 06H, 60H or 66H depending on the Accumulator and flag conditions. Only the C flag may be affected by this instruction which indicates that if the original BCD sum is greater than 100, it allows multiple precision decimal addition.

Operation $[m] \leftarrow ACC + 00H$ or
$[m] \leftarrow ACC + 06H$ or
$[m] \leftarrow ACC + 60H$ or
$[m] \leftarrow ACC + 66H$

Affected flag(s) C

DEC [m] Decrement Data Memory

Description Data in the specified Data Memory is decremented by 1.

Operation $[m] \leftarrow [m] - 1$

Affected flag(s) Z

DECA [m] Decrement Data Memory with result in ACC

Description Data in the specified Data Memory is decremented by 1. The result is stored in the Accumulator. The contents of the Data Memory remain unchanged.

Operation $ACC \leftarrow [m] - 1$

Affected flag(s) Z

HALT Enter power down mode

Description This instruction stops the program execution and turns off the system clock. The contents of the Data Memory and registers are retained. The WDT and prescaler are cleared. The power down flag PDF is set and the WDT time-out flag TO is cleared.

Operation $TO \leftarrow 0$
$PDF \leftarrow 1$

Affected flag(s) TO, PDF

INC [m]	Increment Data Memory
Description	Data in the specified Data Memory is incremented by 1.
Operation	[m] ← [m] + 1
Affected flag(s)	Z
INCA [m]	Increment Data Memory with result in ACC
Description	Data in the specified Data Memory is incremented by 1. The result is stored in the Accumulator. The contents of the Data Memory remain unchanged.
Operation	ACC ← [m] + 1
Affected flag(s)	Z
JMP addr	Jump unconditionally
Description	The contents of the Program Counter are replaced with the specified address. Program execution then continues from this new address. As this requires the insertion of a dummy instruction while the new address is loaded, it is a two cycle instruction.
Operation	Program Counter ← addr
Affected flag(s)	None
MOV A,[m]	Move Data Memory to ACC
Description	The contents of the specified Data Memory are copied to the Accumulator.
Operation	ACC ← [m]
Affected flag(s)	None
MOV A,x	Move immediate data to ACC
Description	The immediate data specified is loaded into the Accumulator.
Operation	ACC ← x
Affected flag(s)	None
MOV [m],A	Move ACC to Data Memory
Description	The contents of the Accumulator are copied to the specified Data Memory.
Operation	[m] ← ACC
Affected flag(s)	None
NOP	No operation
Description	No operation is performed. Execution continues with the next instruction.
Operation	No operation
Affected flag(s)	None
OR A,[m]	Logical OR Data Memory to ACC
Description	Data in the Accumulator and the specified Data Memory perform a bitwise logical OR operation. The result is stored in the Accumulator.
Operation	ACC ← ACC ″OR″ [m]
Affected flag(s)	Z

OR A,x	Logical OR immediate data to ACC
Description	Data in the Accumulator and the specified immediate data perform a bitwise logical OR operation. The result is stored in the Accumulator.
Operation	ACC ← ACC ″OR″ x
Affected flag(s)	Z
ORM A,[m]	Logical OR ACC to Data Memory
Description	Data in the specified Data Memory and the Accumulator perform a bitwise logical OR operation. The result is stored in the Data Memory.
Operation	[m] ← ACC ″OR″ [m]
Affected flag(s)	Z
RET	Return from subroutine
Description	The Program Counter is restored from the stack. Program execution continues at the restored address.
Operation	Program Counter ← Stack
Affected flag(s)	None
RET A,x	Return from subroutine and load immediate data to ACC
Description	The Program Counter is restored from the stack and the Accumulator loaded with the specified immediate data. Program execution continues at the restored address.
Operation	Program Counter ← Stack ACC ← x
Affected flag(s)	None
RETI	Return from interrupt
Description	The Program Counter is restored from the stack and the interrupts are re-enabled by setting the EMI bit. EMI is the master interrupt global enable bit. If an interrupt was pending when the RETI instruction is executed, the pending Interrupt routine will be processed before returning to the main program.
Operation	Program Counter ← Stack EMI ← 1
Affected flag(s)	None
RL [m]	Rotate Data Memory left
Description	The contents of the specified Data Memory are rotated left by 1 bit with bit 7 rotated into bit 0.
Operation	[m].(i+1) ← [m].i; (i = 0~6) [m].0 ← [m].7
Affected flag(s)	None
RLA [m]	Rotate Data Memory left with result in ACC
Description	The contents of the specified Data Memory are rotated left by 1 bit with bit 7 rotated into bit 0. The rotated result is stored in the Accumulator and the contents of the Data Memory remain unchanged.
Operation	ACC.(i+1) ← [m].i; (i = 0~6) ACC.0 ← [m].7
Affected flag(s)	None

RLC [m] Rotate Data Memory left through Carry

Description The contents of the specified Data Memory and the carry flag are rotated left by 1 bit. Bit 7 replaces the Carry bit and the original carry flag is rotated into bit 0.

Operation
[m].(i+1) ← [m].i; (i = 0~6)
[m].0 ← C
C ← [m].7

Affected flag(s) C

RLCA [m] Rotate Data Memory left through Carry with result in ACC

Description Data in the specified Data Memory and the carry flag are rotated left by 1 bit. Bit 7 replaces the Carry bit and the original carry flag is rotated into the bit 0. The rotated result is stored in the Accumulator and the contents of the Data Memory remain unchanged.

Operation
ACC.(i+1) ← [m].i; (i = 0~6)
ACC.0 ← C
C ← [m].7

Affected flag(s) C

RR [m] Rotate Data Memory right

Description The contents of the specified Data Memory are rotated right by 1 bit with bit 0 rotated into bit 7.

Operation
[m].i ← [m].(i+1); (i = 0~6)
[m].7 ← [m].0

Affected flag(s) None

RRA [m] Rotate Data Memory right with result in ACC

Description Data in the specified Data Memory and the carry flag are rotated right by 1 bit with bit 0 rotated into bit 7. The rotated result is stored in the Accumulator and the contents of the Data Memory remain unchanged.

Operation
ACC.i ← [m].(i+1); (i = 0~6)
ACC.7 ← [m].0

Affected flag(s) None

RRC [m] Rotate Data Memory right through Carry

Description The contents of the specified Data Memory and the carry flag are rotated right by 1 bit. Bit 0 replaces the Carry bit and the original carry flag is rotated into bit 7.

Operation
[m].i ← [m].(i+1); (i = 0~6)
[m].7 ← C
C ← [m].0

Affected flag(s) C

RRCA [m] Rotate Data Memory right through Carry with result in ACC

Description Data in the specified Data Memory and the carry flag are rotated right by 1 bit. Bit 0 replaces the Carry bit and the original carry flag is rotated into bit 7. The rotated result is stored in the Accumulator and the contents of the Data Memory remain unchanged.

Operation
ACC.i ← [m].(i+1); (i = 0~6)
ACC.7 ← C
C ← [m].0

Affected flag(s) C

SBC A,[m] Subtract Data Memory from ACC with Carry

Description The contents of the specified Data Memory and the complement of the carry flag are subtracted from the Accumulator. The result is stored in the Accumulator. Note that if the result of subtraction is negative, the C flag will be cleared to 0, otherwise if the result is positive or zero, the C flag will be set to 1.

Operation $ACC \leftarrow ACC - [m] - \overline{C}$

Affected flag(s) OV, Z, AC, C

SBCM A,[m] Subtract Data Memory from ACC with Carry and result in Data Memory

Description The contents of the specified Data Memory and the complement of the carry flag are subtracted from the Accumulator. The result is stored in the Data Memory. Note that if the result of subtraction is negative, the C flag will be cleared to 0, otherwise if the result is positive or zero, the C flag will be set to 1.

Operation $[m] \leftarrow ACC - [m] - \overline{C}$

Affected flag(s) OV, Z, AC, C

SDZ [m] Skip if decrement Data Memory is 0

Description The contents of the specified Data Memory are first decremented by 1. If the result is 0 the following instruction is skipped. As this requires the insertion of a dummy instruction while the next instruction is fetched, it is a two cycle instruction. If the result is not 0 the program proceeds with the following instruction.

Operation $[m] \leftarrow [m] - 1$
Skip if [m] = 0

Affected flag(s) None

SDZA [m] Skip if decrement Data Memory is zero with result in ACC

Description The contents of the specified Data Memory are first decremented by 1. If the result is 0, the following instruction is skipped. The result is stored in the Accumulator but the specified Data Memory contents remain unchanged. As this requires the insertion of a dummy instruction while the next instruction is fetched, it is a two cycle instruction. If the result is not 0, the program proceeds with the following instruction.

Operation $ACC \leftarrow [m] - 1$
Skip if ACC = 0

Affected flag(s) None

SET [m] Set Data Memory

Description Each bit of the specified Data Memory is set to 1.

Operation $[m] \leftarrow FFH$

Affected flag(s) None

SET [m].i Set bit of Data Memory

Description Bit i of the specified Data Memory is set to 1.

Operation $[m].i \leftarrow 1$

Affected flag(s) None

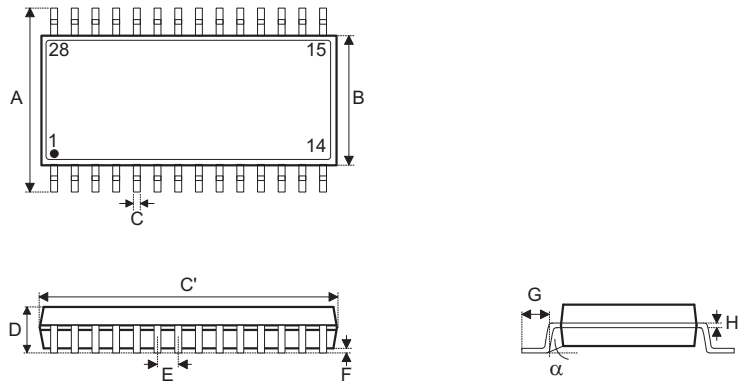
SIZ [m]	Skip if increment Data Memory is 0
Description	The contents of the specified Data Memory are first incremented by 1. If the result is 0, the following instruction is skipped. As this requires the insertion of a dummy instruction while the next instruction is fetched, it is a two cycle instruction. If the result is not 0 the program proceeds with the following instruction.
Operation	[m] ← [m] + 1 Skip if [m] = 0
Affected flag(s)	None
SIZA [m]	Skip if increment Data Memory is zero with result in ACC
Description	The contents of the specified Data Memory are first incremented by 1. If the result is 0, the following instruction is skipped. The result is stored in the Accumulator but the specified Data Memory contents remain unchanged. As this requires the insertion of a dummy instruction while the next instruction is fetched, it is a two cycle instruction. If the result is not 0 the program proceeds with the following instruction.
Operation	ACC ← [m] + 1 Skip if ACC = 0
Affected flag(s)	None
SNZ [m].i	Skip if bit i of Data Memory is not 0
Description	If bit i of the specified Data Memory is not 0, the following instruction is skipped. As this requires the insertion of a dummy instruction while the next instruction is fetched, it is a two cycle instruction. If the result is 0 the program proceeds with the following instruction.
Operation	Skip if [m].i ≠ 0
Affected flag(s)	None
SUB A,[m]	Subtract Data Memory from ACC
Description	The specified Data Memory is subtracted from the contents of the Accumulator. The result is stored in the Accumulator. Note that if the result of subtraction is negative, the C flag will be cleared to 0, otherwise if the result is positive or zero, the C flag will be set to 1.
Operation	ACC ← ACC – [m]
Affected flag(s)	OV, Z, AC, C
SUBM A,[m]	Subtract Data Memory from ACC with result in Data Memory
Description	The specified Data Memory is subtracted from the contents of the Accumulator. The result is stored in the Data Memory. Note that if the result of subtraction is negative, the C flag will be cleared to 0, otherwise if the result is positive or zero, the C flag will be set to 1.
Operation	[m] ← ACC – [m]
Affected flag(s)	OV, Z, AC, C
SUB A,x	Subtract immediate data from ACC
Description	The immediate data specified by the code is subtracted from the contents of the Accumulator. The result is stored in the Accumulator. Note that if the result of subtraction is negative, the C flag will be cleared to 0, otherwise if the result is positive or zero, the C flag will be set to 1.
Operation	ACC ← ACC – x
Affected flag(s)	OV, Z, AC, C

SWAP [m]	Swap nibbles of Data Memory
Description	The low-order and high-order nibbles of the specified Data Memory are interchanged.
Operation	[m].3~[m].0 ↔ [m].7 ~ [m].4
Affected flag(s)	None
SWAPA [m]	Swap nibbles of Data Memory with result in ACC
Description	The low-order and high-order nibbles of the specified Data Memory are interchanged. The result is stored in the Accumulator. The contents of the Data Memory remain unchanged.
Operation	ACC.3 ~ ACC.0 ← [m].7 ~ [m].4 ACC.7 ~ ACC.4 ← [m].3 ~ [m].0
Affected flag(s)	None
SZ [m]	Skip if Data Memory is 0
Description	If the contents of the specified Data Memory is 0, the following instruction is skipped. As this requires the insertion of a dummy instruction while the next instruction is fetched, it is a two cycle instruction. If the result is not 0 the program proceeds with the following instruction.
Operation	Skip if [m] = 0
Affected flag(s)	None
SZA [m]	Skip if Data Memory is 0 with data movement to ACC
Description	The contents of the specified Data Memory are copied to the Accumulator. If the value is zero, the following instruction is skipped. As this requires the insertion of a dummy instruction while the next instruction is fetched, it is a two cycle instruction. If the result is not 0 the program proceeds with the following instruction.
Operation	ACC ← [m] Skip if [m] = 0
Affected flag(s)	None
SZ [m].i	Skip if bit i of Data Memory is 0
Description	If bit i of the specified Data Memory is 0, the following instruction is skipped. As this requires the insertion of a dummy instruction while the next instruction is fetched, it is a two cycle instruction. If the result is not 0, the program proceeds with the following instruction.
Operation	Skip if [m].i = 0
Affected flag(s)	None
TABRDC [m]	Read table (current page) to TBLH and Data Memory
Description	The low byte of the program code (current page) addressed by the table pointer (TBLP) is moved to the specified Data Memory and the high byte moved to TBLH.
Operation	[m] ← program code (low byte) TBLH ← program code (high byte)
Affected flag(s)	None
TABRDL [m]	Read table (last page) to TBLH and Data Memory
Description	The low byte of the program code (last page) addressed by the table pointer (TBLP) is moved to the specified Data Memory and the high byte moved to TBLH.
Operation	[m] ← program code (low byte) TBLH ← program code (high byte)
Affected flag(s)	None

XOR A,[m]	Logical XOR Data Memory to ACC
Description	Data in the Accumulator and the specified Data Memory perform a bitwise logical XOR operation. The result is stored in the Accumulator.
Operation	ACC ← ACC ″XOR″ [m]
Affected flag(s)	Z
XORM A,[m]	Logical XOR ACC to Data Memory
Description	Data in the specified Data Memory and the Accumulator perform a bitwise logical XOR operation. The result is stored in the Data Memory.
Operation	[m] ← ACC ″XOR″ [m]
Affected flag(s)	Z
XOR A,x	Logical XOR immediate data to ACC
Description	Data in the Accumulator and the specified immediate data perform a bitwise logical XOR operation. The result is stored in the Accumulator.
Operation	ACC ← ACC ″XOR″ x
Affected flag(s)	Z

Package Information

28-pin SOP (300mil) Outline Dimensions

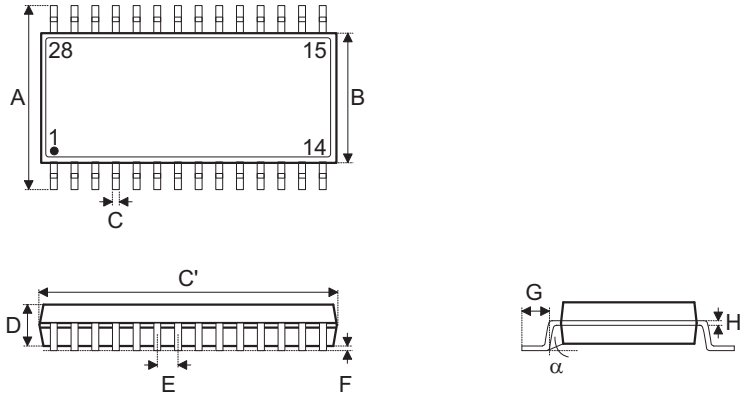


- MS-013MS-013

Symbol	Dimensions in inch		
	Min.	Nom.	Max.
A	0.393	—	0.419
B	0.256	—	0.300
C	0.012	—	0.020
C′	0.697	—	0.713
D	—	—	0.104
E	—	0.050	—
F	0.004	—	0.012
G	0.016	—	0.050
H	0.008	—	0.013
α	0°	—	8°

Symbol	Dimensions in mm		
	Min.	Nom.	Max.
A	9.98	—	10.64
B	6.50	—	7.62
C	0.30	—	0.51
C′	17.70	—	18.11
D	—	—	2.64
E	—	1.27	—
F	0.10	—	0.30
G	0.41	—	1.27
H	0.20	—	0.33
α	0°	—	8°

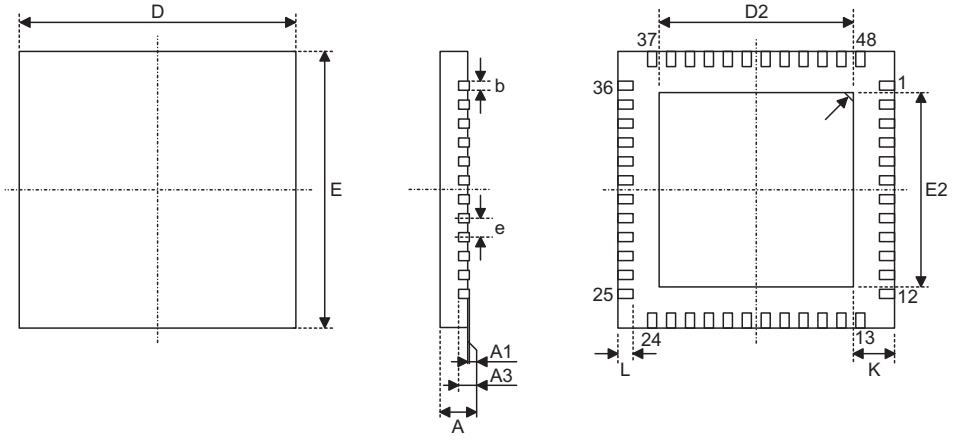
28-pin SSOP (150mil) Outline Dimensions



Symbol	Dimensions in inch		
	Min.	Nom.	Max.
A	0.228	—	0.244
B	0.150	—	0.157
C	0.008	—	0.012
C′	0.386	—	0.394
D	0.054	—	0.060
E	—	0.025	—
F	0.004	—	0.010
G	0.022	—	0.028
H	0.007	—	0.010
α	0°	—	8°

Symbol	Dimensions in mm		
	Min.	Nom.	Max.
A	5.79	—	6.20
B	3.81	—	3.99
C	0.20	—	0.30
C′	9.80	—	10.01
D	1.37	—	1.52
E	—	0.64	—
F	0.10	—	0.25
G	0.56	—	0.71
H	0.18	—	0.25
α	0°	—	8°

SAW Type 48-pin (7mm×7mm) QFN Outline Dimensions

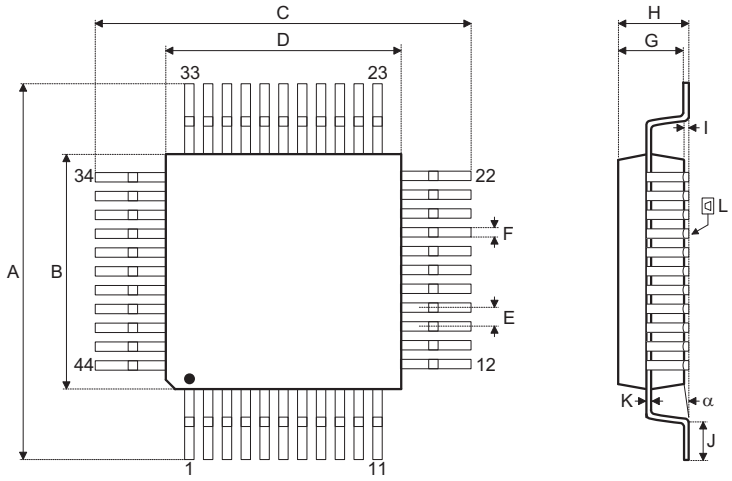


• ASECL

Symbol	Dimensions in inch		
	Min.	Nom.	Max.
A	0.031	0.033	0.035
A1	0.000	0.001	0.002
A3	—	0.008	—
b	0.007	0.010	0.012
D	—	0.276	—
E	—	0.276	—
e	—	0.020	—
D2	0.219	0.222	0.226
E2	0.219	0.222	0.226
L	0.014	0.016	0.018

Symbol	Dimensions in mm		
	Min.	Nom.	Max.
A	0.800	0.850	0.900
A1	0.000	0.035	0.050
A3	—	0.203	—
b	0.180	0.250	0.300
D	—	7.000	—
E	—	7.000	—
e	—	0.500	—
D2	5.550	5.650	5.750
E2	5.550	5.650	5.750
L	0.350	0.400	0.450

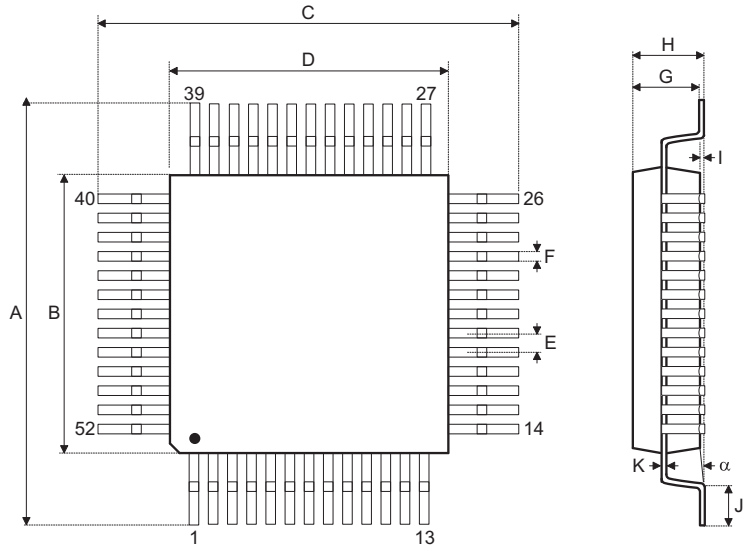
44-pin QFP (10mm×10mm) Outline Dimensions



Symbol	Dimensions in inch		
	Min.	Nom.	Max.
A	0.512	—	0.528
B	0.390	—	0.398
C	0.512	—	0.528
D	0.390	—	0.398
E	—	0.031	—
F	—	0.012	—
G	0.075	—	0.087
H	—	—	0.106
I	0.010	—	0.020
J	0.029	—	0.037
K	0.004	—	0.008
L	—	0.004	—
α	0°	—	7°

Symbol	Dimensions in mm		
	Min.	Nom.	Max.
A	13.00	—	13.40
B	9.90	—	10.10
C	13.00	—	13.40
D	9.90	—	10.10
E	—	0.80	—
F	—	0.30	—
G	1.90	—	2.20
H	—	—	2.70
I	0.25	—	0.50
J	0.73	—	0.93
K	0.10	—	0.20
L	—	0.10	—
α	0°	—	7°

52-pin QFP (14mm×14mm) Outline Dimensions

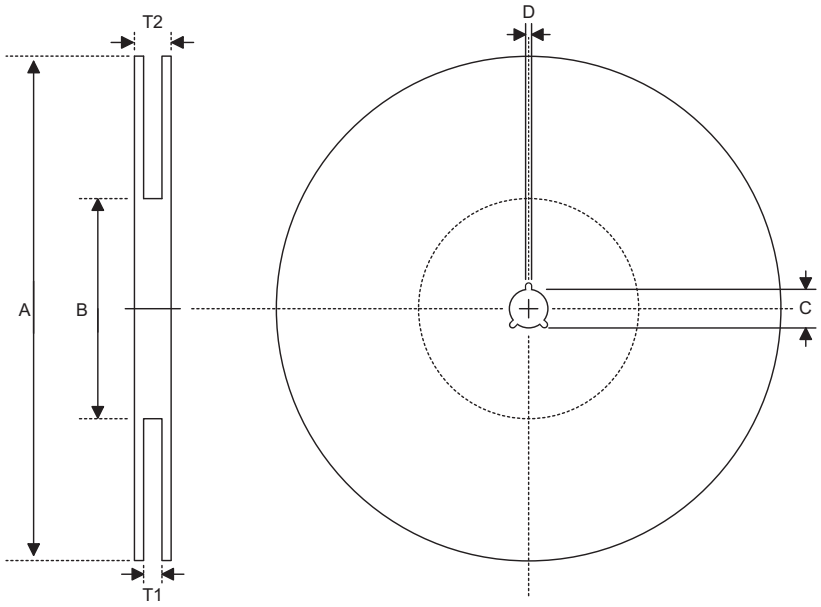


Symbol	Dimensions in inch		
	Min.	Nom.	Max.
A	0.681	—	0.689
B	0.547	—	0.555
C	0.681	—	0.689
D	0.547	—	0.555
E	—	0.039	—
F	—	0.016	—
G	0.098	—	0.122
H	—	—	0.134
I	—	0.004	—
J	0.029	—	0.041
K	0.004	—	0.008
α	0°	—	7°

Symbol	Dimensions in mm		
	Min.	Nom.	Max.
A	17.30	—	17.50
B	13.90	—	14.10
C	17.30	—	17.50
D	13.90	—	14.10
E	—	1.00	—
F	—	0.40	—
G	2.50	—	3.10
H	—	—	3.40
I	—	0.10	—
J	0.73	—	1.03
K	0.10	—	0.20
α	0°	—	7°

Product Tape and Reel Specifications

Reel Dimensions



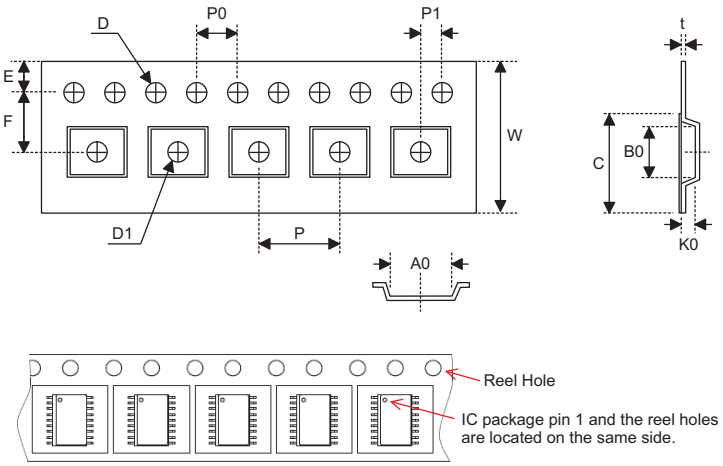
SOP 28W (300mil)

Symbol	Description	Dimensions in mm
A	Reel Outer Diameter	330.0±1.0
B	Reel Inner Diameter	100.0±1.5
C	Spindle Hole Diameter	13.0 $^{+0.5/-0.2}$
D	Key Slit Width	2.0±0.5
T1	Space Between Flange	24.8 $^{+0.3/-0.2}$
T2	Reel Thickness	30.2±0.2

SSOP 28S (150mil)

Symbol	Description	Dimensions in mm
A	Reel Outer Diameter	330.0±1.0
B	Reel Inner Diameter	100.0±1.5
C	Spindle Hole Diameter	13.0 $^{+0.5/-0.2}$
D	Key Slit Width	2.0±0.5
T1	Space Between Flange	16.8 $^{+0.3/-0.2}$
T2	Reel Thickness	22.2±0.2

Carrier Tape Dimensions



SOP 28W (300mil)

Symbol	Description	Dimensions in mm
W	Carrier Tape Width	24.0±0.3
P	Cavity Pitch	12.0±0.1
E	Perforation Position	1.75±0.10
F	Cavity to Perforation (Width Direction)	11.5±0.1
D	Perforation Diameter	1.5 +0.1/-0.0
D1	Cavity Hole Diameter	1.50 +0.25/-0.00
P0	Perforation Pitch	4.0±0.1
P1	Cavity to Perforation (Length Direction)	2.0±0.1
A0	Cavity Length	10.85±0.10
B0	Cavity Width	18.34±0.10
K0	Cavity Depth	2.97±0.10
t	Carrier Tape Thickness	0.35±0.01
C	Cover Tape Width	21.3±0.1

SSOP 28S (150mil)

Symbol	Description	Dimensions in mm
W	Carrier Tape Width	16.0±0.3
P	Cavity Pitch	8.0±0.1
E	Perforation Position	1.75±0.1
F	Cavity to Perforation (Width Direction)	7.5±0.1
D	Perforation Diameter	1.55 +0.10/-0.00
D1	Cavity Hole Diameter	1.50 +0.25/-0.00
P0	Perforation Pitch	4.0±0.1
P1	Cavity to Perforation (Length Direction)	2.0±0.1
A0	Cavity Length	6.5±0.1
B0	Cavity Width	10.3±0.1
K0	Cavity Depth	2.1±0.1
t	Carrier Tape Thickness	0.30±0.05
C	Cover Tape Width	13.3±0.1

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