32Mx72 DRAM 3.3V DIMM MODULE

FEATURES

- Performance range:

	t_{RAC}	t_{CAC}	t_{RC}	t_{PC}
WPD32M72V-60MDC	60ns	20ns	110ns	40ns
WPD32M72V-70MDC	70ns	25ns	130ns	45ns

- Fast Page Mode operation
- $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh capability
- $\overline{\text{RAS}}$-only refresh capability
- LVTTL compatible inputs and outputs
- +3.3V $\pm$ 0.3V power supply
- 8192 cycles/64ms refresh
- JEDEC standard pinout
- ECC Optimized
- Gold edge connectors

GENERAL DESCRIPTION

The WPD32M72V-XMDC is an 32M x 72 bit Dynamic RAM high density memory module. The module consists of thirty-six 16M x 4 bit DRAMs in 32-pin TSOP packages. The DRAMs are mounted in stacks of two on a 168-pin glass epoxy substrate . A 0.1µF decoupling capacitor is mounted for each DRAM. Selected inputs and outputs are buffered for improved performance and easier memory subsystem design.

The WPD32M72V-XMDC is a Dual In-line Memory Module with gold edge connections, 3.3V power supply, 8K refresh, optimized for ECC, and intended for mounting into 168-pin edge connector sockets.

PIN CONFIGURATION

Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
1	V_{SS}	25	NC	49	V_{CC}	73	V_{CC}	97	DQ_{45}	121	A_9	145	NC
2	DQ_0	26	V_{CC}	50	NC	74	DQ_{32}	98	DQ_{46}	122	A_{11}	146	NC
3	DQ_1	27	$\overline{WE}_0$	51	NC	75	DQ_{33}	99	DQ_{47}	123	NC	147	NC
4	DQ_2	28	$\overline{CAS}_0$	52	DQ_{18}	76	DQ_{34}	100	DQ_{48}	124	V_{CC}	148	NC
5	DQ_3	29	NC	53	DQ_{19}	77	DQ_{35}	101	DQ_{49}	125	NC	149	DQ_{61}
6	V_{CC}	30	$\overline{RAS}_0$	54	V_{SS}	78	V_{SS}	102	V_{CC}	126	B_0	150	DQ_{62}
7	DQ_4	31	$\overline{OE}_0$	55	DQ_{20}	79	PD_1	103	DQ_{50}	127	V_{SS}	151	DQ_{63}
8	DQ_5	32	V_{SS}	56	DQ_{21}	80	PD_3	104	DQ_{51}	128	NC	152	V_{SS}
9	DQ_6	33	A_0	57	DQ_{22}	81	PD_5	105	DQ_{52}	129	$\overline{RAS}_3$	153	DQ_{64}
10	DQ_7	34	A_2	58	DQ_{23}	82	PD_7	106	DQ_{53}	130	NC	154	DQ_{65}
11	DQ_8	35	A_4	59	V_{CC}	83	ID_0	107	V_{SS}	131	NC	155	DQ_{66}
12	V_{SS}	36	A_6	60	DQ_{24}	84	V_{CC}	108	NC	132	$\overline{PDE}$	156	DQ_{67}
13	DQ_9	37	A_8	61	NC	85	V_{SS}	109	NC	133	V_{CC}	157	V_{CC}
14	DQ_{10}	38	A_{10}	62	NC	86	DQ_{36}	110	V_{CC}	134	NC	158	DQ_{68}
15	DQ_{11}	39	A_{12}	63	NC	87	DQ_{37}	111	NC	135	NC	159	DQ_{69}
16	DQ_{12}	40	V_{CC}	64	NC	88	DQ_{38}	112	NC	136	DQ_{54}	160	DQ_{70}
17	DQ_{13}	41	NC	65	DQ_{25}	89	DQ_{39}	113	NC	137	DQ_{55}	161	DQ_{71}
18	V_{CC}	42	NC	66	DQ_{26}	90	V_{CC}	114	$\overline{RAS}_1$	138	V_{SS}	162	V_{SS}
19	DQ_{14}	43	V_{SS}	67	DQ_{27}	91	DQ_{40}	115	NC	139	DQ_{56}	163	PD_2
20	DQ_{15}	44	$\overline{OE}_2$	68	V_{SS}	92	DQ_{41}	116	V_{SS}	140	DQ_{57}	164	PD_4
21	DQ_{16}	45	$\overline{RAS}_2$	69	DQ_{28}	93	DQ_{42}	117	A_1	141	DQ_{58}	165	PD_6
22	DQ_{17}	46	$\overline{CAS}_4$	70	DQ_{29}	94	DQ_{43}	118	A_3	142	DQ_{59}	166	PD_8
23	V_{SS}	47	NC	71	DQ_{30}	95	DQ_{44}	119	A_5	143	V_{CC}	167	ID_1
24	NC	48	$\overline{WE}_2$	72	DQ_{31}	96	V_{SS}	120	A_7	144	DQ_{60}	168	V_{CC}

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PIN CONFIGURATION (continued)

Pin Names

Pin Name	Pin Function
A_0, B_0, A_1-A_{12}	Address Inputs (Buffered)
DQ_x	Data In/Out
$\overline{WE}_0$, $\overline{WE}_2$	Read/Write Input (Buffered)
$\overline{OE}_0$, $\overline{OE}_2$	Output Enable (Buffered)
$\overline{RAS}_0$-$\overline{RAS}_3$	Row Address Strobe
$\overline{CAS}_0$, $\overline{CAS}_4$	Column Address Strobe (Buffered)
PD_1-PD_8	Presence Detect (Buffered)
$\overline{PDE}$	Presence Detect Enable
ID_0-ID_1	ID Bits
V_{CC}	Power (+3.3V)
V_{SS}	Ground
NC	No Connection

Presence Detect

For 32Mx72 Bit Configuration with 16M x 4 Bit chips and 8K Refresh:

PD_1=NC, PD_2=V_{SS}, PD_3=V_{SS}, PD_4=V_{SS}

For Fast Page:

PD_5=V_{SS}

Speed:

Pin	60ns	70ns
PD_6	NC	V_{SS}
PD_7	NC	NC

For ECC:

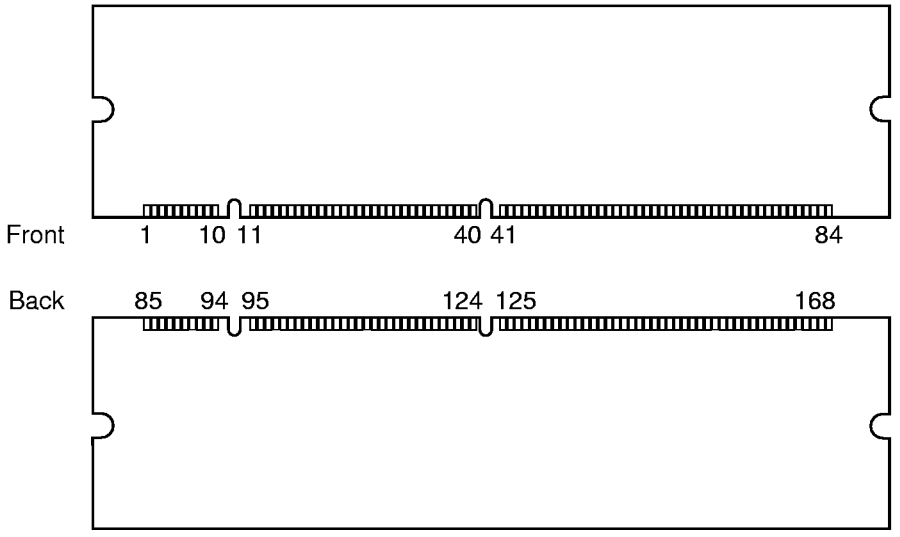
PD_8=V_{SS}

For x72 ECC:

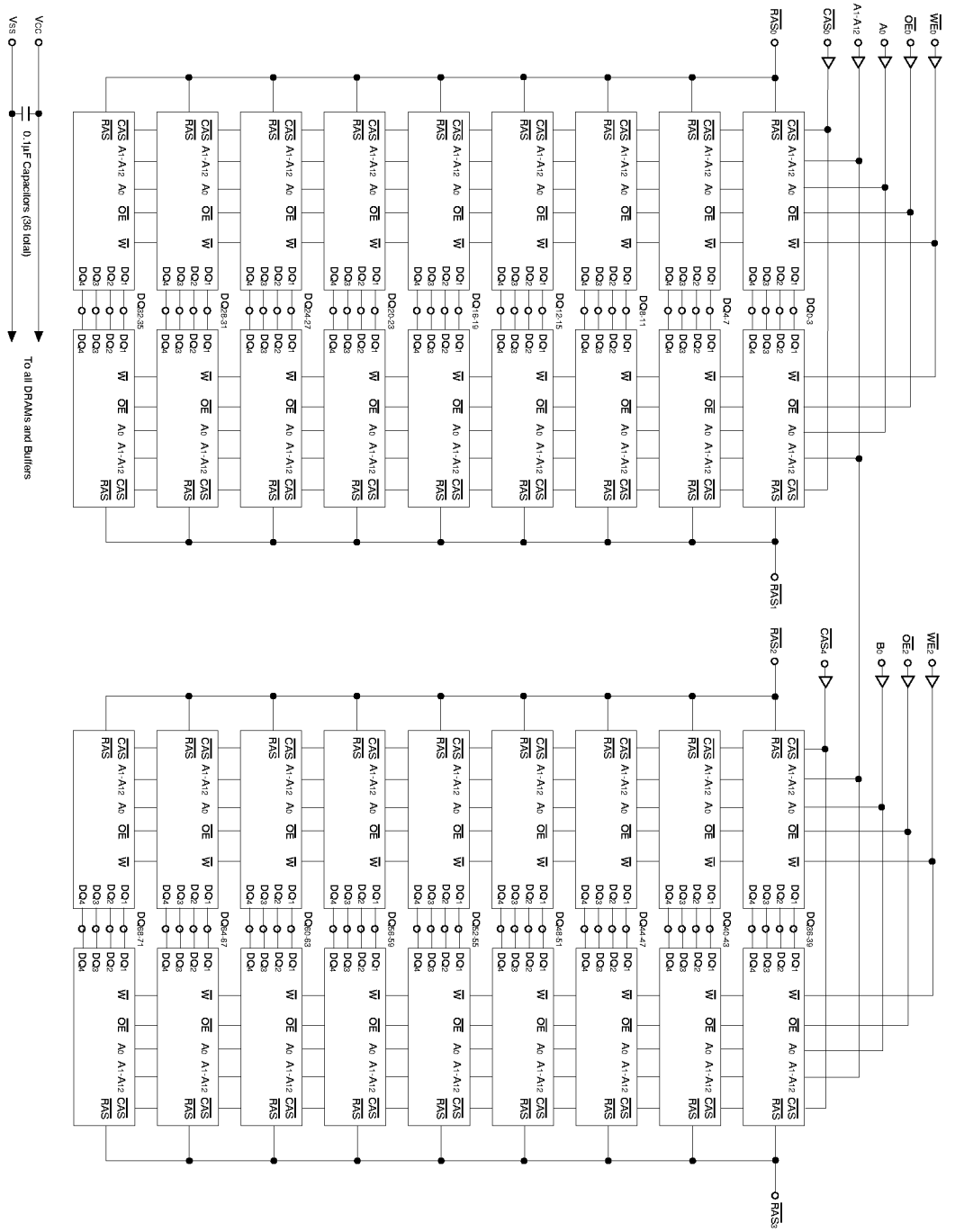
ID_0 =V_{SS}

For Normal Refresh Mode:

ID_1=V_{SS}



FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Item	Symbol	Rating	Units
Voltage on Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	-0.5 to +4.6	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{CC}	-0.5 to +4.6	V
Storage Temperature	T_{stg}	-55 to +150	°C
Power Dissipation	P_D	36	W
Short Circuit Output Current	I_{OS}	50	mA
Short Circuit Output Current (PD)	I_{OUTPD}	60	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional Operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage reference to V_{SS}, T_A=0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	3.0	3.3	3.6	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.0	—	V_{CC}+0.3*	V
Input Low Voltage	V_{IL}	-0.3**	—	0.8	V

* V_{CC}+1.3V at pulse width ≤15ns which is is measured at V_{CC}

** -1.3V at pulse width ≤15ns which is is measured at V_{SS}

DC AND OPERATION CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter		Symbol	Min	Max	Units
Operating Current* ($\overline{RAS}$, $\overline{CAS}$ Cycling @t_{RC}=min.)	WPD32M72V-60 WPD32M72V-70	I_{CC1}	— —	1638 1458	mA mA
Standby Current ($\overline{RAS}$=$\overline{CAS}$=V_{IH})		I_{CC2}	—	36	mA
$\overline{RAS}$-Only Refresh Current* ($\overline{CAS}$=V_{IH}, $\overline{RAS}$ Cycling @t_{RC}=min.)	WPD32M72V-60 WPD32M72V-70	I_{CC3}	— —	1638 1458	mA mA
Fast Page Mode Current* ($\overline{RAS}$=V_{IL}, $\overline{CAS}$, Address Cycling @ t_{PC}=min.)	WPD32M72V-60 WPD32M72V-70	I_{CC4}	— —	1098 1008	mA mA
Standby Current ($\overline{RAS}$=$\overline{CAS}$=V_{CC}-0.2V)		I_{CC5}	—	18	mA
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current* ($\overline{RAS}$ and $\overline{CAS}$ Cycling @t_{RC}=min.)	WPD32M72V-60 WPD32M72V-70	I_{CC6}	— —	1638 1458	mA mA
Input Leakage Current (Any input 0≤V_{IN}≤V_{CC}+0.3V, all other pins not under test=0V)	All but $\overline{RAS}$ $\overline{RAS}$	I_{IL}	-10 -45	10 45	µA µA
Output Leakage Current (Data out is disabled, 0≤V_{OUT}≤V_{CC})		I_{OL}	-10	10	µA
Output High Voltage Level (I_{OH}=-2mA)		V_{OH}	2.4	—	V
Output Low Voltage Level (I_{OL}=2mA)		V_{OL}	—	0.4	V

*I_{CC1}, I_{CC3}, I_{CC4}, and I_{CC6} are dependent on output loading and cycling rates. Specified values are obtained with the output open. I_{CC} is specified as an average current. In I_{CC1}, I_{CC6} and I_{CC3}, address can be changed maximum once while $\overline{RAS}$=V_{IL}. In I_{CC4}, address can be changed maximum once within one fast page mode cycle time, t_{PC}.

CAPACITANCE (T_A=25 °C)

Item	Symbol	Min	Max	Units
Input Capacitance (A_0, B_0)	C_{IN1}	—	13	pF
Input Capacitance (A_{1-9})	C_{IN1}	—	13	pF
Input Capacitance ($\overline{CAS}$, $\overline{WE}$, $\overline{OE}$)	C_{IN2}	—	13	pF
Input Capacitance ($\overline{RAS}$)	C_{IN3}	—	63	pF
Input/Output Capacitance (DQ_x)	C_{IO1}	—	14	pF

AC CHARACTERISTICS (0 °C≤T_A≤70 °C, V_{CC}=3.3V±0.3V, See notes 1, 2, 3, and 4)

Parameter	Symbol	WPD32M72V-60		WPD32M72V-70		Unit	Notes
		Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	110		130		ns	
Access time from $\overline{RAS}$	t_{RAC}		60		70	ns	11, 12
Access time from $\overline{CAS}$	t_{CAC}		20		25	ns	11, 12
Access time from column address	t_{AA}		36		41	ns	11, 12
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	2		2		ns	
Output buffer turn-off delay	t_{OFF}	2	20	2	25	ns	14
Transition time (rise and fall)	t_T	3	30	3	30	ns	2
$\overline{RAS}$ precharge time	t_{RP}	40		50		ns	
$\overline{RAS}$ pulse width	t_{RAS}	60	10,000	70	10,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	20		25		ns	
$\overline{CAS}$ hold time	t_{CSH}	58		68		ns	
$\overline{CAS}$ pulse width	t_{CAS}	15		20		ns	5
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	18	40	18	45	ns	6
$\overline{RAS}$ to column address delay time	t_{RAD}	13	24	13	29	ns	7
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	15		15		ns	
Row address set-up time	t_{ASR}	6		6		ns	
Row address hold time	t_{RAH}	8		8		ns	
Column address set-up time	t_{ASC}	4		4		ns	
Column address hold time	t_{CAH}	17		17		ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	36		41		ns	
Column address to $\overline{CAS}$ lead time	t_{CAL}	36		41		ns	
Read command set-up time	t_{RCS}	2		2		ns	
Read command hold referenced to $\overline{CAS}$	t_{RCH}	2		2		ns	13
Read command hold referenced to $\overline{RAS}$	t_{RRH}	3		3		ns	13
Write command hold time	t_{WCH}	17		17		ns	
Write command pulse width	t_{WP}	15		15		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	20		25		ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	17		22		ns	
Data-in set-up time	t_{DS}	-2		-2		ns	10

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AC CHARACTERISTICS (continued)

Parameter	Symbol	WPD32M72V-60		WPD32M72V-70		Unit	Notes
		Min	Max	Min	Max		
Data-in hold time	t_{DH}	20		20		ns	10
Refresh period	t_{REF}		64		64	ms	15
Write command set-up time	t_{WCS}	2		2		ns	9
$\overline{CAS}$ set-up time (C-B-R refresh)	t_{CSR}	15		15		ns	
$\overline{CAS}$ hold time (C-B-R refresh)	t_{CHR}	18		18		ns	
$\overline{RAS}$ precharge to $\overline{CAS}$ hold time	t_{RPC}	3		3		ns	
Access time from $\overline{CAS}$ precharge	t_{CPA}		40		45	ns	11, 12
Fast Page mode cycle time	t_{PC}	40		45		ns	
$\overline{CAS}$ precharge time (fast page)	t_{CP}	10		10		ns	
$\overline{RAS}$ pulse width (fast page)	t_{RASP}	60	100,000	70	100,000	ns	
$\overline{WE}$ to $\overline{RAS}$ precharge time (C-B-R refresh)	t_{WRP}	15		15		ns	
$\overline{WE}$ to $\overline{RAS}$ hold time (C-B-R refresh)	t_{WRH}	8		8		ns	
$\overline{OE}$ to D_{IN} delay time	t_{ODD}	20		25		ns	8
$\overline{OE}$ delay time from D_{IN}	t_{DZO}	-2		-2		ns	
$\overline{CAS}$ delay time from D_{IN}	t_{DZC}	-2		-2		ns	
Access time from $\overline{OE}$	t_{OEA}		20		25	ns	11, 12
Output data hold time	t_{OH}	2		2		ns	
Output data hold time from $\overline{OE}$	t_{OHO}	2		2		ns	
Output buffer turn-off delay from $\overline{OE}$	t_{OEZ}	2	20	2	25	ns	14
$\overline{CAS}$ to D_{IN} delay time	t_{CDD}	20		25		ns	8
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{CPRH}	40		45		ns	
Read-Modify-Write cycle time	t_{RWC}	158		188		ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	t_{RWD}	83		98		ns	9
$\overline{CAS}$ to $\overline{WE}$ delay time	t_{CWD}	45		55		ns	9
Column address to $\overline{WE}$ delay time	t_{AWD}	59		69		ns	9
$\overline{OE}$ command hold time	t_{OEH}	15		20		ns	
Fast Page Mode Read-Modify-Write cycle	t_{PRWC}	83		98		ns	
$\overline{WE}$ delay time from $\overline{CAS}$ precharge	t_{CPW}	63		73		ns	9
$\overline{PDE}$ to valid presence detect data	t_{PD}		10		10	ns	11
$\overline{PDE}$ inactive to presence detects inactive	t_{PDOFF}	0	10	0	10	ns	16

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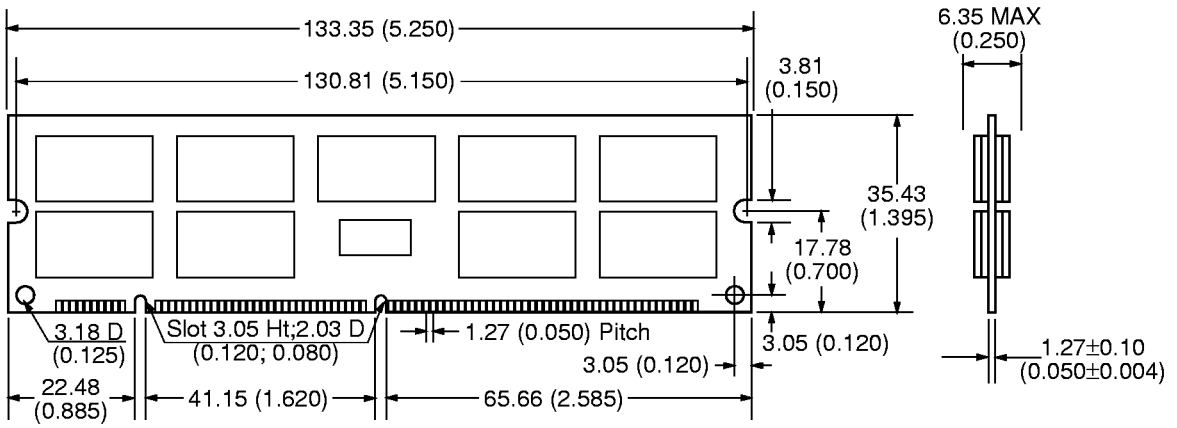
AC CHARACTERISTICS (continued)

Notes

1. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
2. An initial pause of 200µs is required after power-up followed by 8 $\overline{RAS}$-only refresh cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ refresh cycles instead of 8 $\overline{RAS}$-only refresh cycles is required. The DRAM outputs will remain disabled until these 8 cycles have occurred. This prevents data contention (excessive current) during power on. To prevent excess power dissipation during power-up, $\overline{RAS}$ should rise coincident with the power supply voltage.
3. The specified timings include buffer, loading, and skew delay adders: 2ns minimum, 5ns ($\overline{CAS}$, $\overline{WE}$, $\overline{OE}$) or 6ns (address) maximum delay, no pulse shrinkage to the DRAM device timings. The data and $\overline{RAS}$ signals are not buffered, which preserves the DRAM access specifications of 60ns and 70ns.
4. AC measurements assume t_T = 5ns.
5. The minimum t_{CAS} requires t_{CSH} to be met for both writes and reads. Also, because of the buffer, the minimum t_{CAS} for a read cycle must be extended to guarantee the data out window (t_{OH}) in the application. For example, a t_{CAS} of 15ns plus a minimum t_{OH} of 2ns would result in turning data out of the DIMM at 17ns (3ns before max t_{CAC} of 20ns).
6. Operation within the t_{RCD}(max) limit ensures that t_{RAC}(max) can be met. The t_{RCD}(max) is specified as a reference point only: If t_{RCD} is greater that the specified t_{RCD}(max) limit, then access time is controlled by t_{CAC}.
7. Operation within the t_{RAD}(max) limit ensures that t_{RAC}(max) can be met. The t_{RAD}(max) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD}(max) limit, then access time is controlled by t_{AA}.
8. Either t_{CDD} or t_{ODD} must be satisfied.
9. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD}, and t_{CPW} are not restrictive parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$(min), the entire cycle is an early write cycle and the data pin will remain open circuit (high impedance) through the entire cycle. If $t_{RWD} \geq t_{RWD}$(min), $t_{CWD} \geq t_{CWD}$(min), $t_{AWD} \geq t_{AWD}$(min), and $t_{CPW} \geq t_{CPW}$(min)(Fast Page Mode), the cycle is a Read-Modify-Write cycle and the data will contain read from the selected cell. If neither of the above sets of conditions are met, the condition of the data (at access time) is indeterminate.
10. Data-in set-up and hold is measured from the latter of the two timings, $\overline{CAS}$ or $\overline{WE}$.
11. Measured with the specified current load and 100pF.
12. Access time is determined by the latter of t_{RAC}, t_{CAC}, t_{CPA}, t_{AA}, t_{OEA}.
13. Either t_{RCH} or t_{RRH} must be satisfied.
14. t_{OFF}(max) and t_{OEZ}(max) define the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
15. 8192 refreshes are required every 64ms.
16. t_{PDOFF}(max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

PACKAGE: 168-PIN DIMM



±0.13 (±0.005) TOLERANCE UNLESS OTHERWISE SPECIFIED
ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

ORDERING INFORMATION

W P D 32M72 V - X MD C X

LEAD FINISH:
T = Tin Edge Connectors
Blank = Gold Edge Connectors

DEVICE GRADE:
C = Commercial 0 to + 70°C

PACKAGE TYPE:
MD = 168 pin DIMM

ACCESS TIME (ns)

3.3V ± 0.3V Supply Voltage

ORGANIZATION, 32M x 72

DRAM

Plastic Module

WHITE MICROELECTRONICS