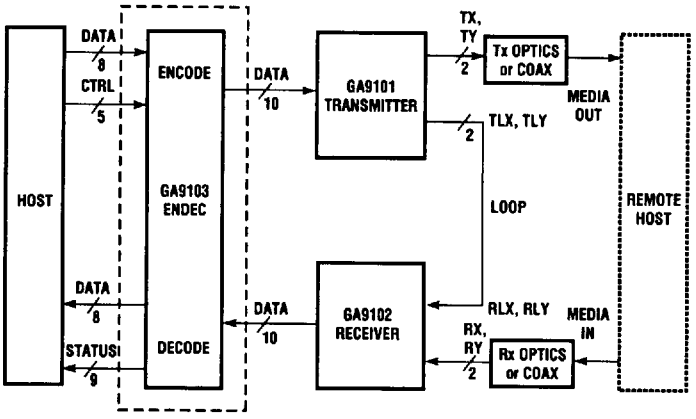


TriQuint's GA9103 is one of the three devices of the FC–265 chip set designed to support the requirements of Fiber Channel Standard X3T9.3. The GA9103 is an encoder/decoder (ENDEC) integrated circuit which implements the 8b/10b encoding/decoding scheme for data, ordered sets and line states associated with the Fiber Channel Physical Level Standard (FC-PH). In addition, the CMOS ENDEC chip performs 32-bit CRC and parity generate/check functions. It interfaces to TriQuint's GA9101 and GA9102 Transmitter and Receiver, respectively, and to either the fabric or the device link protocol controller.

The FC–265 (GA9101, GA9102 and GA9103) provides a comprehensive electrical and physical interface for Fiber Channel. These chips are designed to operate at 265.625 Megabaud, one of the operating speeds specified by the standard.

The Fiber Channel provides a transport vehicle for the upper layer Intelligent Peripheral Interface (IPI) and Small Computer System Interface (SCSI) command sets, the High-Performance Parallel Interface (HIPPI) data link layer, and other user-defined command sets. The Fiber Channel is capable of replacing the SCSI, IPI, and HIPPI physical interfaces with a protocol-efficient alternative that provides performance improvements in distance and/or speed.

IPI and SCSI commands and HIPPI data link operations may all be intermixed on the Fiber Channel. Proprietary and other command sets may also use and share the Fiber Channel. See Figure 1.

The Fiber Channel is optimized for predictable transfers of large blocks of data such as those used in file transfers between processors (supercomputer, mainframe, super-mini, etc.), storage systems (disk and tape), communications, and output-only devices such as laser printers and raster-scan graphics terminals.

GA9103

265 Mbaud Fiber Channel ENDEC

Features

- *For Fiber Channel, point-to-point, network, and SCSI applications*
- *With fiber optics, the FC-265 chip set provides a complete FC-0, FC-1 solution*
- *8b/10b Encode/Decode of data, ordered sets, and line states*
- *TTL-compatible 10-bit-wide Transmitter/Receiver interface with 26.5625 MHz byte clock*
- *CRC and Parity Generate/Check*
- *Common chip for fabric and device adapters*
- *Multiplexed data/control 8-bit system interface*
- *68-pin PLCC*

The Transmitter/Receiver chips, designed with TriQuint's proprietary 0.7 micron One-Up™GaAs process, interface either directly to the electrical medium or to the fiber-optic interface. The chips implement parallel-to-serial conversion, bit clock generation, receive clock/data recovery, and serial-to-parallel conversion.

The Fiber Channel protocol is simple and economical and enhances system throughput. The transmission medium is isolated from the control protocol so that implementation of point-to-point links, multi-drop buses, rings, crosspoint switches, or other special implementations may be made in a technology best suited to the usage environment. Fiber channel is organized into five layers as shown in Figure 1. With this standard, the user may communicate over distances up to 10 km at baud rates of 132.8125 Megabaud to 1.0625 Gigabaud. This standard will support links over coaxial and fiber-optic cables.

Along with a fiber-optic module, this chipset will provide complete FC-0 and FC-1 solutions for a Fiber Channel data link.

GA9103 ENDEC Block Diagram

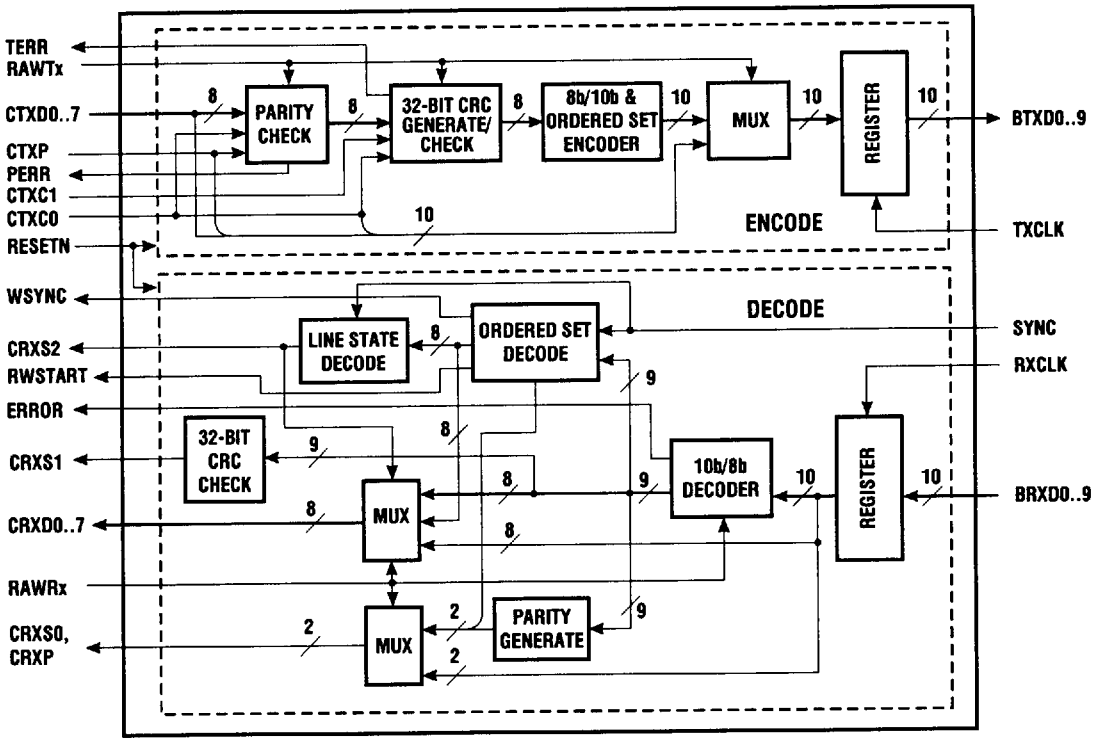
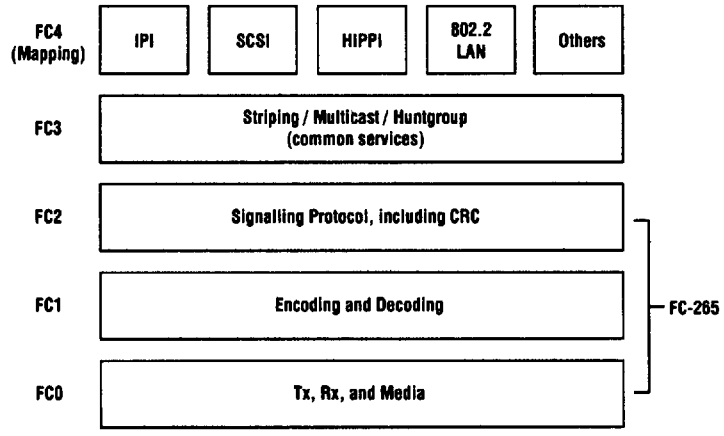


Figure 1. Layers of Fiber Channel



Functional Description

The GA9103 has an 8-bit interface to the host side and a 10-bit interface to the Transmitter (Tx) and the Receiver (Rx). The device has two major independent functional blocks, the ENCODE and the DECODE. The ENCODE block interfaces with the Tx and the DECODE with the Rx. Below are the details of the two functional blocks.

Encode

The PARITY CHECK block compares the input odd parity with that of the incoming data, CTXD0..7 and CTXC0. If the number of ones in the input is an even number, CTXP will be HIGH. If the number of ones in the input data is odd, CTXP will be LOW. If there is a parity error, it is flagged through the PERR signal. In the pass-through mode (RAWTx=1), PERR is forced to zero.

The 32-bit Generate/Check CRC block either generates or checks the 32-bit CRC for the incoming 8-bit bus, CTXD0..7. The methodology, polynomials, and equations for the 32-bit CRC are the same as the FDDI's Frame Check Sequence, as adopted by Fiber Channel. A 32-bit CRC is computed for every frame and the computation begins after the receipt of the Start-of-Frame (SOF) ordered set and finishes one byte before the End-of-Frame (EOF). The CRC corresponds to the ones complement of the remainder obtained by dividing the frame sequence polynomial H(x) by the following generator polynomial:

$$G(x) = X^{32} + X^{26} + X^{23} + X^{22} + X^{16} + X^{12} + X^{11} + X^{10} + X^8 + X^7 + X^5 + X^4 + X^2 + X + 1$$

The frame sequence polynomial is formed as follows: the bits of the frame are treated as a coefficient of a polynomial D(x) of order k, where k is one degree less than the total number of bits. The polynomial H(x) is formed by multiplying D(x) by X^{32} and inverting the 32 terms of the resulting polynomial starting at the X(k+32) term. The order of computation within a byte is made starting with the least significant bit (CTXD0) and continuing through to the most significant bit (CTXD7). The CRC is appended to the incoming data, starting with the most significant coefficient (X^{31}) and continuing through to the least significant coefficient.

The CRC check is performed by checking the remainder at the end of the incoming frame against the expected value. If the incoming CRC is correct, the remainder should be "C704DD7B" (Hex), in the order of reception. If an error occurs, it is flagged by the TERR pin. In the pass-through mode, the CRC function is disabled. The Generate CRC function is enabled at the device interface and the Check CRC function is enabled at the fabric interface by means of the CTXC1 input signal. A logic HIGH on the CTXC1 pin indicates the Generate CRC function is selected, while a logic LOW indicates that the Check CRC is selected. When initiated, the Generate/Check CRC commences after the Start-of-Frame signal, and ends prior to the End-of-Frame signal. (See Figures 3 and 4.)

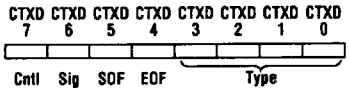
To start the computation of the 32-bit Generate CRC mode in the ENCODE block, the following conditions must be met: CTXC1 is HIGH, the previous encoded word was Start-of-Frame (SOF), and the CTXC0 signal goes from HIGH to LOW. The CRC computation is complete when the CTXC0 signal goes back HIGH. The CTXC0 signal must be HIGH for at least four byte clocks in order to append the CRC to the transmitted data. In the Generate CRC mode, the signal at the TERR pin (CRC Error) is LOW. The timing for the Generate CRC mode is shown in Figure 3. While the internal logic does check for parity during the CRC Append cycle, the four input bytes at CTXD0..7 are ignored.

To initiate the 32-bit Check CRC mode in the ENCODE block, the following state is required: the CTXC0 signal goes from HIGH to LOW, the previous encoded ordered set was SOF, and CTXC1 is LOW. When the CTXC0 signal goes back to HIGH, the CRC computation is complete. The computed value is compared to "C704DD7B" (Hex) to see if an error occurred. If there is a CRC error, it is flagged through the TERR pin going HIGH for one byte time at the End-of-Frame. The timing for the Check CRC mode is shown in the figure below and in Figure 4.

The 8b/10b and Ordered Set ENCODER encodes the data as per the Fiber Channel rules for encoding. The encoding of valid data and special characters are shown in Tables 1 and 2. The tables have two columns of encoded output based on the current Running Disparity (R_D). The current Running Disparity may be positive or negative on power up, but on RESETN being activated, it is always negative. A new Running Disparity is calculated from the transmitted character. It is forced negative if: 1) **Sig** = 1, CTXC0 = 1, and the Ordered Set encode is a primitive, such as R-Rdy, etc., or 2) when the link exits the diagnostic (RAW) mode. The ordered sets are then encoded according to Table 3. Each ordered set is four bytes wide.

The ordered set encoding procedure is as follows: the ENCODER looks at the CXTD0..7 signal inputs while the Ordered Set, CXTC0, signal is HIGH and encodes four bytes, based on the contents of CTXD0..7. The contents of CTXD0..7 in the next three bytes are ignored.

Figure 2. Data Fields for Fiber Channel Ordered Set Encoding



The fields within the first byte, CTXD0..7, of the word for the Ordered Set Encoding is shown in Figure 2. CTXD7 corresponds to the **Cntl** signal. The **Cntl** signal, when LOW, indicates Fiber Channel-defined ordered sets are being transmitted. When the **Cntl** signal is HIGH, undefined ordered sets are being transmitted. The **Sig** signal (CTXD6), when HIGH, indicates the Line State ordered set is being transmitted, and, when LOW, indicates an ordered set other than the Line State is being transmitted. **SOF** (CTXD5), when HIGH, indicates the Start-of-Frame ordered set is being transmitted, and **EOF** (CTXD4), when HIGH, indicates the End-of-Frame ordered set is being transmitted. **Type** (CTXD3..0) indicates the type of ordered sets within the SOF, EOF, Line States and Undefined categories that is being transmitted.

If PERR or TERR is HIGH within a frame, EOF_n and EOF_t for that particular frame are transmitted as EOF_{ni} (see Table 3). Similarly, if PERR or TERR is HIGH while EOF_{dt} is being transmitted, it is encoded as EOF_{dti}, to indicate an invalid condition at the node.

The MUX selects between the 8b/10b ENCODER output and the data inputs, CTXD0..7. When the RAWTx input signal is HIGH, the inputs CTXD0..7, CTXP, and CTXC0 are selected, and TERR = 0. When the RAWTx input is LOW, the ENCODER output is selected. The output of the MUX is 10 bits wide and is clocked into the REGISTER using the transmit byte clock, TXCLK, from the Transmitter chip, GA9101. The output of the REGISTER interface goes directly to the GA9101, the Transmitter I.C. of the FC-265.

The asynchronous RESETN input, when LOW, is used to clear all internal state machine registers. It will take up to five byte clocks to clear the internal state machines after the RESETN input goes back HIGH.

The bit ordering for transmission in the RAW mode is CTXD0..7, CTXP1 and CTXC0. It corresponds to mapping these signals to BTXD9..0, respectively.

CRC Error Timing

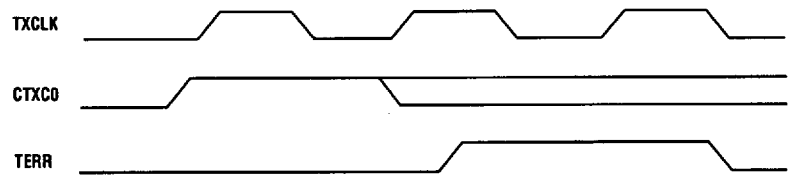
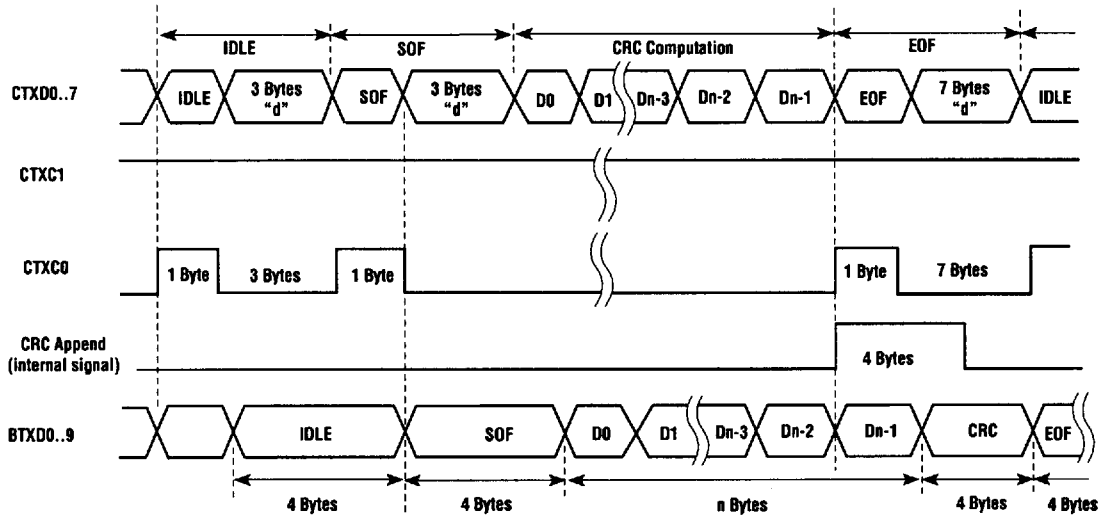


Figure 3. Generate CRC Mode Timing



"n" is the data packet size. "n" is divisible by 4
"d" is "don't care," but parity is checked.

Figure 4. Check CRC Mode Timing

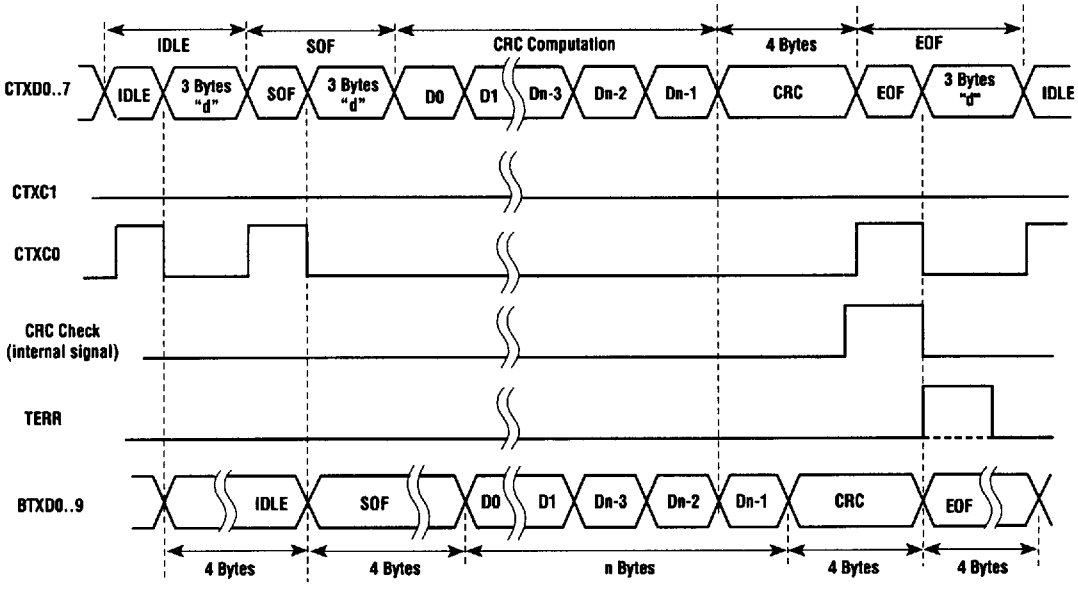


Table 1. Valid Data Characters – Encoding

Data Byte Name	Bits HGF	Bits EDCBA [1]	Current RD – abcdei	Current RD – fghj [2]	Current RD + abcdei	Current RD + fghj [2]
D0.0	000	00000	100111	0100	011000	1011
D1.0	000	00001	011101	0100	100010	1011
D2.0	000	00010	101101	0100	010010	1011
D3.0	000	00011	110001	1011	110001	0100
D4.0	000	00100	110101	0100	001010	1011
D5.0	000	00101	101001	1011	101001	0100
D6.0	000	00110	011001	1011	011001	0100
D7.0	000	00111	111000	1011	000111	0100
D8.0	000	01000	111001	0100	000110	1011
D9.0	000	01001	100101	1011	100101	0100
D10.0	000	01010	010101	1011	010101	0100
D11.0	000	01011	110100	1011	110100	0100
D12.0	000	01100	001101	1011	001101	0100
D13.0	000	01101	101100	1011	101100	0100
D14.0	000	01110	011100	1011	011100	0100
D15.0	000	01111	010111	0100	101000	1011
D16.0	000	10000	011011	0100	100100	1011
D17.0	000	10001	100011	1011	100011	0100
D18.0	000	10010	010011	1011	010011	0100
D19.0	000	10011	110010	1011	110010	0100
D20.0	000	10100	001011	1011	001011	0100
D21.0	000	10101	101010	1011	101010	0100
D22.0	000	10110	011010	1011	011010	0100
D23.0	000	10111	111010	0100	000101	1011
D24.0	000	11000	110011	0100	001100	1011
D25.0	000	11001	100110	1011	100110	0100
D26.0	000	11010	010110	1011	010110	0100
D27.0	000	11011	110110	0100	001001	1011
D28.0	000	11100	001110	1011	001110	0100
D29.0	000	11101	101110	0100	010001	1011
D30.0	000	11110	011110	0100	100001	1011
D31.0	000	11111	101011	0100	010100	1011
D0.1	001	00000	100111	1001	011000	1001
D1.1	001	00001	011101	1001	100010	1001
D2.1	001	00010	101101	1001	010010	1001
D3.1	001	00011	110001	1001	110001	1001
D4.1	001	00100	110101	1001	001010	1001
D5.1	001	00101	101001	1001	101001	1001
D6.1	001	00110	011001	1001	011001	1001
D7.1	001	00111	111000	1001	000111	1001
D8.1	001	01000	111001	1001	000110	1001
D9.1	001	01001	100101	1001	100101	1001
D10.1	001	01010	010101	1001	010101	1001
D11.1	001	01011	110100	1001	110100	1001
D12.1	001	01100	001101	1001	001101	1001
D13.1	001	01101	101100	1001	101100	1001
D14.1	001	01110	011100	1001	011100	1001
D15.1	001	01111	010111	1001	101000	1001
D16.1	001	10000	011011	1001	100100	1001
D17.1	001	10001	100011	1001	100011	1001
D18.1	001	10010	010011	1001	010011	1001
D19.1	001	10011	110010	1001	110010	1001
D20.1	001	10100	001011	1001	001011	1001
D21.1	001	10101	101010	1001	101010	1001
D22.1	001	10110	011010	1001	011010	1001
D23.1	001	10111	111010	1001	000101	1001
D24.1	001	11000	110011	1001	001100	1001
D25.1	001	11001	100110	1001	100110	1001
D26.1	001	11010	010110	1001	010110	1001
D27.1	001	11011	110110	1001	001001	1001
D28.1	001	11100	001110	1001	001110	1001
D29.1	001	11101	101110	1001	010001	1001
D30.1	001	11110	011110	1001	100001	1001
D31.1	001	11111	101011	1001	010100	1001
D0.2	010	00000	100111	0101	011000	0101
D1.2	010	00001	011101	0101	100010	0101
D2.2	010	00010	101101	0101	010010	0101
D3.2	010	00011	110001	0101	110001	0101
D4.2	010	00100	110101	0101	001010	0101
D5.2	010	00101	101001	0101	101001	0101
D6.2	010	00110	011001	0101	011001	0101
D7.2	010	00111	111000	0101	000111	0101
D8.2	010	01000	111001	0101	000110	0101

Data Byte Name	Bits HGF	Bits EDCBA [1]	Current RD – abcdei	Current RD – fghj [2]	Current RD + abcdei	Current RD + fghj [2]
D9.2	010	01001	100101	0101	100101	0101
D10.2	010	01010	010101	0101	010101	0101
D11.2	010	01011	110100	0101	110100	0101
D12.2	010	01100	001101	0101	001101	0101
D13.2	010	01101	101100	0101	101100	0101
D14.2	010	01110	011100	0101	011100	0101
D15.2	010	01111	010111	0101	101000	0101
D16.2	010	10000	011011	0101	100100	0101
D17.2	010	10001	100011	0101	100011	0101
D18.2	010	10010	010011	0101	010011	0101
D19.2	010	10011	110010	0101	110010	0101
D20.2	010	10100	001011	0101	001011	0101
D21.2	010	10101	101010	0101	101010	0101
D22.2	010	10110	011010	0101	011010	0101
D23.2	010	10111	111010	0101	000101	0101
D24.2	010	11000	110011	0101	001100	0101
D25.2	010	11001	100110	0101	100110	0101
D26.2	010	11010	010110	0101	010110	0101
D27.2	010	11011	110110	0101	001001	0101
D28.2	010	11100	001110	0101	001110	0101
D29.2	010	11101	101110	0101	010001	0101
D30.2	010	11110	011110	0101	100001	0101
D31.2	010	11111	101011	0101	010100	0101
D0.3	011	00000	100111	0011	011000	1100
D1.3	011	00001	011101	0011	100010	1100
D2.3	011	00010	101101	0011	010010	1100
D3.3	011	00011	110001	1100	110001	0011
D4.3	011	00100	110101	0011	001010	1100
D5.3	011	00101	101001	1100	101001	0011
D6.3	011	00110	011001	1100	011001	0011
D7.3	011	00111	111000	1100	000111	0011
D8.3	011	01000	111001	0011	000110	1100
D9.3	011	01001	100101	1100	100101	0011
D10.3	011	01010	010101	1100	010101	0011
D11.3	011	01011	110100	1100	110100	0011
D12.3	011	01100	001101	1100	001101	0011
D13.3	011	01101	101100	1100	101100	0011
D14.3	011	01110	011100	1100	011100	0011
D15.3	011	01111	010111	0011	101000	1100
D16.3	011	10000	011011	0011	100100	1100
D17.3	011	10001	100011	1100	100011	0011
D18.3	011	10010	010011	1100	010011	0011
D19.3	011	10011	110010	1100	110010	0011
D20.3	011	10100	001011	1100	001011	0011
D21.3	011	10101	101010	1100	101010	0011
D22.3	011	10110	011010	1100	011010	0011
D23.3	011	10111	111010	0011	000101	1100
D24.3	011	11000	110011	0011	001100	1100
D25.3	011	11001	100110	1100	100110	0011
D26.3	011	11010	010110	1100	010110	0011
D27.3	011	11011	110110	0011	001001	1100
D28.3	011	11100	001110	1100	001110	0011
D29.3	011	11101	101110	0011	010001	1100
D30.3	011	11110	011110	0011	100001	1100
D31.3	011	11111	101011	0011	010100	1100
D0.4	100	00000	100111	0010	011000	1101
D1.4	100	00001	011101	0010	100010	1101
D2.4	100	00010	101101	0010	010010	1101
D3.4	100	00011	110001	1101	110001	0010
D4.4	100	00100	110101	0010	001010	1101
D5.4	100	00101	101001	1101	101001	0010
D6.4	100	00110	011001	1101	011001	0010
D7.4	100	00111	111000	1101	000111	0010
D8.4	100	01000	111001	0010	000110	1101
D9.4	100	01001	100101	1101	100101	0010
D10.4	100	01010	010101	1101	010101	0010
D11.4	100	01011	110100	1101	110100	0010
D12.4	100	01100	001101	1101	001101	0010
D13.4	100	01101	101100	1101	101100	0010
D14.4	100	01110	011100	1101	011100	0010
D15.4	100	01111	010111	0010	101000	1101
D16.4	100	10000	011011	0010	100100	1101
D17.4	100	10001	100011	1101	100011	0010

Table 1. Valid Data Characters – Encoding (cont.)

Data Byte Name	Bits HGF	Bits EDCBA [1]	Current RD – abcdei	Current RD – fghj [2]	Current RD + abcdei	Current RD + fghj [2]
D16.4	100	10010	010011	1101	010011	0010
D19.4	100	10011	110010	1101	110010	0010
D20.4	100	10100	001011	1101	001011	0010
D21.4	100	10101	101010	1101	101010	0010
D22.4	100	10110	011010	1101	011010	0010
D23.4	100	10111	111010	0010	000101	1101
D24.4	100	11000	110011	0010	001100	1101
D25.4	100	11001	100110	1101	100110	0010
D26.4	100	11010	010110	1101	010110	0010
D27.4	100	11011	110110	0010	001001	1101
D28.4	100	11100	001110	1101	001110	0010
D29.4	100	11101	101110	0010	010001	1101
D30.4	100	11110	011110	0010	100001	1101
D31.4	100	11111	101011	0010	010100	1101
D0.5	101	00000	100111	1010	011000	1010
D1.5	101	00001	011101	1010	100010	1010
D2.5	101	00010	101101	1010	010010	1010
D3.5	101	00011	110001	1010	110001	1010
D4.5	101	00100	110101	1010	001010	1010
D5.5	101	00101	101001	1010	101001	1010
D6.5	101	00110	011001	1010	011001	1010
D7.5	101	00111	111000	1010	000111	1010
D8.5	101	01000	111001	1010	000110	1010
D9.5	101	01001	100101	1010	100101	1010
D10.5	101	01010	010101	1010	010101	1010
D11.5	101	01011	110100	1010	110100	1010
D12.5	101	01100	001101	1010	001101	1010
D13.5	101	01101	101100	1010	101100	1010
D14.5	101	01110	011100	1010	011100	1010
D15.5	101	01111	010111	1010	101000	1010
D16.5	101	10000	011011	1010	100100	1010
D17.5	101	10001	100011	1010	100011	1010
D18.5	101	10010	010011	1010	010011	1010
D19.5	101	10011	110010	1010	110010	1010
D20.5	101	10100	001011	1010	001011	1010
D21.5	101	10101	101010	1010	101010	1010
D22.5	101	10110	011010	1010	011010	1010
D23.5	101	10111	111010	1010	000101	1010
D24.5	101	11000	110011	1010	001100	1010
D25.5	101	11001	100110	1010	100110	1010
D26.5	101	11010	010110	1010	010110	1010
D27.5	101	11011	110110	1010	001001	1010
D28.5	101	11100	001110	1010	001110	1010
D29.5	101	11101	101110	1010	010001	1010
D30.5	101	11110	011110	1010	100001	1010
D31.5	101	11111	101011	1010	010100	1010
D0.6	110	00000	100111	0110	011000	0110
D1.6	110	00001	011101	0110	100010	0110
D2.6	110	00010	101101	0110	010010	0110
D3.6	110	00011	110001	0110	110001	0110
D4.6	110	00100	110101	0110	001010	0110
D5.6	110	00101	101001	0110	101001	0110
D6.6	110	00110	011001	0110	011001	0110
D7.6	110	00111	111000	0110	000111	0110
D8.6	110	01000	111001	0110	000110	0110
D9.6	110	01001	100101	0110	100101	0110
D10.6	110	01010	010101	0110	010101	0110
D11.6	110	01011	110100	0110	110100	0110
D12.6	110	01100	001101	0110	001101	0110
D13.6	110	01101	101100	0110	101100	0110
D14.6	110	01110	011100	0110	011100	0110
D15.6	110	01111	010111	0110	101000	0110
D16.6	110	10000	011011	0110	100100	0110
D17.6	110	10001	100011	0110	100011	0110
D18.6	110	10010	010011	0110	010011	0110
D19.6	110	10011	110010	0110	110010	0110
D20.6	110	10100	001011	0110	001011	0110
D21.6	110	10101	101010	0110	101010	0110
D22.6	110	10110	011010	0110	011010	0110
D23.6	110	10111	111010	0110	000101	0110
D24.6	110	11000	110011	0110	001100	0110
D25.6	110	11001	100110	0110	100110	0110
D26.6	110	11010	010110	0110	010110	0110
D27.6	110	11011	110110	0110	001001	0110
D28.6	110	11100	001110	0110	001110	0110
D29.6	110	11101	101110	0110	010001	0110
D30.6	110	11110	011110	0110	100001	0110
D31.6	110	11111	101011	0110	010100	0110
D0.7	111	00000	100111	0001	011000	1110
D1.7	111	00001	011101	0001	100010	1110
D2.7	111	00010	101101	0001	010010	1110
D3.7	111	00011	110001	1110	110001	0001
D4.7	111	00100	110101	0001	001010	1110
D5.7	111	00101	101001	1110	101001	0001
D6.7	111	00110	011001	1110	011001	0001
D7.7	111	00111	111000	1110	000111	0001
D8.7	111	01000	111001	0001	000110	1110
D9.7	111	01001	100101	1110	100101	0001
D10.7	111	01010	010101	1110	010101	0001
D11.7	111	01011	110100	1110	110100	1000
D12.7	111	01100	001101	1110	001101	0001
D13.7	111	01101	101100	1110	101100	1000
D14.7	111	01110	011100	1110	011100	1000
D15.7	111	01111	010111	0001	101000	1110
D16.7	111	10000	011011	0001	100100	1110
D17.7	111	10001	100011	0111	100011	0001
D18.7	111	10010	010011	0111	010011	0001
D19.7	111	10011	110010	1110	110010	0001
D20.7	111	10100	001011	0111	001011	0001
D21.7	111	10101	101010	1110	101010	0001
D22.7	111	10110	011010	1110	011010	0001
D23.7	111	10111	111010	0001	000101	1110
D24.7	111	11000	110011	0001	001100	1110
D25.7	111	11001	100110	1110	100110	0001
D26.7	111	11010	010110	1110	010110	0001
D27.7	111	11011	110110	0001	001001	1110
D28.7	111	11100	001110	1110	001110	0001
D29.7	111	11101	101110	0001	010001	1110
D30.7	111	11110	011110	0001	100001	1110
D31.7	111	11111	101011	0001	010100	1110

Table 2. Valid Special Characters – Encoding

Special Code Name	Current RD – abcdei	Current RD – fghj [2]	Current RD + abcdei	Current RD + fghj [2]
K28.0	001111	0100	110000	1011
K28.1	001111	1001	110000	0110
K28.2	001111	0101	110000	1010
K28.3	001111	0011	110000	1100
K28.4	001111	0010	110000	1101
K28.5	001111	1010	110000	0101
K28.6	001111	0110	110000	1001
K28.7	001111	1000	110000	0111
K23.7	111010	1000	000101	0111
K27.7	110110	1000	001001	0111
K29.7	101110	1000	010001	0111
K30.7	011110	1000	100001	0111

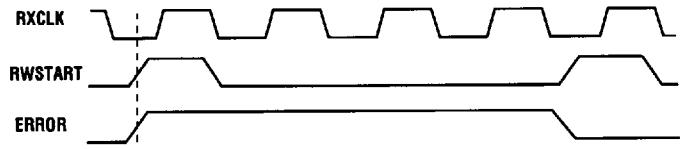
NOTES: *1. "HGF EDCBA" correspond to Data Inputs CTXD7..0, in that order.*
2. "a" is to be transmitted first, followed by "b", "c", ..., "j". "abcdeifghj", in that order, correspond to BTXD9 . . BTXD0.

Table 3. Ordered Set Encoding – Fiber Channel

C-Interface Signals (Mode: $\overline{\text{Raw}}$) Inputs (CTxD7..0)										8Tx D 9..0
Function	**Byte 1**					**Byte 2**	**Byte 3**	**Byte 4**	**Begin. RD**	**Output (4 Encoded Bytes)**
	Cntl	**Sig**	**SOF**	**EOF**	**Type**					**Byte 1-Byte 2-Byte 3-Byte 4**
SOFn1[3]	0	0	1	0	0001	_[1]	_[1]	_[1]	Neg	(K28.5–D21.5–D23.1–D23.1)
SOFn2	0	0	1	0	0010	_[1]	_[1]	_[1]	Neg	(K28.5–D21.5–D21.1–D21.1)
SOFn3	0	0	1	0	0011	_[1]	_[1]	_[1]	Neg	(K28.5–D21.5–D22.1–D22.1)
SOFi1	0	0	1	0	0101	_[1]	_[1]	_[1]	Neg	(K28.5–D21.5–D23.2–D23.2)
SOFi2	0	0	1	0	0110	_[1]	_[1]	_[1]	Neg	(K28.5–D21.5–D21.2–D21.2)
SOFi3	0	0	1	0	0111	_[1]	_[1]	_[1]	Neg	(K28.5–D21.5–D22.2–D22.2)
SOFc1	0	0	1	0	1101	_[1]	_[1]	_[1]	Neg	(K28.5–D21.5–D23.0–D23.0)
SOFf	0	0	1	0	1000	_[1]	_[1]	_[1]	Neg	(K28.5–D21.5–D24.2–D24.2)
EOFn[4,5]	0	0	0	1	0000	_[1]	_[1]	_[1]	Neg	(K28.5–D21.4–D21.6–D21.6)
									Pos	(K28.5–D21.5–D21.6–D21.6)
EOFt[5]	0	0	0	1	0100	_[1]	_[1]	_[1]	Neg	(K28.5–D21.4–D21.3–D21.3)
									Pos	(K28.5–D21.5–D21.3–D21.3)
EOFdt[6]	0	0	0	1	1100	_[1]	_[1]	_[1]	Neg	(K28.5–D21.4–D21.4–D21.4)
									Pos	(K28.5–D21.5–D21.4–D21.4)
EOFa	0	0	0	1	1001	_[1]	_[1]	_[1]	Neg	(K28.5–D21.4–D21.7–D21.7)
									Pos	(K28.5–D21.5–D21.7–D21.7)
EOFni	0	0	0	1	0001	_[1]	_[1]	_[1]	Neg	(K28.5–D10.4–D21.6–D21.6)
									Pos	(K28.5–D10.5–D21.6–D21.6)
EOFdti	0	0	0	1	1101	_[1]	_[1]	_[1]	Neg	(K28.5–D10.4–D21.4–D21.4)
									Pos	(K28.5–D10.5–D21.4–D21.4)
Idle	0	1	0	0	0000	_[1]	_[1]	_[1]	Neg	(K28.5–D21.4–D21.5–D21.5)
R-Rdy	0	1	0	0	0110	_[1]	_[1]	_[1]	Neg	(K28.5–D21.4–D10.2–D10.2)
NOS	0	1	0	0	1000	_[1]	_[1]	_[1]	Neg	(K28.5–D21.2–D31.5–D5.2)
OLS	0	1	0	0	1001	_[1]	_[1]	_[1]	Neg	(K28.5–D21.1–D10.4–D21.2)
LR	0	1	0	0	1010	_[1]	_[1]	_[1]	Neg	(K28.5–D9.2–D31.5–D9.2)
LRR	0	1	0	0	1011	_[1]	_[1]	_[1]	Neg	(K28.5–D21.1–D31.5–D9.2)
Undefined	1	0	0	0	0000	$(XY_B)^2$	$(XY_C)^2$	$(XY_D)^2$		(K28.0–DX.Y_B–DX.Y_C–DX.Y_D)
Undefined	1	0	0	0	0001	$(XY_B)^2$	$(XY_C)^2$	$(XY_D)^2$		(K28.1–DX.Y_B–DX.Y_C–DX.Y_D)
Undefined	1	0	0	0	0010	$(XY_B)^2$	$(XY_C)^2$	$(XY_D)^2$		(K28.2–DX.Y_B–DX.Y_C–DX.Y_D)
Undefined	1	0	0	0	0011	$(XY_B)^2$	$(XY_C)^2$	$(XY_D)^2$		(K28.3–DX.Y_B–DX.Y_C–DX.Y_D)
Undefined	1	0	0	0	0100	$(XY_B)^2$	$(XY_C)^2$	$(XY_D)^2$		(K28.4–DX.Y_B–DX.Y_C–DX.Y_D)
Undefined	1	0	0	0	0101	$(XY_B)^2$	$(XY_C)^2$	$(XY_D)^2$		(K28.5–DX.Y_B–DX.Y_C–DX.Y_D)
Undefined	1	0	0	0	0110	$(XY_B)^2$	$(XY_C)^2$	$(XY_D)^2$		(K28.6–DX.Y_B–DX.Y_C–DX.Y_D)
Undefined	1	0	0	0	0111	$(XY_B)^2$	$(XY_C)^2$	$(XY_D)^2$		(K28.7–DX.Y_B–DX.Y_C–DX.Y_D)
Undefined	1	0	0	0	1000	$(XY_B)^2$	$(XY_C)^2$	$(XY_D)^2$		(K23.7–DX.Y_B–DX.Y_C–DX.Y_D)
Undefined	1	0	0	0	1001	$(XY_B)^2$	$(XY_C)^2$	$(XY_D)^2$		(K27.7–DX.Y_B–DX.Y_C–DX.Y_D)
Undefined	1	0	0	0	1010	$(XY_B)^2$	$(XY_C)^2$	$(XY_D)^2$		(K29.7–DX.Y_B–DX.Y_C–DX.Y_D)
Undefined	1	0	0	0	1011	$(XY_B)^2$	$(XY_C)^2$	$(XY_D)^2$		(K30.7–DX.Y_B–DX.Y_C–DX.Y_D)

NOTES:
1. *Don't care (any value).*
2. *Outputs for the data characters in the ordered set must be encoded to the correct data values.*
3. *SOF – Start-of-frame delimiter*
4. *EOF – End-of-frame delimiter*
5. *Encoded as EOFni if TERR or PERR = 1*
6. *Encoded as EOFdti if TERR or PERR = 1*

ERROR Signal Timing



Decode

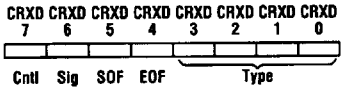
The Decode block of the GA9103 is in the return path of a serial link from a remote transmitter to the host. It takes the encoded 10-bit data from the GA9102 (Rx) and decodes it into 8-bit data for the host. The 10-bit-wide input, BRXD0..9, is first clocked into the REGISTER, using the Receiver byte clock, RXCLK.

The 10b/8b DECODER decodes data and special characters according to Tables 1 and 2. Initially, the current Running Disparity is negative and each of the characters are decoded based on the received character. The DECODER also checks for the validity of received characters based on Tables 1 and 2. The ERROR flag is set if there are code violations in any one of the four bytes of the word, or if the running disparity is in error. The ERROR signal is active for the entire duration of the word transmission, regardless of which byte was in error. The ERROR pin is also used to flag three other invalid conditions which may occur: 1) when a special character is detected in the second, third, or fourth character of a transmission word, 2) if SYNC = 1 when BRXD0..9 is not a K28.5, and 3) when an ordered set is received with improper beginning running disparity. Examples of improper running disparity are: 1) SOF with positive running disparity, and 2) EOF content specified for positive running disparity, but received with BRD-. (See Table 4).

Four bytes of the received signal must be analyzed in order to perform the ORDERED SET DECODE. For the purpose of ordered set decoding, the SYNC signal is used to align the four bytes of information to generate a word. The ordered sets are decoded according to Table 4 (Ordered Set Decoding). The ORDERED SET DECODE block generates the Data/Ordered Set signal, CRXS0, along with the 8-bit decoded ordered set. The RWSTART signal is also generated from this block. The SYNC signal is used to generate a periodic signal, RWSTART, which is HIGH on the first byte output, CRXD0..7, of every word. RWSTART is initialized by RESETN, RAWRx, or if K28.5 is followed by three valid data bytes ($DX.Y_A$, $DX.Y_B$, and $DX.Y_C$). The relationship between ERROR, RXCLK, and RWSTART is shown in the figure above.

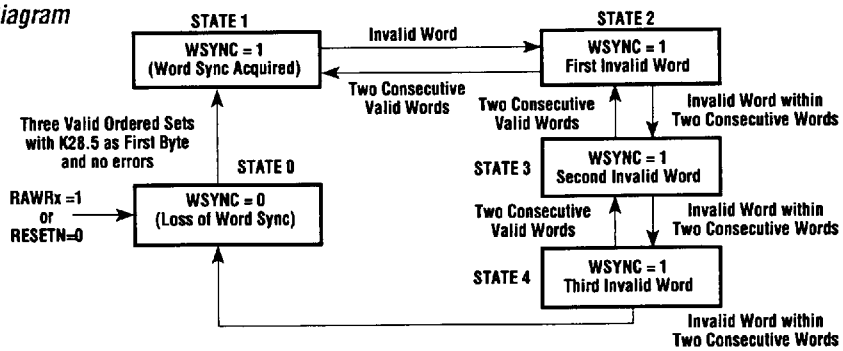
The WSYNC signal from the ORDERED SET DECODE block is used to denote whether or not the link is word-synchronized. As shown in the WSYNC State Diagram below, WSYNC = 0 under the following conditions: if the link loses word synchronization, is in a reset condition, or in the "RAW" mode. The link achieves word synchronization, (WSYNC = 1), only after three valid ordered sets are received without error and the first byte is a K28.5 character. Once synchronized, the link could lose synchronization if it receives a minimum of four invalid words within a consecutive set of seven words as per the sequence shown in the State Diagram. During this sequence, the link can reacquire word synchronization (State 1) if it receives two consecutive valid words in each of the States as shown in the State Diagram. If RAWRx = 1, WSYNC = 0.

Figure 5. Data Fields for Fiber Channel Ordered Set Decoding



If the ordered sets received correspond to a primitive sequence, the LINE STATE DECODER increments a counter using the SYNC signal. The primitive sequences, as defined by the Fiber Channel standard, are

WSYNC State Diagram



MUX Selection Table

RAW Rx	CRXS2	CRXS0	MUX Output
0	0	0	Decoded Data
0	0	1	Ordered set/line state
0	1	0	Decoded line state word
1	0	X	Undecoded data*

**CRXS0 is part of this data*

Offline State (OLS), Not-Operational State (NOS), Link Reset (LR), and Link Reset Response (LRR). These are transmitted to indicate a specific condition within a port. Transmission of NOS indicates the port has detected a link failure condition. OLS indicates the port is preparing to either initialize, to go into the diagnostic mode, or to power down. LR is sent after a link timeout error has occurred or OLS is received. LRR is transmitted to recognize Link Reset. If three consecutive ordered sets are received, the corresponding information is sent through CRXD0..7, according to the Ordered Set Decoding table. CRXS2 is active as long as one of the four possible line state signals, (OLS, NOS, LR, and LRR), is being received. Once active, CRXS2 remains active for the count of two line state ordered sets. On the third count, CRXS2 goes inactive and CRXS0 goes active. The proper line state output signals are flagged on CRXD0..7, as per Table 4. The figure below shows an example timing sequence for line states when RAWRx = 0.

The fields within the first byte, CRXD0..7, of the word for Ordered Set Decoding are shown in Figure 5. CRXD7 corresponds to the **Cntl** signal which, when logic LOW, indicates the Fiber Channel-defined ordered set has been received. When the **Cntl** signal is HIGH, it indicates a non-Fiber Channel (undefined) ordered set has been received. The **Sig** signal (CRXD6), when HIGH, indicates the Line State ordered set, IDLE or R_RDY, has been received, and when LOW, the **Sig** signal indicates an ordered set other than Line State has been received. **SOF** (CRXD5), when HIGH, indicates the Start-of-Frame ordered set has been received and **EOF** (CRXD4), when HIGH, indicates the End-of-Frame ordered set. **Type** (CRXD3..0) indicates the different types of ordered sets within the SOF, EOF, Line State and Undefined categories.

The CRC CHECK block performs a 32-bit Cyclic Redundancy Check on the received data. The CRC check begins after the Start-of-Frame Detect and finishes prior to End-of-Frame. CRC errors are flagged at the CRXS1 pin if RAWRx = 1 and CRXS1 = 0.

The RAW Rx mode is used whenever the 10-bit-wide input data to the receiver is to be passed through, undecoded, to the receive outputs, CRXD0..7, CRXP, and CRXS0. The MUX is used to choose between the decoded data/ordered set and the register output. When the RAWRx input signal is active, the undecoded data is selected; otherwise, the decoded data/ ordered set/line state is chosen.

If CRXS2 and CRXS0 are LOW, decoded data output is selected through the MUX. If CRXS0 is HIGH and CRXS2 is LOW, the ordered set/line state is selected. If CRXS2 goes HIGH, the MUX output is disabled (that is, the output data is ignored). The selection table for the MUX is shown above.

The PARITY GENERATE block is used to generate the odd parity signal CRXP for every byte of data, CRXD0..7 and CRXS0. If the number of ones in the output, CRXD0..7 and CRXS0, is an even number, CRXP will be HIGH. If the number of ones in the output, CRXD0..7 and CRXS0, is odd, CRXP will be LOW.

Example Timing Sequence for Line States

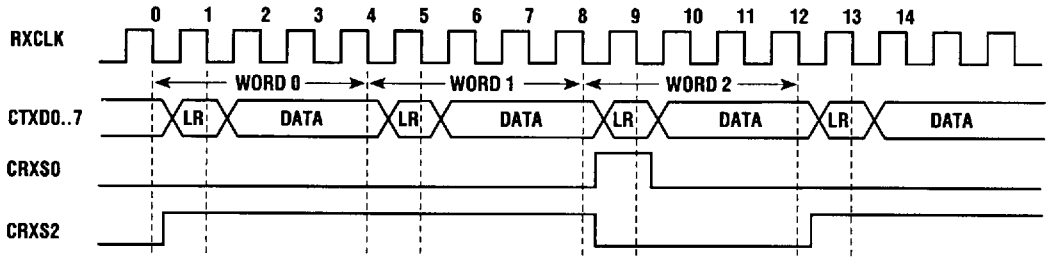
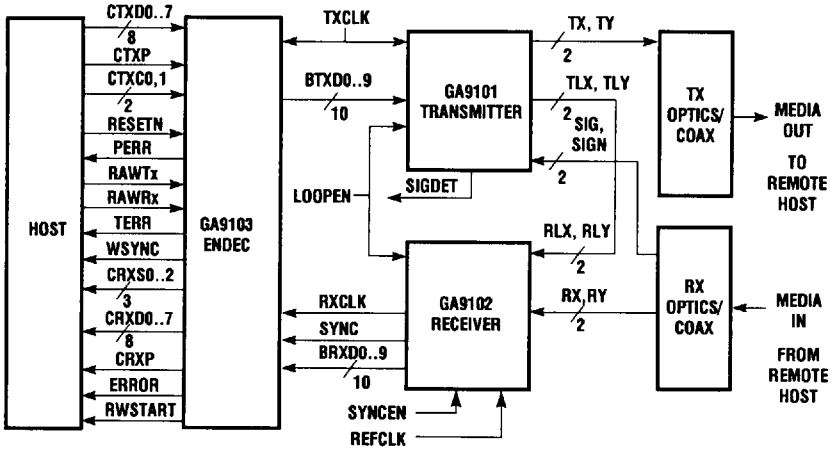


Table 4. Ordered Set Decoding – Fiber Channel

Rx Input	C-Interface Signals (Mode: Raw) Outputs (CRXD7..0)								
	Byte 1				Byte 2			Byte 3	Byte 4
	Cntl	Sig	SOF	EOF	Type	BR_D – [2]	BR_D + [3]		
SOFn1	0	0	1	0	0001		($B5_{16}$)	(37_{16})	(37_{16})
SOFn2	0	0	1	0	0010		($B5_{16}$)	(35_{16})	(35_{16})
SOFn3	0	0	1	0	0011		($B5_{16}$)	(36_{16})	(36_{16})
SOFi1	0	0	1	0	0101		($B5_{16}$)	(57_{16})	(57_{16})
SOFi2	0	0	1	0	0110		($B5_{16}$)	(55_{16})	(55_{16})
SOFi3	0	0	1	0	0111		($B5_{16}$)	(56_{16})	(56_{16})
SOFc1	0	0	1	0	1101		($B5_{16}$)	(17_{16})	(17_{16})
SOFf	0	0	1	0	1000		($B5_{16}$)	(58_{16})	(58_{16})
EOFn	0	0	0	1	0000	(95_{16})	($B5_{16}$)	($D5_{16}$)	($D5_{16}$)
EOFt	0	0	0	1	0100	(95_{16})	($B5_{16}$)	(75_{16})	(75_{16})
EOFdt	0	0	0	1	1100	(95_{16})	($B5_{16}$)	(95_{16})	(95_{16})
EOFa	0	0	0	1	1001	(95_{16})	($B5_{16}$)	($F5_{16}$)	($F5_{16}$)
EOFni	0	0	0	1	0001	($8A_{16}$)	(AA_{16})	($D5_{16}$)	($D5_{16}$)
EOFdti	0	0	0	1	1101	($8A_{16}$)	(AA_{16})	(95_{16})	(95_{16})
Idle	0	1	0	0	0000		(95_{16})	($B5_{16}$)	($B5_{16}$)
R_Rdy	0	1	0	0	0110		(95_{16})	($4A_{16}$)	($4A_{16}$)
NOS	0	1	0	0	1000		(55_{16})	(BF_{16})	(45_{16})
OLS	0	1	0	0	1001		(35_{16})	($8A_{16}$)	(55_{16})
LR	0	1	0	0	1010		(49_{16})	(BF_{16})	(49_{16})
LRR	0	1	0	0	1011		(95_{16})	(BF_{16})	(49_{16})
(K28.0-DX.Y_B-DX.Y_C-DX.Y_D)	1	0	0	0	0000		(XY_B)	(XY_C)	(XY_D)
(K28.1-DX.Y_B-DX.Y_C-DX.Y_D)	1	0	0	0	0001		(XY_B)	(XY_C)	(XY_D)
(K28.2-DX.Y_B-DX.Y_C-DX.Y_D)	1	0	0	0	0010		(XY_B)	(XY_C)	(XY_D)
(K28.3-DX.Y_B-DX.Y_C-DX.Y_D)	1	0	0	0	0011		(XY_B)	(XY_C)	(XY_D)
(K28.4-DX.Y_B-DX.Y_C-DX.Y_D)	1	0	0	0	0100		(XY_B)	(XY_C)	(XY_D)
(K28.5-DX.Y_B-DX.Y_C-DX.Y_D)[1]	1	0	0	0	0101		(XY_B)	(XY_C)	(XY_D)
(K28.6-DX.Y_B-DX.Y_C-DX.Y_D)	1	0	0	0	0110		(XY_B)	(XY_C)	(XY_D)
(K28.7-DX.Y_B-DX.Y_C-DX.Y_D)	1	0	0	0	0111		(XY_B)	(XY_C)	(XY_D)
(K23.7-DX.Y_B-DX.Y_C-DX.Y_D)	1	0	0	0	1000		(XY_B)	(XY_C)	(XY_D)
(K27.7-DX.Y_B-DX.Y_C-DX.Y_D)	1	0	0	0	1001		(XY_B)	(XY_C)	(XY_D)
(K29.7-DX.Y_B-DX.Y_C-DX.Y_D)	1	0	0	0	1010		(XY_B)	(XY_C)	(XY_D)
(K30.7-DX.Y_B-DX.Y_C-DX.Y_D)	1	0	0	0	1011		(XY_B)	(XY_C)	(XY_D)

NOTES: *1. Valid for any unrecognized control sequence starting with 'K28.5'. Not valid for acquiring Word Sync.*
2. BR_D – Beginning Running Disparity Negative.
3. BR_D + Beginning Running Disparity Positive

System Block Diagram



Absolute Maximum Ratings

Exceeding the absolute maximum ratings may damage the device.

Storage temperature	-65°C to +150°C
Ambient temperature	-55°C to +125°C
Supply voltage to ground	-0.5 V to +7.0 V
DC input voltage	-0.5 V to (V_{CC} +0.5 V)
DC input current	-30 mA to +5 mA

Operating Conditions

Proper functionality is guaranteed under these conditions:

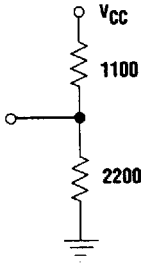
Supply voltage	5 V ±5%
Ambient temperature	0 to 70°C

DC Characteristics (Over operating range unless otherwise specified.)

Symbol	Description	Test Conditions		Limits[1] Min.	Typ.	Max.	Unit
V_{OH}	Output HIGH voltage	V_{CC} = Min	I_{OH} = -4 mA V_{IN} = V_{IH} or V_{IL}	3.6			V
V_{OL}	Output LOW voltage	V_{CC} = Min V_{IN}[3] = V_{IH} or V_{IL}	I_{OL} = 4 mA			0.37	V
V_{IH}[2]	Input HIGH level	Guaranteed input logical HIGH voltage for all inputs		2.0			V
V_{IL}[2]	Input LOW level	Guaranteed input logical LOW voltage for all inputs				0.8	V
I_{IL}	Input Leakage current	V_{CC} = Max	V_{IN} = 0.40 V		-150	-400	µA

Notes: 1. Typical limits are: V_{CC} = 5.0 V and T_A = 25°C.
2. These are absolute values with respect to device ground, and all overshoots due to system or tester noise are included.
3. V_{IN}, the TTL input, can be HIGH or LOW.

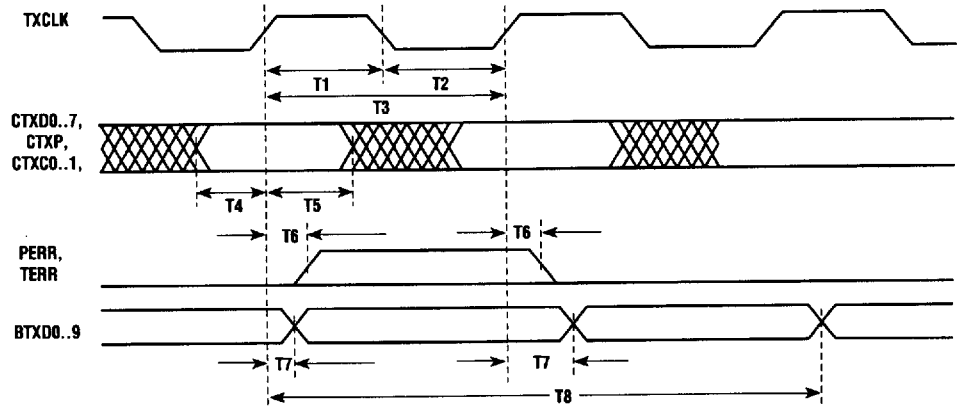
TTL Test Load, TLL Outputs



AC Characteristics – ENCODE

Parameter	Description	Min.	Typ.	Max.	Unit
T1	TXCLK Pulse Width HIGH	15.00			ns
T2	TXCLK Pulse Width LOW	15.00	T3 -T1		ns
T3	TXCLK Period	37.51	37.79	37.89	ns
T4	CTXD0..7; CTXP; CTXC0,1 Setup Time	2.00			ns
T5	CTXD0..7; CTXP; CTXC0,1 Hold Time	7.00			ns
T6	TXCLK ↑ to PERR, TERR	3.50		17.00	ns
T7	TXCLK ↑ to BTXD0..9	5.00		19.00	ns
T8	ENCODE Latency	2*T3 +7		3*T3 +12	ns

ENCODE Timing Diagram

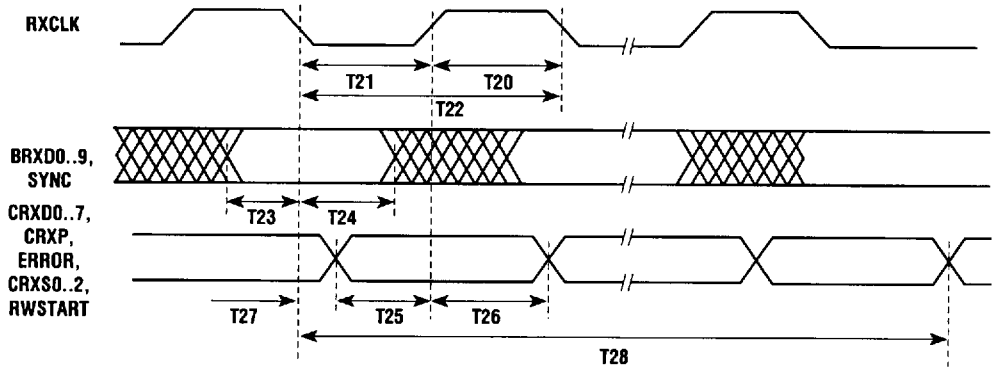


AC Characteristics – DECODE

Parameter	Description	Min.	Typ.	Max.	Unit
T20	RXCLK Pulse Width HIGH	(T22/2) - 3			ns
T21	RXCLK Pulse Width LOW	(T22/2) - 3			ns
T22	RXCLK Period	37.51	37.70	37.89	ns
T23	BRXD0..9, SYNC Valid to RXCLK ↓	1.00			ns
T24	BRXD0..9, SYNC Valid from RXCLK ↓	8.00			ns
T25	CRXD0..7, CRXP, ERROR, CRXS0..2, RWSTART Valid to RXCLK ↑	4.70			ns
T26	CRXD0..7, CRXP, ERROR, CRXS0..2, RWSTART Valid from RXCLK ↑	18.25			ns
T27	CRXD0..7, CRXP, ERROR, CRXS0..2, RWSTART from RXCLK ↓	2.50		11.00	ns
T28	DECODE Latency	6*T22		7*T22 +10	ns

Note: The DECODE functional block clocks off the negative edge of RXCLK.

DECODE Timing Diagram



AC Characteristics – Miscellaneous

Parameter	Description	Min.	Typ.	Max.	Unit
T29	RESETN Pulse Width LOW	10			ns

RESETN Timing Diagram

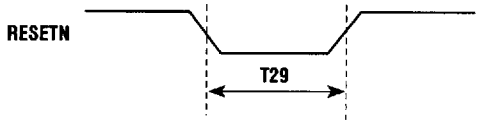
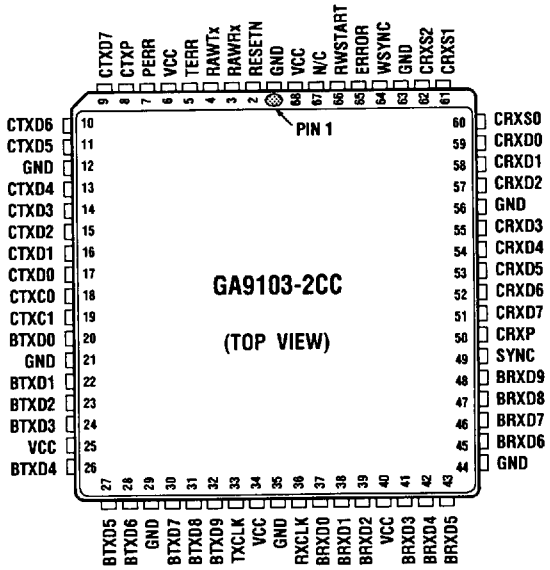


Table 5. Pin Definitions

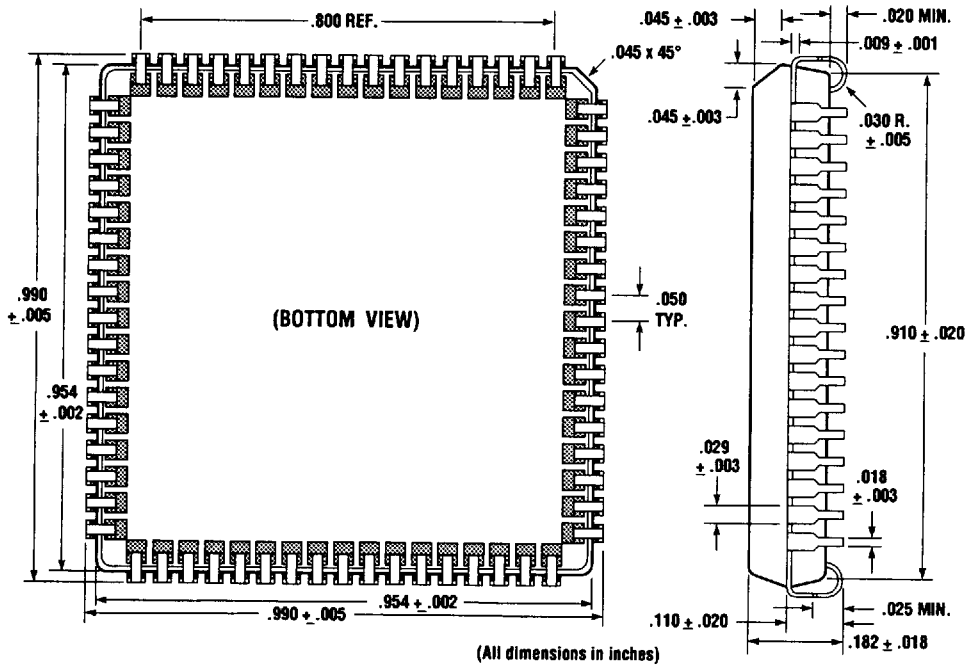
Symbol	I/O	Quantity	Logic Level	Active	Description	Pin #
CRXD0..7	Output	8	TTL	HIGH	Receive Data Output	59-57, 55-51
CRXS0	Output	1	TTL	HIGH	Receive Control	60
CRXS1	Output	1	TTL	HIGH	Receive CRC Error	61
CRXS2	Output	1	TTL	HIGH	Line State	62
BRXD0..9	Input	10	TTL	HIGH	Receive Data Input	37-39, 41-43, 45-48
RXCLK	Input	1	TTL	HIGH	Receive Byte Clock	36
SYNC	Input	1	TTL	HIGH	Receive Byte Sync	49
TXCLK	Input	1	TTL	HIGH	Transmit Byte Clock	33
BTXD0..9	Output	10	TTL	HIGH	Transmit Data Output	20, 22-24, 26-28, 30-32
CTXD0..7	Input	8	TTL	HIGH	Transmit Data Input	17-13, 11-9
CTXC0	Input	1	TTL	HIGH	Transmit Control	18
TERR	Output	1	TTL	HIGH	Transmit CRC Error	5
RWSTART	Output	1	TTL	HIGH	Start of Word	66
CTXC1	Input	1	TTL	HIGH	Generate CRC	19
WSYNC	Output	1	TTL	HIGH	Word Synchronized	64
RAWTx	Input	1	TTL	HIGH	Raw Mode Transmit	4
RESETN	Input	1	TTL	LOW	System Reset	2
ERROR	Output	1	TTL	HIGH	Illegal Line Code or Disparity Received	65
PERR	Output	1	TTL	HIGH	Parity Error	7
CRXP	Output	1	TTL	HIGH	Odd Parity Output	50
CTXP	Input	1	TTL	HIGH	Odd Parity Input	8
RAWRx	Input	1	TTL	HIGH	Raw Mode Receive	3
VCC	Input	5	N/A	N/A	+5 Volt Supply	6, 25, 34, 40, 68
GND	Input	8	N/A	N/A	Ground	1, 12, 21, 29, 35, 44, 56, 63
RESERVED		1				67

Total Pins = 68

GA9103 Pinout



68-Pin Plastic Leaded Chip Carrier (PLCC)



Ordering Information

For Fiber Channel applications, order the chip set as FC-265.

FC–265

GA9101 - 2CC – Transmitter
GA9102 - 2CC – Receiver
GA9103 - 2CC – ENDEC

TriQuint SEMICONDUCTOR

2-61

Section 6 - Packaging

Thermal Resistance Information 6-3

Device Markings 6-3

Package Outlines 6-4

Thermal Resistance Information

Power Dissipation Calculations

The maximum power dissipation that an IC can tolerate is determined by the thermal impedance characteristics of the package. The equation to find the allowable power dissipation at a given ambient operating temperature is:

$$P_D = (T_J - T_A) / \theta J_A, \text{ where:}$$

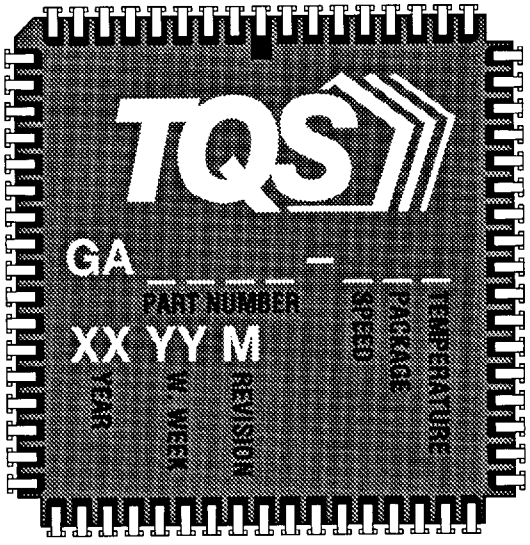
P_D = power dissipation at ambient operating temperature
T_J = maximum junction operating temperature (150°C is typically used)
T_A = maximum ambient operating temperature (free air)
θJ_A = typical thermal resistance of junction to ambient (°C/W)

Packaging Notes

Unless otherwise indicated, all thermal impedances listed are typical range values or values in still air for the package only. These impedances will vary when additional heat sinking capability is provided through PCB solder attachment or air flow.

Device Markings

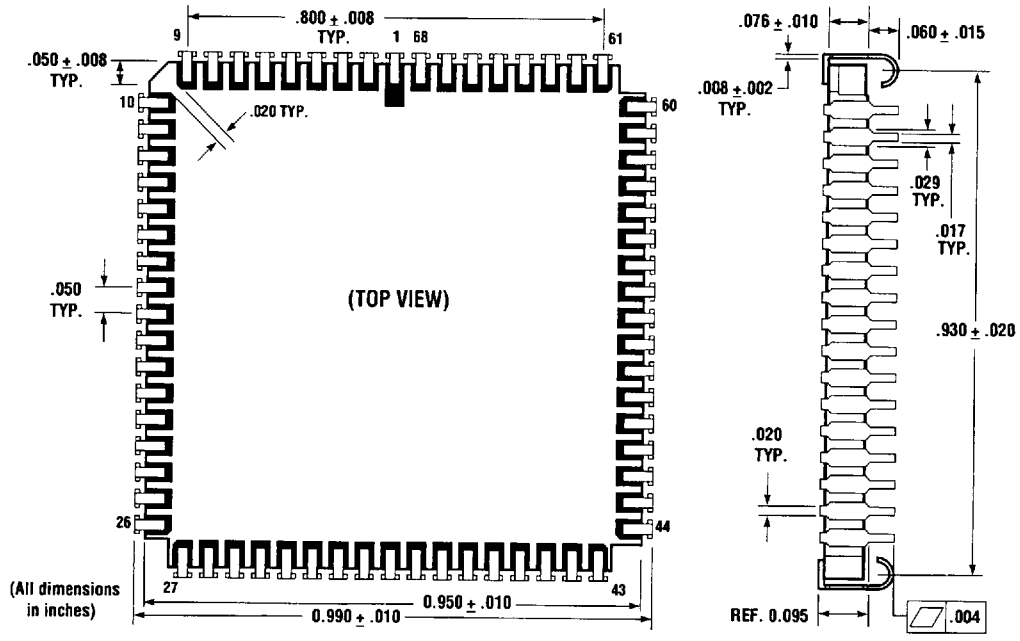
TriQuint's Standard Device Markings



Package Outlines

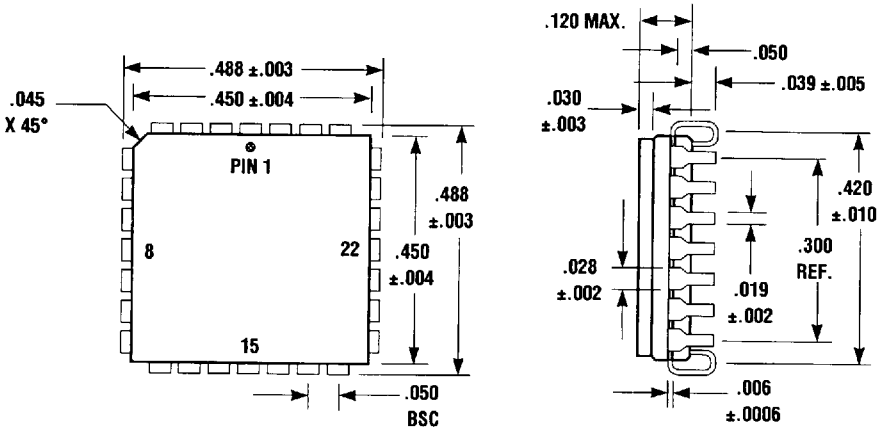
68-Pin J-Lead (CLCC) Package

Packaging for: GA9011, GA9012 (θJ_A = 25°C/Watt)



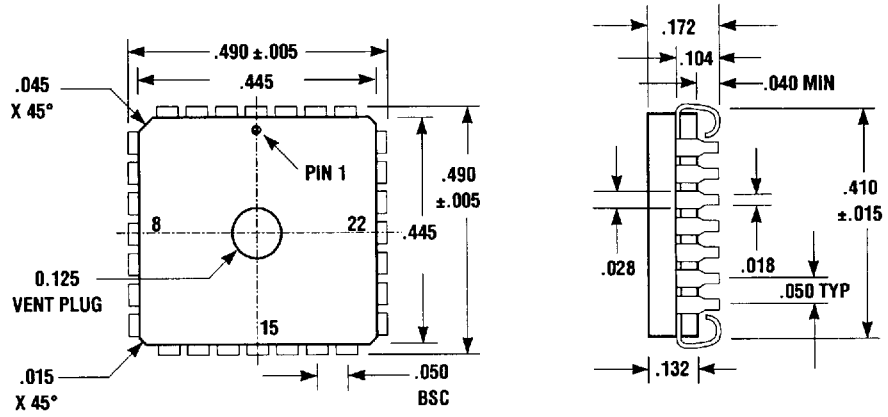
28-Pin J-Lead CerQuad Package

Packaging for: GA9101, GA9102 (θJ_A = 60°C/Watt)



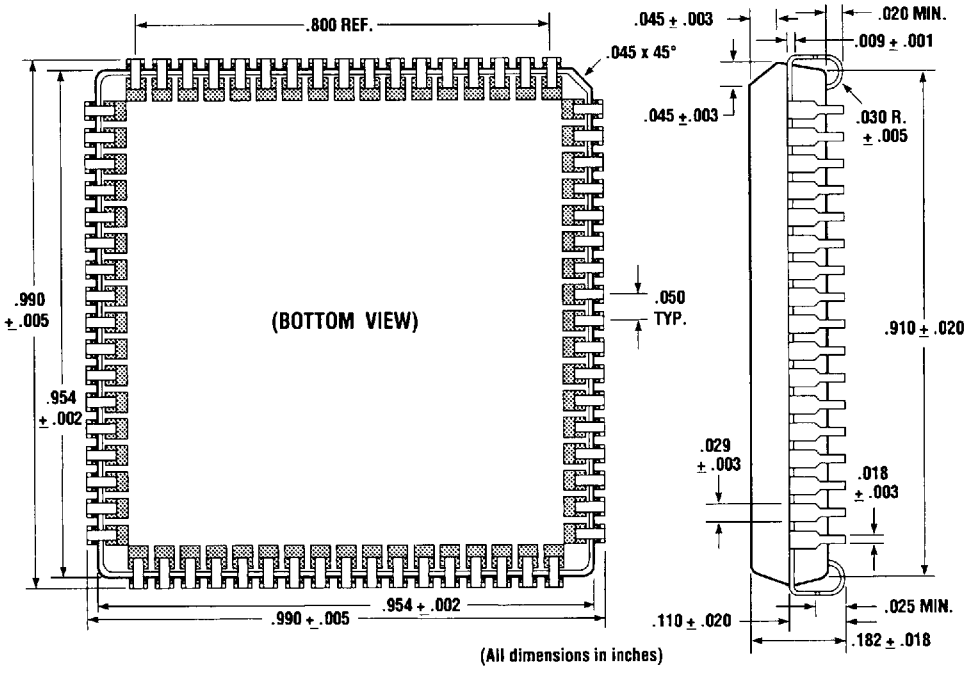
28-Pin J-Lead MQuad Package

Packaging for: GA9101, GA9102 (θJ_A = 42°C/Watt)



68-Pin PLCC Package

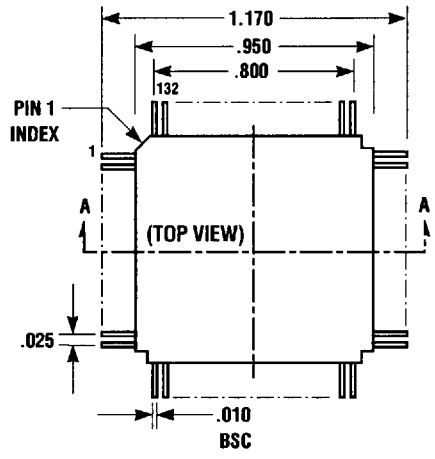
Packaging for: GA9103, GA9104 (θJ_A = 47°C/Watt)

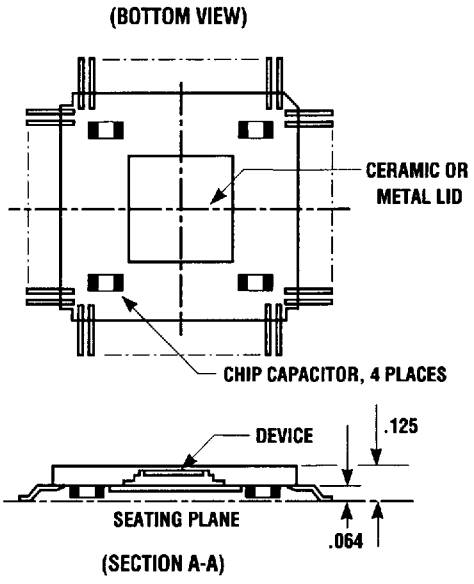


(All dimensions in inches)

132-Pin Leaded Ceramic Chip Carrier

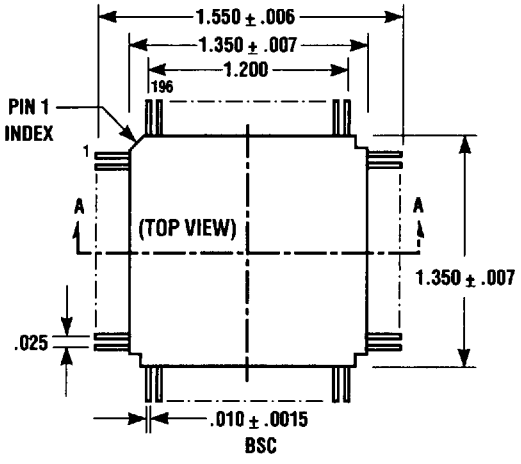
Packaging for: TQ8016 (Heat sink required, θJ_C = 8°C/Watt)

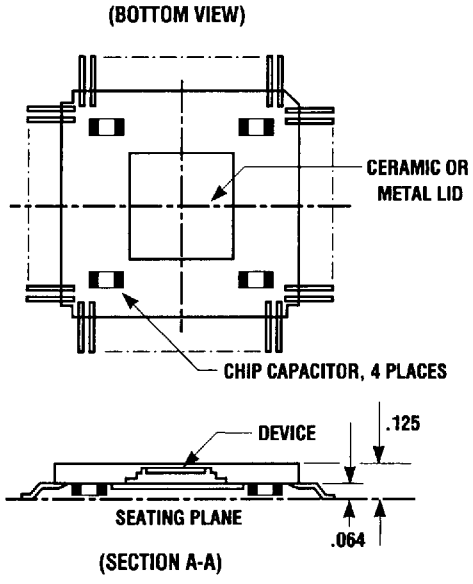




196-Pin Leaded Ceramic Chip Carrier

Packaging for: TQ8032 (Heat sink required, θJ_C = 8°C/Watt)





TriQuint SEMICONDUCTOR