

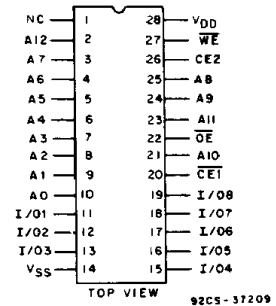
# CDM6264AC/3

## Advance Information

### High-Reliability CMOS 8192-Word By 8-Bit LSI Static RAM

**Features:**

- Fully static operation
- Single power supply: 4.5 V to 5.5 V
- All inputs and outputs directly TTL compatible
- 3-state outputs
- Industry-standard 28-pin configuration
- Input address buffers gated off with chip disable
- Fast access time:  $t_{AA} = 150 \text{ ns}$
- Low operating power:  $I_{OPER} = 15 \text{ mA}$  maximum
- Data retention voltage: 2 V min. -55°C to +125°C
- Operating temperature range (max. rating): -55°C to +125°C



**TERMINAL ASSIGNMENT**  
28-Lead Package

### Package Specifications

See Section 11, Fig. 7, b1

The RCA-CDM6264AC/3 is a high-reliability 8192-word by 8-bit static random-access memory. It is designed for use in memory systems where high-speed, low power and simplicity in use are desirable. This device has common data input and data output and utilizes a single power supply of 4.5 V to 5.5 V.

Either chip enable ( $\overline{CE1}$  or CE2), when not valid, will gate off the address and output buffers and power down the chip to

minimum standby power with inputs toggling. The output enable (OE) controls the output buffers to eliminate bus contention.

The CDM6264AC/3 is supplied in 28-lead hermetic, dual-inline side-braced ceramic package (D suffix) and in a 32-terminal leadless chip carrier (LCC) ceramic package (J suffix).

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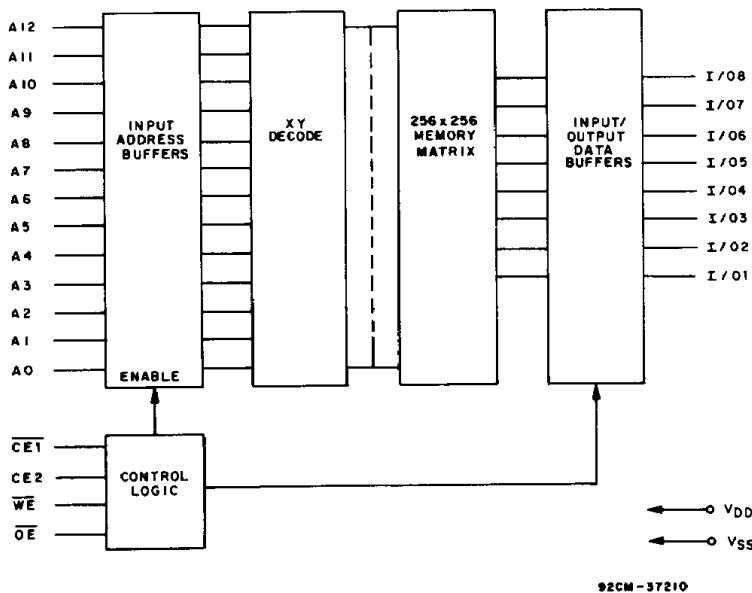
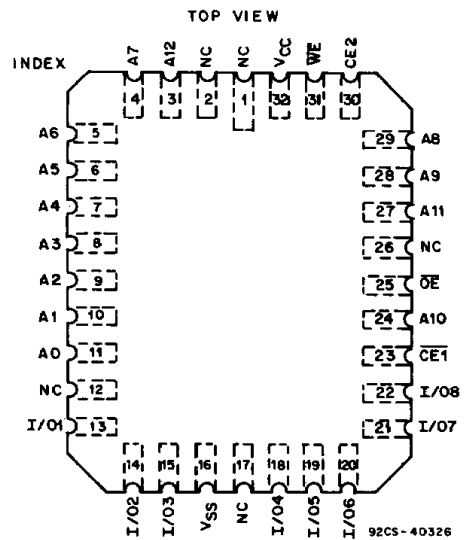


Fig. 1 - Functional block diagram.



**TERMINAL ASSIGNMENT**  
32-Terminal LCC Package

### Package Specifications

See Section 11, Fig. 40, c1

**CDM6264AC/3****TRUTH TABLE**

$\overline{\text{CE1}}$	$\text{CE2}$	$\overline{\text{OE}}$	$\overline{\text{WE}}$	A0 to A12	MODE	DATA I/O	DEVICE CURRENT
H	X	X	X	X	NOT SELECTED	HIGH Z	STANDBY
X	L	X	X	X	NOT SELECTED	HIGH Z	STANDBY
L	H	L	H	STABLE	READ	DATA OUT	ACTIVE
L	H	X	L	STABLE	WRITE	DATA IN	ACTIVE
L	H	H	H	STABLE	OUTPUT DISABLE	HIGH Z	ACTIVE

L = Low    H = High    X = H or L

**MAXIMUM RATINGS, Absolute-Maximum Values:**DC SUPPLY-VOLTAGE RANGE, ( $V_{DD}$ ):(Voltage reference to  $V_{SS}$  terminal) ..... -0.3 to +7 VINPUT VOLTAGE RANGE, ALL INPUT ..... -0.3 to  $V_{DD} + 0.3$  VPOWER DISSIPATION PER PACKAGE ( $P_D$ ):For  $T_A = -55^\circ$  to  $100^\circ\text{C}$  ..... 500 mWFor  $T_A = 100^\circ$  to  $125^\circ\text{C}$  ..... Derate Linearly at 12 mW/ $^\circ\text{C}$  to 200 mW

DEVICE DISSIPATION PER OUTPUT TRANSISTOR

For  $T_A = \text{FULL PACKAGE-TEMPERATURE RANGE}$  ..... 100 mWOPERATING-TEMPERATURE RANGE ( $T_A$ ): ..... -55 to +125 $^\circ\text{C}$ STORAGE TEMPERATURE RANGE ( $T_{stg}$ ): ..... -65 to +150 $^\circ\text{C}$ 

LEAD TEMPERATURE FOR D TYPE PACKAGE (DURING SOLDERING):

At distance  $1/16 \pm 1/32$  in. ( $1.59 \pm 0.79$  mm) from case for 10 s max. .... +265 $^\circ\text{C}$ **OPERATING CONDITIONS at  $T_A = -55$  to +125 $^\circ\text{C}$** 

For maximum reliability, operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS	
	ALL TYPES			
	MIN.	MAX.		
DC Operating Voltage Range	4.5	5.5	V	
Input Voltage Range	$V_{IH}$	2.2		$V_{DD} + 0.3$
	$V_{IL}$	-0.3		0.8
Input Signal Rise or Fall Time $\Delta$	$t_r, t_f$	—	5	$\mu\text{s}$

$\Delta$  Input signal rise and fall times with a duration greater than the maximum value can cause loss of stored data in the selected mode.

## CDM6264AC/3

STATIC ELECTRICAL CHARACTERISTICS at  $T_A = -55$  to  $+125^\circ\text{C}$ ,  $V_{DD} = 5\text{ V} \pm 10\%$ , Except as noted

CHARACTERISTIC	CONDITIONS	LIMITS				UNITS	
		+25/-55° C		+125° C			
		MIN.	MAX.	MIN.	MAX.		
Standby Device Current	$I_{DD5}$	$\overline{CE1} = V_{IH}$ or $CE2 = V_{IL}$	—	3	—	4	mA
	$I_{DD51}$	$\overline{CE1} = CE2 \geq V_{DD} - 0.2\text{ V}$ or $CE2 \leq 0.2\text{ V}$	—	0.1	—	1	mA
Output Voltage Low Level	$V_{OL}$ Max.	$I_{OL} = 2.1\text{ mA}$	—	0.4	—	0.4	V
Output Voltage High Level	$V_{OH}$ Min.	$I_{OH} = -1\text{ mA}$	2.4	—	2.4	—	V
Input Leakage Current	$I_{IN}$ Max.	$V_{IN} = 0\text{ V}$ to $V_{DD}$	—	$\pm 2$	—	$\pm 2$	$\mu\text{A}$
3-State Output Leakage	$I_{OUT}$	$V_{IO} = 0\text{ V}$ to $V_{DD}$	—	$\pm 2$	—	$\pm 2$	
Operating Device Current	$I_{OPER}$ #	$V_{IN} = V_{IL}, V_{IH}$ $t_{cyc} = 1\ \mu\text{s}$	—	15	—	15	mA
Input Capacitance	$C_{IN}$	$V_{IO} = 0\text{ V}$ , $f = 1\text{ MHz}$ , $T_A = 25^\circ\text{C}$	—	6*	—	6*	pF
Output Capacitance	$C_{IO}$	$V_{IO} = 0\text{ V}$ , $f = 1\text{ MHz}$ , $T_A = 25^\circ\text{C}$	—	8*	—	8*	

# Output open circuited.

\* Guaranteed, not tested.

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### SIGNAL DESCRIPTIONS

#### A0-A12 (Address Inputs):

These inputs must be stable prior to a write operation, but may change asynchronously during read functions.

#### I/O1-I/O8:

8-bit tristate data bus.

#### $\overline{CE1}$ , CE2 (Chip Enable):

Either chip enable, when not true, powers down the chip, disables Read and Write functions, and gates off address and output buffers.

#### $\overline{OE}$ (Output Enable):

Enables tristate outputs if  $\overline{CE1}$  and CE2 are valid and  $\overline{WE}$  is high.

#### $\overline{WE}$ (Write Enable):

Enables Write function, if  $\overline{CE1}$  and CE2 are valid.  $\overline{WE}$  will dominate if both  $\overline{WE}$  and  $\overline{OE}$  are low (i.e., the bus will be tristated and a Write will occur).

#### $V_{DD}$ , $V_{SS}$ :

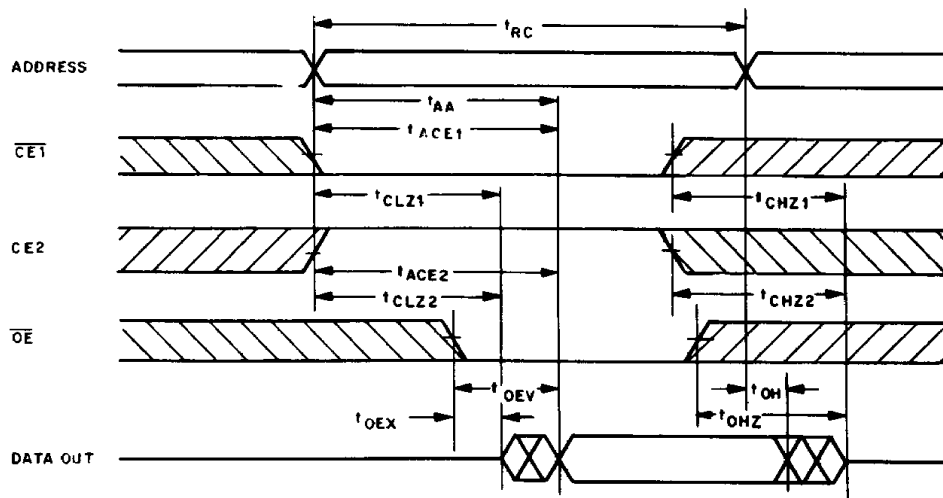
Power supply connections.

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DYNAMIC ELECTRICAL CHARACTERISTICS at  $T_A = -55$  to  $+125^\circ\text{C}$ ,  $V_{DD} = 5\text{ V} \pm 10\%$ , Input  $t_r = 10\text{ ns}$ ,  
 Input Pulse Levels: 0 V to 3 V

CHARACTERISTIC		LIMITS		UNITS
		+25°C/-55°C/+125°C		
		MIN.	MAX.	
<b>Read Cycle Times, See Fig. 2</b>				
Read Cycle Time	$t_{RC}$	150	—	ns
Address Access Time	$t_{AA}^*$	—	150	
Chip Enable Access Time	$t_{ACE1}, t_{ACE2}^*$	—	150	
Chip Enable to Output Active	$t_{CLZ1}, t_{CLZ2}$	10	—	
Output Enable to Output Valid	$t_{OEV}^*$	—	70	
Output Enable to Output Active	$t_{OEX}$	5	—	
Chip Disable to Output "High"	$t_{CHZ1}, t_{CHZ2}$	0	70	
Output Disable to Output "High" Z	$t_{OHZ}$	0	60	
Output Hold from Address Change	$t_{OH}$	30	—	

\* Indicates 100% testing.



$\overline{WE}$  IS HIGH DURING READ CYCLE. TIMING MEASUREMENT REFERENCE LEVEL IS 1.5 V.

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Fig. 2 - Read-cycle timing waveforms.

**CDM6264AC/3**

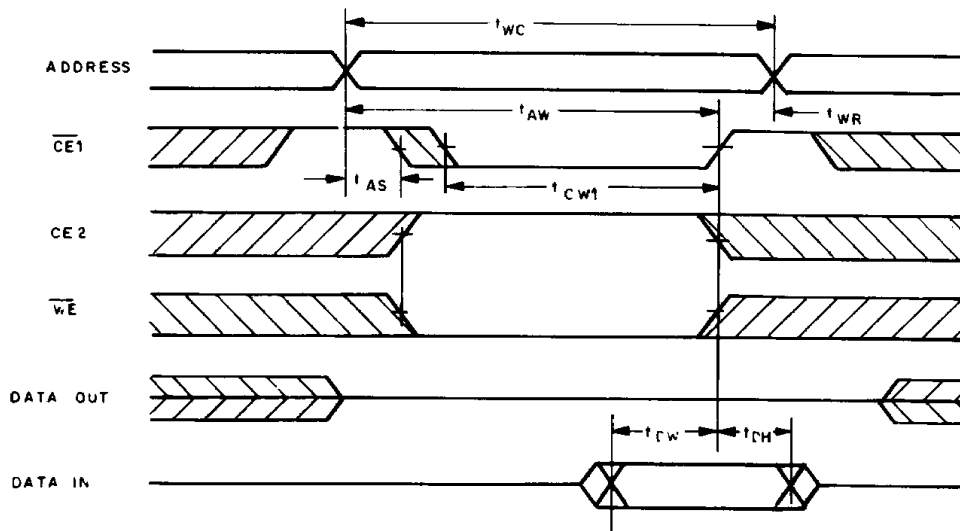
**DYNAMIC ELECTRICAL CHARACTERISTICS** at  $T_A = -55$  to  $+125^\circ\text{C}$ ,  $V_{DD} = 5\text{ V} \pm 10\%$ , Input  $t_r, t_f = 10\text{ ns}$ ;  
**Input Pulse Levels: 0 V to 3 V**

CHARACTERISTIC		LIMITS		UNITS
		+25°C/-55°C/+125°C		
		MIN.	MAX.	
<b>Write Cycle Times, See Fig. 3</b>				
Write Cycle Time	$t_{WC}^*$	150	—	ns
Chip Enable to End of WRITE	$t_{CW1}, t_{CW2}^*$	120	—	
Address Valid to End of WRITE	$t_{AW}^*$	120	—	
Address Setup Time	$t_{AS}^*$	0	—	
Write Enable Width	$t_{WW}^*$	100	—	
Write Recovery Time	$t_{WR}^*$	0	—	
Write to Output "High Z"	$t_{WHZ}$	—	70	
Input Data Setup Time	$t_{DW}^*$	60	—	
Input Data Hold Time	$t_{DH}^*$	0	—	
Output Active from End of Write	$t_{OW}$	10	—	

\* Indicates 100% testing.

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**WRITE CYCLE 1 ( $\overline{CE1}$  CONTROL)**



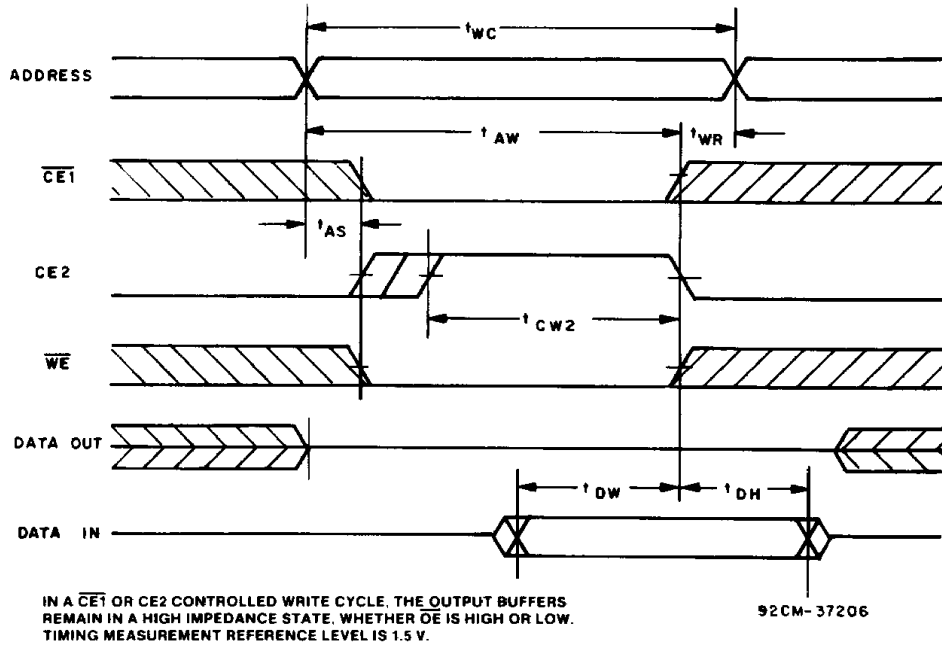
IN A  $\overline{CE1}$  OR  $\overline{CE2}$  CONTROLLED WRITE CYCLE, THE OUTPUT BUFFERS REMAIN IN A HIGH IMPEDANCE STATE, WHETHER  $\overline{OE}$  IS HIGH OR LOW. TIMING MEASUREMENT REFERENCE LEVEL IS 1.5 V.

92CM-37204

Fig. 3 - Write-cycle timing waveforms.

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## WRITE CYCLE 2 (CE2 CONTROL)



## WRITE CYCLE 3 ( $\overline{WE}$ CONTROL)

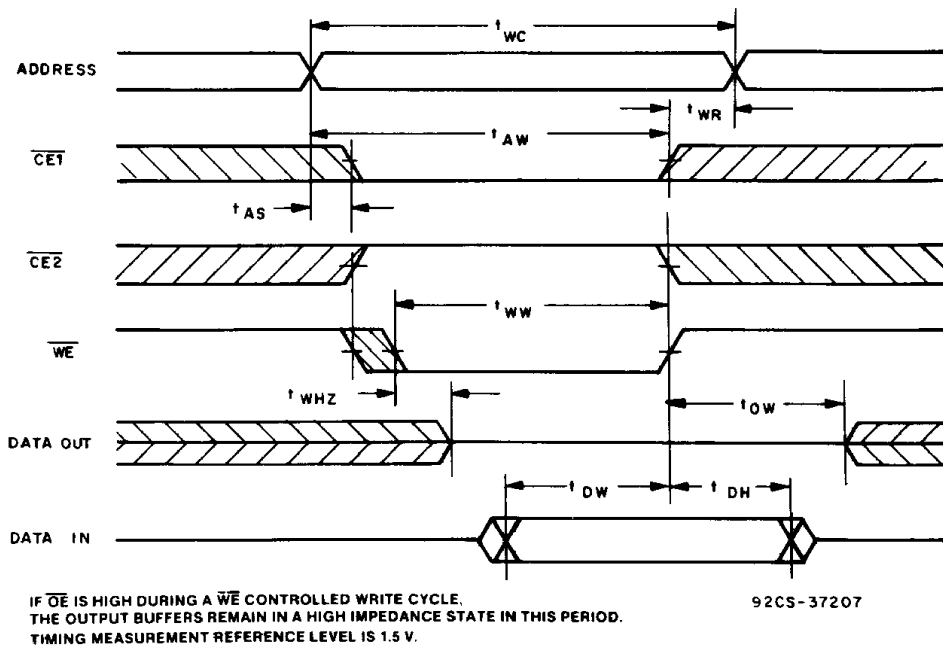


Fig. 3 - Write-cycle timing waveforms (cont'd).

**CDM6264AC/3**

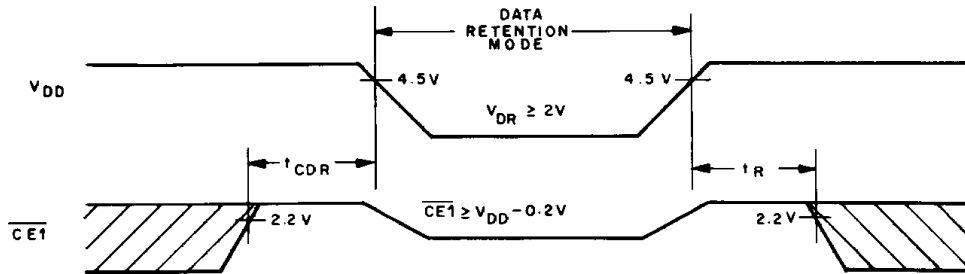
**DATA RETENTION CHARACTERISTICS at  $T_A = -55^\circ\text{C}$  to  $+125^\circ\text{C}$ ; See Fig. 4**

CHARACTERISTIC	TEST CONDITIONS	LIMITS		UNITS
		ALL TYPES		
		MIN.	MAX.	
Minimum Data Retention Voltage $V_{DR}$	$\overline{CE1} \geq V_{DD} - 0.2\text{ V}$ or $CE2 \leq 0.2\text{ V}$	2	5.5	V
Data Retention Quiescent Current $I_{DDDR}$	$V_{DD} = 3\text{ V}$ , $\overline{CE1}$ , $CE2 \geq V_{DD} - 0.2\text{ V}$ or $CE2 \leq 0.2\text{ V}$	—	350	$\mu\text{A}$
Chip Disable to Data Retention Time $t_{CDR}$	See Fig. 4	0	—	ns
Recovery to Normal Operation Time $t_R$	See Fig. 4	* $t_{RC}$	—	

\* $t_{RC}$  = Read Cycle Time.

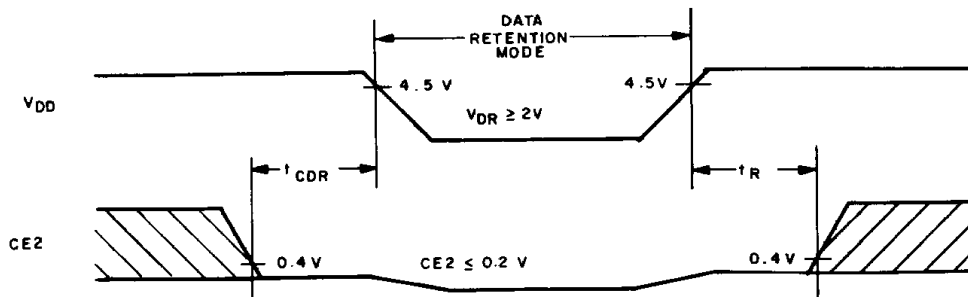
Power Down Time = 500 ns

**DATA RETENTION WAVEFORM 1 ( $\overline{CE1}$  CONTROL)**



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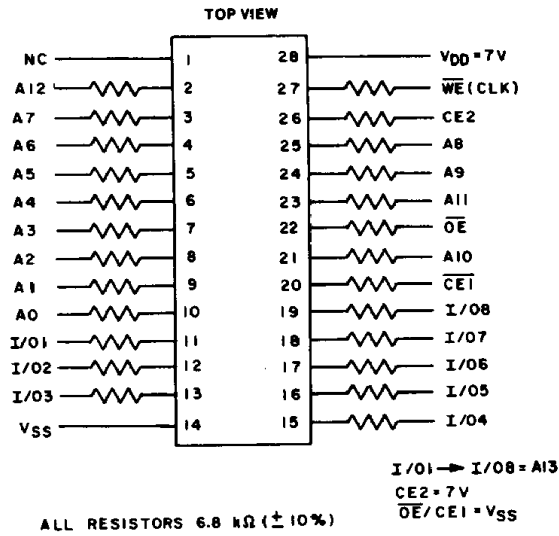
**DATA RETENTION WAVEFORM 2 (CE2 CONTROL)**



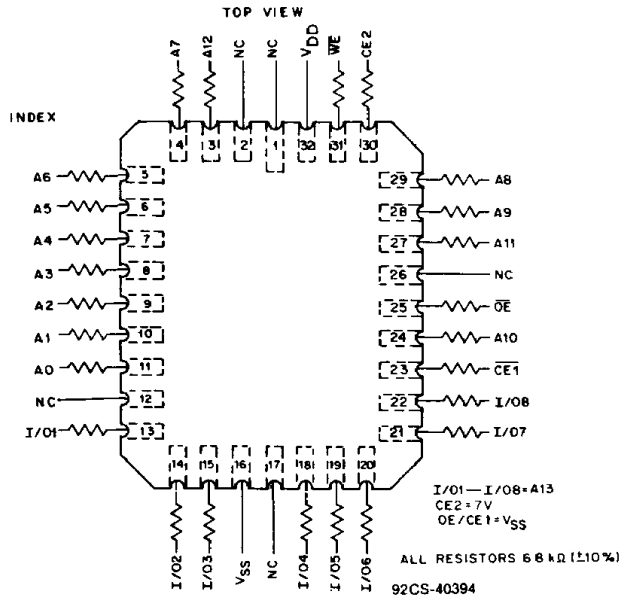
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Fig. 4 - Low  $V_{DD}$  data-retention timing waveforms.

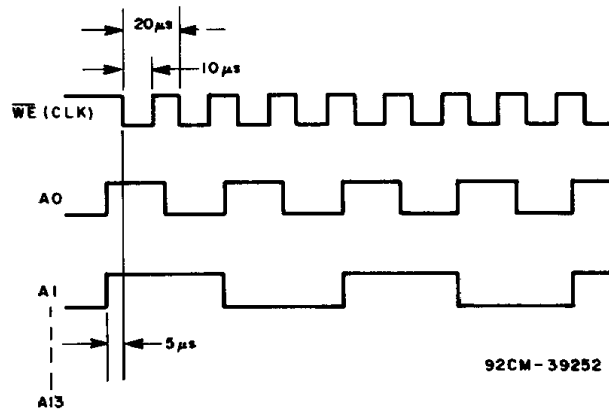
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(a) Burn-in circuit for 28-lead D package.



(b) Burn-in circuit from 32-terminal leadless chip-carrier, (LCC), J package.



(c) Burn-in circuits timing waveforms.

TYPE NO.	V <sub>DD</sub>	TEMP.	TIME
CDM6264ACD/3 CDM6264ACJ/3	7 V	+125° C	160 Hrs, Min.

Fig. 5 - Dynamic burn-in circuits and timing waveforms.