

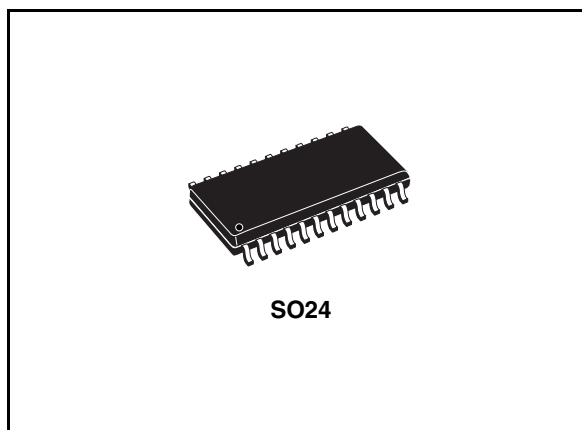


# L9524C

## Glow plug system control IC

### Features

- Quad gate driver for external n-channel power MOSFETs in high-side configuration:
  - Gates driven by PWM output signal
  - Adjustable gate charge/discharge currents
  - Limited gate-to-source voltages
  - Negative clamping for inductive loads
  - Advanced run-off control
  - Regulation of the power through the glow plugs
- Control output for external relay driver
- Battery-voltage-compatible two-wire interface
- Supply voltage monitoring with shutdown
- Battery voltage monitoring with shutdown
- Junction temperature monitoring with shutdown
- Monitoring of currents through the glow plugs with shutdown at overcurrent (adjustable threshold)
- Monitoring of external switches
- Charge pump voltage monitoring with shutdown
- Active clamping during load dump



### Description

The L9524C is a control IC for up to six glow plugs of diesel engines. The glow plugs are switched by up to four external PWM-controlled n-channel power MOSFETs or a single relay in high-side configuration. Supply voltage, battery voltage, junction temperature, switches, currents through the glow plugs, and charge pump voltage are monitored. A two-wire interface is used to communicate with the diesel engine management system.

### Order codes

Part number	Package	Packing
L9524C-TR	SO24	Tape & reel

# Contents

<b>1</b>	<b>Block diagram</b> .....	<b>5</b>
<b>2</b>	<b>Pin description</b> .....	<b>6</b>
<b>3</b>	<b>Electrical specifications</b> .....	<b>7</b>
3.1	Absolute maximum ratings .....	7
3.2	Thermal data .....	7
3.3	Electrical characteristics .....	8
<b>4</b>	<b>Functional description</b> .....	<b>12</b>
4.1	Operating modes .....	12
4.2	Supply .....	13
4.3	Diagnostic output .....	15
4.4	Current monitoring .....	17
4.5	Switch monitoring .....	18
4.6	Thermal shutdown .....	18
4.7	Gate drivers .....	18
4.8	Relay output .....	18
4.9	Gate charge/discharge current variation .....	19
4.10	Overcurrent threshold variation .....	19
4.11	Advanced run-off control .....	20
4.12	Output timing .....	20
4.13	Power regulation .....	21
<b>5</b>	<b>Application diagrams</b> .....	<b>22</b>
<b>6</b>	<b>Package information</b> .....	<b>25</b>
<b>7</b>	<b>Revision history</b> .....	<b>26</b>

## List of tables

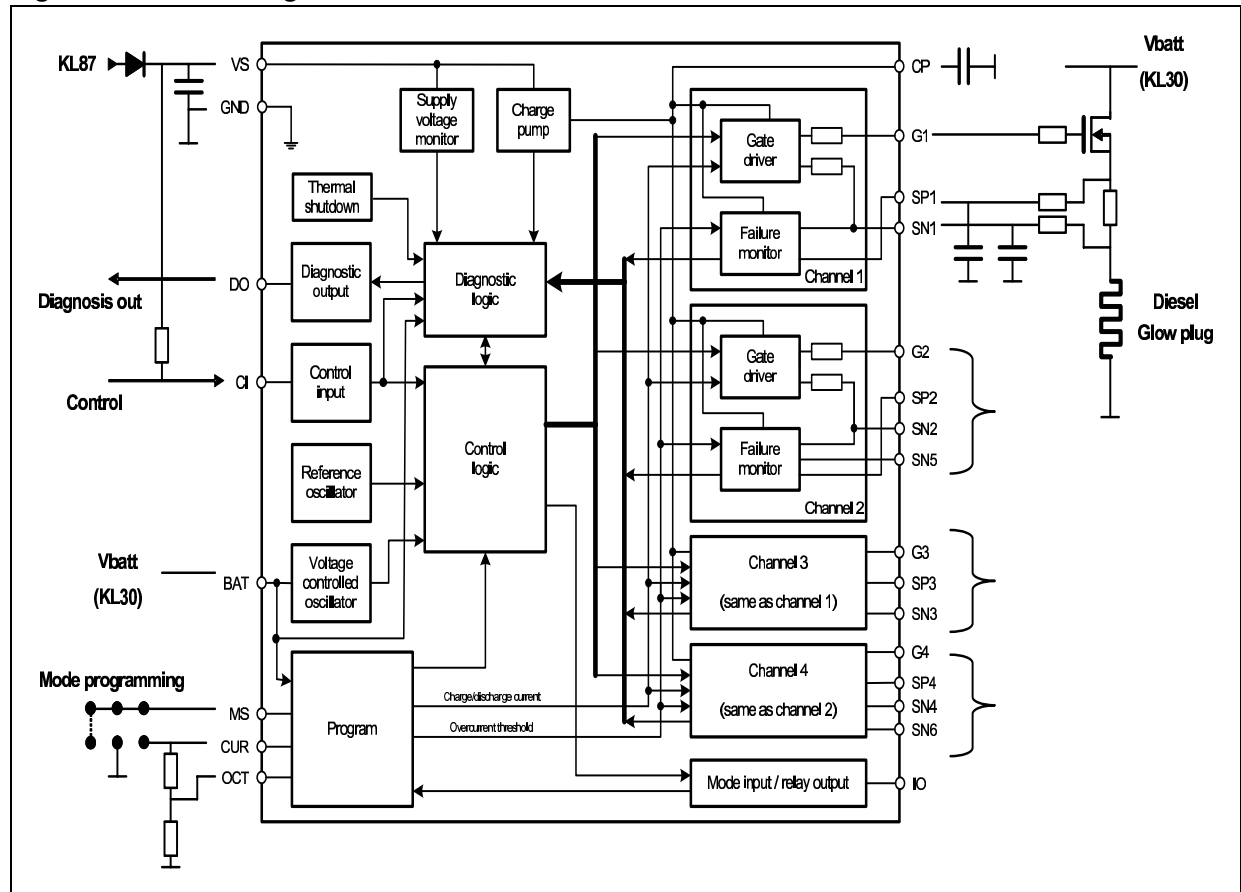
Table 1.	Pin Description . . . . .	6
Table 2.	Absolute maximum ratings . . . . .	7
Table 3.	Thermal data . . . . .	7
Table 4.	Electrical characteristics . . . . .	8
Table 5.	Mode . . . . .	12
Table 6.	Document revision history . . . . .	26

## List of figures

Figure 1.	Block Diagram . . . . .	5
Figure 2.	Pin Connection (Top view) . . . . .	6
Figure 3.	Shunt sense versus transistor sense . . . . .	13
Figure 4.	Control input signal in transistor mode (modes 3 to 6) . . . . .	14
Figure 5.	Permanent switch on of glow plugs at first falling edge in transistor mode (modes 3 to 6) . . . . .	14
Figure 6.	Control input signal in mode 2 for permanent switch on . . . . .	15
Figure 7.	Serial diagnostic interface protocol . . . . .	17
Figure 8.	Variation of gate charge/discharge current . . . . .	19
Figure 9.	Timing diagram of advanced run-off control . . . . .	20
Figure 10.	Output timing . . . . .	20
Figure 11.	Mode 1: relay mode, go/no-go diagnostic interface protocol . . . . .	22
Figure 12.	Mode 2: relay mode, serial diagnostic interface protocol . . . . .	22
Figure 13.	Mode 3: transistor mode, shunt sense, no power regulation . . . . .	23
Figure 14.	Mode 4: transistor mode, shunt sense, power regulation . . . . .	23
Figure 15.	Mode 5: transistor mode, transistor sense, no power regulation . . . . .	24
Figure 16.	Mode 6: transistor mode, transistor sense, power regulation . . . . .	24
Figure 17.	SO24 mechanical data and package dimensions . . . . .	25

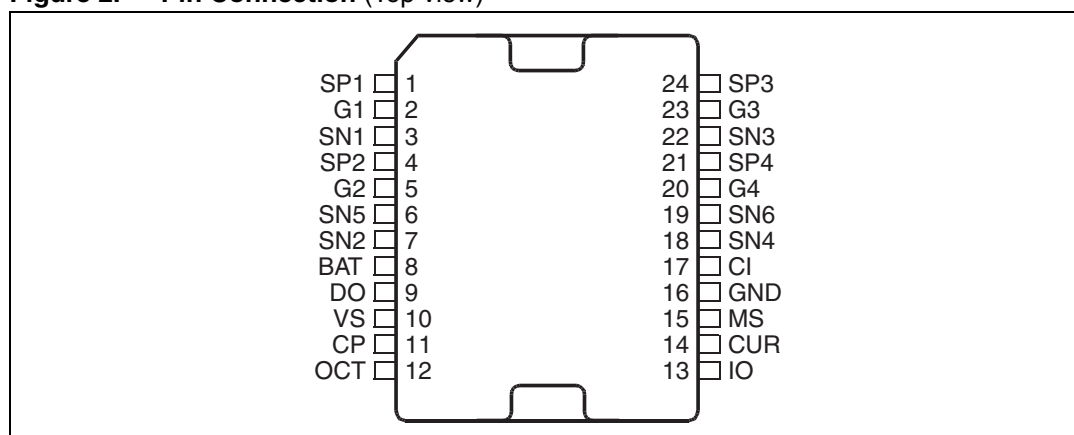
# 1 Block diagram

Figure 1. Block Diagram



## 2 Pin description

**Figure 2. Pin Connection (Top view)**



**Table 1. Pin Description**

N°	Pin	Function
1	SP1	Positive sense input, glow plug 1
2	G1	Driver output for external high-side power MOSFET, transistor 1
3	SN1	Negative sense input, glow plug 1
4	SP2	Positive sense input, glow plugs 2 and 5
5	G2	Driver output for external high-side power MOSFET, transistor 2
6	SN5	Negative sense input, glow plug 5
7	SN2	Negative sense input, glow plug 2
8	BAT	Battery voltage input
9	DO	Diagnostic output
10	VS	Supply voltage input
11	CP	Charge pump output
12	OCT	Overcurrent threshold setting
13	IO	Transistor mode: input for selection of power regulation feature Relay mode: output to control external relay driver
14	CUR	Power MOSFET gate charge/discharge current setting
15	MS	Mode selection input: transistor modes (transistor sense / shunt sense) / relay mode
16	GND	Ground pin
17	CI	Control input
18	SN4	Negative sense input, glow plug 4
19	SN6	Negative sense input, glow plug 6
20	G4	Driver output for external high-side power MOSFET, transistor 4
21	SP4	Positive sense input, glow plugs 4 and 6
22	SN3	Negative sense input, glow plug 3
23	G3	Driver output for external high-side power MOSFET, transistor 3
24	SP3	Positive sense input, glow plug 3

## 3 Electrical specifications

### 3.1 Absolute maximum ratings

**Table 2. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{VS}$	Supply voltage range	-0.3 to 45	V
$IdV_{VS}/dt$	Supply voltage slope	10	V/ $\mu$ s
$V_{CP}$	Charge pump voltage range	-0.3 to 45	V
$V_{BAT}, V_{CI},$ $V_{SP1-4},$ $V_{SN1-6}$	Input pin voltage range (BAT, CI, SP1-4, SN1-6)	-16 to 45	V
$V_{OCT}, V_{CUR},$ $V_{MS}, V_{IO}$	Input pin voltage range (OCT, CUR, MS, IO)	-0.3 to 7	V
$V_{DO}, V_{G1-4}$	Output pin voltage range (DO, G1-4)	-16 to 45	V

**Warning: The device may become damaged if using externally applied voltages or currents exceeding these limits!**

All pins of the IC are protected against ESD. The verification is performed according to MIL883C, human body model with  $R=1.5k\Omega$ ,  $C=100pF$  and discharge voltage  $\pm 2KV$ , corresponding to a maximum discharge energy of 0.2mJ.

### 3.2 Thermal data

**Table 3. Thermal data**

Symbol	Parameter	Value	Unit
$T_J$	Operating junction temperature	-40 to 125	$^{\circ}C$
$T_{JSD}$	Junction temperature thermal shutdown threshold	125 to 150	$^{\circ}C$

### 3.3 Electrical characteristics

$5V \leq V_{VS}; V_{BAT} \leq 18V, -40^{\circ}C \leq T_J \leq 125^{\circ}C$ , unless otherwise specified. The voltages are referred to GND and currents are assumed positive, when current flows into the pin.

**Table 4. Electrical characteristics**

Item	Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
<b>Supply (VS)</b>							
1.1	$I_{VS}$	Supply current		1	5	20	mA
1.2	$V_{VS\ uv}$	Undervoltage threshold		4		5	V
1.3	$V_{VS\ uvh}$	Undervoltage threshold hysteresis <sup>(1)</sup>		0.2		0.4	V
1.4	$V_{VS\ ol}$	Open-load detection threshold		5.5		7.2	V
1.5	$V_{VS\ ov}$	Overvoltage threshold		18		22	V
1.6	$V_{VS\ ovh}$	Overvoltage threshold hysteresis <sup>(1)</sup>		0.4		1.6	V
1.7	$V_{VS\ ld}$	Load dump threshold		28		35	V
1.8	$t_{VS\ fil}$	Filter time <sup>(2)</sup>		2		4	ms
1.9	$t_{VS\ ld}$	Load dump delay time <sup>(1)</sup>			10		$\mu$ s
<b>Supply (BAT)</b>							
2.1	$I_{BAT\ leak}$	Leakage current	$V_{VS} \leq 3V$ $0V \leq V_{BAT} \leq 12V$	0		5	$\mu$ A
2.2	$R_{BAT}$	Internal pull-down resistance		25		100	k $\Omega$
2.3	$V_{BAT\ uv}$	Battery undervoltage threshold	$V_{MS} > V_{MS\ tr}$ (transistor mode)	1		2	V
2.4	$t_{BAT\ fil}$	Filter time <sup>(2)</sup>		300		760	$\mu$ s
<b>Charge pump (CP)</b>							
3.1	$V_{CP}$	Charge pump voltage	$I_{CP} = -100\mu A$	$V_{VS}$ +5V		$V_{VS}$ +18V	
3.2	$I_{CP}$	Charging current	$V_{CP} = V_{VS} + 5V$	-1500		-100	$\mu$ A
3.3	$V_{CP\ uv}$	Charge pump undervoltage threshold		$V_{VS}$ +3.5V		$V_{VS}$ +5V	
3.4	$f_{CP}$	Charge pump frequency <sup>(1)</sup>		1.5		7	MHz
3.5	$t_{CP\ fil}$	Filter time <sup>(2)</sup>		400		950	$\mu$ s



Table 4. Electrical characteristics (continued)

Item	Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
<b>Control input (CI)</b>							
4.1	$V_{CI\ off}$	Input "off" level		$0.6 \cdot V_{VS}$			
4.2	$V_{CI\ on}$	Input "on" level				$0.4 \cdot V_{VS}$	
4.3	$V_{CI\ h}$	Off-to-on hysteresis <sup>(1)</sup>		$0.03 \cdot V_{VS}$	$0.04 \cdot V_{VS}$	$0.05 \cdot V_{VS}$	
4.4	$V_{CI\ to}$	Input "timeout" threshold		1		1.8	V
4.5	$R_{CI}$	Internal pull-up resistance	$V_{CI} \leq V_{VS}$	20		80	k $\Omega$
4.6	$t_{CI\ fil}$	Filter time <sup>(2)</sup>		0.5		1	ms
4.7	$t_{CI\ to}$	PWM timeout <sup>(2)</sup>		50		100	ms
<b>Diagnostic output (DO)</b>							
5.1	$V_{DOL}$	Output low voltage	$V_{VS} \geq 4.5V; I_{DO} \leq 5mA$	0.3		1.5	V
5.2	$R_{DO}$	Internal pull-up resistance	$V_{DO} \leq V_{VS}$	20		80	k $\Omega$
5.3	$I_{DO\ max}$	Current limitation		5		20	mA
<b>Monitoring of currents through glow plugs (SP1-SN1, SP2-SN2, SP3-SN3, SP4-SN4, SP2-SN5, SP4-SN6)</b>							
6.1	$\Delta V_{OL}$	Open-load threshold	$6V \leq V_{SPX}; V_{SNX} \leq V_{VS} + 3V$	8		16	mV
6.2	$\Delta V_{OC\ 0}$	Overcurrent threshold	$1.5V \leq V_{SPX}; V_{SNX} \leq V_{VS} + 3V$ $V_{MS} < V_{MS\ tc}$ (shunt sense) OCT pin open	160		185	mV
			$1.5V \leq V_{SPX}; V_{SNX} \leq V_{VS} + 3V$ $V_{MS} < V_{MS\ tc}$ (shunt sense) $0V \leq V_{OCT} \leq V_{CUR}$	$V_{OCT} \cdot 0.385$		$V_{OCT} \cdot 0.445$	
			$1.5V \leq V_{SPX}; V_{SNX} \leq V_{VS} + 3V$ $V_{MS} > V_{MS\ tc}$ (transistor sense) $\vartheta = -40^{\circ}C; OCT\ pin\ open$	145		200	mV
			$1.5V \leq V_{SPX}; V_{SNX} \leq V_{VS} + 3V$ $V_{MS} > V_{MS\ tc}$ (transistor sense) $\vartheta = -40^{\circ}C; 0V \leq V_{OCT} \leq V_{CUR}$	$V_{OCT} \cdot 0.345$		$V_{OCT} \cdot 0.485$	
6.3	$TC_{OC}$	Overcurrent threshold temperature coefficient	$V_{MS} < V_{MS\ tc}$ (shunt sense) <sup>1)</sup>		0		K <sup>-1</sup>
			$V_{MS} > V_{MS\ tc}$ (transistor sense) OCT pin open	0.008		0.012	K <sup>-1</sup>
6.4	$t_{OL\ fil}$	Open-load filter time <sup>(2)</sup>	$V_{MS} > V_{MS\ tr}$ (transistor mode)	0.8		1.7	ms
			$V_{MS} < V_{MS\ tr}$ (relay mode)	2		4	ms
6.5	$t_{OC\ fil}$	Overcurrent filter time <sup>(2)</sup>		400		950	$\mu s$

## Electrical specifications

L9524C

Table 4. Electrical characteristics (continued)

Item	Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
<b>Monitoring of external switches (SN1, SN2, SN3, SN4)</b>							
7.1	$V_{SD}$	Switch defect threshold		$V_{VS} \cdot 0.4$		$V_{VS} \cdot 0.6$	
7.2	$t_{SD\ fil}$	Switch defect filter time (2)		2		4	ms
<b>Gate driver outputs (G1, G2, G3, G4)</b>							
8.1	$V_{G\ off}$	Gate off voltage	$I_{GX} \leq 100\mu A$	$V_{SNX}$		$V_{SNX} + 0.7V$	
8.2	$V_{G\ on}$	Gate on voltage	$V_{SNX} = V_{VS}$	$V_{VS} + 5V$		$V_{VS} + 10V$	
8.3	$V_{G\ cl}$	Gate clamping voltage	$V_{SNX} = -20V$	-18		-16	V
8.4	$I_{G\ off}$	Gate discharge current	$4V \leq V_{GX} \leq V_{CP}$ $I_{CUR} = 0$	0.7		1.5	mA
8.5	$I_{G\ on}$	Gate charge current	$0V \leq V_{GX} \leq V_{VS}$ $I_{CUR} = 0$	-1.5		-0.7	mA
8.6	$\frac{dI_{G\ off}}{dI_{CUR}}$	Variation of gate discharge current	$-150\mu A \leq I_{CUR} \leq 0$	4.25		5.25	
8.7	$\frac{dI_{G\ on}}{dI_{CUR}}$	Variation of gate charge current	$-150\mu A \leq I_{CUR} \leq 0$	-5.25		-4.25	
8.8	$R_G$	Output resistance (1)			1		k $\Omega$
8.9	$\Delta t_{G\ on}$	Jitter of output on time		-300		300	$\mu s$
<b>Mode input / relay output (IO)</b>							
9.1	$V_{IO\ on}$	Output on voltage	$I_{IO} \geq -100\mu A$	3		6	V
9.2	$R_{IO}$	Output resistance	$I_{IO} \geq -1mA$	100		500	W
9.3	$I_{IO}$	Input pull-down current	$V_{IO} \geq 1V$	25		100	$\mu A$
			$V_{VS} = 0V$	50		500	$\mu A$
9.4	$I_{IO\ max}$	Current limitation		-25		-5	mA
9.5	$V_{IO\ pr}$	Power regulation threshold		1		2	V
9.6	$t_{IO\ sup}$	Pulse suppress time (2)		2.5		5	ms
<b>Positive sense inputs (SP1, SP2, SP3, SP4)</b>							
10.1	$I_{SP}$	Input pull-down current	$V_{SNX} = V_{SPX} \geq 6V$	15		215	$\mu A$
10.2	$I_{SP\ leak}$	Leakage current	$V_{VS} \leq 3V$ $0 \leq V_{SPX} \leq V_{BAT}$	0		5	$\mu A$
<b>Negative sense inputs (SN1, SN2, SN3, SN4, SN5, SN6)</b>							
11.1	$I_{SN}$	Input pull-down current	$V_{SNX} = V_{SPX} \geq 6V$	15		780	$\mu A$

Table 4. Electrical characteristics (continued)

Item	Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
11.2	$R_{SN1-4}$	Input resistance	$6V \leq V_{SNX} = V_{SPX} \leq 20V$	40		160	$k\Omega$
<b>Overcurrent threshold setting (OCT)</b>							
12.1	$I_{OCT}$	Input pull-up current	$V_{VS} \geq 6V$ $V_{OCT} = 3.5V$	-40		-10	$\mu A$
<b>Power MOSFET gate charge/discharge current setting (CUR)</b>							
13.1	$V_{CUR}$	Output voltage	$I_{CUR} \geq -150\mu A$	2.35	2.5	2.65	V
13.2	$I_{CUR\ max}$	Current limitation	$V_{CUR} \leq 2V$	-500		-250	$\mu A$
<b>Input pin for mode selection (MS)</b>							
14.1	$I_{MS}$	Pull-up current	$V_{MS} = 3V$	-60		-15	$\mu A$
14.2	$V_{MS\ tr}$	Transistor mode threshold		1		2	V
14.3	$V_{MS\ tc}$	Temperature compensation threshold	$V_{VS} \geq 6V$	3		4	V
<b>Output timing</b>							
15.1	$t_{del}$	Delay time <sup>(2)</sup>		2.5		5	ms
15.2	$t_{gap}$	Gap between channels <sup>(2)</sup>		50		250	$\mu s$
15.3	$t_{sup}$	Failure suppress time <sup>(2)</sup>		400		950	$\mu s$
<b>Power regulation</b>							
16.1	$\Delta V_{RMS}$	Accuracy	$8V \leq V_{BAT} \leq 16V$ $30ms \leq T_{CI} \leq 33ms$ $t_{Cl\ on}/T_{CI} \geq 20\%$	-1.5% · $V_{RMSr\ ef}$		1.5% · $V_{RMSr\ ef}$	

1. not tested, guaranteed by design

2. time constants created digitally, verified by scan path test

## 4 Functional description

### 4.1 Operating modes

The L9524C can operate in a total of 6 modes. The selection is done by short-circuiting the appropriate pins and voltages as shown in the following table:

**Table 5. Mode**

Mode	Description	MS pin	BAT pin	IO pin	CI pin
1	relay mode, go/no-go diagnostic interface protocol	ground	ground	output	statical signal
2	relay mode, serial diagnostic interface protocol	ground	battery	output	PWM signal
3	transistor mode, shunt sense, no power regulation	CUR pin	battery	CUR pin	PWM signal
4	transistor mode, shunt sense, power regulation	CUR pin	battery	ground	PWM signal
5	transistor mode, transistor sense, no power regulation	open	battery	CUR pin	PWM signal
6	transistor mode, transistor sense, power regulation	open	battery	ground	PWM signal

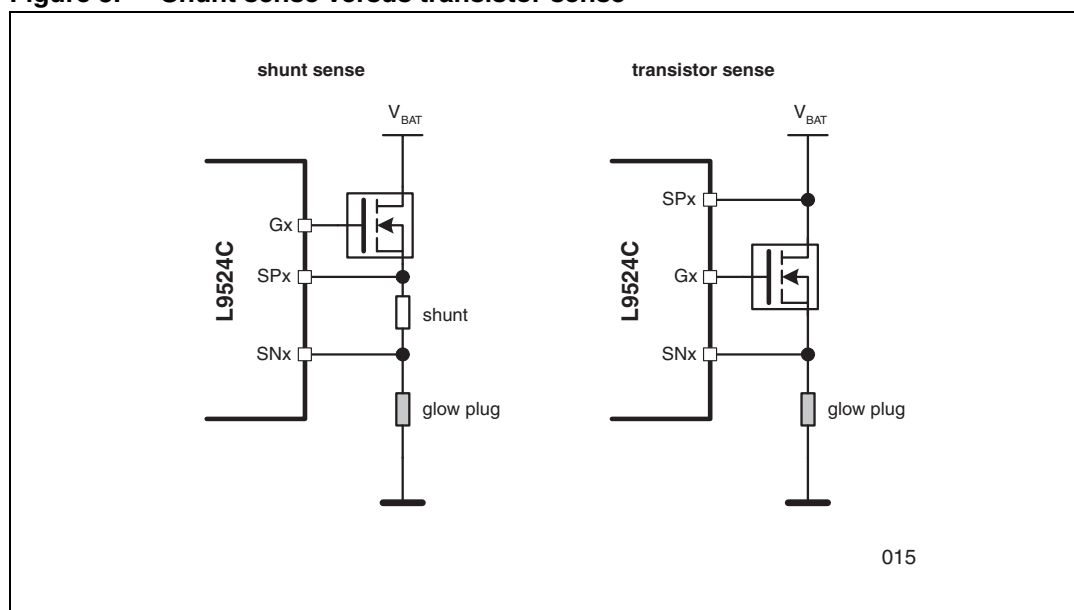
Modes 1 and 2 are for relay usage (referred to as “relay mode”) and modes 3 to 6 for transistors usage (referred to as “transistor mode”).

In relay mode the protocol of the diagnostic interface (DO pin) can be selected from go/no-go protocol and serial protocol (see section “Diagnostic output” for protocol description).

In transistor mode the protocol of the diagnostic interface is the serial protocol. It can be distinguished between using shunts for monitoring the current through the glow plugs (referred to as “shunt sense”) or using the  $R_{DS(on)}$  of the power MOSFETs themselves (referred to as “transistor sense”). In shunt sense mode the resistance of the shunt is assumed to be constant with respect to the temperature while in transistor sense mode the  $R_{DS(on)}$  of the power MOSFETs is assumed to vary with respect to the temperature and therefore overcurrent monitoring is adjusted appropriately.

In transistor mode there are two possibilities to control the output timing. In modes 3 and 5 the timing of the PWM control input signal determines the timing of the PWM signals applied to the external power MOSFETs (“no power regulation”). In modes 4 and 6 the timing of the PWM control input signal determines the power through the glow plugs (“power regulation”) and the timing of the PWM signals applied to the external power MOSFETs is adjusted depending on the battery voltage (see section “Power regulation”).

Figure 3. Shunt sense versus transistor sense



## 4.2 Supply

The main supply pin of the L9524C is the VS pin. The voltage applied to it ( $V_{VS}$ ) is monitored

- to switch off all glow plugs if it is less than  $V_{VS\ uv}$  for at least  $t_{VS\ fil}$  (“undervoltage failure”),
- to switch off all glow plugs if it is greater than  $V_{VS\ ov}$  for at least  $t_{VS\ fil}$  (“overvoltage failure”),
- to switch on all glow plugs if it is greater than  $V_{VS\ ld}$  for at least  $t_{VS\ ld}$  (“active clamping during load dump”),
- to ignore open-load failures if it is less than  $V_{VS\ ol}$ .

*Note:* The glow plugs are switched on again if the corresponding switch-on condition disappears, except if the glow plugs are switched on because of load dump. Then they remain switched on until  $V_{VS}$  is less than  $V_{VS\ ov}$  for at least  $t_{VS\ fil}$ .

In modes 2 to 6, the L9524C is additionally supplied by the BAT pin. This auxiliary supply ensures that the external power MOSFETs are switched off if no main supply voltage is available at the VS pin.

The BAT pin is additionally used to sense the battery voltage  $V_{BAT}$  for power regulation in modes 4 and 6 (see section “Power regulation”) and for detecting “battery undervoltage failure” (fuse between battery and module is defect) if  $V_{BAT}$  is less than  $V_{BAT\ uv}$  for at least  $t_{BAT\ fil}$  in modes 2 to 6.

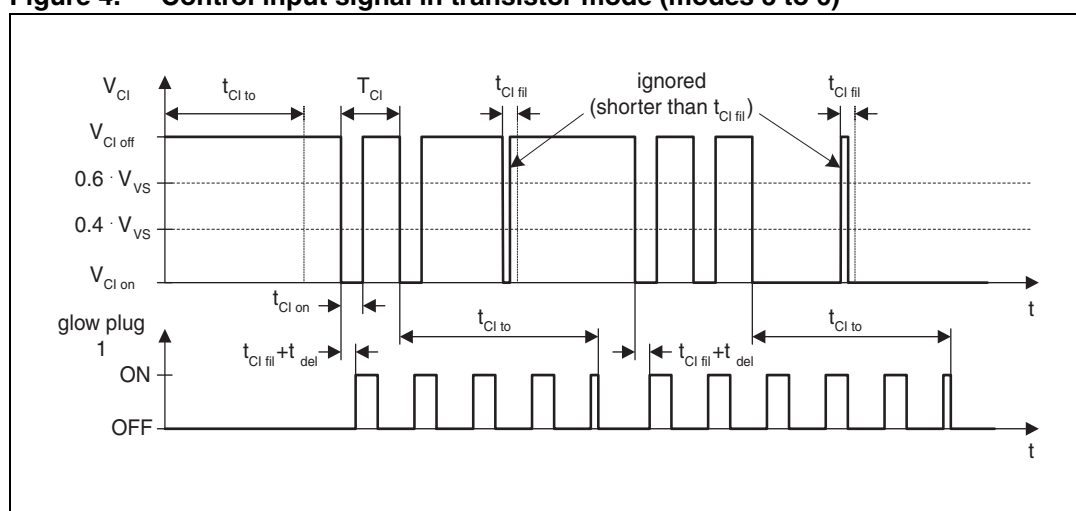
An additional supply voltage higher than the main supply voltage is generated by an internal charge pump which charges an external storage capacitor connected to the CP pin. This capacitor mainly supplies the gates of the external n-channel power MOSFETs. The charge pump voltage  $V_{CP}$  is monitored and the glow plugs are switched off if it is less than  $V_{CP\ uv}$  for at least  $t_{CP\ fil}$  (“charge pump undervoltage”). Afterwards, the glow plugs remain switched

off even if the charge pump voltage becomes greater than  $V_{CP\ uv}$  until they are explicitly switched on again by the CI (control input) pin. Control input

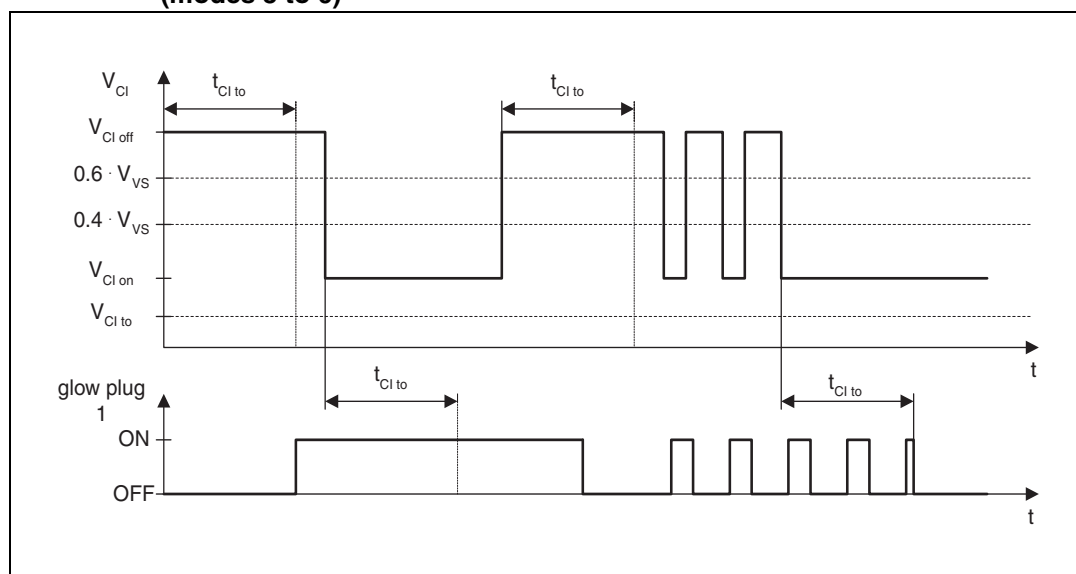
The control input (CI) pin is resistively pulled up  $R_{CI}$  to the supply voltage  $V_{VS}$  such that  $V_{CI}=V_{CI\ off}$  and the glow plugs are switched off by default. The L9524C is controlled by transitions of  $V_{CI}$  from  $V_{CI\ off}$  to  $V_{CI\ on}$  (falling edge) and vice versa (rising edge). Voltage level changes of  $V_{CI}$  which last shorter than  $t_{CI\ fil}$  are ignored.

In transistor mode (modes 3 to 6) the L9524C expects a PWM signal at the CI pin. Each falling edge starts measuring its on time  $t_{CI\ on}$  (time until next rising edge, i.e. length of this low pulse) and its period  $T_{CI}$  (time until next falling edge). The end of a pulse group is detected if no falling edge occurs for a time greater than  $t_{CI\ to}$  and the glow plugs are switched off. Therefore, it is not possible to switch on the glow plugs permanently with one exception: if the low voltage level of the first falling edge is greater than  $V_{CI\ to}$  the glow plugs remain switched on as long as this low pulse lasts.

**Figure 4. Control input signal in transistor mode (modes 3 to 6)**

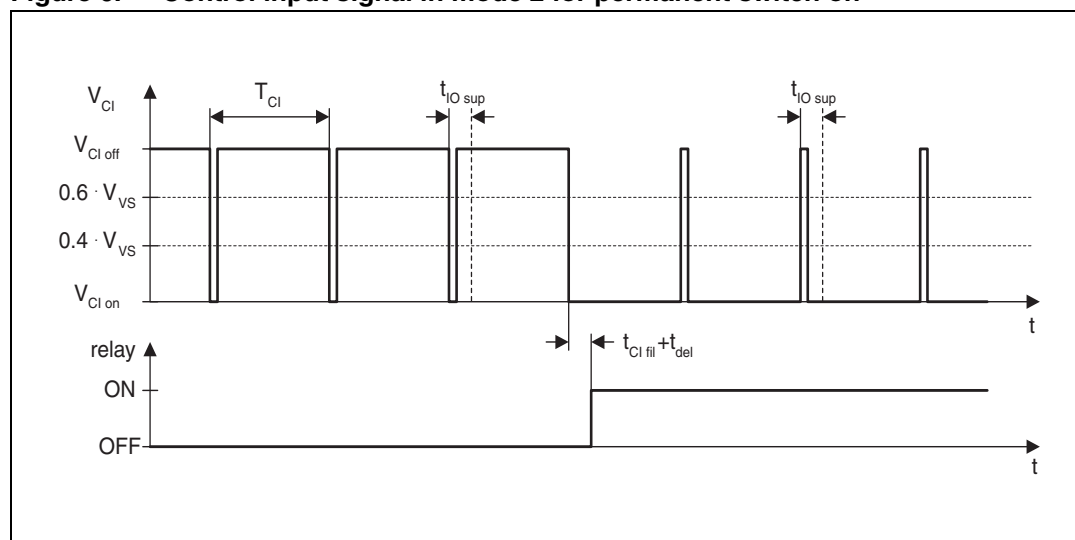


**Figure 5. Permanent switch on of glow plugs at first falling edge in transistor mode (modes 3 to 6)**



Though in mode 2 (relay mode, serial diagnostic interface protocol) the relay should be switched permanently the L9524C also expects a PWM signal at the CI pin since the serial diagnostic interface protocol is synchronized by falling edges of the CI signal (see section “Diagnostic output”). The relay then is switched on permanently if the off time (time between rising and falling edge) of the PWM signal is less than  $t_{IO\ sup}$  since the relay output suppresses pulses shorter than  $t_{IO\ sup}$  (see section “Relay output”). For the same reason the relay is switched off permanently if the on time (time between falling and rising edge) of the PWM signal is less than  $t_{IO\ sup}$ . In all other cases the relay is switched according to the PWM signal at the CI pin.

**Figure 6. Control input signal in mode 2 for permanent switch on**



In mode 1 (relay mode, go/no-go diagnostic interface protocol) no edges are necessary for the go/no-go protocol. Therefore the relay is switched on if  $V_{CI} = V_{CI\ on}$  and it is switched off if  $V_{CI} = V_{CI\ off}$ .

### 4.3 Diagnostic output

The diagnostic output stage of the L9524C (DO pin) consists of a current-limited low-side switch and a pull-up resistor  $R_{DO}$  to the VS pin. The voltage level of a logical low signal  $V_{DOL}$  is given by the drop across the low-side switch and the voltage level of a logical high signal is equal to  $V_{VS}$ .

The L9524C is able to detect the following failures (see sections “Supply”, “Current monitoring”, and “Switch monitoring”):

- open-load (6 glow plugs),
- overcurrent (6 glow plugs, stored until power-down),
- any switch is defect (4 switches),
- supply voltage ( $V_{VS}$ ) is too low (“undervoltage”),
- supply voltage ( $V_{VS}$ ) is too high (“overvoltage”),
- junction temperature ( $T_J$ ) is too high,
- charge pump voltage ( $V_{CP}$ ) is too low (“charge pump undervoltage”), and
- battery voltage ( $V_{BAT}$ ) is too low (“battery undervoltage”).

In order to report the occurrence of any of the above-listed failures to the diesel engine management system the L9524C provides two protocols: go/no-go protocol for mode 1 and serial protocol for modes 2 to 6.

The go/no-go protocol is only able to report if any of the above-listed failures occurred. This is done according to the following table:

$V_{CI}$	$V_{DO}$ at “no failure”	$V_{DO}$ at “any failure”
$V_{CI\ off}$	$V_{DOL}$	$V_{VS}$
$V_{CI\ on}$	$V_{VS}$	$V_{DOL}$

*Note:* overcurrent failures are stored until power-down.

The serial protocol is able to report different kinds of failures and to assign them to the corresponding glow plugs. Therefore, occurring failures are written into an internal 8-bit failure register:

Bit	Meaning of high state
1	Open-load or overcurrent <sup>(1)</sup> failure at glow plug 1
2	Open-load or overcurrent <sup>(1)</sup> failure at glow plug 2
3	Open-load or overcurrent <sup>(1)</sup> failure at glow plug 3
4	Open-load or overcurrent <sup>(1)</sup> failure at glow plug 4
5	Open-load or overcurrent <sup>(1)</sup> failure at glow plug 5
6	Open-load or overcurrent <sup>(1)</sup> failure at glow plug 6
7	Overcurrent failure at any glow plug <sup>(1)</sup> or battery voltage ( $V_{BAT}$ ) is too low <sup>(2)</sup> (“battery undervoltage”)
8	One or more of the following failures (“module failure”): any switch is defect supply voltage ( $V_{VS}$ ) is too low (“undervoltage”) supply voltage ( $V_{VS}$ ) is too high (“overvoltage”) junction temperature ( $T_J$ ) is too high charge pump voltage ( $V_{CP}$ ) is too low (“charge pump undervoltage”) battery voltage ( $V_{BAT}$ ) is too low <sup>(2)</sup> (“battery undervoltage”)

- overcurrent failures are stored until power-down
- if battery voltage is too low (“battery undervoltage”) bits 7 and 8 are high

Bits 1 to 6 are assigned to the glow plugs. Depending on bit 7 they show open-load (bit 7 is low) or overcurrent failures (bit 7 is high). Bit 8 shows if there is any of the listed failures (“module failure”). In case of a battery undervoltage failure bits 7 and 8 are high and all other bits are low as long as there is no overcurrent failure stored.

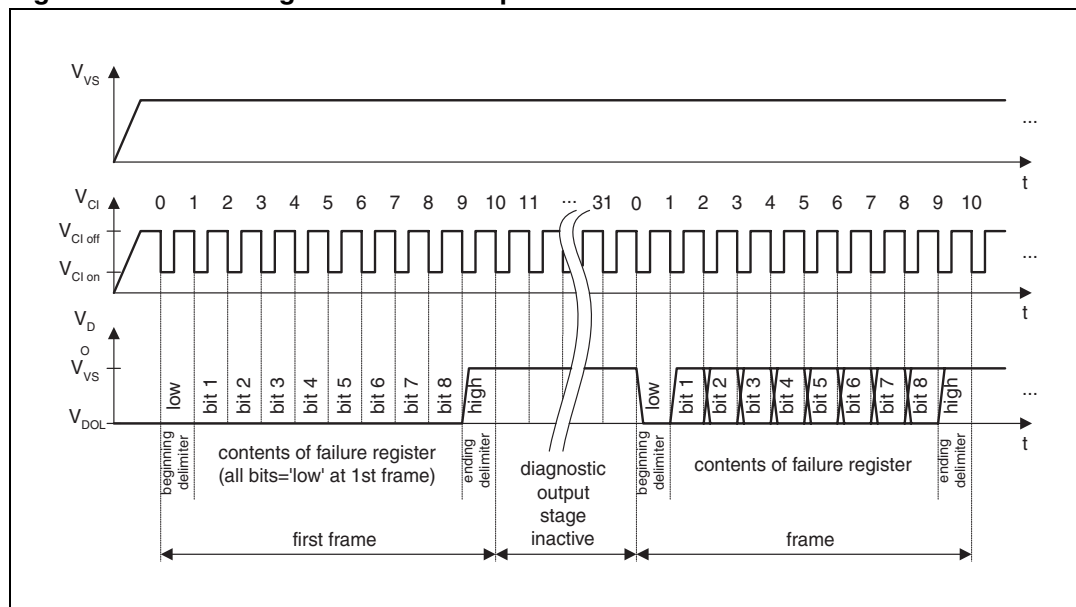
For transmitting the contents of the failure register the PWM signal applied to the CI pin is used as clock input: at any falling edge of the CI signal (see section “Control input”) the DO pin shows the value of the next bit of the bitstream after  $t_{DO\ del}$ .

Each transmission frame consists of a beginning delimiter (one low bit) followed by the 8 bits of the failure register beginning with bit 1. After the ending delimiter (one high bit) the diagnostic output stage is inactive and is resistively pulled up to  $V_{VS}$ .



The L9524C starts transmitting the first frame at the very first falling edge of the CI signal after power-on. Since at that time the contents of the failure register are clear the first 9 bits (beginning delimiter followed by the contents of the 8-bit failure register) which are transmitted are always low. The L9524C repeats transmission of the frame every 32 falling edges of the CI signal. Only during the time when the diagnostic output stage is inactive (i.e. between the transmission of two frames) the contents of the failure register can be written.

**Figure 7. Serial diagnostic interface protocol**



## 4.4 Current monitoring

The L9524C is able to monitor the current through 6 glow plugs by measuring the voltage drop across sense resistors. Therefore, there are 4 positive sense input pins (SP1, SP2, SP3, SP4) and 6 negative sense input pins (SN1, SN2, SN3, SN4, SN5, SN6). The sense input pins must be connected to the sense resistors according to the following table:

Sense resistor of glow plug	Positive sense input pin	Negative sense input pin
1	SP1	SN1
2	SP2	SN2
3	SP3	SN3
4	SP4	SN4
5	SP2	SN5
6	SP4	SN6

In relay mode (modes 1 and 2) the positive sense input pins are short-circuited since the relay is the only switch. In transistor mode (modes 3 to 6) glow plug 5 is switched with transistor 2 and glow plug 6 with transistor 4. Therefore only 4 positive sense input pins are necessary.

If the voltage drop across the sense resistor is less than  $\Delta V_{OL}$  for at least  $t_{OL\ fill}$  an open-load failure is detected as long as  $V_{VS} > V_{VS\ ol}$ . If it is greater than  $\Delta V_{OC}$  (see below for definition) for at least  $t_{OC\ fill}$  an overcurrent failure is detected and the corresponding switch is switched off and remains switched off until power-down. The threshold for overcurrent failures  $\Delta V_{OC}$  can be varied by the voltage applied to the OCT pin (see section "Overcurrent threshold variation").

In modes 1 to 4 the overcurrent threshold is constant with respect to the temperature ( $TC_{OC} = 0$ ). But in modes 5 and 6 the overcurrent threshold increases linearly with the temperature  $\vartheta$  to compensate the first-order temperature coefficient of the  $R_{DS(on)}$  of the external power MOSFETs which are used as sense resistors in these modes:

#### Equation 1

$$\Delta V_{OC} = \Delta V_{OC\ 0} (1 + TC_{OC} (\vartheta + 40^{\circ}\text{C})).$$

## 4.5 Switch monitoring

The L9524C monitors the voltages across the glow plugs (using the negative sense input pins SN1, SN2, SN3, and SN4) to detect if the corresponding switches work properly or not. A switch is detected as defect if it is switched on but the voltage across the corresponding glow plug(s) is less than  $V_{SD}$  for at least  $t_{SD\ fill}$  or if it is switched off but the voltage across the glow plug(s) is greater than  $V_{SD}$  for at least  $t_{SD\ fill}$ .

## 4.6 Thermal shutdown

If the junction temperature becomes greater than  $T_{JSD}$  all glow plugs are switched off. They are switched on again if the junction temperature falls below  $T_{JSD}$ .

## 4.7 Gate drivers

The L9524C contains four gate drivers (Gx pins) for external n-channel power MOSFETs in high-side configuration. Each gate driver provides a slope control by charging and discharging the gates of the external power MOSFETs with constant currents ( $I_{G\ on}$  or  $I_{G\ off}$ ). To adjust the slopes these currents can be varied using the CUR pin (see section "Gate charge/discharge current variation"). The charging current source is supplied by an external capacitor connected to the charge pump output (CP) pin. The gate-to-source voltages are limited internally and without supply voltage ( $V_{VS}$ ) the gates and the sources of the external power MOSFETs are short-circuited.

During free-wheeling of inductive loads the gates of the external power MOSFETs are clamped to  $V_{G\ cl}$ . As a result, the power MOSFETs become conducting and the energy in the inductive loads is recirculated through the power MOSFETs.

## 4.8 Relay output

In relay mode (modes 1 and 2) the IO pin is used as output pin to control an external relay driver (e.g. a low-side switch which drives the relay). If the output stage of the IO pin is switched on it behaves like a voltage source ( $V_{IO}$ ) with output resistance  $R_{IO}$ . If it is switched off a pull-down current source is activated ( $I_{IO}$ ). The relay output suppresses pulses shorter

than  $t_{IO\ sup}$  such that the relay can be permanently switched by applying appropriate PWM signals to the CI pin (see section "Control input").

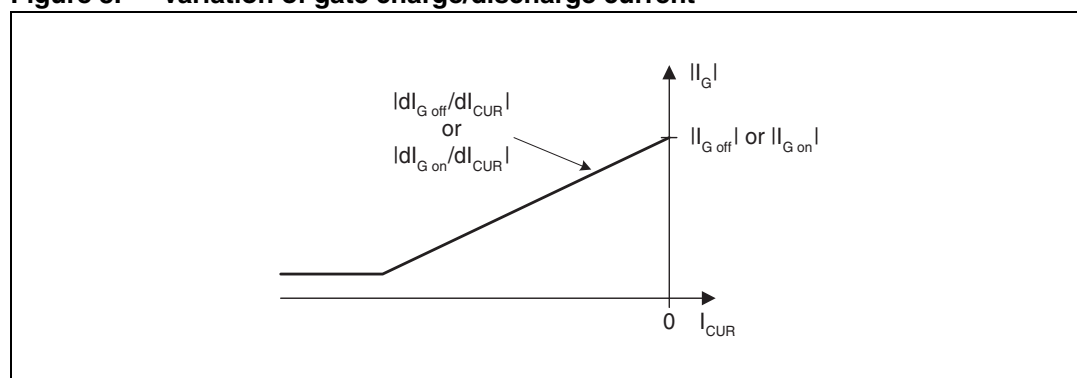
In transistor mode (modes 3 to 6) the IO pin is used as input pin. Left open it is pulled down to ground and the power regulation feature (see section "Power regulation") is activated ( $V_{IO} < V_{IO\ pr}$ ). To deactivate the power regulation feature the IO pin must be connected to the CUR pin ( $V_{IO} = V_{CUR} > V_{IO\ pr}$ ).

## 4.9 Gate charge/discharge current variation

The CUR pin provides a constant current-limited output voltage  $V_{CUR}$ . This voltage can be applied to an external resistor making current flow out of the CUR pin. As a result, the default gate charge (or discharge) current  $I_{G\ on}$  (or  $I_{G\ off}$ ) is reduced by a multiple  $dI_{G\ on}/dI_{CUR}$  (or  $dI_{G\ off}/dI_{CUR}$ ) of the current flowing out of the CUR pin.

In order to select the mode of operation the IO pin and/or the MS pin may be connected to the CUR pin (see section "Modes"). The IO pin contains a pull-down current source and the MS pin contains a pull-up current source. These currents are compensated if the corresponding pin is connected to the CUR pin in order not to affect the gate charge/discharge current.

**Figure 8. Variation of gate charge/discharge current**



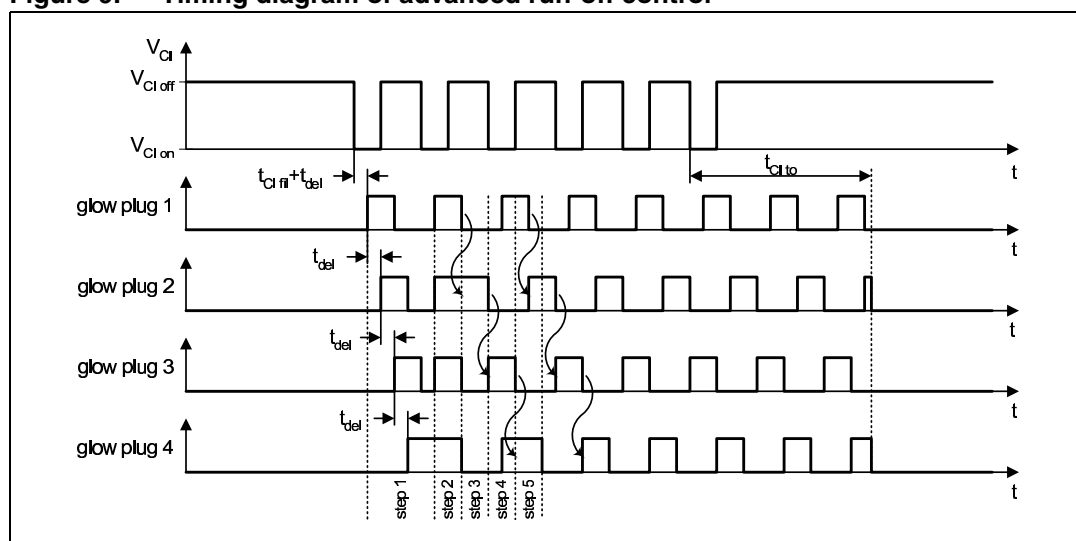
## 4.10 Overcurrent threshold variation

The overcurrent threshold  $\Delta V_{OC}$  can be varied by connecting the OCT pin to an external resistive voltage divider between CUR pin and ground. If the OCT pin is left open it is pulled up to an internal supply voltage by a current source and a default value is used for the overcurrent threshold. This default value corresponds to the condition:  $V_{OCT} = V_{CUR}/6$ . In order not to detune the voltage divider the pull-up current  $I_{OCT}$  source is deactivated when any glow plug is switched on.

## 4.11 Advanced run-off control

In transistor mode (modes 3 to 6) the glow plugs are switched by an advanced run-off control. The target is to minimize changes in the load current. Therefore, the PWM signals applied to the glow plugs are phase-shifted to each other. There is a 5-step start-up procedure at the beginning of a switching sequence. In step 1 the phase shift between the glow plugs is set to a fixed value  $t_{del}$ . Therefore, all glow plugs are switched on once in the first period of the PWM control input signal (CI) and are heated up quite simultaneously. During the start-up procedure the phase shift becomes a value equal to the on time of one glow plug. As a result, after the start-up procedure the glow plugs are switched on one after the other to get minimal changes in the load current.

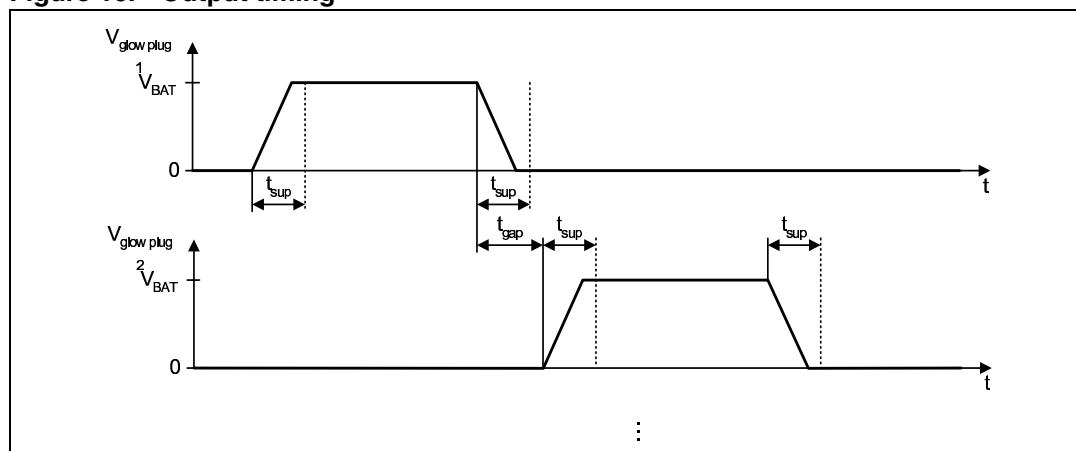
**Figure 9. Timing diagram of advanced run-off control**



## 4.12 Output timing

In transistor mode (modes 3 to 6) there is a delay  $t_{gap}$  between switching off one glow plug and switching on the next one to avoid overlaps. Additionally, failures occurring during the slope (i.e. in the time period  $t_{sup}$  after switching) are suppressed in all modes.

**Figure 10. Output timing**



## 4.13 Power regulation

The power through each glow plug (here expressed by  $V_{\text{RMS}}$  which is the root-mean-square voltage across one glow plug) depends on the battery voltage  $V_{\text{BAT}}$  and the duty cycle  $t_{\text{G on}}/T_{\text{G}}$  of the PWM signal applied to the external power MOSFETs:

### Equation 2

$$V_{\text{RMS}} = V_{\text{BAT}} \cdot \sqrt{\frac{t_{\text{G on}}}{T_{\text{G}}}}$$

In order to regulate the power through the glow plugs the L9524C measures  $V_{\text{BAT}}$  and adjusts  $t_{\text{G on}}/T_{\text{G}}$  of the gate drivers (G1...4) such that  $V_{\text{RMS}} = V_{\text{RMS ref}}$ , where  $V_{\text{RMS ref}}$  represents the desired power through each glow plug.

The desired power  $V_{\text{RMS ref}}$  is given by the input duty cycle  $t_{\text{Cl on}}/T_{\text{Cl}}$  which represents the desired output duty cycle at a nominal battery voltage of 12V:

### Equation 3

$$V_{\text{RMS ref}} = 12\text{V} \cdot \sqrt{\frac{t_{\text{Cl on}}}{T_{\text{Cl}}}}$$

As a result, the actual output duty cycle of the gate drivers is given by:

### Equation 4

$$\frac{t_{\text{G on}}}{T_{\text{G}}} = \left(\frac{12\text{V}}{V_{\text{BAT}}}\right)^2 \cdot \frac{t_{\text{Cl on}}}{T_{\text{Cl}}}$$

*Note:* the L9524C varies both the on time  $t_{\text{G on}}$  and the period  $T_{\text{G}}$  of the PWM output signal to vary the duty cycle  $t_{\text{G on}}/T_{\text{G}}$ .

The accuracy of the power regulation is given by  $\Delta V_{\text{RMS}} = V_{\text{RMS}} - V_{\text{RMS ref}}$ .

# 5 Application diagrams

Figure 11. Mode 1: relay mode, go/no-go diagnostic interface protocol

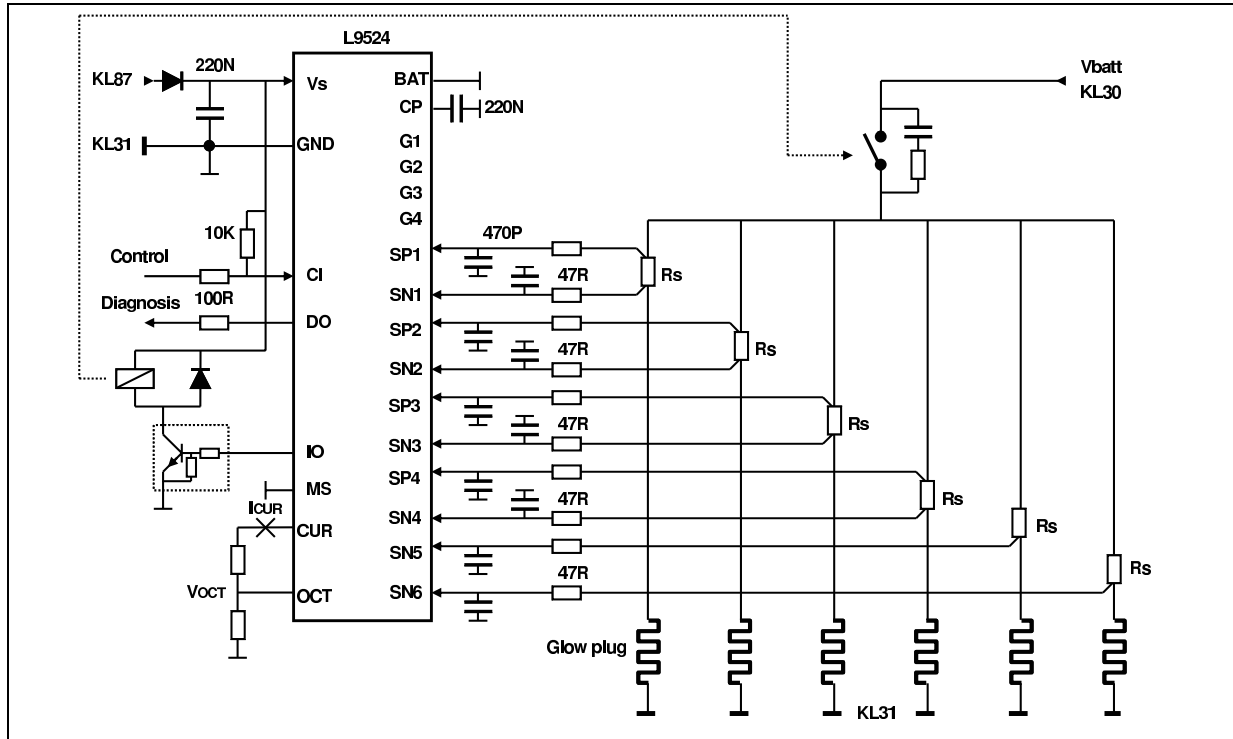


Figure 12. Mode 2: relay mode, serial diagnostic interface protocol

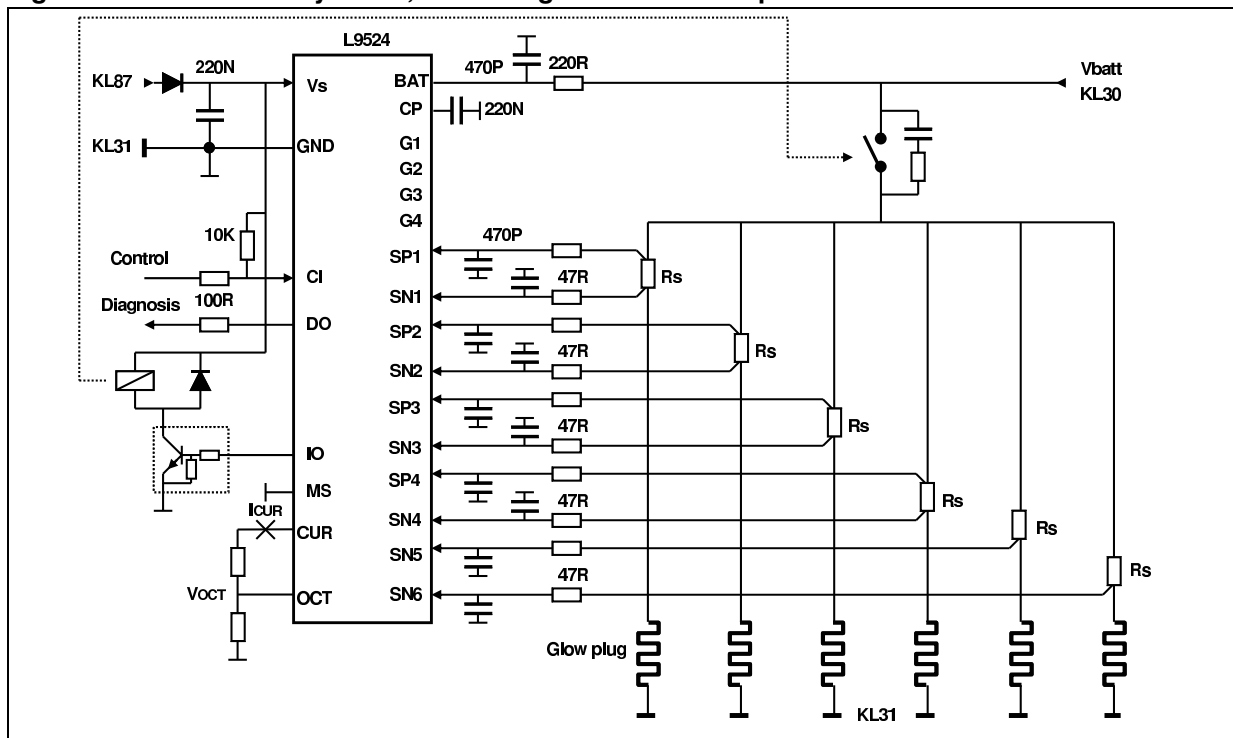


Figure 13. Mode 3: transistor mode, shunt sense, no power regulation

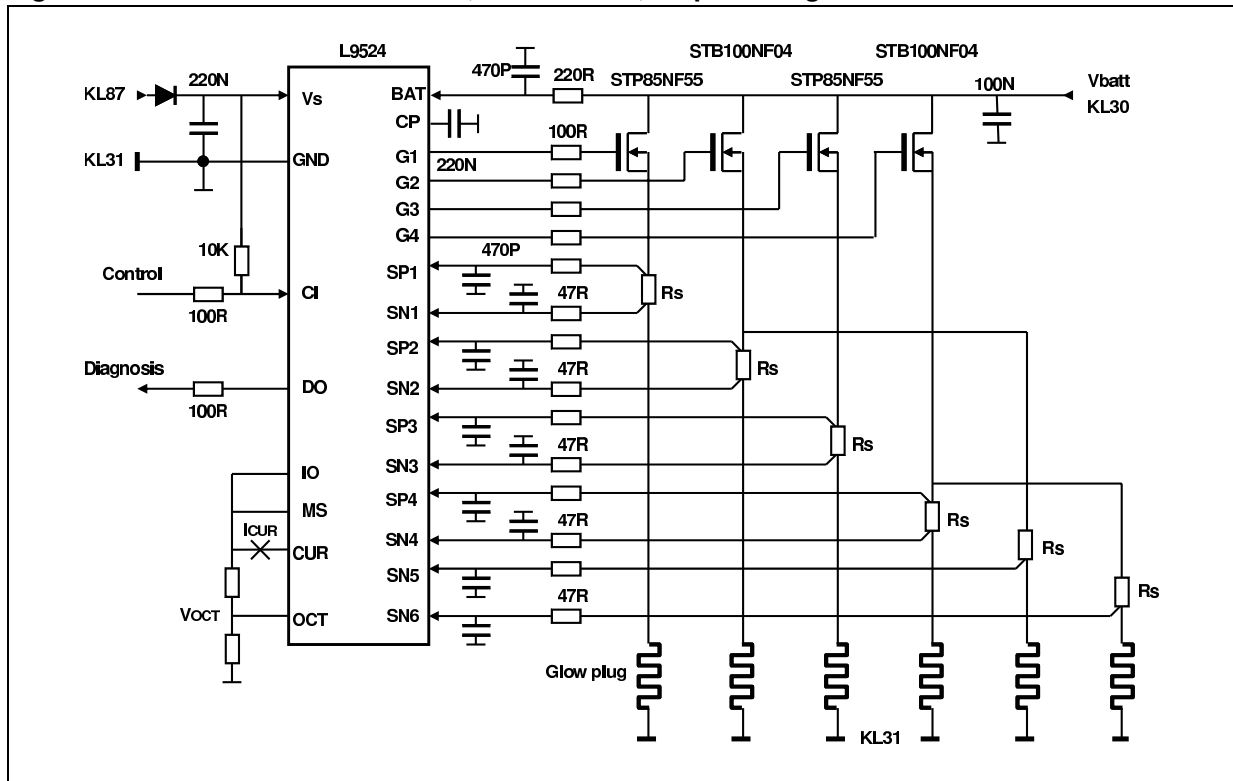


Figure 14. Mode 4: transistor mode, shunt sense, power regulation

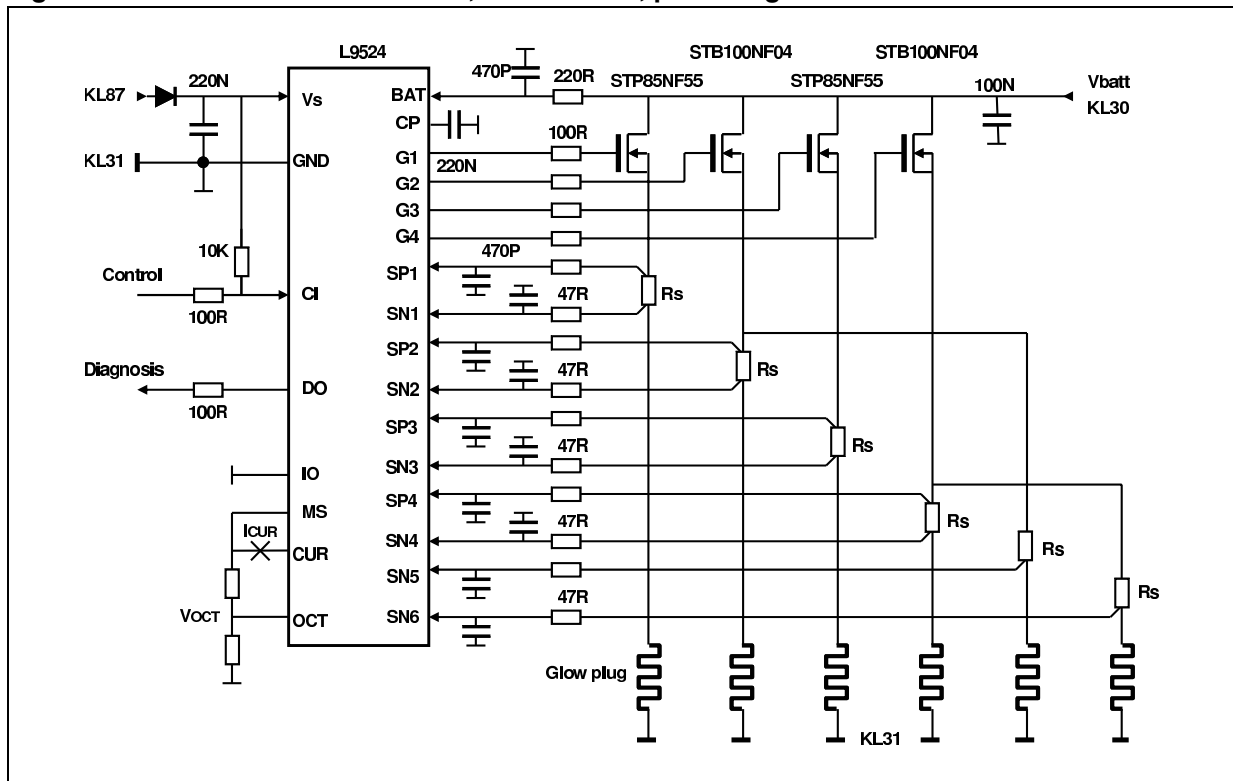


Figure 15. Mode 5: transistor mode, transistor sense, no power regulation

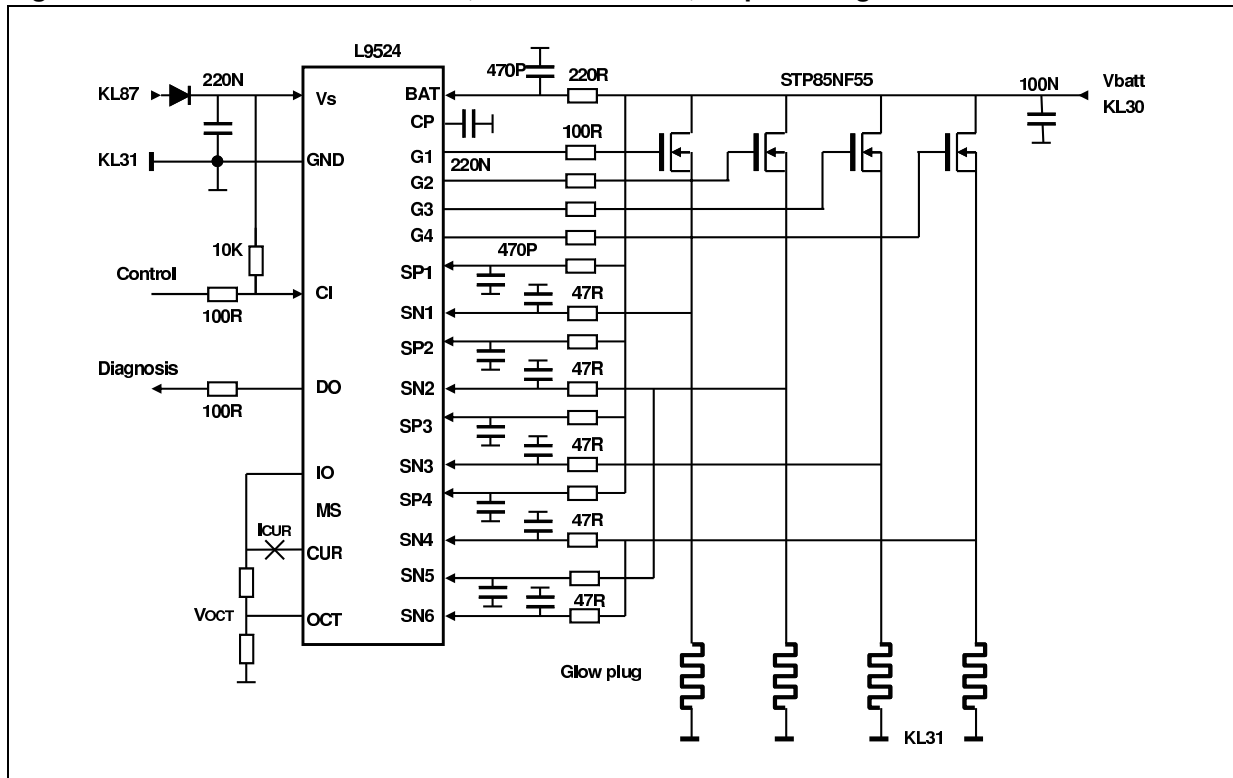
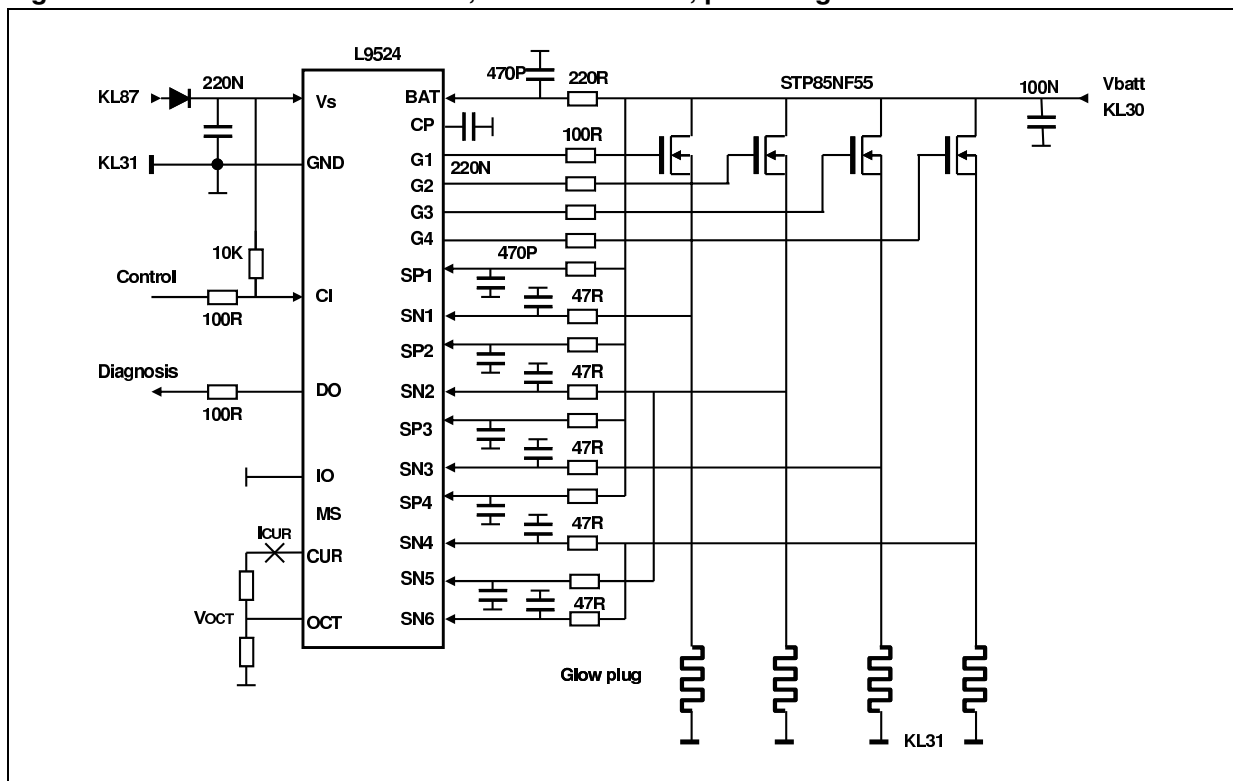


Figure 16. Mode 6: transistor mode, transistor sense, power regulation

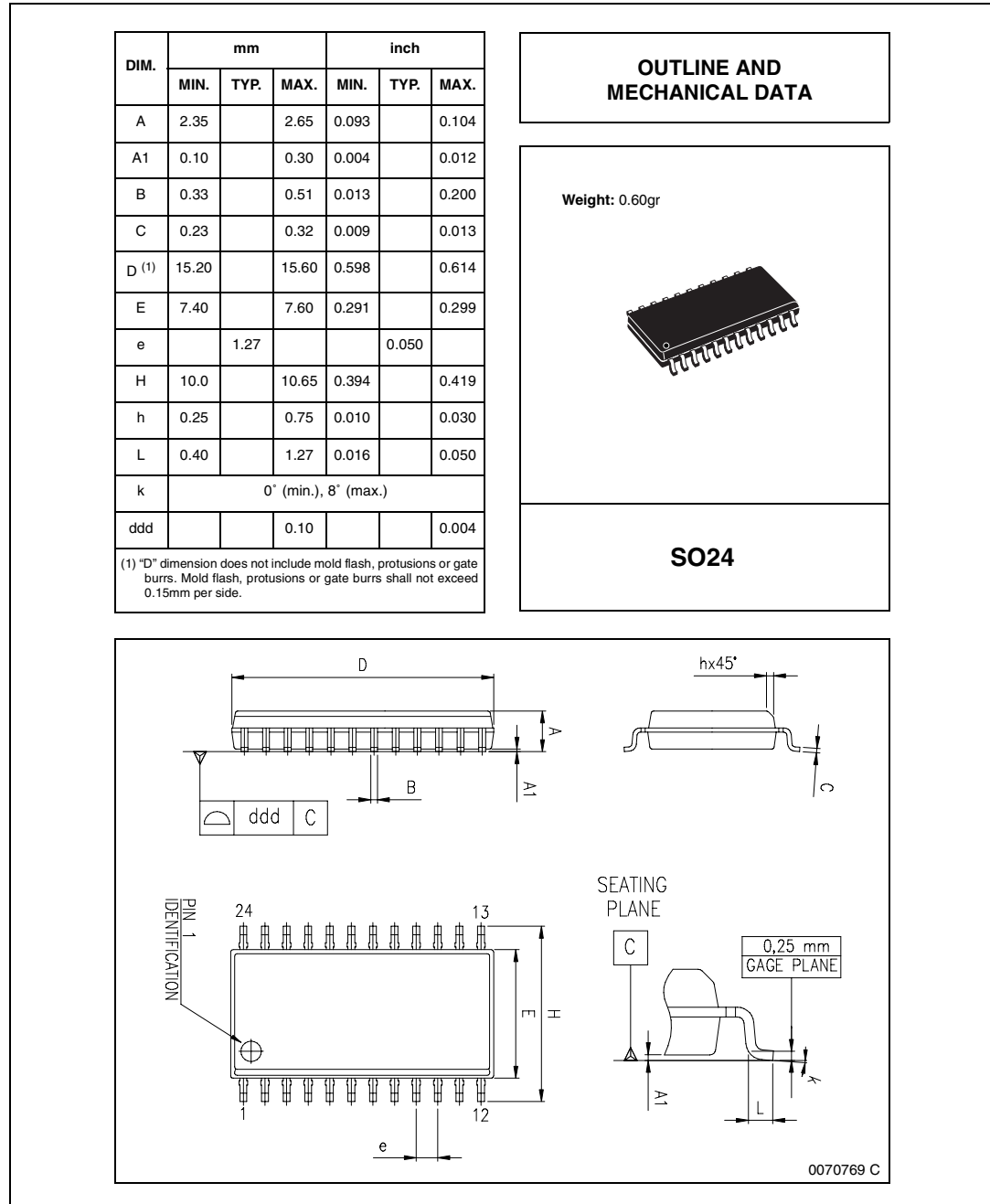




## 6 Package information

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect. The category of second Level Interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: [www.st.com](http://www.st.com).

**Figure 17. SO24 mechanical data and package dimensions**



## 7 Revision history

**Table 6. Document revision history**

Date	Revision	Description of Changes
22-Sep-2006	1	Initial release

**L9524C**

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