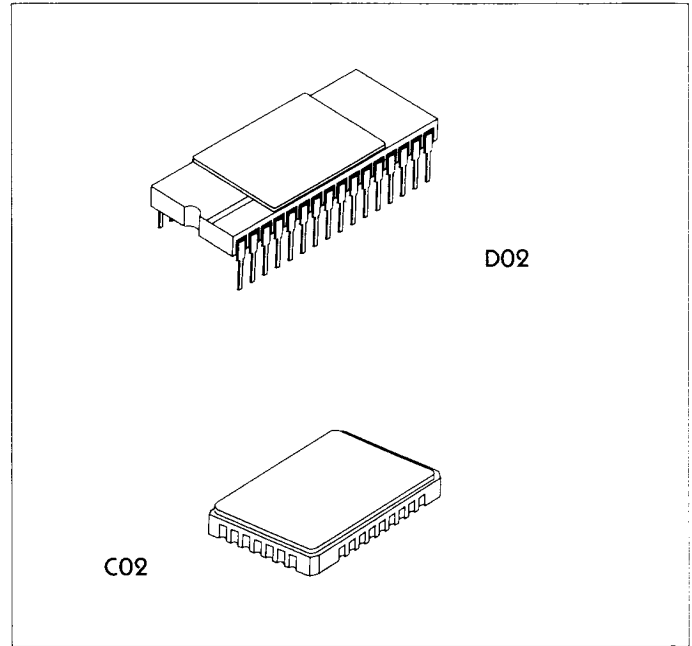


DESCRIPTION

The ELMO EIC01MS08 is a monolithic 131,072-word x 8-bit high speed CMOS static RAM suitable for use in low power and high speed applications. It comes in several package styles and operates from a single +5V supply.

FEATURES

- ❖ 131,072-word x 8-bit Organization
- ❖ Fast Access Times: 35, 45 or 55 ns
- ❖ Low Power Operation:
 - Standby: 50uW (Typ.)
 - Operating: 150mW (Typ.)
- ❖ Single +5V ($\pm 10\%$) Power Supply
- ❖ TTL Compatible Inputs and Outputs
- ❖ Fully Static Operation
- ❖ MIL Temp. Range (-55 to 125°C)
- ❖ Available In:
 - 32 Pin 600-mil DIP
 - 32 Pad 700x450-mil LCC



PACKAGE/SPEED OPTIONS

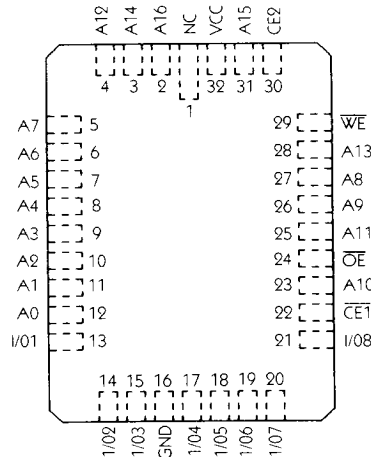
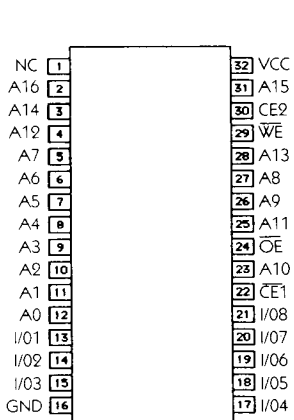
Package: 32 Pad LCC 700x450-mils

Part Number	Speed
EIC01MS08C02 -035D	35ns
-045D	45ns
-055D	55ns

Package: 32 Pin 600-mil-DIP (JEDEC)

Part Number	Speed
EIC01MS08D02 -035D	35ns
-045D	45ns
-055D	55ns

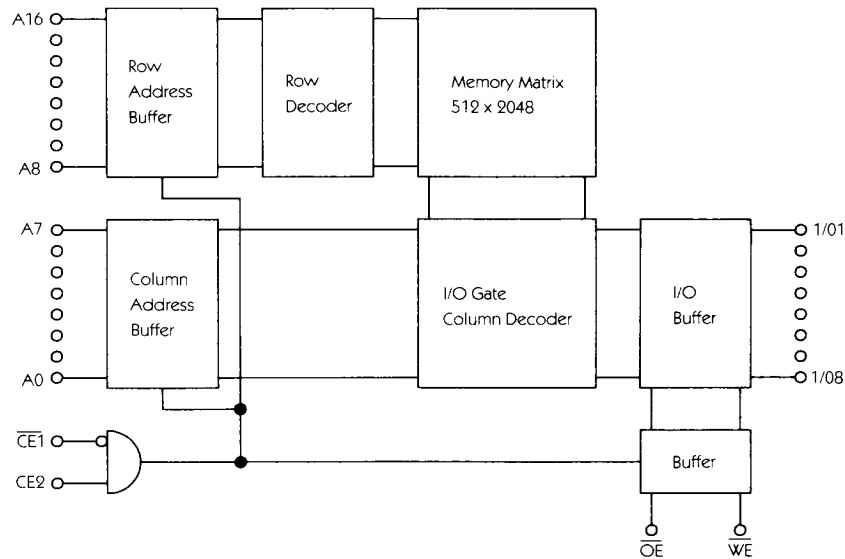
PIN CONFIGURATION



PIN NAMES

A0 to A16	Address Input
I/O1 to I/O8	Data Input/Output
CE1, CE2	Chip Enable
WE	Write Enable
OE	Output Enable
VCC	+5V Power Supply
GND	Ground
NC	No Connect

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Supply Voltage	V _{cc}	-0.5 to +7.0	V
Input Voltage	V _{in}	-0.5 to V _{cc} +0.5	V
Input and Output Voltage	V _{i/o}	-0.5 to V _{cc} +0.5	V
Allowable Power Dissipation	P _d	1.0	W
Operating Temperature	T _{opr}	-55 to +125	C
Storage Temperature	T _{stg}	-65 to +150	C

TRUTH TABLE

CE1	CE2	OE	WE	MODE	I/01 TO I/08	V _{cc} Current
H	X	X	X	Not Selected	High Z	ISB1, ISB2
X	L	X	X	Not Selected	High Z	ISB1, ISB2
L	H	H	H	Output Disable	High Z	ICC1, ICC2
L	H	L	H	Read	Data Out	ICC1, ICC2
L	H	X	L	Write	Data In	ICC1, ICC2

DC OPERATING CONDITIONS (T_a = -55 to +125°C)

Item	Symbol	Min	Typ.	Max.	Unit
Supply Voltage	V _{cc}	5.5	5.0	5.5	V
Input High Voltage	V _{IH}	2.2		V _{cc} +0.3	V
Input Low Voltage	V _{IL}	-0.3		0.8	V

DC OPERATING CHARACTERISTICS (V_{CC}= 5V±10%, T_a= -55°C to +125°C)

Item	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Input Leakage Current	I _{IL}	V _{IN} =GND to V _{CC}	-2		2	μA
Output Leakage Current	I _{OL}	V _{I/O} =GND to V _{CC} , $\overline{CE1}$ =V _{IH} or CE ₂ =V _{IL} or \overline{OE} =V _{IH} or \overline{WE} =V _{IL}	-2		2	μA
Operating Power Supply Current	ICC1	$\overline{CE1}$ =V _{IL} , CE ₂ =V _{IH} , V _{IN} =V _{IH} or V _{IL} , I _O UT=0mA		30	80	mA
Average Operating Current	ICC2	Cycle=Min., Duty=100%, I _O UT=0mA		60	120	mA
Standby Current	ISB1	$\overline{CE1}$ ≥V _{CC} -0.2V or CE ₂ ≤0.2V, V _{IN} ≥V _{CC} -0.25 or V _{IN} ≤0.2V		0.01	2	mA
	ISB2	$\overline{CE1}$ =V _{IH} or CE ₂ =V _{IL} , V _{IN} =V _{IL} or V _{IH}			15	mA
Output High Voltage	V _{OH}	I _{OH} = -4.0mA	2.4			V
Output Low Voltage	V _{OL}	I _{OL} = -8.0mA			0.4	V

I/O CAPACITANCE (T_a=25°C, f=1MHz)

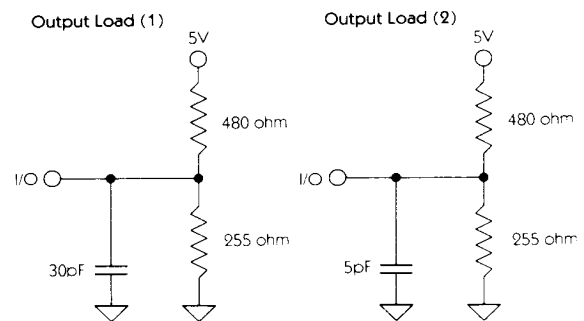
Item	Symbol	Test Condition	Min.	Max.	Unit
Input Capacitance	C _{IN}	V _{IN} =0V		7	pF
I/O Capacitance	C _{I/O}	V _{I/O} =0V		7	pF

Note.) This parameter is sampled and is not 100% tested.

AC CHARACTERISTICS

AC test conditions (V_{CC}=5V±10%, T_A=-55°C to +125°C)

Item	Condition
Input Pulse High Level	V _{IH} =3.0V
Input Pulse Low Level	V _{IL} =0V
Input Rise Time	t _r =5ns
Input Fall Time	t _f =5ns
Input and Output Reference Level	1.5V
Output Load	Fig.1



Note. Load capacitance includes scope and jig capacitances

Figure1

READ CYCLE

Item	Symbol	-35		-45		-55		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle Time	TAVAV	35		45		55		ns
Address Access Time	TAVQV		35		45		55	ns
Chip Enable Access Time (2)	TE1LQV TE2HQV		35		45		55	ns
Output Enable to Output Valid	TGLQV		20		25		30	ns
Chip Enable to Output in High Z (1) (2)	TE1HQZ TE2LQZ		15		20		25	ns
Chip Enable to Output in Low Z (1) (2)	TE1LQX TE2HQX	5		5		5		ns
Chip Disable to Output in High Z (1)	TGHQZ		15		20		25	ns
Chip Enable to Output in Low Z (1)	TGLQX	0	1	0	2	0	2	ns
Output Hold from Address Change	TAVQX	5		5		5		ns

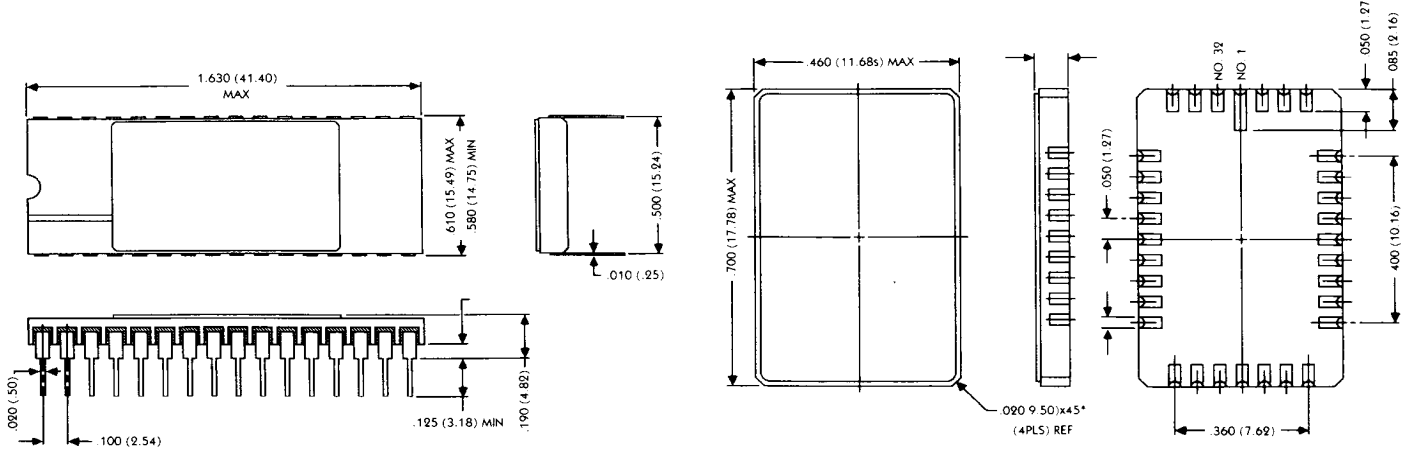
WRITE CYCLE

Item	Symbol	-35		-45		-55		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Write Cycle Time	TAVAV	35		45		55		ns
Address Valid to End of Write	TAVWH	30		40		45		ns
Chip Enable to End of Write (2)	TE1LWH TE2HWH	30		40		45		ns
	TWLE1H TWLE2L	30		40		45		ns
Data to Write Time Overlap (2)	TDVWH	18		20		25		ns
	TDVE1H TDVE2L	18		20		25		ns
Data Hold Time from Write (2)	TWHDX TE1HDX TE2LDX	0		0		0		ns
Write Pulse Width (2)	TWLWH TE1LEH TE2HEL	30		35		40		ns
Address Set -UpTime (2)	TAVWL	0		0		0		ns
	TAVE1L TAVE2H	0		0		0		ns
Write Recovery Time (2)	TWHAX TE1HAX TE2LAX	3		3		3		ns
		3		3		3		ns
Write to Output in High Z (1)	TWLQZ		15		15		15	ns
Output Active from End of Write (1)	TWHQX	5		5		5		ns

Note 1: Parameters tested on a sample basis only. Note 2: Symbols "E1" and "E2" are "CE1" and "CE2" resp.

PACKAGE OUTLINE

Dimensions in Inches (Millimeters)



Package Type DO2, 32 Lead .600" Sidebraced DIP

Package Type CO2, 32 Pad LCC

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