SM550/SM551/SM552 4-Bit Microcomputer (Controller)

■ Description

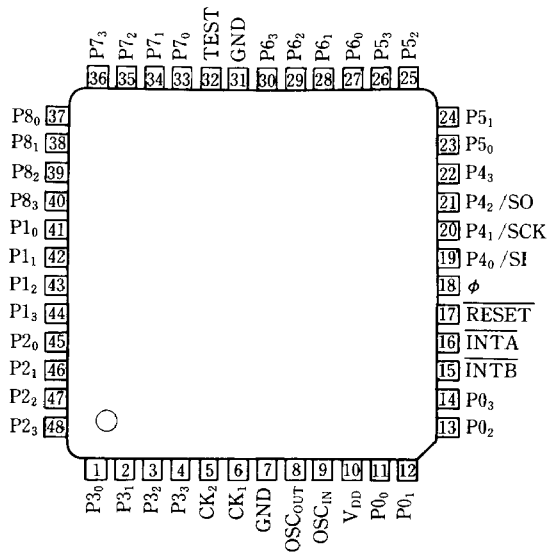
The SM550/SM551/SM552 is a CMOS 4-bit microcomputer which integrates a 4-bit parallel processing function, a ROM, a RAM, I/O ports, a serial interface, a timer/event counter in a single chip.

It provides five kinds of interrupt and a sub-routine stack function using the RAM area, and accesses on a byte-by-byte basis.

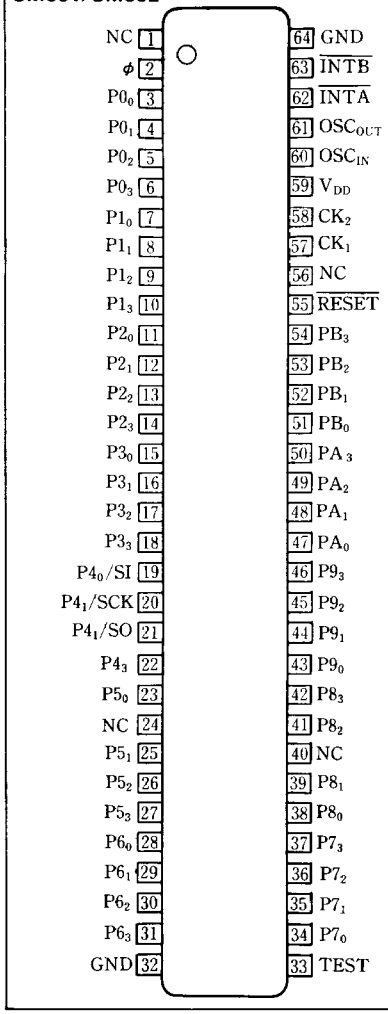
Operated from 3 to 5V single power supply with high speed, this microcomputers applicable to many applications from a battery back-up system to a high performance system.

■ Pin Connections

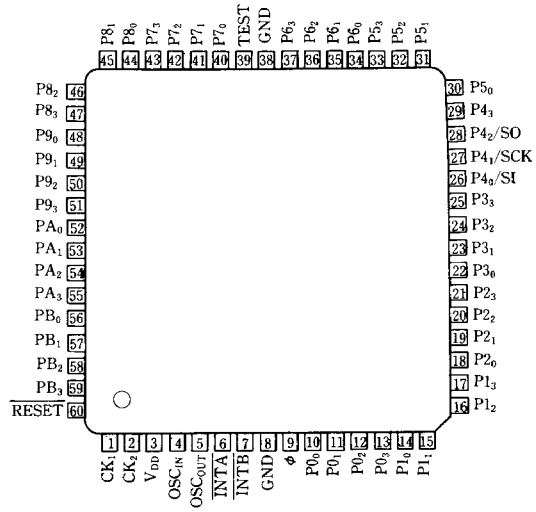
SM550



SM551/SM552



SM551/SM552

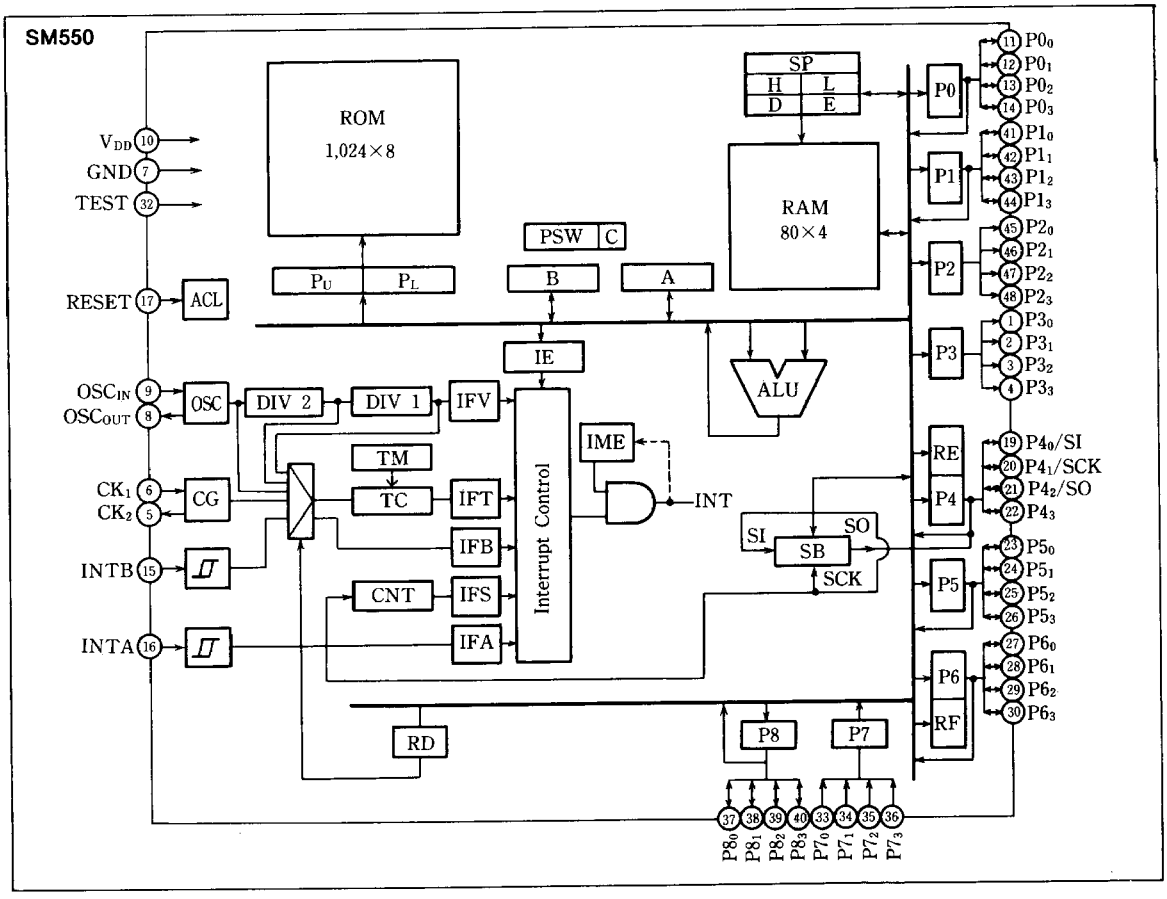


Top View

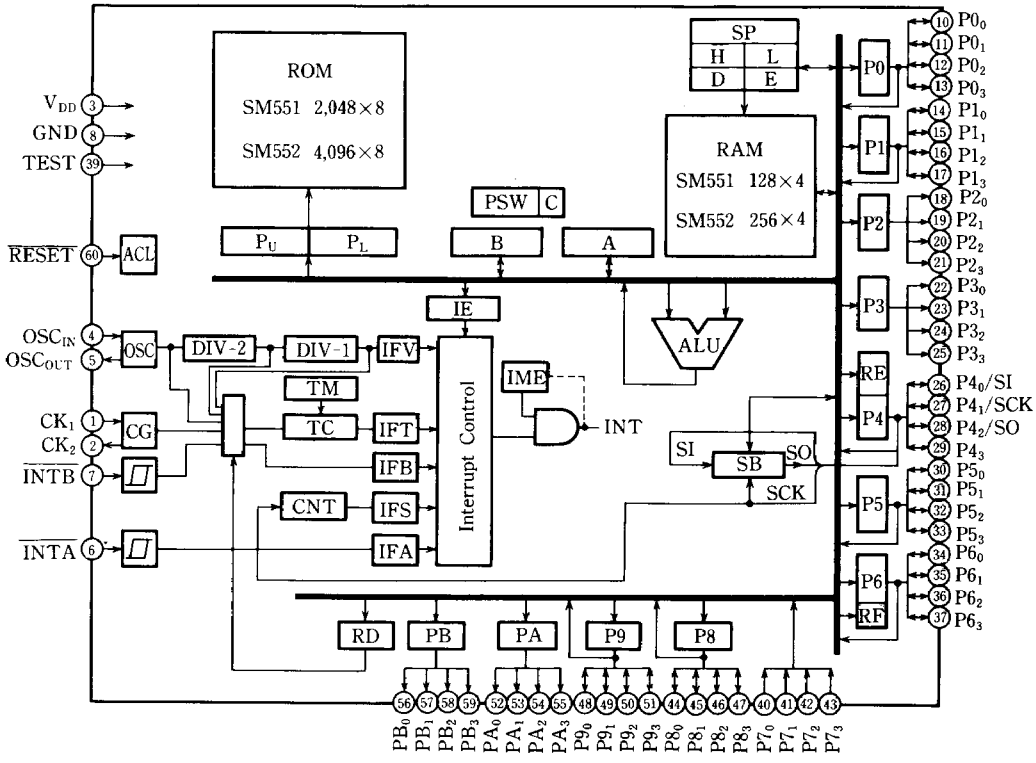
■ Features

1. CMOS process
2. ROM capacity
   SM550: 1,024×8 bits
   SM551: 2,048×8 bits
   SM552: 4,096×8 bits
3. RAM capacity
   SM550: 80×4 bits
   SM551: 128×4 bits
   SM552: 256×4 bits
4. Instruction set: 94
5. Subroutine stack: using RAM area
6. Instruction cycle:
   1.74 μs (MIN.) (V_{DD}=5V)
   5.3 μs (MIN.) (V_{DD}=3V)
7. Interrupts
   External interrupts: 2
   Internal interrupts: 3
8. Input/output ports
   SM550: I/O ports 24
   Input ports 4
   Output ports 8
   SM551/SM552: I/O ports 28
   Input ports 4
   Output ports 16
9. 8-bit serial I/O
10. Timer/counter: 1 set
11. On-chip crystal oscillator circuit and clock divider circuit
12. On-chip system clock oscillator
13. Standby function
14. Expandable external data ROM/RAM
15. Supply voltage: 2.7 to 5.5V
16. SM550: 48-pin QFP (QFP48-P-1010)
    SM551/SM552: 60-pin QFP
    (QFP60-P-1414)
    64-pin SDIP
    (SDIP64-P-750)

■ Block Diagram



SM551/SM552



Symbol description

A,B	: Accumulators	PU,PX	: Program counters
ACL	: Auto clear circuit	P0-PB	: Registers
ALU	: Arithmetic logic unit	PSW	: Program status word register
CG	: Clock generator	RD, RE, RF	: Mode registers
DIV	: Divider	SB	: Shift registers
H, L, D, E	: General-purpose registers	SP	: Stack pointer
IE	: Interrupt enable F/F	TC	: Count registers
IFT, IFA, IFS, IFB, IVV	: Interrupt requests	TM	: Module registers
IME	: Interrupt mask enable F/F		

Note: Pin numbers apply to a 60-pin QFP.

■ Pin Description

Symbol	I/O	Circuit type	Function	Note
$P0_0$-$P0_3$, $P1_0$-$P1_3$, $P4_0$-$P4_3$, $P5_0$-$P5_3$, $P6_0$-$P6_3$, $P8_0$-$P8_3$	I/O	Pull-up (I)	Input/output ports	
$P9_0$-$P9_3$	I/O	Pull-up (I)	Input/output ports	1
$P2_0$-$P2_3$, $P3_0$-$P3_3$	O		Output ports	
PA_0-PA_3, PB_0-PB_3	O		Output ports	1
$P7_0$-$P7_3$	I	Pull-up	Input ports	
$\overline{INTA}$, $\overline{INTB}$	I	Pull-up	Interrupt input ports	
CK_1, CK_2			System clock CR oscillator	
OSC_{IN}, OSC_{OUT}			Crystal oscillator	
ϕ	O		Synchronous clock output	
V_{DD}, GND			Power supply	
TEST	I	Pull-down	Test input (normally connected to GND)	
$\overline{RESET}$	I	Pull-up	Reset input	

Note 1: Applied to the SM551/SM552.

■ Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit	Note
Supply voltage	V_{DD}	−0.3 to +7.5	V	1
Input voltage	V_{IN}	−0.3 to V_{DD}+0.3	V	1
Output voltage	V_{OUT}	−0.3 to V_{DD}+0.3	V	1
Output current	I_{OUT}	40	mA	2
Operating temperature	Topr	−20 to +70	℃	
Storage temperature	Tstg	−55 to +150	℃	

Note 1: The maximum applicable voltage on any pin with respect to GND.
Note 2: Sum of current output from (or flowing into) output pin.

■ Recommended Operating Conditions

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit	Note
Supply voltage	V_{DD}		2.7		5.5	V	
Crystal oscillator frequency	f_{OSC}			32.768		kHz	1
Basic clock oscillator frequency	f	V_{DD}=5V	0.25		2.3	MHz	2
		V_{DD}=3V	0.25		0.75		

Note 1: Oscillation starting time: within 10 seconds
Note 2: Degree of fluctuation frequency: ±30%
(Tolerance of voltage fluctuation: ±10%)

■ Electrical Characteristics

(V_{DD}=2.7 to 5.5V, Ta=−20 to +70℃)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit	Note
Input voltage	V_{IH1}		$0.7V_{DD}$		V_{DD}	V	1
	V_{IL1}		0		$0.3V_{DD}$	V	
	V_{IH2}		$V_{DD}-0.5$		V_{DD}	V	2, 9
	V_{IL2}		0		0.5	V	
Input current	I_{IN}	V_{IH}=0V	2		200	μA	1, 9
		V_{DD}=5.0V±10%	20		200		
Output current	I_{OH1}	$V_{OH}=V_{DD}-0.5V$	50			μA	3
	I_{OL1}	V_{OL}=0.5V	250			μA	
	I_{OH2}	$V_{OH}=V_{DD}-0.5V$	100			μA	4
	I_{OL2}	V_{OL}=0.5V	500			μA	
	I_{OH3}	$V_{OH}=V_{DD}-0.5V$	100			μA	5
		V_{DD}=5.0V±10%	400				
	I_{OL3}	V_{OL}=0.5V	0.5			mA	
		V_{DD}=5.0V±10%	1.6				
Current consumption	I_{OP}	f=0.5MHz, V_{DD}=3.0V±10%		0.3	1.2	mA	6
		f=1MHz, V_{DD}=5.0V±10%		1	4		
	I_{ST}			1	5	μA	7
		Standby current V_{DD}=3.0V±10%		12	40		8
		V_{DD}=5.0V±10%		50	200		

Note 1: Applied to pins $P0_0$-$P0_3$, $P1_0$-$P1_3$, $P4_0$-$P4_3$, $P5_0$-$P5_3$, $P6_0$-$P6_3$, $P8_0$-$P8_3$ (during input mode), $P7_0$-$P7_3$, $\overline{RESET}$.
Note 2: Applied to pins CK_1, OSC_{IN}, TEST.
Note 3: Applied to pin CK_2.
Note 4: Applied to pin ϕ.
Note 5: Applied to pins $P0_0$-$P0_3$, $P1_0$-$P1_3$, $P4_0$-$P4_3$, $P5_0$-$P5_3$, $P6_0$-$P6_3$, $P8_0$-$P8_3$ (during output mode), $P2_0$-$P2_3$, $P3_0$-$P3_3$.
Note 6: No-load condition.
Note 7: No-load condition when crystal oscillation circuit is not operating. Connect OSC_{IN} pin to GND.
Note 8: No-load condition when crystal oscillation circuit is operating.
Note 9: Applied to pins $\overline{INTA}$, $\overline{INTB}$.

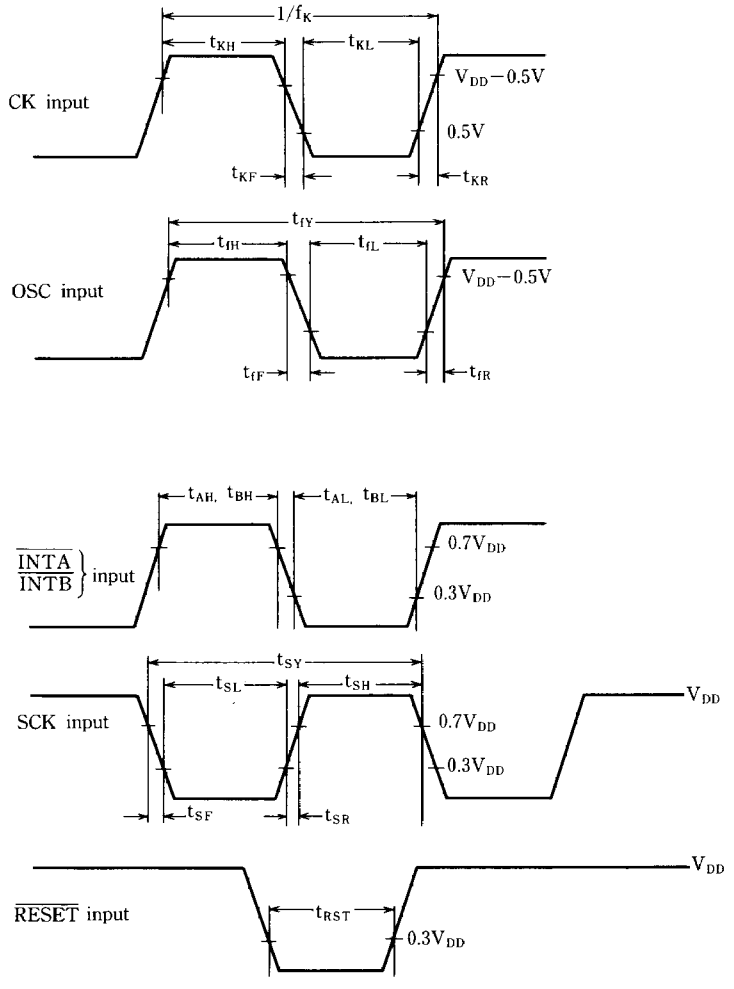
■ AC Characteristics

(V_{DD}=2.7 to 5.5V, Ta=−20 to +70℃)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit	Note
Reference clock oscillator frequency (CR oscillator)	f_{CR}	V_{DD}=5V±10%	1.7	2.0	2.3	MHz	1
		V_{DD}=3V±10%	0.5	0.75	1.0	MHz	2
		R=50kΩ±5%	0.5	0.75	1.0	MHz	
Reference clock input frequency (CK_1)	f_K	V_{DD}=5.0V±10%	0.25		2.3	MHz	
			0.25		1.0		
CK_1 input rise time	t_{KR}				100	ns	
CK_1 input fall time	t_{KF}				100	ns	
CK_1 input HIGH width	t_{KH}	V_{DD}=5.0V±10%	0.1			μs	
			0.4				
CK_1 input LOW width	t_{KL}	V_{DD}=5.0V±10%	0.1			μs	
			0.4				
Crystal oscillator frequency	f_{OSC}			32.768		kHz	
OSC_{OUT} input cycle time	t_{fY}		2			t_{CYC}	3
OSC_{OUT} iuput rise time	t_{fR}				500	ns	
OSC_{OUT} input fall time	t_{fF}				500	ns	
OSC_{OUT} input HIGH width	t_{fH}		1			t_{CYC}	3
OSC_{OUT} input LOW width	t_{fL}		1			t_{CYC}	3
$\overline{INTA}$ HIGH width	t_{AH}		2			t_{CYC}	3
$\overline{INTA}$ LOW width	t_{AL}		2			t_{CYC}	3
$\overline{INTB}$ HIGH width	t_{BH}		2			t_{CYC}	3
$\overline{INTB}$ LOW width	t_{BL}		2			t_{CYC}	3
SCK cycle time	t_{SY}		1			t_{CYC}	3
SCK HIGH width	t_{SH}		1/2			t_{CYC}	3
SCK LOW width	t_{SL}		1/2			t_{CYC}	3
SCK rise time	t_{SR}				500	ns	
SCK fall time	t_{SF}				500	ns	
$\overline{RESET}$ pulse LOW width	t_{RST}		300			ns	

Note 1: SM550: R=17kΩ±5%, SM551/SM552: R=10kΩ±5%
Note 2: SM550: R=50kΩ±5%, SM551/SM552: lR=33kΩ±5%
Note 3: Cycle time at one fouth of a reference clock frequency.

■ Timing Diagram



■ Hardware Configuration

(1) Program memory (ROM)

The on-chip ROM of the SM550/SM551/SM552 has a configuration of 16/32/64 pages×64 steps×8 bits respectively, and stores programs and table data.

The program counter of the SM550/SM551/SM552 consists of a 4-bit/5-bit/6-bit page address counter P_U and a 6-bit binary counter P_L used to specify the steps within a page.

Fig. 1 shows the locations allocated in the on-chip ROM.

(2) Data memory (RAM)

Data memory of the SM550/SM551/SM552 has 80-word/128-word/160-word×4 bit configuration respectively.

Fig. 2 shows the RAM configuration.

(3) General-purpose registers (H, L, D, E)

Registers H and L are 4-bit general-purpose registers. They can transfer and compare data with the A_{CC} on 4-bit basis.

Registers D and E are 4-bit registers and can transfer data with the H and L registers on an 8-bit basis.

The H and L as well as the D and E registers can be combined into 8-bit register pairs, and can be used as pointers to data memory locations.

The L register can be incremented or decremented and is used to access I/O ports and mode registers.

(4) Clock divider (DIV)

The device contains a crystal oscillator and a 15-stage divider. A real-time clock can be provided by connecting an external crystal oscillator between the oscillator pins.

The on-chip divider is reset by an ACL operation or an IDIV instruction. The low-order 8 bits of the divider can be loaded into the B/A register pair by the LDDIV instruction.

When an external 32.768kHz crystal oscillator is used, the final state signal is set at a frequency of 1Hz.

(5) Timer/event counter (TC)

The timer/event counter consists of an 8-bit count register (TC) and an 8-bit modulo register (TM).

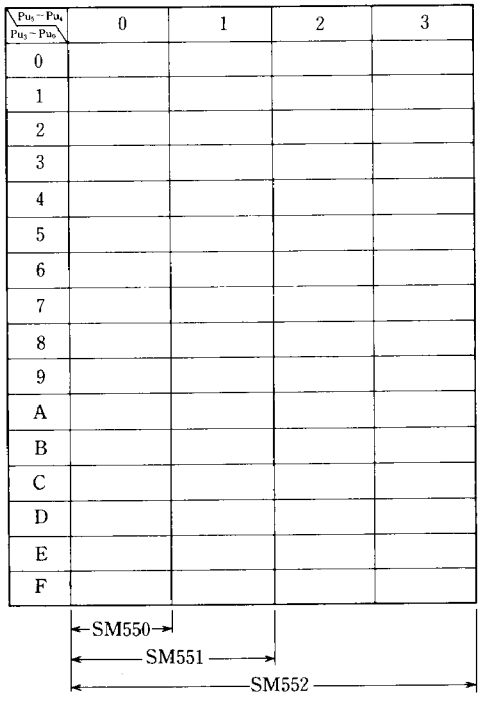


Fig. 1 ROM configuration

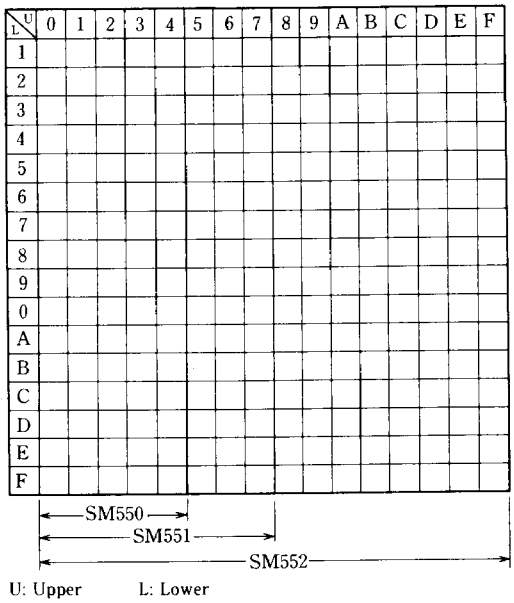


Fig. 2 RAM configuration

Table 1 Interrupt request

Interrupt request		Int./Ext.	Priority	Interrupt routine start address
INTT	Timer/event counter interrupt	Int.	1	Page 1, Address 0
INTA	External signal INTA interrupt	Ext.	2	Address 2
INTS	Serial I/O interrupt	Int.	3	Address 4
INTB	External signal INTB and frame frequency interrupts	Ext.	4	Address 6
INTV	Divider overflow interrupt	Int.	5	Address 8

The count register is an 8-bit incremental binary counter. It is incremented by one at the falling edge of its count pulse (CP) input. If the count register overflows, the timer interrupt request flag IFT is set, and the contents of the modulo register (TM) are loaded into the count register. The contents of the count register can be loaded into the B/A register pair by the LDTC instruction.

(6) Serial Interface (SIO)

The serial interface consists of an 8-bit shift register (SB) and a 3-bit counter, which is used to input and output the serial data.

In serial shift operations, the highest bit data of the shift register (SB) is output from the SO pin at the falling edge of the serial clock, and the data input from the SI pin is loaded into the lowest bit of the shift register.

When the internal clock is used, the serial operation stops with 8 clocks of serial shift operations which are output from the SCK pin.

(7) Interrupts

The interrupts can be selected within three kinds of internal interrupts and two kinds of external interrupts as shown in Table 1.

(8) I/O ports and mode registers (RD, RE, RF)

The device has I/O ports and three mode registers (RED, RE, RF). Data can be transferred between these ports and registers under instruction control or L register control.

- Ports P0, P1, P4, P5, P8 and P9* can be switched between input and output modes, 4 bits at a time.
- Ports P2, P3, PA* and PB* are 4-bit parallel output ports.
- Port P7 is a 4-bit parallel input port.
- Each bit of port P2 can be independently placed in input or output mode by setting the corresponding bit of mode register RF.
- Ports (P0, P1), (P2, P3), (P8, P9)*, and (PA, PB)* can be paired for use in data transfer on a byte-by-byte basis. However, port pairs (P2, P3) and (PA, PB)* are usable only for output.
- The mode registers RD, RE and RF are treated in much the same way as output ports.
- Each bit of port P2 can be set to the I/O modes (SI, SO and SCK) of a serial interface under program control.
- Pins P50 and P51 can output the OD and R/W signals respectively when an external memory is accessed. In those cases, these pins should be kept High in output mode.

* Applicable to the SM551 and SM552.

Every input port has pull-up resistors.

Pull-up resistors can be omitted and output ports can be designed to consist of open-drain transistors with a mask option.

(9) Standby mode

Executing the CEND instruction places the device in standby mode. To reduce power consumption, the system clock is inactivated.

Standby mode may be cleared with the Interrupt request or the RESET signal.

(10) Reset function (ACL)

Applying a Low level signal to the RESET pin resets the internal logic of the device, and starts execution of the program at address 0, page 0.

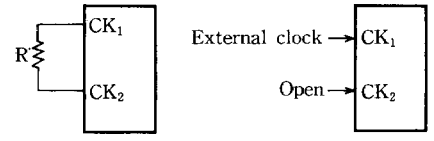
Once the device is reset, all I/O ports are placed in input mode to disable all interrupts. The mode registers RD, RE and RF are all cleared. The output ports P2, P3, PA* and PB* are all cleared to output "0". The device is also reset when it is powered up. The program starts (master clock period $\times 2^{14}$) clock periods after the reset signal is ineffected.

* Applicable to the SM551 and SM552.

(11) Master clock oscillator circuit

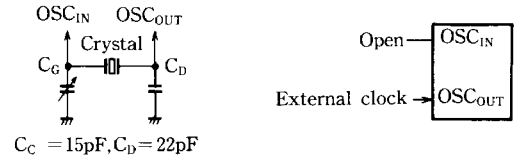
The master clock oscillator requires an external resistor across pins CK_1 and CK_2. Instead of using on-chip oscillator, an external clock may be applied to pin CK_1. In this case, pin CK_2 should be left open.

The system clock ϕ has a frequency of one fourth that of the clock applied to pin CK_1. When applying an external clock to pin OSC_{OUT}, the external clock frequency should be set at one eighth of the master clock frequency.



(a) CR oscillator (b) External clock

Fig. 3



(a) Crystal oscillator (b) External clock

Fig. 4

■ Instruction Set

(1) RAM address instructions

Mnemonic	Machine code	Operation
STL	69	L←A
STH	68	H←A
EXHD	3F	H↔D L↔E
LIHL xy (2-byte)	3D 00-FF	H←x(I_7-I_4), L←y(I_3-I_0)

(2) ROM address instructions

Mnemonic	Machine code	Operation
TR x	80-BF	P_L←x(I_5-I_0)
TL xy (2-byte)	E0-EF 00-FF	P_U←x(I_9-I_6) P_L←y(I_5-I_0)
TRS x	C0-DF	(SP-1), (SP-2), (SP-3)←PC SP←SP-4 P_U←0(SM550), P_U←10_H(SM551/SM552) P_L←x($I_4I_3I_2I_1I_00$)
CALL xy (2-byte)	F0-FF 00-FF	(SP-1), (SP-2), (SP-3)←PC SP←SP-4, P_U←x(I_9-I_6) P_L←x($I_5I_4I_3I_2I_1I_0$)
JBA x (2-byte)	7F 30-3F	P_{U5}-P_{U2}←x(I_3-I_0) P_{U1}, P_{U0}, P_{L5}, P_{L4}←B, P_{L3}-P_{L0}←A
RTN	61	P_U, P_L←(SP+1), (SP+2), (SP+3), SP←SP+4
RTNS	62	P_U, P_L←(SP+1), (SP+2), (SP+3), SP←SP+4
RTNI	63	P_U, P_L←(SP+1), (SP+2) (SP+3), PSW←(SP), SP←SP+4, IME←1

(3) Data transfer instructions

Mnemonic	Machine code	Operation
EX pr	5C-5F	A↔(pr)
LDX adr (2-byte)	7D 00-FF	A←(adr)
STX adr (2-byte)	7E 00-FF	(adr)←A
EXX adr (2-byte)	7C 00-FF	A↔(adr)
LAX x	10-1F	A←x(I_3-I_0)
LIBA xy (2-byte)	3C 00-FF	B←x(I_7-I_4) A←y(I_3-I_0)
LBAT	60	B←ROM(P_{U5}-P_{U2}, B, A)$_H$ A←ROM(P_{U5}-P_{U2}, B, A)$_L$
LDL	65	A←L
LD pr	54-57	A←(pr)
ST pr	58-5B	(pr)←A
EXH	6C	A↔H
EXL	6D	A↔L
EXB	6E	A↔B
STB	6A	B←A
LDB	66	A←B
LDH	64	A←H
PSHBA	28	(SP-1)←B, (SP←2)←A, SP←SP-2
PSHHL	29	(SP-1)←B, (SP←2)←A, SP←SP-2
POPBA	38	B←(SP+1), A←(SP), SP←SP+2
POPHL	39	H←(SP+1), L←(SP), SP←SP+2
STSB	70	SB_H←B, SB_L←A
STSP	71	SP_H←B, SP_L←A
STTC	72	TC←TM
STTM	73	TM_H←B, TM_L←A
LDSB	74	B←SB_H, A←SB_L
LDSP	75	B←SP_H, A←SP_L
LDTC	76	B←TC_H, A←TC_L
LDDIV	77	B←DIV_H, A←DIV_L

(4) Arithmetic instructions

Mnemonic	Machine code	Operation
ADX x	00-0F	A←A+x(I_3-I_0), Skip if Cy=1
ADD	36	A←A+(HL)
ADDC	37	A←A+(HL)+C, C←Cy Skip if Cy=1
OR	31	A←A+(HL)
AND	32	A←A・(HL)
EOR	33	A←A⊕(HL)
ANDB	22	A←A・B
ORB	21	A←A+B
EORB	23	A←A⊕B
COMA	6F	A←$\overline{A}$
ROTR	25	C→A_3→A_2→A_1→A_0→C
ROTL	35	C←A_3←A_2←A_1←A_0←C
INCB	52	Skip if B=F, B←B+1
DECB	53	Skip if B=0, B←B−1
INCL	50	Skip if L=F, L←L+1
DECL	51	Skip if L=0, L←L−1
DECM adr	79 00-FF	Skip if (adr)=0, (adr)←(adr)−1
INCM adr	78 00-FF	Skip if (adr)=F, (adr)←(adr)+1

(5) Test instructions

Mnemonic	Machine code	Operation
TAM	30	Skip if A=(HL)
TAH	24	Skip if A=H
TAL	34	Skip if A=L
TAB	20	Skip if A=B
TC	2A	Skip if C=0
TM x	48-4B	Skip if (HL)x=1
TA x	4C-4F	Skip if Ax=1
TSTT	2B	Skip if IFT=1, IFT←0
TSTA	2C	Skip if IFA=1, IFA←0
TSTS	2D	Skip if IFS=1, IFS←0
TSTB	2E	Skip if IFB=1, IFB←0
TSTV	2F	Skip if IFV=1, IFV←0

(6) Bit manipulation instructions

Mnemonic	Machine code	Operation
SM x	40-43	(HL)x←1
RM x	44-47	(HL)x←0
RC	26	C←0
SC	27	C←1
RIME	3A	IME←0
SIME	3B	IME←1
DI x (2-byte)	7F C0-DF	IEF←IEF・x
EI x (2 byte)	7F E0-FF	IEF←IEF+x

(7) I/O instructions

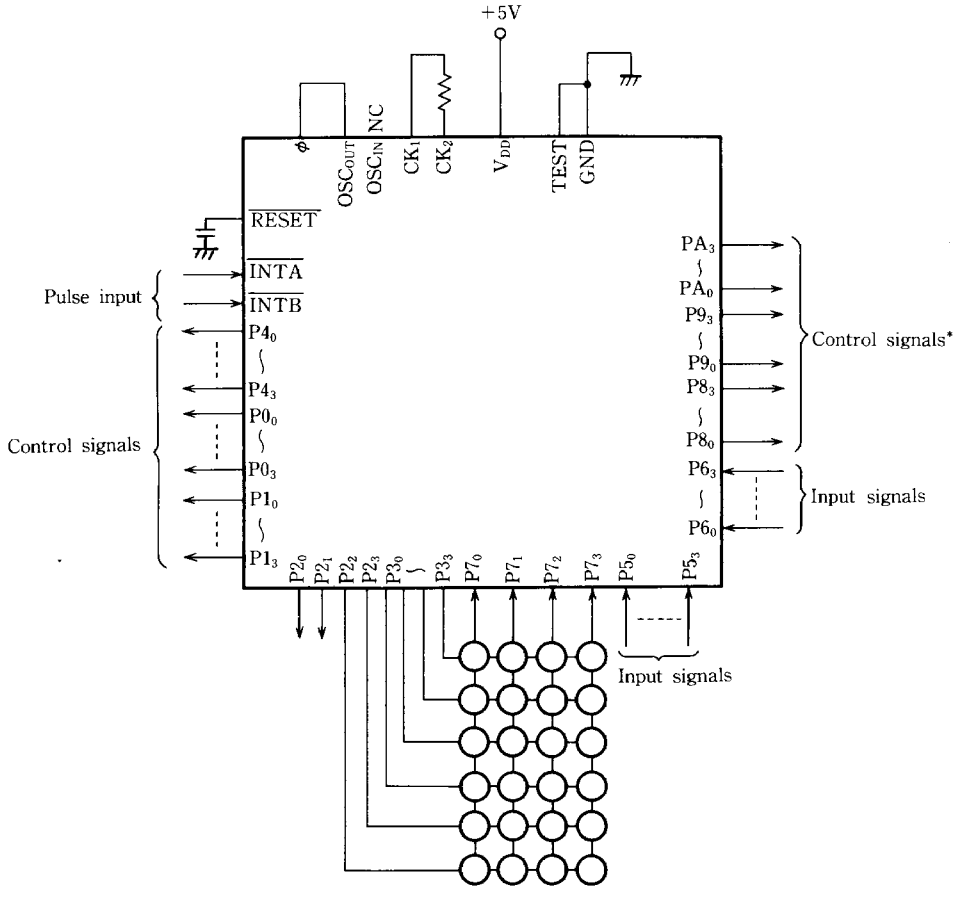
Mnemonic	Machine code	Operation
IN	67	A←P(L)
OUT	6B	P(L), R(L)←A
INA x (2-byte)	7F A0-A9	A←P(x)
OUTA x (2-byte)	7F B0-BF	P(x), R(x)←A
INBA x	7F 80; 82	B←P(x+1) A←P(x)
OUTBA x (2-byte)	7F 90-93	P(x+1)←B P(x)←A
SP xy (2-byte)	7A 00-F6	P(y)←P(y)+x
RP xy (2-byte)	7B 00-F6	P(y)←P(y) x
READ (2-byte)	7F 60	A←P0 with O/D
WRIT (2-byte)	7F 70	P0←A with R/W
READB (2-byte)	7F 61	B←P1 A←P0 with O/D
WRITB (2-byte)	7F 71	P1←B P0←A with R/W

(8) Special instructions

Mnemonic	Machine code	Operation
SIO	3E	Sperial I/O start
IDIV (2-byte)	7F 10	DIV←0
SKIP	00	No operation
CEND (2-byte)	7F 00	System clock stop

Note: The machine code consists of 8 bits including I_7, I_6, I_5, I_4, I_3,I_2, I_1 and I_0.

System Configuration Example (Mechanism controller)



*Ports $P8_0$-$P8_3$ $P9_0$-$P9_3$, PA_0-PA_3 apply to the SM551 and SM552.