NEC

MOS INTEGRATED CIRCUIT

μPD30700,30700L,30710

VR10000™, VR12000™
64-BIT MICROPROCESSORS

DESCRIPTION

The μPD30700 and 30700L (VR10000) and μPD30710 (VR12000) are new members of NEC's VR series™ RISC (Reduced Instruction Set Computer) microprocessors. These new high-performance 64-bit microprocessors employ a new RISC architecture developed by MIPS™, ANDES™ architecture.

The VR10000 and VR12000 are designed to be used in high-performance computers and achieve considerably higher processing speed through the employment of a super scalar pipeline.

Remark ANDES: Architecture with Non-sequential Dynamic Execution Scheduling

The functions of these microprocessors are described in detail in the following manuals. Be sure to read these manuals when designing systems.

VR10000, VR12000 User's Manual : U10278E
VR5000™, VR10000 User's Manual - Instruction : U12754E

FEATURES

- MIPS 64-bit RISC architecture
- High-speed operation processing
  Super scalar pipeline executing five instructions in parallel

<VR10000>
  - 14SPECint95, 23SPECfp95

<VR12000>
  - 17SPECint95, 27SPECfp95

- Instruction set upward-compatible with VR4000™, VR4200™, and VR4400™ (conforms to MIPS-I/II/III/IV)
- High-speed translation lookaside buffer (TLB) (64 double entries)
- Address space Physical: 40 bits
  Virtual: 44 bits
- Floating-point unit (FPU)
- Primary cache memory (32K bytes for each of instruction and data, 2-way set associative)
- Secondary cache memory interface
  - 128-bit secondary cache interface
  - SSRAM interface (VR10000: 250 MHz MAX., VR12000: 200 MHz MAX.)
  - Supports up to 16M bytes
- Operating frequency

<VR10000>
  - Internal: 250 MHz MAX.
  - External: 250 MHz MAX.
  - External/internal multiplication factor selectable from 1 to 4

<VR12000>
  - Internal: 300 MHz MAX.
  - External: 150 MHz MAX.
  - External/internal multiplication factor selectable from 2 to 10

- Multi-processor function
  - Up to four buses of cluster connection can be connected.
- Supply voltage

<VR10000>
  V_{DD} = 3.3 V ±0.165 V (μPD30700)
  V_{DD} = 2.6 V ±0.1 V (μPD30700L)

<VR12000>
  V_{DD} = 2.6 V ±0.1 V (μPD30710)

Unless otherwise specified, the VR10000 is treated as the representative model throughout this document.

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Date Published June 1998 N CP(K)
Printed in Japan

APPLICATIONS

- UNIX™ servers
- Windows NT™ servers
- Desktop workstations, etc.

ORDERING INFORMATION

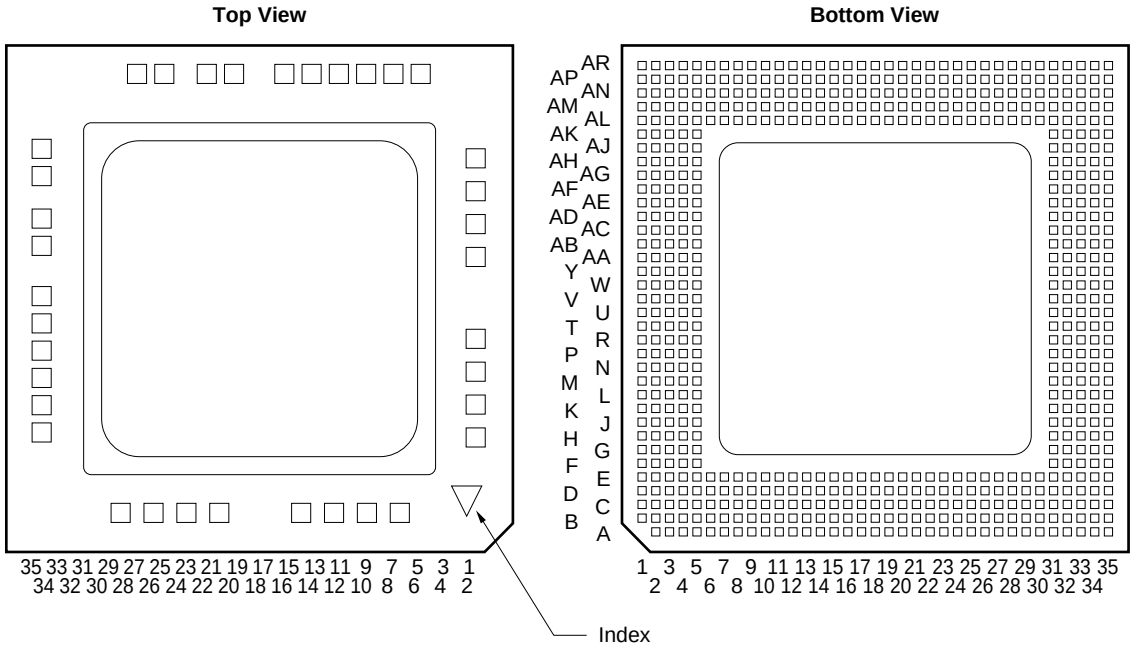
Part Number	Package	Maximum Internal Operating Frequency
μPD30700RS-180	599-pin ceramic LGA	180
μPD30700RS-200	599-pin ceramic LGA	200
μPD30700LRS-225Note	599-pin ceramic LGA	225
μPD30700LRS-250Note	599-pin ceramic LGA	250
μPD30710RS-300Note	599-pin ceramic LGA	300

Note Under development

Remark LGA: Land Grid Array

PIN CONFIGURATION

- **599-pin ceramic LGA**
  μPD30700RS-180
  μPD30700RS-200
  μPD30700LRS-225
  μPD30700LRS-250
  μPD30710RS-300



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No.	Name	No.	Name	No.	Name	No.	Name
A1	–	B9	$\overline{\text{SCADCS}}$	C17	SysAD41	D25	V_{SS}
A2	V_{DD}	B10	SCAAddr5	C18	V_{DD}	D26	V_{DD}
A3	V_{SS}	B11	V_{SS}	C19	SysAD36	D27	SCData68
A4	V_{DD}QSC	B12	SCData78	C20	SysAD32	D28	SCData64
A5	SCData89	B13	SCClk0	C21	V_{SS}	D29	V_{SS}
A6	SCData85	B14	V_{DD}	C22	V_{SS}	D30	SCAAddr12
A7	V_{SS}	B15	SCData72	C23	$\overline{\text{SysClkRet}}$	D31	SCAAddr16
A8	$\overline{\text{SCADWr}}$	B16	SysAD44	C24	V_{SS}	D32	V_{SS}
A9	SCAAddr8	B17	V_{SS}	C25	V_{DD}Pa	D33	SCDataChk0
A10	V_{DD}QSC	B18	SysAD40	C26	SCData71	D34	SCData29
A11	SCAAddr1	B19	V_{SS}	C27	V_{SS}	D35	V_{DD}QSC
A12	SCData76	B20	SysAD33	C28	SCData67	E1	SCClk5
A13	V_{SS}	B21	V_{SS}	C29	SCDataChk2	E2	V_{SS}
A14	SCData74	B22	DCOK	C30	V_{DD}QSC	E3	V_{DD}
A15	SysAD46	B23	SysClkRet	C31	SCAAddr13	E4	SCDataChk6
A16	V_{DD}QSys	B24	V_{SS}Pa	C32	SCAAddr18	E5	V_{DD}
A17	SysAD42	B25	V_{SS}Pa	C33	V_{DD}QSC	E6	SCData90
A18	SysAD37	B26	$\overline{\text{SCClk1}}$	C34	V_{DD}	E7	SCData86
A19	SysAD35	B27	SCDataChk9	C35	V_{SS}	E8	V_{DD}QSC
A20	V_{DD}QSys	B28	V_{DD}	D1	V_{DD}QSC	E9	SCData80
A21	V_{SS}	B29	SCData65	D2	$\overline{\text{SCTCS}}$	E10	SCADWay
A22	SysClk	B30	SCAAddr9	D3	SCDataChk8	E11	V_{SS}
A23	$\overline{\text{SysClk}}$	B31	V_{SS}	D4	V_{SS}	E12	SCAAddr4
A24	V_{SS}Pa	B32	SCAAddr15	D5	SCData92	E13	SCAAddr0
A25	NC	B33	SCAAddr17	D6	SCData88	E14	V_{DD}QSC
A26	SCClk1	B34	V_{SS}	D7	V_{SS}	E15	$\overline{\text{SCClk0}}$
A27	V_{SS}	B35	V_{DD}	D8	SCData82	E16	SysAD47
A28	SCData70	C1	V_{SS}	D9	$\overline{\text{SCADOE}}$	E17	V_{SS}
A29	V_{SS}	C2	V_{DD}	D10	V_{DD}	E18	SysAD39
A30	SCDataChk4	C3	V_{DD}QSC	D11	SCAAddr6	E19	V_{SS}
A31	SCAAddr11	C4	SCData94	D12	SCAAddr2	E20	$\overline{\text{SysCyc}}$
A32	V_{DD}QSC	C5	SCData91	D13	V_{SS}	E21	V_{SS}
A33	V_{SS}	C6	V_{DD}QSC	D14	SCData77	E22	V_{DD}Pd
A34	V_{DD}	C7	SCData84	D15	SCData73	E23	V_{SS}
A35	V_{SS}	C8	SCData81	D16	V_{DD}	E24	V_{SS}
B1	V_{DD}	C9	V_{SS}	D17	SysAD43	E25	V_{SS}
B2	V_{SS}	C10	SCAAddr7	D18	SysAD38	E26	SCData69
B3	SCData95	C11	SCAAddr3	D19	SysAD34	E27	SCData66
B4	SCData93	C12	V_{DD}QSC	D20	V_{DD}	E28	V_{DD}QSC
B5	V_{SS}	C13	SCData79	D21	V_{SS}	E29	SCAAddr10
B6	SCData87	C14	SCData75	D22	V_{SS}Pd	E30	SCAAddr14
B7	SCData83	C15	V_{SS}	D23	V_{SS}	E31	V_{DD}
B8	V_{DD}	C16	SysAD45	D24	V_{SS}	E32	SCData31

Note Connect this pin via a100-Ω resistor.

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No.	Name	No.	Name	No.	Name	No.	Name
E33	V_{DD}	K1	V_{DD}QSC	P4	SCTag6	V32	SysAD6
E34	V_{SS}	K2	SCTag14	P5	V_{DD}QSC	V33	V_{DD}
E35	SCData27	K3	SCTag17	P31	V_{DD}QSC	V34	SysAD4
F1	V_{DD}	K4	V_{DD}	P32	SCData4	V35	SysAD2
F2	$\overline{\text{SCTWr}}$	K5	SCTag19	P33	SCData2	W1	SCClk4
F3	V_{DD}QSC	K31	SCData18	P34	V_{DD}	W2	V_{SS}
F4	$\overline{\text{SCClk5}}$	K32	V_{DD}	P35	SysAD15	W3	SCTagChk1
F5	V_{SS}Note	K33	SCData16	R1	SCTag0	W4	$\overline{\text{SCClk4}}$
F31	SCData30	K34	SCData11	R2	V_{DD}QSC	W5	V_{SS}
F32	SCData28	K35	V_{DD}QSC	R3	V_{SS}	W31	V_{SS}
F33	V_{DD}QSC	L1	SCTag12	R4	SCTag1	W32	SysAD1
F34	SCData25	L2	V_{SS}	R5	SCTag3	W33	JTCK
F35	SCData23	L3	V_{DD}	R31	SCData0	W34	V_{SS}
G1	V_{SS}	L4	SCTag15	R32	SysAD13	W35	JTDI
G2	SCTag22	L5	V_{SS}	R33	V_{SS}	Y1	V_{CC}QSys
G3	SCTag24	L31	V_{SS}	R34	SysAD14	Y2	SysCmd0
G4	V_{SS}	L32	SCData14	R35	SysAD12	Y3	SysCmd1
G5	$\overline{\text{SCTOE}}$	L33	SCData9	T1	V_{DD}QSC	Y4	V_{DD}
G31	SCData26	L34	V_{SS}	T2	NC	Y5	SysCmd3
G32	V_{SS}	L35	SCData7	T3	SCTWay	Y31	JTDO
G33	SCData21	M1	SCTag7	T4	V_{DD}	Y32	V_{DD}
G34	SCData19	M2	SCTag9	T5	SCTagLSBAddr	Y33	VrefSys
G35	V_{SS}	M3	V_{DD}QSC	T31	SysAD11	Y34	SysAD0
H1	SCTag20	M4	SCTag11	T32	V_{DD}	Y35	V_{DD}QSys
H2	V_{DD}	M5	SCTag13	T33	SysAD9	AA1	SysCmd2
H3	V_{DD}QSC	M31	SCData12	T34	SysAD10	AA2	SysCmd4
H4	SCTag25	M32	SCData10	T35	V_{DD}QSys	AA3	V_{SS}
H5	V_{DD}QSC	M33	V_{DD}QSC	U1	SCTagChk6	AA4	SysCmd5
H31	V_{DD}QSC	M34	SCData5	U2	V_{SS}	AA5	SysCmd7
H32	SCData24	M35	SCData3	U3	SCTagChk5	AA31	SCClk2
H33	V_{DD}QSC	N1	V_{SS}	U4	V_{SS}Note	AA32	SCData32
H34	V_{DD}	N2	SCTag5	U5	V_{SS}	AA33	V_{SS}
H35	SCData17	N3	SCTag8	U31	V_{SS}	AA34	JTMS
J1	SCTag16	N4	V_{SS}	U32	SysAD7	AA35	VrefSC
J2	SCTag18	N5	SCTag10	U33	SysAD5	AB1	SysCmd6
J3	V_{SS}	N31	SCData8	U34	V_{SS}	AB2	V_{DD}
J4	SCTag21	N32	V_{SS}	U35	SysAD8	AB3	SysCmd8
J5	SCTag23	N33	SCData6	V1	SCTagChk4	AB4	SysCmd10
J31	SCData22	N34	SCData1	V2	SCTagChk2	AB5	V_{DD}QSys
J32	SCData20	N35	V_{SS}	V3	V_{DD}	AB31	V_{DD}QSC
J33	V_{SS}	P1	SCTag2	V4	SCTagChk0	AB32	SCData35
J34	SCData15	P2	V_{DD}	V5	SCTagChk3	AB33	$\overline{\text{SCClk2}}$
J35	SCData13	P3	SCTag4	V31	SysAD3	AB34	V_{DD}

Note Connect this pin via a100-Ω resistor.

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No.	Name	No.	Name	No.	Name	No.	Name
AB35	SCData33	AG3	V_{SS}	AL6	SCData124	AM14	SCData110
AC1	V_{SS}	AG4	$\overline{\text{SysGblPerf}}$	AL7	SCData120	AM15	SCClk3
AC2	SysCmd9	AG5	$\overline{\text{SysWrRdy}}$	AL8	V_{DD}QSC	AM16	V_{DD}
AC3	SysCmdPar	AG31	SCData53	AL9	SCData114	AM17	SysAD58
AC4	V_{SS}	AG32	SCData51	AL10	$\overline{\text{SCBDOE}}$	AM18	SysAD54
AC5	$\overline{\text{SysReq}}$	AG33	V_{SS}	AL11	SCBAddr8	AM19	SysAD52
AC31	SCData39	AG34	SCData48	AL12	SCBAddr4	AM20	V_{DD}
AC32	V_{SS}	AG35	SCData46	AL13	SCBAddr0	AM21	SysADChk4
AC33	SCData37	AH1	SysResp2	AL14	V_{DD}QSC	AM22	SysAD30
AC34	SCData34	AH2	V_{DD}	AL15	SCData106	AM23	V_{SS}
AC35	V_{SS}	AH3	V_{DD}QSys	AL16	SCData104	AM24	SysAD26
AD1	SysCmd11	AH4	SysStatePar	AL17	SysAD60	AM25	SysAD22
AD2	$\overline{\text{SysVal}}$	AH5	V_{DD}QSys	AL18	SysAD56	AM26	V_{DD}
AD3	V_{DD}QSys	AH31	V_{DD}QSC	AL19	SysAD50	AM27	SCData102
AD4	$\overline{\text{SysGnt}}$	AH32	SCData55	AL20	SysADChk6	AM28	SCData98
AD5	$\overline{\text{SysReset}}$	AH33	V_{DD}QSC	AL21	SysADChk2	AM29	V_{SS}
AD31	SCData43	AH34	V_{DD}	AL22	V_{DD}QSys	AM30	SCBAddr11
AD32	SCData41	AH35	SCData50	AL23	SysAD28	AM31	SCBAddr15
AD33	V_{DD}QSC	AJ1	V_{SS}	AL24	SysAD24	AM32	V_{SS}
AD34	SCData38	AJ2	SysResp0	AL25	SysAD20	AM33	SCData63
AD35	SCData36	AJ3	$\overline{\text{SysRdRdy}}$	AL26	SysAD16	AM34	SCData62
AE1	$\overline{\text{SysRel}}$	AJ4	V_{SS}	AL27	SCData100	AM35	V_{DD}QSC
AE2	V_{SS}	AJ5	SysState1	AL28	V_{DD}QSC	AN1	V_{SS}
AE3	V_{DD}	AJ31	SCData57	AL29	SCBAddr9	AN2	V_{DD}
AE4	SysRespPar	AJ32	V_{SS}	AL30	SCBAddr13	AN3	V_{DD}QSC
AE5	V_{SS}	AJ33	SCData54	AL31	V_{DD}	AN4	SCDataChk7
AE31	V_{SS}	AJ34	SCData52	AL32	SCDataChk1	AN5	SCData125
AE32	SCData45	AJ35	V_{SS}	AL33	V_{DD}	AN6	V_{DD}QSC
AE33	SCData42	AK1	SysStateVal	AL34	V_{SS}	AN7	SCData118
AE34	V_{SS}	AK2	SysState2	AL35	SCData60	AN8	SCData115
AE35	SCData40	AK3	V_{DD}QSys	AM1	V_{DD}QSys	AN9	V_{SS}
AF1	V_{DD}QSys	AK4	$\overline{\text{SysCorErr}}$	AM2	$\overline{\text{SysUncErr}}$	AN10	$\overline{\text{SCBDCS}}$
AF2	DCOk	AK5	$\overline{\text{SysNMI}}$	AM3	V_{SS}[Note]	AN11	SCBAddr5
AF3	SysResp3	AK31	SCData61	AM4	V_{SS}	AN12	V_{DD}QSC
AF4	V_{DD}	AK32	SCData59	AM5	SCData126	AN13	SCData109
AF5	SysResp1	AK33	V_{DD}QSC	AM6	SCData122	AN14	SCData108
AF31	SCData49	AK34	SCData58	AM7	V_{SS}	AN15	V_{SS}
AF32	V_{DD}	AK35	SCData56	AM8	SCData116	AN16	SysAD62
AF33	SCData47	AL1	SysState0	AM9	SCData112	AN17	SysAD59
AF34	SCData44	AL2	V_{SS}	AM10	V_{DD}	AN18	V_{DD}
AF35	V_{DD}QSC	AL3	V_{DD}	AM11	SCBAddr6	AN19	SysAD51
AG1	$\overline{\text{SysRespVal}}$	AL4	V_{SS}[Note]	AM12	SCBAddr2	AN20	SysAD48
AG2	SysResp4	AL5	V_{DD}	AM13	V_{SS}	AN21	V_{SS}

Note Connect this pin via a100-Ω resistor.

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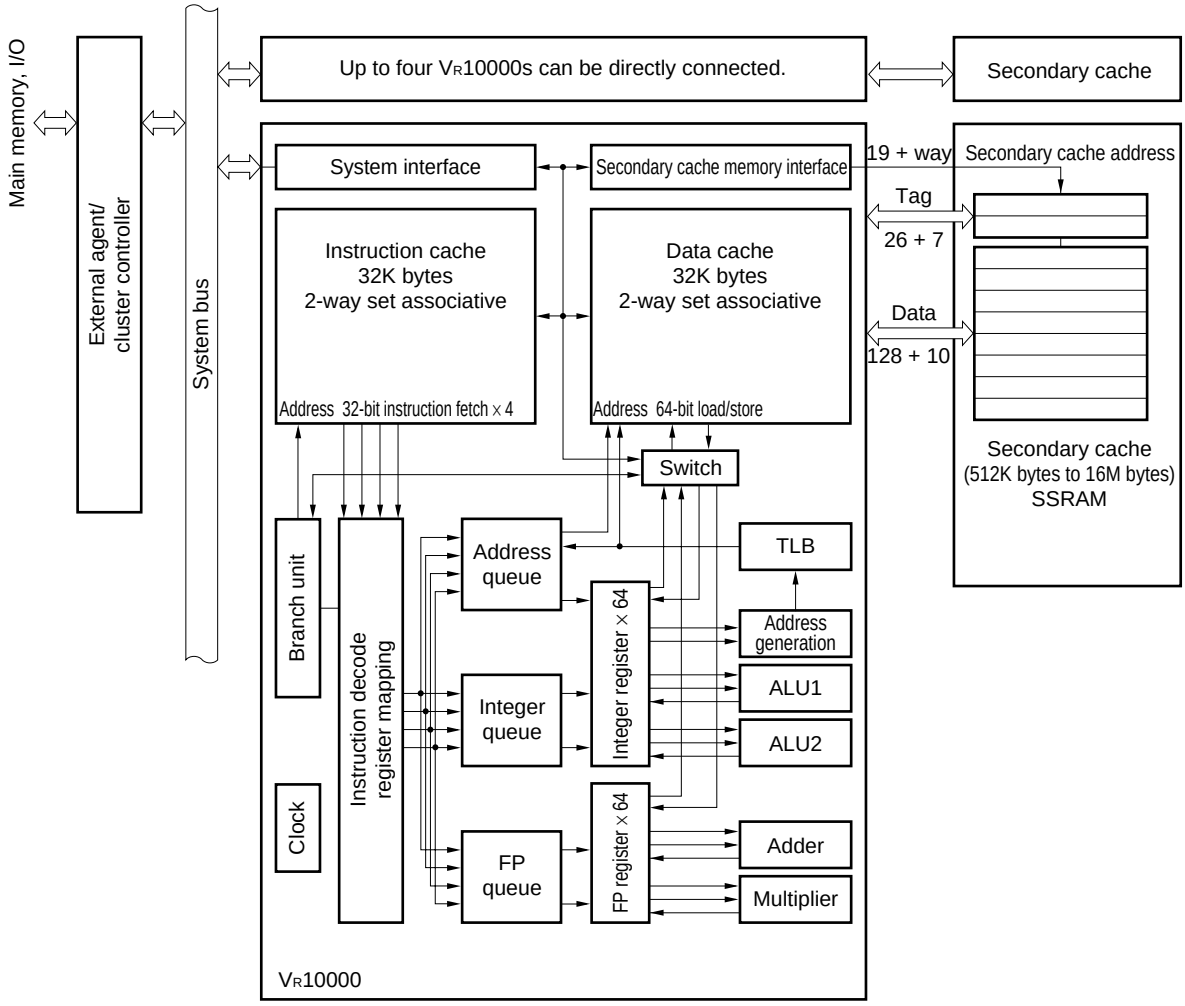
No.	Name	No.	Name	No.	Name	No.	Name
AN22	SysADChk0	AP8	V_{DD}	AP29	SCData97	AR15	SysAD63
AN23	SysAD29	AP9	$\overline{SCBDWr}$	AP30	SCBAddr10	AR16	V_{DD}QSys
AN24	V_{DD}QSys	AP10	SCBAddr7	AP31	V_{SS}	AR17	SysAD57
AN25	SysAD21	AP11	V_{SS}	AP32	SCBAddr16	AR18	SysAD55
AN26	SysAD18	AP12	SCBAddr1	AP33	SCBAddr17	AR19	SysAD49
AN27	V_{SS}	AP13	SCData107	AP34	V_{SS}	AR20	V_{DD}QSys
AN28	SCData99	AP14	V_{DD}	AP35	V_{DD}	AR21	SysADChk5
AN29	SCData96	AP15	SCData105	AR1	V_{SS}	AR22	SysADChk1
AN30	V_{DD}QSC	AP16	SysAD61	AR2	V_{DD}	AR23	V_{SS}
AN31	SCBAddr14	AP17	V_{SS}	AR3	V_{SS}	AR24	SysAD27
AN32	SCBAddr18	AP18	SysAD53	AR4	V_{SS}QSC	AR25	SysAD23
AN33	V_{DD}QSC	AP19	V_{SS}	AR5	SCData123	AR26	V_{DD}QSys
AN34	V_{DD}	AP20	SysADChk7	AR6	SCData119	AR27	SysAD17
AN35	V_{SS}	AP21	SysADChk3	AR7	V_{SS}	AR28	SCData101
AP1	V_{DD}	AP22	V_{DD}	AR8	SCData113	AR29	V_{SS}
AP2	V_{SS}	AP23	SysAD31	AR9	SCBDWay	AR30	SCDataChk3
AP3	SCDataChk5	AP24	SysAD25	AR10	V_{DD}QSC	AR31	SCBAddr12
AP4	SCData127	AP25	V_{SS}	AR11	SCBAddr3	AR32	V_{DD}QSC
AP5	V_{SS}	AP26	SysAD19	AR12	SCData111	AR33	V_{SS}
AP6	SCData121	AP27	SCData103	AR13	V_{SS}	AR34	V_{DD}
AP7	SCData117	AP28	V_{DD}	AR14	$\overline{SCClk3}$	AR35	V_{SS}

PIN NAMES

DCOK	: DC Voltage OK
JTCK	: JTAG Clock
JTDI	: JTAG Serial Data Input
JTDO	: JTAG Serial Data Output
JTMS	: JTAG Mode Select
SCAAddr (18 : 0), SCBAddr (18 : 0)	: Secondary Cache Address Bus
$\overline{\text{SCADCS}}$, $\overline{\text{SCBDCS}}$	: Secondary Cache Data Chip Select
$\overline{\text{SCADOE}}$, $\overline{\text{SCBDOE}}$	: Secondary Cache Data Output Enable
SCADWay, SCBDWay	: Secondary Cache Data Way
$\overline{\text{SCADWr}}$, $\overline{\text{SCBDWr}}$	: Secondary Cache Data Write Enable
SCClk (5 : 0), $\overline{\text{SCClk (5 : 0)}}$	: Secondary Cache Clock
SCData (127 : 0)	: Secondary Cache Data Bus
SCDataChk (9 : 0)	: Secondary Cache Data Check Bus
SCTag (25 : 0)	: Secondary Cache Tag Bus
SCTagChk (6 : 0)	: Secondary Cache Tag Check Bus
SCTagLSBAddr	: Secondary Cache Tag LSB Address
$\overline{\text{SCTCS}}$	: Secondary Cache Chip Select
$\overline{\text{SCTOE}}$	: Secondary Cache Tag Output Enable
SCTWay	: Secondary Cache Tag Way
$\overline{\text{SCTWr}}$	: Secondary Cache Tag Write Enable
SysAD (63 : 0)	: System Address/Data Bus
SysADChk (7 : 0)	: System Address/Data Check Bus
SysClk, $\overline{\text{SysClk}}$	: System Clock
SysClkRet, $\overline{\text{SysClkRet}}$	: System Clock Return
SysCmd (11 : 0)	: System Command Bus
SysCmdPar	: System Command Bus Parity
$\overline{\text{SysCorErr}}$	: System Correctable Error
$\overline{\text{SysCyc}}$	: System Cycle
$\overline{\text{SysGbPerf}}$	: System Globally Performed
$\overline{\text{SysGnt}}$	: System Grant
$\overline{\text{SysNMI}}$	: System Non-maskable Interrupt
$\overline{\text{SysRdRdy}}$	: System Read Ready
$\overline{\text{SysReset}}$	: System Reset
SysResp (4 : 0)	: System Response Bus
SysRespPar	: System Response Bus Parity
$\overline{\text{SysRespVal}}$	: System Response Bus Valid
$\overline{\text{SysUncErr}}$	: System Uncorrectable Error
$\overline{\text{SysVal}}$	: System Valid
$\overline{\text{SysWrRdy}}$	: System Write Ready
$\overline{\text{SysRel}}$	: System Release
$\overline{\text{SysReq}}$	: System Request

SysState (2 : 0)	: System State Bus
SysStatePar	: System State Bus Parity
$\overline{\text{SysStateVal}}$	: System State Bus Valid
V_{DD}	: Power Supply
V_{DD}Pa	: V_{DD} for the PLL Analog
V_{DD}Pd	: V_{DD} for the PLL Digital
V_{DD}QSC	: V_{DD} for the Secondary Cache
V_{DD}QSys	: V_{DD} for the System Interface
VrefSC	: Voltage Reference for the Secondary Cache
VrefSys	: Voltage Reference for the System Interface
V_{SS}	: Ground
V_{SS}Pa	: V_{SS} for the PLL Analog
V_{SS}Pd	: V_{SS} for the PLL Digital
NC	: No Connection

BLOCK DIAGRAM



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1. PIN FUNCTIONS

1.1 Pin Function List

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Pin Name	I/O	Function
SCClk (5 : 0)	Output	Secondary cache clock signals.
$\overline{\text{SCClk (5 : 0)}}$	Output	Secondary cache clock signals. Inverted SCClk (5:0) signals.
SCAAddr (18 : 0), SCBAddr (18 : 0)	Output	Secondary cache address bus. 19-bit address bus for secondary cache.
SCTagLSBAddr	Output	Secondary cache tag LSB address. Specifies the LSB address of a secondary cache tag.
SCADWay, SCBDWay	Output	Secondary cache data way. Specifies a way of secondary cache data.
SCData (127 : 0)	I/O	Secondary cache data bus. 128-bit bus to read or write data from or to the secondary cache.
SCDataChk (9 : 0)	I/O	Secondary cache data check bus. 10-bit bus used to read or write ECC and even parity for secondary cache data.
$\overline{\text{SCADOE}}$, $\overline{\text{SCBDOE}}$	Output	Secondary cache data output enable. Signals enabling output of secondary cache data.
$\overline{\text{SCADWr}}$, $\overline{\text{SCBDWr}}$	Output	Secondary cache data write enable. Signals enabling writing of secondary cache data.
$\overline{\text{SCADCS}}$, $\overline{\text{SCBDCS}}$	Output	Secondary cache data chip select. Signals enabling access of secondary cache data.
SCTWay	Output	Secondary cache tag way. Specifies the way of a secondary cache tag.
SCTag (25 : 0)	I/O	Secondary cache tag bus. 26-bit bus to read or write a tag to or from the secondary cache.
SCTagChk (6 : 0)	I/O	Secondary cache tag check bus. 7-bit bus used to read or write ECC for secondary cache tag.
$\overline{\text{SCTOE}}$	Output	Secondary cache tag output enable. Signal enabling output of a secondary cache tag.
$\overline{\text{SCTWr}}$	Output	Secondary cache tag write enable. Signal enabling writing of a secondary cache tag.
$\overline{\text{SCTCS}}$	Output	Secondary cache tag chip select. Signal enabling access to a secondary cache tag.
SysClk	Input	System clock. System clock input.
$\overline{\text{SysClk}}$	Input	System clock. System clock input. Inverted SysClk signal.
SysClkRet	Output	System clock. System clock output used for termination of system clock.
$\overline{\text{SysClkRet}}$	Output	System clock. System clock output used for termination of system clock. Inverted SysClkReset signal.
$\overline{\text{SysReq}}$	Output	System request. Signal requesting enabling issuance of a processor request when the V_R10000 serves as a slave.

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Pin Name	I/O	Function
$\overline{\text{SysGnt}}$	Input	System enable. Signal used by an external agent to request the VR10000 for use of the system interface.
$\overline{\text{SysRel}}$	I/O	System release. The master side of the system interface asserts this signal active for the duration of 1 SysClk cycle when it releases the right to use the system interface in the subsequent SysClk cycle.
$\overline{\text{SysRdRdy}}$	Input	System read ready. Indicates that the external agent is ready to accept a processor read request and upgrade request.
$\overline{\text{SysWrRdy}}$	Input	System write ready. Indicates that the external agent is ready to accept a processor write request and processor eliminate request.
SysAD (63 : 0)	I/O	System address/data bus. 64-bit address/data bus for communication between the VR10000 and external agent.
SysADChk (7 : 0)	I/O	System address/data check bus. 8-bit ECC bus for SysAD bus.
SysCmd (11 : 0)	I/O	System command bus. 12-bit bus for command communication between the VR10000 and external agent.
SysCmdPar	I/O	System command bus parity. One odd parity bit for the system command bus.
$\overline{\text{SysVal}}$	I/O	System valid. Signal indicating that the master side of the system interface drives a valid address/command/data onto the SysAD bus and SysCmd bus.
SysState (2 : 0)	Output	System state bus. 3-bit bus indicating issuance or addition of a processor coherent status response.
SysStatePar	Output	System state bus parity. One odd parity bit for the system state bus.
$\overline{\text{SysStateVal}}$	Output	System state bus valid. The VR10000 asserts this signal active for the duration of 1 SysClk cycle when it issues a processor coherent response status to the SysState bus.
SysResp (4 : 0)	Input	System response bus. 5-bit bus used by the external agent to issue an external end response.
SysRespPar	Input	System response bus parity. One odd parity bit for the system response bus.
$\overline{\text{SysRespVal}}$	Input	System response bus valid. The external agent asserts this signal active for 1 SysClk cycle when it issues an external end response to the SysResp bus.
$\overline{\text{SysReset}}$	Input	System reset. Signal used by the external agent to reset the VR10000.
$\overline{\text{SysNMI}}$	Input	System non-maskable interrupt. Signal used by the external agent to issue NMI.
$\overline{\text{SysCorErr}}$	Output	System correctable error. The VR10000 asserts this signal active for 1 SysClk cycle when it finds and correct a correctable error.
$\overline{\text{SysUncErr}}$	Output	System uncorrectable error. The VR10000 asserts this signal active for 1 SysClk cycle when it finds an uncorrectable tag error.

(3/3)

Pin Name	I/O	Function
$\overline{\text{SysGblPerf}}$	Input	System global perfect. An external agent uses this signal to indicate completion of a processor request to all external agents.
$\overline{\text{SysCyc}}$	Input	System cycle. The external agent uses this signal to define a virtual system interface clock in hardware emulation environment.
JTDI	Input	JTAG data input. Inputs JTAG serial data.
JTDO	Output	JTAG data output. Outputs JTAG serial data.
JTCK	Input	JTAG clock input. Inputs JTAG serial clock. Keep this signal low when the JTAG interface is not used.
JTMS	Input	JTAG mode select. Selects a mode of JTAG.
DCOK	Input	DC voltage enable. The external agent asserts this signal active when the following signals are stable: V_{DD}, V_{DD}QSC, V_{DD}QSys, V_{ref}SC, V_{ref}Sys, V_{DD}Pa, V_{DD}Pd, SysClk
V_{DD}	Input	Power supply pin. Power supply for the CPU core.
V_{DD}QSC	Input	Secondary cache V_{DD}. Power supply for the output driver of the secondary cache interface.
V_{DD}QSys	Input	System interface V_{DD}. Power supply for the output driver of the system interface.
VrefSC	Input	Secondary cache voltage. Reference voltage for the input pins of the secondary cache interface.
VrefSys	Input	System interface voltage. Reference voltage for the input pins of the system interface.
V_{DD}Pa	Input	PLL analog V_{DD}. Power supply for the PLL analog circuit.
V_{DD}Pd	Input	PLL digital V_{DD}. Power supply for the PLL digital circuit.
V_{SS}	Input	Ground potential pin. Ground for the CPU core and output driver.
V_{SS}Pa	Input	PLL analog GND. Ground for the PLL analog.
V_{SS}Pd	Input	PLL digital GND. Ground for PLL digital.
NC	—	No connection. Leave this pin unconnected.

1.2 Recommended Connection of Unused Pins

Table 1-1 shows the recommended connection of unused pins.

Table 1-1. Recommended Connection of Unused Pins

Pin Name	I/O	Recommended Connection
JTDI	Input	Connect each of these pins to V_{DD} via a resistor.
JTCK		
JTMS		
$\overline{\text{SysNMI}}$		Connect this pin to V_{DD}QSys via resistor of 100 Ω or more.
$\overline{\text{SysRdRdy}}$		Connect each of these pins to V_{SS} via a resistor of 100 Ω or more.
$\overline{\text{SysWrRdy}}$		
$\overline{\text{SysGblPerf}}$		
$\overline{\text{SysCyc}}$		
SysADChk (7 : 0)	I/O	Connect each of these pins to V_{SS} or V_{DD}QSys via a resistor or 100 Ω or more.

2. CPU INTERNAL ARCHITECTURE

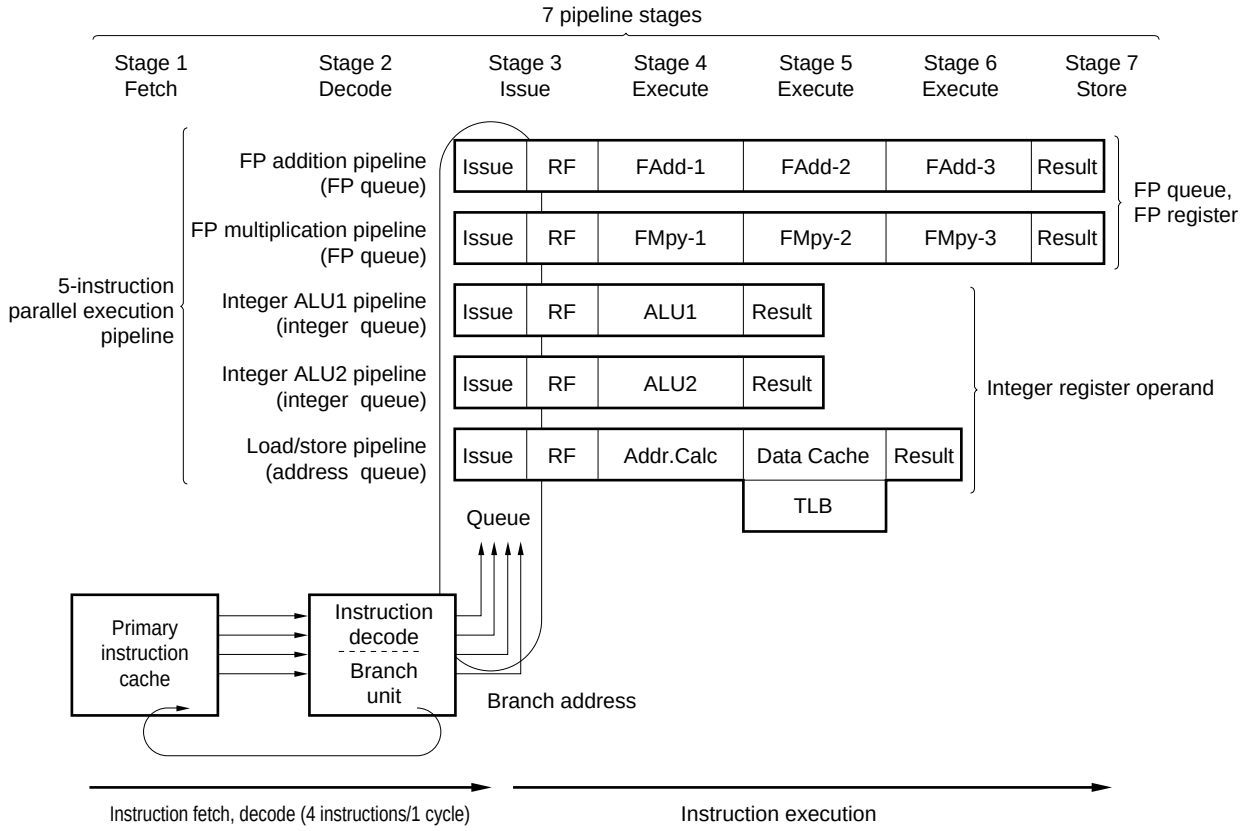
2.1 Pipeline

2.1.1 Configuration

The VR10000 has a 5-way super scalar pipeline as illustrated below. This pipeline can simultaneously fetch and decode four instructions in 1 Pcycle.

(1) FP addition pipeline
(2) FP multiplication pipeline
(3) Integer ALU1 pipeline
(4) Integer ALU2 pipeline
(5) Load/store pipeline

Figure 2-1. Pipeline



2.1.2 Operation

The pipeline of the VR10000 has seven stages. The operation of each stage is described below:

(1) Stage 1 (fetch)

Four instructions are fetched in 1 cycle and stored to the instruction register.

(2) Stage 2 (decode)

The four instructions fetched in stage 1 are decoded.

(3) Stage 3 (issue)

The decoded instructions are written to a queue. The VR10000 has an FP queue, integer queue, and address queue. In addition, an operand is read from the register file.

(4) Stage 4 through stage 6 (execute)

The instructions are executed. The execution pipeline and execution cycle differ depending on the type of instruction.

(a) FP addition pipeline

Executes floating-point addition instructions in 3 PCycle.

(b) FP multiplication pipeline

Executes floating-point multiplication, division, and square root instructions in 3 PCycle.

(c) Integer ALU1 pipeline

Executes integer addition, subtraction, shift, and logic instructions in 1 Pcycle.

(d) Integer ALU2 pipeline

Executes integer addition, subtraction, and logic instructions in 1 PCycle.

(e) Load/store pipeline

Generates a memory address used for integer or floating-point load/store instructions.

(5) Stage 7 (store)

The results of executing the instructions are stored to registers.

2.2 CPU Registers (virtual registers)

Figure 2-2 shows the CPU registers of the VR10000. Physically, sixty-four general-purpose registers are available. Of these, however, only thirty-two can be accessed by software or an external agent. Mapping of the other registers is automatically controlled by the CPU. The bit width of a register is determined by the operation mode of the VR10000 (32 bits in 32-bit mode, or 64 bits in 64-bit mode).

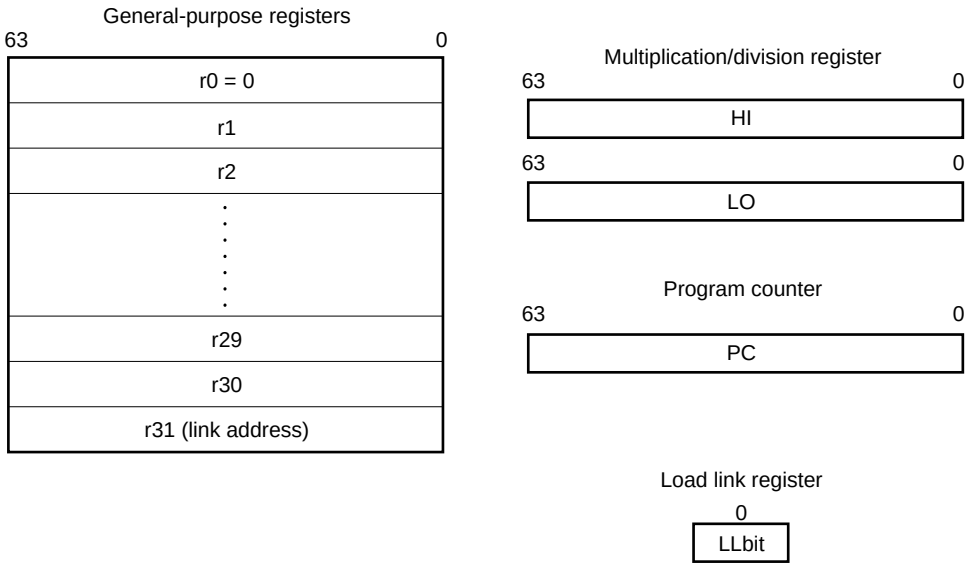
Of the thirty-two general-purpose registers, the following two have special meanings.

- Register r0 : The contents of this register are always 0. Register r0 can be used as the target register of an instruction when the result of an operation is to be discarded. This register can also be used as a source register when the value of 0 is necessary.
- Register r31 : This is a link system for the JAL and JALR instructions. Therefore, do not use this register with any other instructions.

Two multiplication/division registers (HI and LO) are used to store the result of integer multiplication, or quotient (LO) and remainder (HI) resulting from integer division.

The load link register is used to synchronize two or more VR10000s in a multi-processor system.

Figure 2-2. CPU Registers



There is no program status word (PSW). The function of PSW is substituted by the status register and cause register incorporated into the system control coprocessor (CP0).

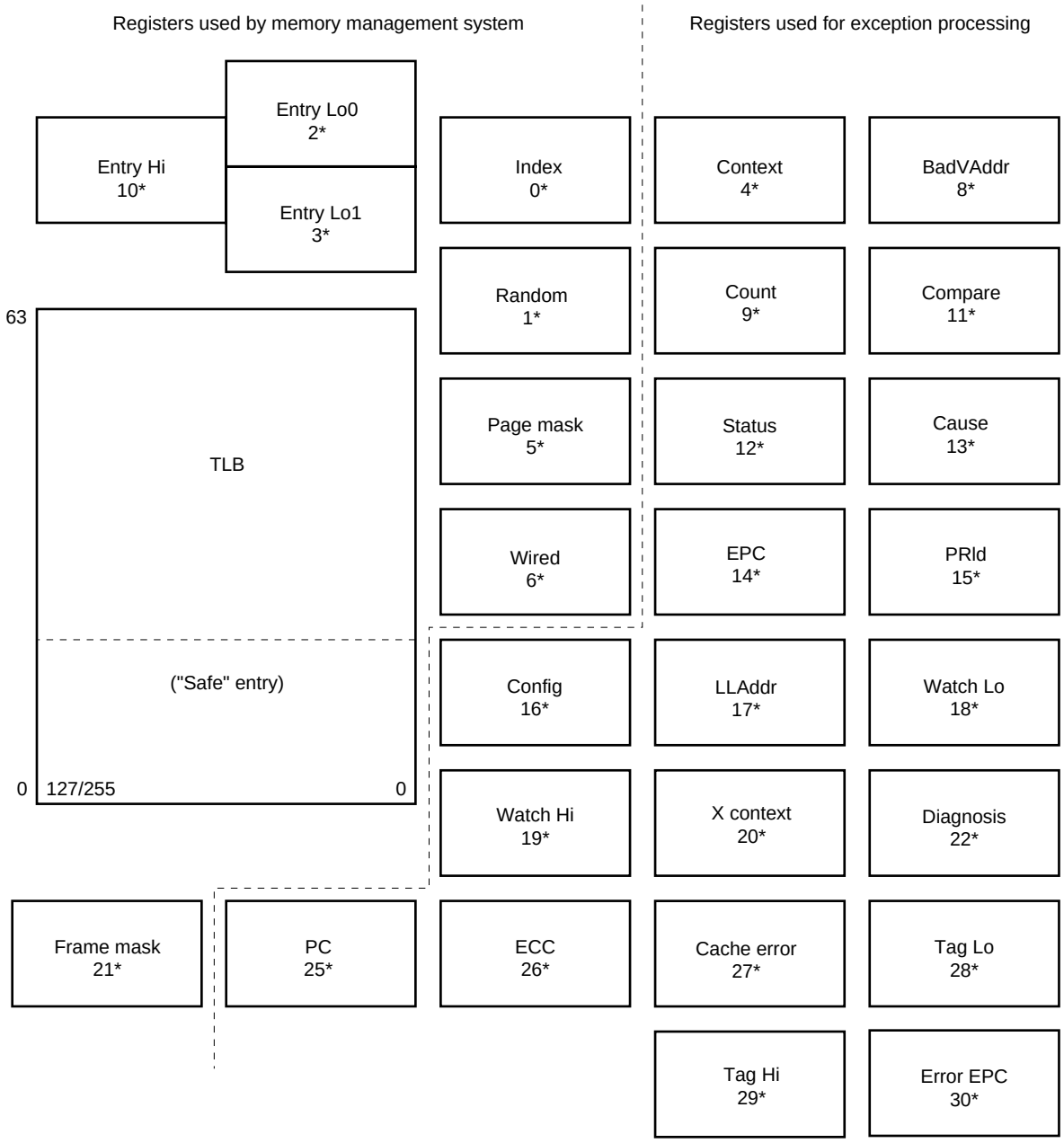
2.3 System Control Coprocessor (CP0)

The CP0 registers/CP0 instructions access the TLB and cache. Manipulating a mode in which the VR10000 is used, exceptions, and interrupts are also controlled by the CP0. In addition, the CP0 also has a test/debug function.

2.3.1 CP0 registers

All the CP0 registers that can be used with the VR10000 are listed below. Writing or reading an unused register (RFU) is undefined.

Figure 2-3. CPU0 Registers and TLB



Remark "*" indicates a register number.

Table 2-1. CP0 Register List

No.	Register	Description
0	Index	TLB entry programmable pointer
1	Random	TLB entry random pointer
2	Entry Lo0	Second half of TLB entry for even number VPN
3	Entry Lo1	Second half of TLB entry for odd number VPN
4	Context	Pointer to virtual PTE table of kernel in 32-bit mode
5	Page mask	TLB page mask
6	Wired	Number of wired TLB entries
7	—	RFU (Reserved for Future Use)
8	BadVAddr	Virtual address at which last error has occurred
9	Count	Timer count
10	Entry Hi	First half of TLB entry (including VPN and ASID)
11	Compare	Timer comparison
12	Status	Status register
13	Cause	Cause of last exception
14	EPC	Exception program counter
15	PRId	Processor revision identifier
16	Config	Configuration register
17	LLAddr	Address of LL instruction
18	Watch Lo	Low-order bits of memory reference trap address
19	Watch Hi	High-order bits of memory reference trap address
20	X context	Pointer to virtual PTE table of kernel in 64-bit mode
21	Frame mask	Bit mask of entry Lo register
22	Diagnosis	Branch diagnosis
23, 24	—	RFU
25	PC	Performance counter
26	ECC	ECC of secondary cache and parity of primary cache
27	Cache error	Index of cache error and status field
28	Tag Lo	Cache tag register, low-order
29	Tag Hi	Cache tag register, high-order
30	Error EPC	Error exception program counter
31	—	RFU

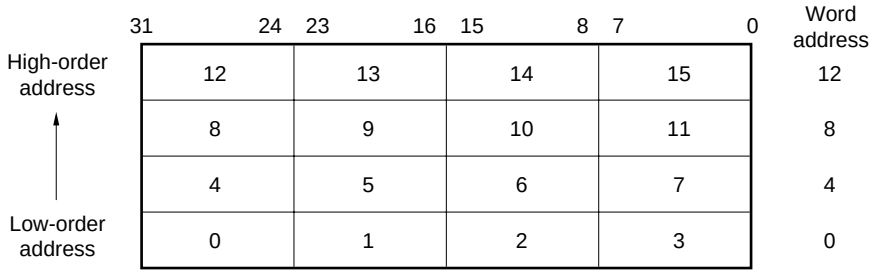
2.4 Data Format and Addressing

The VR10000 has the following four types of data formats:

Double word (64 bits)
Word (32 bit)
Half word (16 bits)
Byte (8 bits)

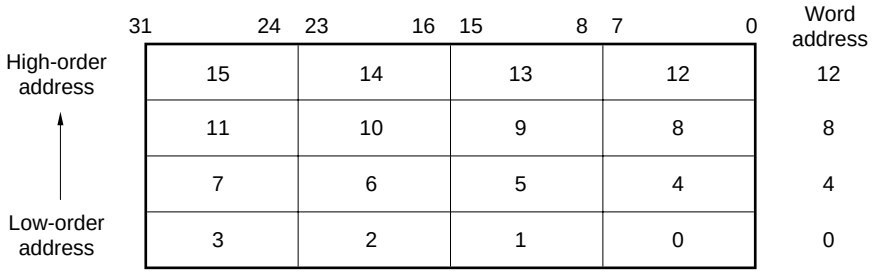
If the data format is double word, word, or half word, the byte order can be set to bit endian or little endian by using the BE bit of the config register.

Figure 2-4. Byte Address in Word: Big Endian



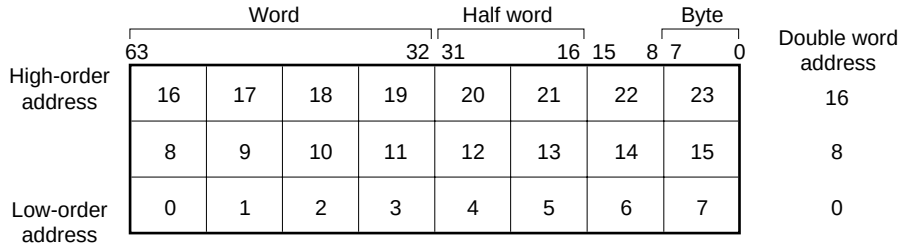
Remarks 1. The most significant byte is the least significant address.
2. A word is addressed by the address of the most significant byte.

Figure 2-5. Byte Address in Word: Little Endian



Remarks 1. The least significant byte is the least significant address.
2. A word is addressed by the address of the least significant byte.

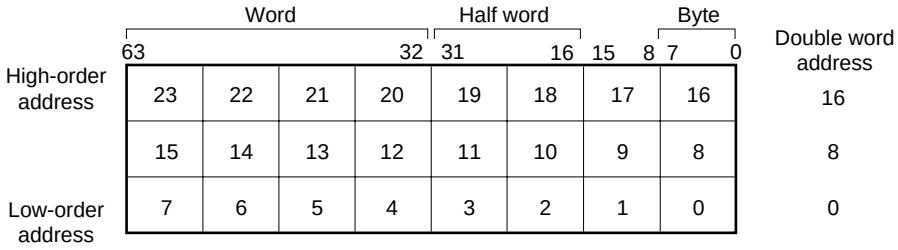
Figure 2-6. Byte Address in Double Word: Big Endian



Remarks 1. The most significant byte is the least significant address.

2. A word is addressed by the address of the most significant byte.

Figure 2-7. Byte Address in Double Word: Little Endian



Remarks 1. The least significant byte is the least significant address.

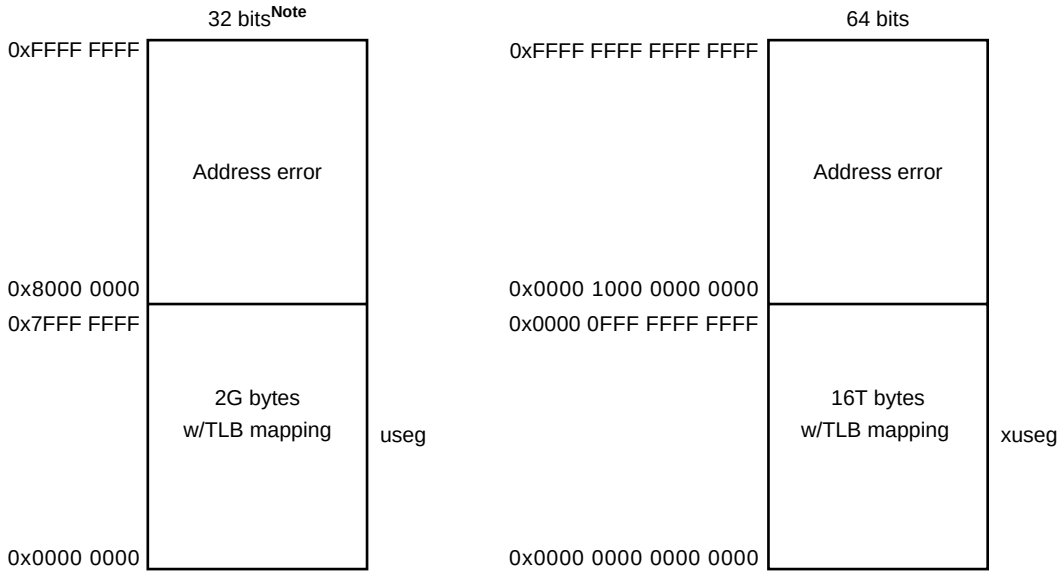
2. A word is addressed by the address of the least significant byte.

2.5 Virtual Storage

2.5.1 Virtual address space

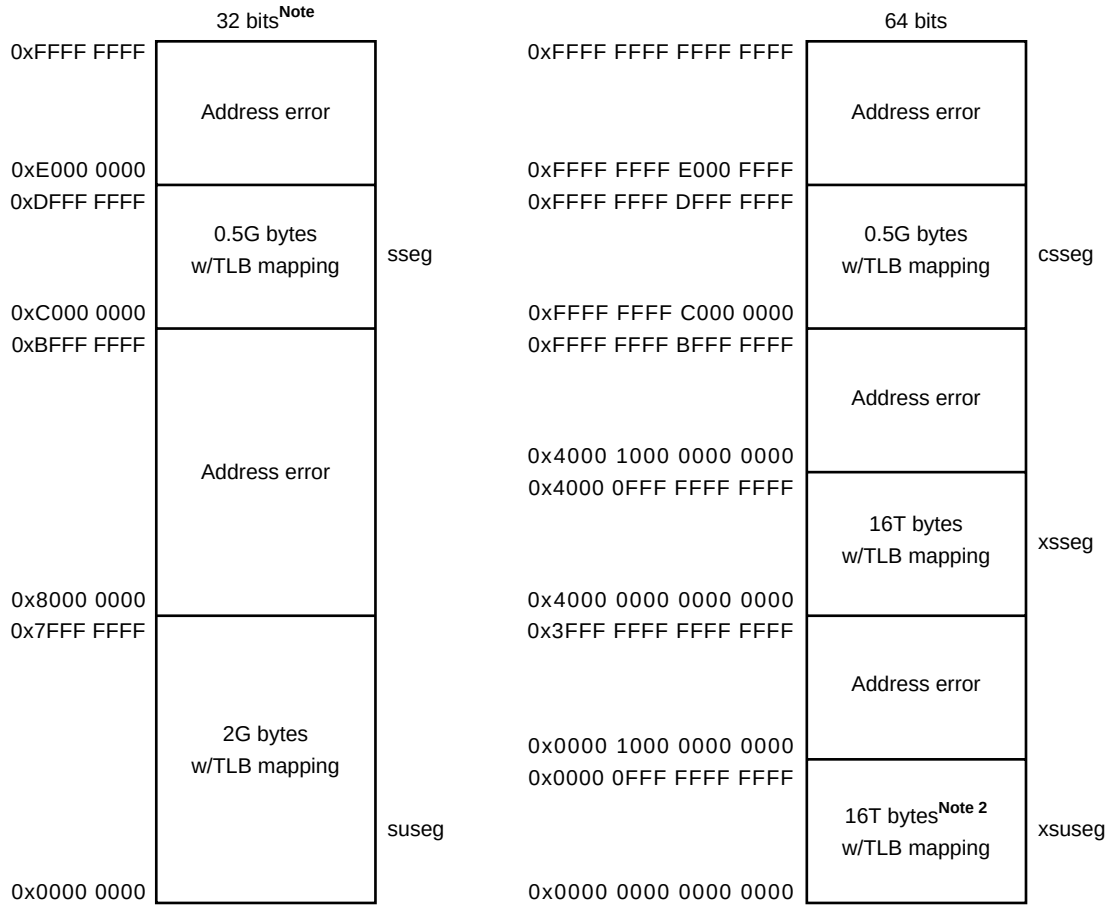
The VR10000 has two operation modes, the 32-bit and 64-bit modes. In addition, it has three operating modes: the user mode, supervisor mode, and kernel mode. Figures 2-8 through 2-11 show the virtual address spaces in the respective modes.

Figure 2-8. User Mode Address Space



Note In the 32-bit mode, the value of bit 31 is sign-extended to bits 32 through 63.

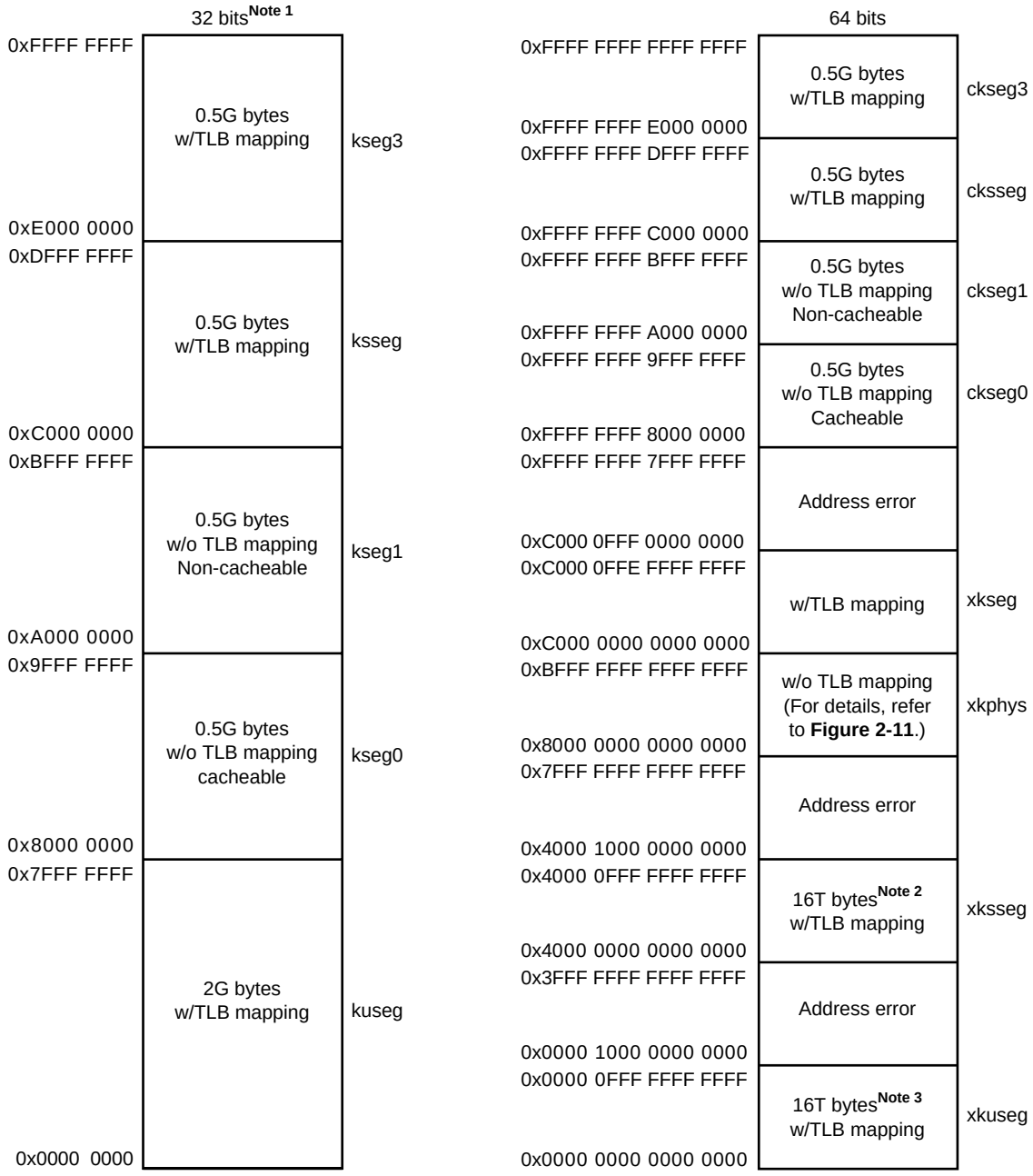
Figure 2-9. Supervisor Mode Address Space



Notes 1. In the 32-bit mode, the value of bit 31 is sign-extended to bits 32 through 63.

2. If the UX bit of the status register is 0, 0x0000 0000 8000 0000 through 0x0000 0FFF FFFF FFFF cause an address error.

Figure 2-10. Kernel Mode Address Space

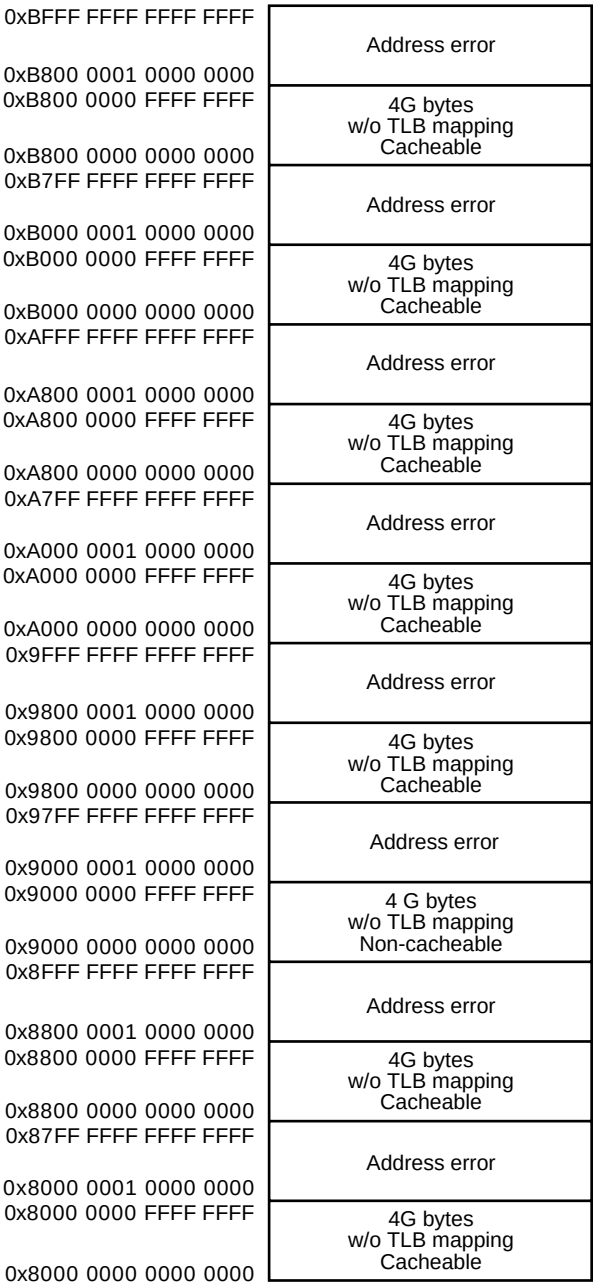


Notes 1. In the 32-bit mode, the value of bit 31 is sign-extended to bits 32 through 63.

2. If the SX bit of the status register is 0, this area causes an address error.

3. If the UX bit of the status register is 0, 0x0000 0000 8000 0000 through 0x0000 0FFF FFFF FFFF cause an address error.

Figure 2-11. Details of xkphys Area



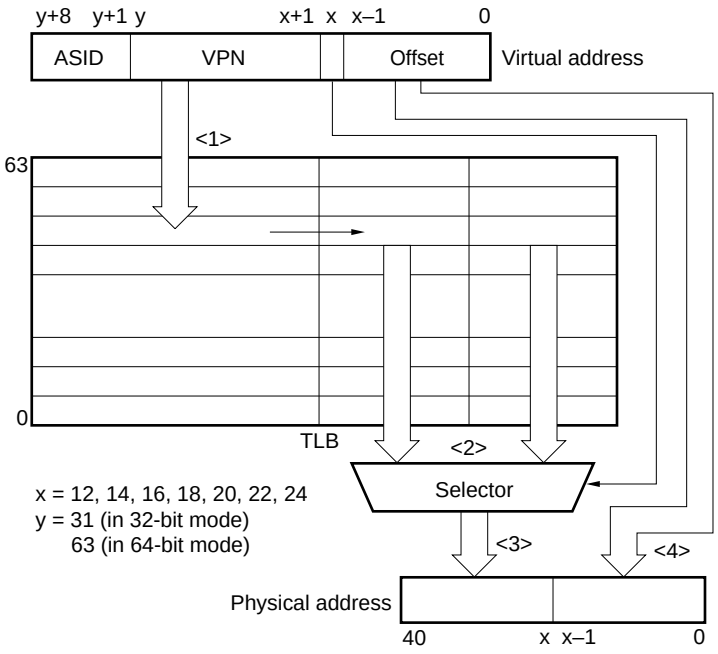
2.5.2 Address translation

Virtual addresses are translated into physical addresses by the internal TLB (Translation Lookaside Buffer) in page units. The TLB is of full-associative configuration and has 64 entries at the virtual address side and 32 entries at the physical address side. The page size can be changed from 4K bytes to 16M bytes.

If a hit of a TLB entry does not occur, a TLB non-coincidence exception occurs in the 32-bit mode and an XTLB non-coincidence exception occurs in the 64-bit mode. If this happens, replace the contents of the TLB by software.

Figure 2-12 outlines address translation.

Figure 2-12. Outline of Address Translation



<1> A virtual address page number (VPN) is compared with VPN in TLB.

<2> If the two VPNs coincide, a page frame number (PFN) indicating the high-order bits of a physical address is output to the selector.

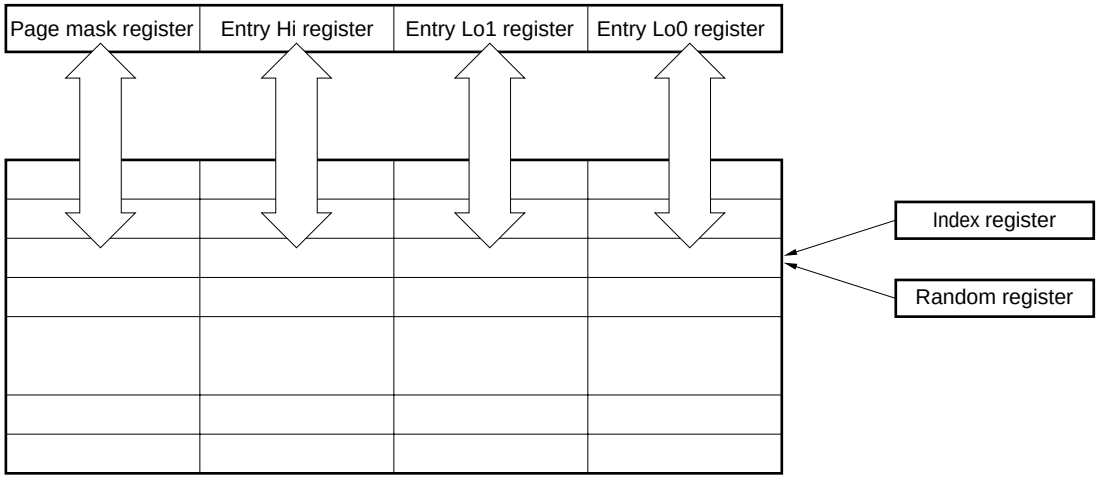
<3> If the least significant bit of VPN is 0, an even page is selected; if it is 1, an odd page is selected. The selected page is output to the high-order bits of the physical address.

<4> The offset is output to the low-order bits of the physical address without via TLB.

TLB entries are read or written by loading/storing the TLB entry indicated by the index register and the random register from or to the entry Hi, entry Lo1, Entry Lo0, and page mask registers.

Figure 2-13 outlines TLB manipulation.

Figure 2-13. Outline of TLB Manipulation



2.6 Cache

The VR10000 has a primary instruction cache and primary data cache. In addition, it has a secondary cache interface to connect an external secondary cache.

2.6.1 Primary cache

(1) Primary instruction cache

Here are the features of the primary instruction cache:

- Internal cache memory
- Capacity: 32K bytes
- 16-word cache line
- 2-way set associative
- Physical index address
- Physical tag check

(2) Primary data cache

Here are the features of the primary data cache.

- Internal cache memory
- Capacity: 32K bytes
- 8-word cache line
- 2-bank configuration
- 2-way set associative
- Non-Blocking method
- Write back method
- Physical index address
- Physical tag check

2.6.2 Secondary cache

The VR10000 can use an external secondary cache. The features of the secondary cache are as follows:

- Capacity: 512K to 16M bytes
- 16-/32-word cache line
- 2-way set associative
- Way prediction table
- Write back method
- Non-Blocking method
- Physical index address
- Physical tag check

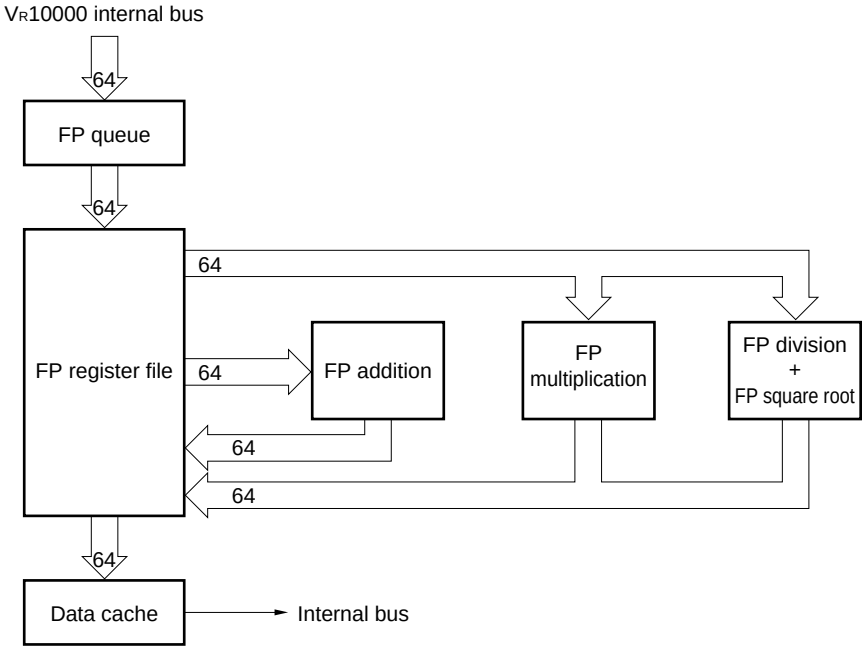
3. FPU INTERNAL ARCHITECTURE

3.1 Internal Function Block

Figure 3-1 shows the internal block of the FPU.

The FPU can execute all the floating-point instructions defined by MIPS ISA.

Figure 3-1. Internal Block of FPU



3.2 FPU Registers

(1) Floating-point general-purpose registers (FGR)

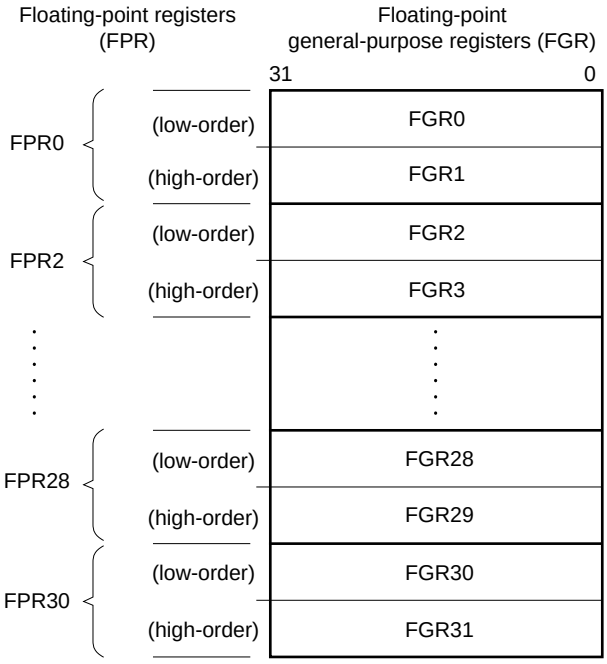
These are physical general-purpose registers that can be directly accessed. Thirty-two of these registers are available. The bit length of each register differs depending on the content of the FR bit of the status register.

(2) Floating-point registers (FPR)

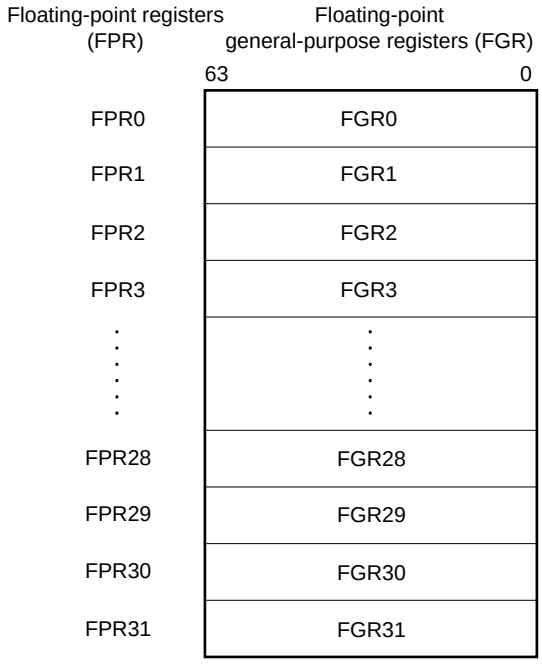
These are logical 64-bit registers that hold a floating-point value when a floating-point operation is executed. The number of these registers varies depending on the content of the FR bit of the status register.

Figure 3-2. Registers of FPU

(a) When FR bit = 0 (MIPS I, MIPS II)



(b) When FR bit = 1 (MIPS III, MIPS IV)



3.3 Data Format

(1) Floating-point format

The FPU supports IEEE754 floating-point operations of 32 bits (single precision) and 64 bits (double precision).

(2) Fixed-point format

A fixed-point value is calculated in the form of 2's complement.

4. INTERFACE

4.1 System Interface

The I/O timing of the VR10000 is as follows:

- Output starts changing at the rising edge of SysClk.
- Input is latched at the rising edge of SysClk.

The following two buses are used for system interfacing.

- SysAD (63:0) : This bus transfers addresses and data.
- SysCmd (11:0) : This bus transfers command data identifiers.

Both SysAD and SysCmd are bidirectional buses and are driven by the VR10000 or external agent. Depending on the direction in which they are driven, these buses are in the following two statuses.

- Master status : Driven by the VR10000 to issue a processor request.
- Slave status : Driven by the external agent to issue an external request.

The following two cycles are used depending on the information included in the SysAD bus.

- Address cycle : A valid address is included in the SysAD bus.
- Data cycle : Valid data is included in the SysAD bus.

Next, the interface control signals are briefly explained.

- $\overline{\text{SysReq}}$: Signal used by the VR10000 to request the right to use the system interface.
- $\overline{\text{SysGnt}}$: Signal used by the external agent to grant the VR10000 the right to use the system interface.
- $\overline{\text{SysRel}}$: Asserted active when the master of the system interface releases the right of use.
- $\overline{\text{SysRdRdy}}$: Indicates that the external agent is ready to accept a processor read request and upgrade request.
- $\overline{\text{SysWrRdy}}$: Indicates that the external agent is ready to accept a processor write request and processor eliminate request.
- $\overline{\text{SysVal}}$: Asserted active when the master of the system interface outputs valid data to the SysAD and SysCmd buses.
- SysState (2:0) : Signal used by the VR10000 to issue a coherent status request.
- SysResp (4:0) : Signal used by the external agent to issue an external end response.
- $\overline{\text{SysGblPerf}}$: Signal used by the external agent to indicate that all processor requests have been completed.

4.1.1 Setting operating frequency of system interface

The VR10000 can select the operating frequency of the system interface.

The clock (PClk) for pipeline operation is generated based on the clock (SysClk) input from an external source. The factor by which SysClk is multiplied to generate PClk is set by using the BTMC interface at reset. For details, refer to SysAD (9:12) in **Table 4-1 Mode Setting in Boot Time Mode**.

4.2 Secondary Cache Interface

The VR10000 has a secondary cache control circuit, so that an external secondary cache memory can be connected. The VR10000 can also selects the operating frequency of the secondary cache interface.

SCClk, at which the secondary cache is to operate, is generated based on the operating clock (PClk) of the VR10000. The factor by which SysClk is multiplied to generate PClk is set by using the BTMC interface at reset. For details, refer to SysAD (9:12) in **Table 4-1 Mode Setting in Boot Time Mode**.

4.3 Clock Interface

4.3.1 System interface clock and processor clock

The VR10000 generates a processor clock (PClk), which is the internal operating clock, from the clock (SysClk and $\overline{\text{SysClk}}$) input to the VR10000, by using the PLL. It always samples the SysClk and $\overline{\text{SysClk}}$ signals during operation, in order to check to see if the following expression is satisfied.

$$\text{PClk} = \text{SysClk} \times (\text{SysClkDiv} + 1)/2$$

Example Where SysClk = 50 MHz and SysClkDiv = 7
PClk = 50 × 8/2 = 200 MHz

4.3.2 Secondary cache clock

The VR10000 supplies clocks for secondary cache (SCClk (5:0) and $\overline{\text{SCClk (5:0)}}$) to the external secondary cache. SCClk (5:0) are generated from SysClk.

The relation between SCClk (5:0) and SysClk can be expressed by the following expression.

$$\text{SCClk} = \text{SysClk} \times (\text{SysClkDiv} + 1)/(\text{SCClkDiv} + 1)$$

Example Where SysClk = 50 MHz, SysClkDiv = 7, and SCClkDiv = 2
SCClk = 50 × 8/3 = 133 MHz

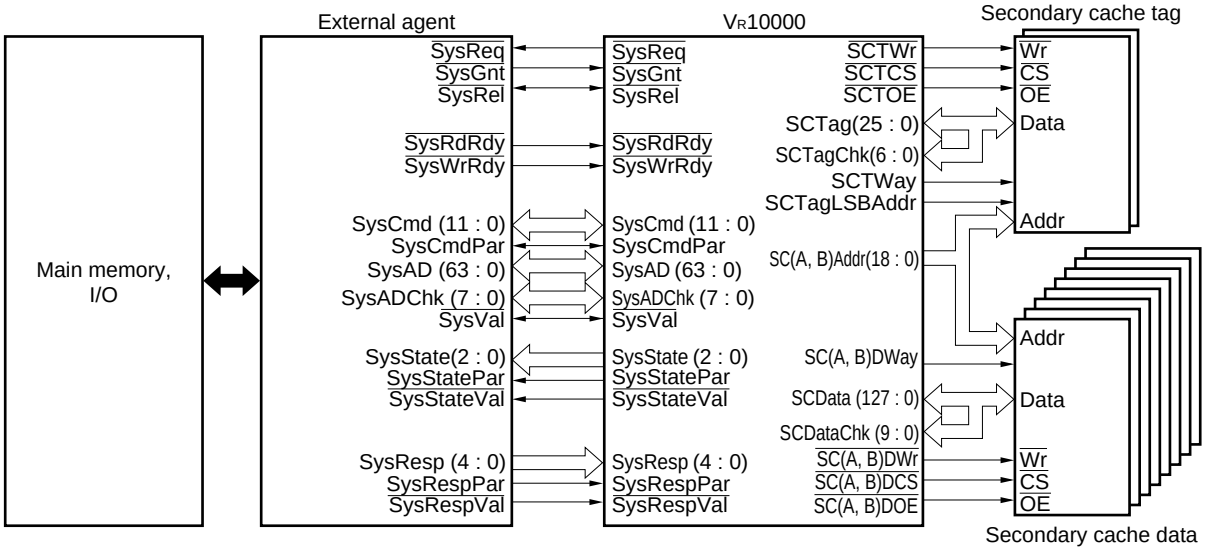
4.4 System Configuration Example

Because the VR10000 employs a cluster bus, it can also support a multi-processor system. Examples of configuration of a uni-processor system and a multi-processor system are shown below.

4.4.1 Uni-processor system

This system uses only one VR10000, as shown in Figure 4-1.

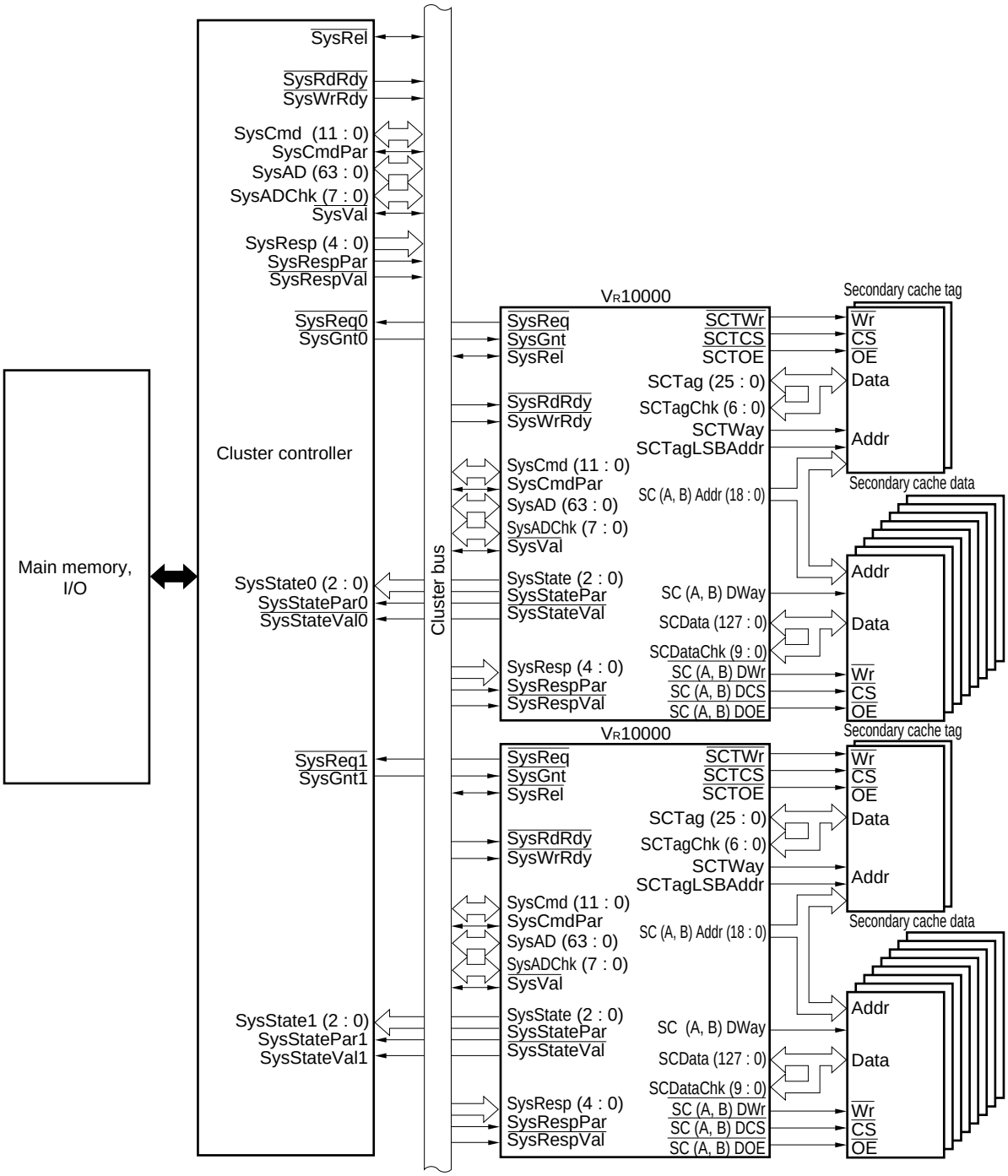
Figure 4-1. Example of Configuration of Uni-Processor System



4.4.2 Multi-processor system

Up to four VR10000s can be connected to the cluster bus. While a VR10000 stands by for a response after it has issued a request, it can receive up to four processings. Figure 4-2 shows an example of multi-processor system configuration.

Figure 4-2. Example of Configuration of Multi-Processor System



4.5 BTMC Interface

The operation of the VR10000 is set by the mode bit. The content of the mode bit is stored to the processor via SysAD (63:0) at power-ON reset or by cold reset sequence while $\overline{\text{SysGnt}}$ is active. The content of the mode bit that is set via SysAD (24:0) is stored to bits 24 through 0 of the config register.

Table 4-1 shows the correspondence between the SysAD bus and mode setting in the boot time mode.

Table 4-1. Mode Setting in Boot Time Mode (1/2)

SysAD	Mode Setting	
	VR10000	VR12000
0 : 2	Kseg0CA: Kseg0 cache status 0, 1: RFU 2: Non-cacheable 3: Cacheable, non-coherent 4: Cacheable, coherent exclusive 5: Cacheable, coherent exclusive on write 6: RFU 7: Non-cacheable, accelerate	
3, 4	DevNum: Processor number	
5	CohPrcReqTar: Issuance destination of processor coherent request 0: External agent 1: All	
6	PrcElmReq: Enables processor eliminate request 0: Disabled 1: Enabled	
7, 8	PrcReqMax: Number of processor requests that can be kept pending on system bus 0: 1 1: 2 2: 3 3: 4	
9 : 12	SysClkDiv: Multiple of PClk in respect to SysClk 0: RFU 1: × 1 2: × 1.5 3: × 2 4: × 2.5 5: × 3 6: × 3.5 7: × 4 8 to F: RFU	SysClkDiv: Multiple of PClk in respect to SysClk 0: RFU 1: RFU 2: RFU 3: × 2 4: × 2.5 5: × 3 6: × 3.5 7: × 4 8: × 4.5 9: × 5 A: × 5.5 B: × 6 C: × 7 D: × 8 E: × 9 F: × 10
13	SCBlkSize: Line size of secondary cache 0: 16 words 1: 32 words	

Table 4-1. Mode Setting in Boot Time Mode (2/2)

SysAD	Mode Setting	
	VR10000	VR12000
14	SCCorEn: ECC error correction of secondary cache data 0: Re-access 1: Always access	
15	MemEnd: Endian 0: Little endian 1: Big endian	
16 : 18	SCSize: Secondary cache size 0: 512K 1: 1M bytes 2: 2M bytes 3: 4M bytes 4: 8M bytes 5: 16M bytes 6 and 7: RFU	
19 : 21	SCClkDiv: Multiple of PClk in respect to SCClk 0: RFU 1: × 1 2: × 1.5 3: × 2 4: × 2.5 5: × 3 6 and 7: RFU	SCClkDiv: Multiple of PClk in respect to SCClk 0: RFU 1: × 1 2: × 1.5 3: × 2 4: × 2.5 5: × 3 6: RFU 7: × 4
22 : 24	RFU	DSD[Note 1]: DSD (Delay Speculative Dirty) mode 0 to 3: RFU 4: DSD 5 to 7: RFU
25 : 28	SCClkTap: Internal secondary cache: Phase comparison of clock and SysClk (5:0), $\overline{\text{SysClk}}$ (5:0) 0: Same phase 1: SCClk leads 1/12PClk cycle 2: SCClk leads 2/12PClk cycle 3: SCClk leads 3/12PClk cycle 4: SCClk leads 4/12PClk cycle 5: SCClk leads 5/12PClk cycle 6 and 7: Undefined 8: SCClk leads 6/12PClk cycle 9: SCClk leads 7/12PClk cycle A: SCClk leads 8/12PClk cycle B: SCClk leads 9/12PClk cycle C: SCClk leads 10/12PClk cycle D: SCClk leads 11/12PClk cycle E and F: Undefined	
29	RFU	
30	ODrainSys: Processing of system interface signal[Note 2]	
31 : 63	RFU	

Notes 1. Refer to **4.6 DSD (Delay Speculative Dirty) mode**.

2. $\overline{\text{SysReq}}$, $\overline{\text{SysRel}}$, SysCmd (11:0), SysCmdPar, SysAD (63: 0), SysADChk (7:0), $\overline{\text{SysVal}}$, SysState (2:0), SysStatePar, $\overline{\text{SysStateVal}}$, $\overline{\text{SysCorErr}}$, $\overline{\text{SysUncErr}}$

4.6 DSD (Delay Speculative Dirty) Mode (VR12000 only)

The DSD (Delay Speculative Dirty) mode prevents a dirty bit from being set by speculative storing.

Bit 24 in the boot mode coincides with bit 24 of the config register and sets the DSD mode in the kernel mode and supervisor mode. However, the DSD mode can be also executed in the user mode by setting bit 24 of the status register. Bit 24 of the config register is read-only and can be set only during boot time.

When the DSD mode has been set, the dirty bit of the secondary cache block of the VR12000 are not set until the store instruction has become the oldest instruction in the active list and ready to be executed (the dirty bit may be set by an interrupt (and the store instruction is no longer in the speculative status), but the store instruction is not immediately completed).

4.6.1 DSD mode delay

The DSD mode delays setting of a dirty bit but slightly slows down the processing speed. This slowdown occurs each time a block is refilled from the main memory if it is necessary to set the dirty bit. It takes 10 cycles to set the dirty bit. During this time, the processor executes the other instructions in parallel.

Once a block becomes dirty in the secondary cache, this mode does not affect the performance.

4.6.2 Secondary cache status in DSD mode

The secondary cache in the DSD mode enters the Clean Exclusive status if a miss hit occurs when the store instruction is no longer the oldest instruction in the pipeline.

Because the cache is upgraded to the Clean Exclusive status immediately after a hit occurs in a line in the Shared status, bus manipulation is started in the speculative status (the processing speed relatively slows down).

4.6.3 Other features

The VR12000 delays loading of the non-coherent cache until this instruction becomes the oldest, regardless of the DSD mode. This is because speculative loading that accesses an address of the xkphys area not mapped as a non-coherent cache may send data to the secondary cache without appropriate coherency check.

5. INTERNAL/EXTERNAL CONTROL FUNCTIONS

5.1 Reset Function

The following three types of reset functions are available:

- Power-ON reset
- Cold reset
- Software reset

Cold reset and software reset are executed with the power turned on.

As a result of reset, the internal status is initialized. However, software reset does not affect the internal clock and secondary cache clock.

5.1.1 Power-ON reset and cold reset

Power-ON reset and cold reset are executed when the $\overline{\text{SysGnt}}$ and $\overline{\text{SysRespVal}}$ signals are deasserted inactive and the $\overline{\text{SysReset}}$ signal is asserted active. During reset, 64-bit data is received from the mode bit, and the internal status of the processor is initialized (for further information, refer to **4.5 BTMC Interface**).

5.1.2 Software reset

Software reset is executed when the $\overline{\text{SysGnt}}$ and $\overline{\text{SysRespVal}}$ signals are deasserted inactive and the $\overline{\text{SysReset}}$ signal is asserted active. As a result, all the statuses of the external interface are initialized, but the internal clock and secondary cache clock continues operating. Like the primary and secondary cache, the contents of the CP0 and FPU registers are retained.

5.2 Interrupt Functions

There are two major types of interrupt requests:

- Maskable interrupt request
- Non-maskable interrupt (NMI) request

(1) Maskable interrupt requests

These interrupts can be masked by using the status register (each interrupt can be serviced independently, or all interrupts can be serviced in batch).

There is no priority assigned to the interrupts.

(a) Hardware interrupt requests (five sources)

These interrupts are acknowledged when the corresponding external interrupt request is issued.

(b) Software interrupt requests (two sources)

These interrupts are acknowledged when the IP0 and IP1 bits of the cause register are set.

(c) Timer interrupt request (1 source)

This interrupt is acknowledged when the IP7 bit of the cause register is set because the value of the count register has become equal to the value of the compare register, or when one of the two performance counters has overflown.

(2) NMI request (1 source)

This is an interrupt request that cannot be masked and is acknowledged when the $\overline{\text{SysNMI}}$ signal is asserted active.

5.3 JTAG Function

The JTAG boundary scan function is a mechanism to test mutual connections among the VR10000 and other components, and not to test the processor itself.

As the minimum functions of JTAG, the following functions are provided to the VR10000. Functionally, however, the VR10000 only has the external test function of the JTAG boundary scan register.

- TAP controller
- JTAG instruction register
- JTAG bypass register
- JTAG boundary scan register

6. INSTRUCTION SET

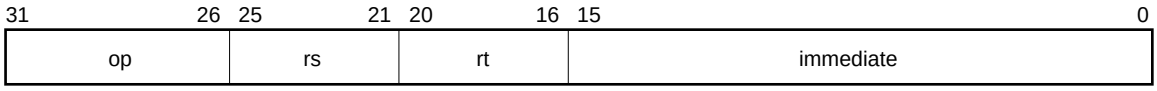
The instructions of the VR10000 consists of 1 word (32 bits) located at a word boundary, and come in three formats as shown in Figure 6-1. Because only three types of instructions are provided, decoding instructions is simplified. Complicated operations and addressing modes that are not so often used are implemented by a compiler.

6.1 Instruction Formats

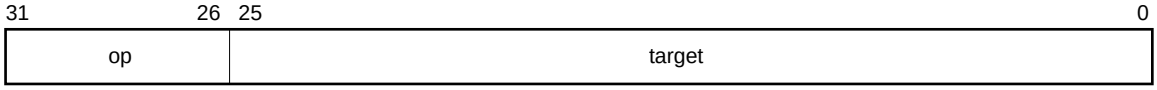
The instruction formats of the VR10000 are shown below.

Figure 6-1. CPU Instruction Format

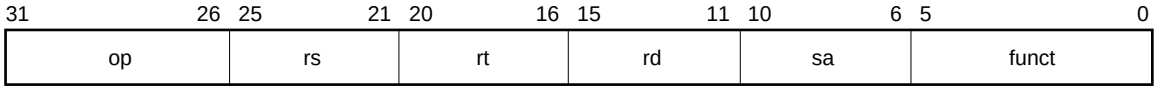
I - type (immediate format)



J - type (jump format)



R - type (register format)



op	6-bit instruction code
rs	5-bit source register specifier
rt	5-bit target (source/destination) register, or branch condition
immediate	16-bit immediate value, branch displacement, or address displacement
target	26-bit unconditional branch target address
rd	5-bit destination register specifier
sa	5-bit shift amount
funct	6-bit function field

6.2 CPU Instruction Set List

The CPU instructions of the VR10000 can be classified into an instruction set common to all the VR series processors (ISA: Instruction Set Architecture), instruction set that is executed by the VR4000 series and VR10000 series (expanded ISA), and system control coprocessor instruction set. Tables 6-1 through 6-4 list each instruction set.

Table 6-1. CPU Instruction Set: MIPS I (1/2)

Instruction	Description	Format	
Load/store instruction	op | base | rt | offset		
LB	Load Byte	LB	rt, offset (base)
LBU	Load Byte Unsigned	LBU	rt, offset (base)
LH	Load Halfword	LH	rt, offset (base)
LHU	Load Halfword Unsigned	LHU	rt, offset (base)
LW	Load Word	LW	rt, offset (base)
LWL	Load Word Left	LWL	rt, offset (base)
LWR	Load Word Right	LWR	rt, offset (base)
SB	Store Byte	SB	rt, offset (base)
SH	Store Halfword	SH	rt, offset (base)
SW	Store Word	SW	rt, offset (base)
SWL	Store Word Left	SWL	rt, offset (base)
SWR	Store Word Right	SWR	rt, offset (base)
ALU immediate instruction	op | rs | rt | offset		
ADDI	Add Immediate	ADDI	rt, rs, immediate
ADDIU	Add Immediate Unsigned	ADDIU	rt, rs, immediate
SLTI	Set On Less Than Immediate	SLTI	rt, rs, immediate
SLTIU	Set On Less Than Immediate Unsigned	SLTIU	rt, rs, immediate
ANDI	And Immediate	ANDI	rt, rs, immediate
ORI	Or Immediate	ORI	rt, rs, immediate
XORI	Exclusive Or Immediate	XORI	rt, rs, immediate
LUI	Load Upper Immediate	LUI	rt, immediate
3-operand type instruction	op | rs | rt | rd | sa | funct		
ADD	Add	ADD	rd, rs, rt
ADDU	Add Unsigned	ADDU	rd, rs, rt
SUB	Subtract	SUB	rd, rs, rt
SUBU	Subtract Unsigned	SUBU	rd, rs, rt
SLT	Set On Less Than	SLT	rd, rs, rt
SLTU	Set On Less Than Unsigned	SLTU	rd, rs, rt
AND	And	AND	rd, rs, rt
OR	Or	OR	rd, rs, rt
XOR	Exclusive Or	XOR	rd, rs, rt
NOR	Nor	NOR	rd, rs, rt
Shift instruction	op | rs | rt | rd | sa | funct		
SLL	Shift Left Logical	SLL	rd, rt, sa
SRL	Shift Right Logical	SRL	rd, rt, sa
SRA	Shift Right Arithmetic	SRA	rd, rt, sa
SLLV	Shift Left Logical Variable	SLLV	rd, rt, rs
SRLV	Shift Right Logical Variable	SRLV	rd, rt, rs
SRAV	Shift Right Arithmetic Variable	SRAV	rd, rt, rs

Table 6-1. CPU Instruction Set: MIPS I (2/2)

Instruction	Description	Format
Multiplication/division instruction	op | rs | rt | rd | sa | funct	
MULT	Multiply	MULT rs, rt
MULTU	Multiply Unsigned	MULTU rs, rt
DIV	Divide	DIV rs, rt
DIVU	Divide Unsigned	DIVU rs, rt
MFHI	Move From HI	MFHI rd
MFLO	Move From LO	MFLO rd
MTHI	Move To HI	MTHI rs
MTLO	Move To LO	MTLO rs
Jump instruction (1)	op | target	
J	Jump	J target
JAL	Jump And Link	JAL target
Jump instruction (2)	op | rs | rt | rd | sa | funct	
JR	Jump Register	JR rs
JALR	Jump And Link Register	JALR rs
		JALR rs, rd
Branch instruction (1)	op | rs | rt | offset	
BEQ	Branch On Equal	BEQ rs, rt, offset
BNE	Branch On Not Equal	BNE rs, rt, offset
BLEZ	Branch On Less Than Or Equal To Zero	BLEZ rs, offset
BGTZ	Branch On Greater Than Zero	BGTZ rs, offset
Branch instruction (2)	REGIMM | rs | sub | offset	
BLTZ	Branch On Less Than Zero	BLTZ rs, offset
BGEZ	Branch On Greater Than Or Equal to Zero	BGEZ rs, offset
BLTZAL	Branch On Less Than Zero And Link	BLTZAL rs, offset
BGEZAL	Branch On Greater Than Or Equal To Zero And Link	BGEZAL rs, offset
Special instruction	SPECIAL | rs | rt | rd | sa | funct	
SYSCALL	System Call	SYSCALL
BREAK	Breakpoint	BREAK
Coprocessor instruction (1)	op | base | rt | offset	
LWCz	Load Word To Coprocessor z	LWCz rt, offset (base)
SWCz	Store Word From Coprocessor z	SWCz rt, offset (base)
Coprocessor instruction (2)	COPz | CO | cofun	
COPz	Coprocessor z Operation	COPz cofun

Table 6-2. CPU Instruction Set: MIPS II

Instruction	Description	Format
Load/store instruction	op | base | rt | offset	
LL	Load Linked	LL rt, offset (base)
SC	Store Conditional	SC rt, offset (base)
Branch instruction (1)	op | rs | rt | offset	
BEQL	Branch On Equal Likely	BEQL rs, rt, offset
BNEL	Branch On Not Equal Likely	BNEL rs, rt, offset
BLEZL	Branch On Less Than Or Equal To Zero Likely	BLEZL rs, offset
BGTZL	Branch On Greater Than Zero Likely	BGTZL rs, offset
Branch instruction (2)	REGIMM | rs | sub | offset	
BLTZL	Branch On Less Than Zero Likely	BLTZL rs, offset
BGEZL	Branch On Greater Than Or Equal To Zero Likely	BGEZL rs, offset
BLTZALL	Branch On Less Than Zero And Link Likely	BLTZALL rs, offset
BGEZALL	Branch On Greater Than Or Equal To Zero And Link Likely	BGEZALL rs, offset
Exception instruction	SPECIAL | rs | rt | rd | sa | funct	
TGE	Trap If Greater Than Or Equal	TGE rs, rt
TGEU	Trap If Greater Than Or Equal Unsigned	TGEU rs, rt
TLT	Trap If Less Than	TLT rs, rt
TLTU	Trap If Less Than Unsigned	TLTU rs, rt
TEQ	Trap If Equal	TEQ rs, rt
TNE	Trap If Not Equal	TNE rs, rt
Exception immediate instruction	REGIMM | rs | sub | immediate	
TGEI	Trap If Greater Than Or Equal Immediate	TGEI rs, immediate
TGEIU	Trap If Greater Than Or Equal Immediate Unsigned	TGEIU rs, immediate
TLTI	Trap If Less Than Immediate	TLTI rs, immediate
TLTIU	Trap If Less Than Immediate Unsigned	TLTIU rs, immediate
TEQI	Trap If Equal Immediate	TEQI rs, immediate
TNEI	Trap If Not Equal Immediate	TNEI rs, immediate
Special instruction	SPECIAL | rs | rt | rd | sa | funct	
SYNC	Synchronize	SYNC
Coprocessor instruction	op | base | rt | offset	
LDCz	Load Doubleword To Coprocessor z	LDCz rt, offset (base)
SDCz	Store Doubleword From Coprocessor z	SDCz rt, offset (base)

Table 6-3. CPU Instruction Set: MIPS III

Instruction	Description	Format
Load/store instruction	op | base | rt | offset	
LD	Load Doubleword	LD rt, offset (base)
LDL	Load Doubleword Left	LDL rt, offset (base)
LDR	Load Doubleword Right	LDR rt, offset (base)
LLD	Load Linked Doubleword	LLD rt, offset (base)
LWU	Load Word Unsigned	LWU rt, offset (base)
SCD	Store Conditional Doubleword	SCD rt, offset (base)
SD	Store Doubleword	SD rt, offset (base)
SDL	Store Doubleword Left	SDL rt, offset (base)
SDR	Store Doubleword Right	SDR rt, offset (base)
ALU immediate instruction	op | rs | rt | immediate	
DADDI	Doubleword Add Immediate	DADDI rt, rs, immediate
DADDIU	Doubleword Add Immediate Unsigned	DADDIU rt, rs, immediate
3-operand type instruction	op | rs | rt | rd | sa | funct	
DADD	Doubleword Add	DADD rd, rs, rt
DADDU	Doubleword Add Unsigned	DADDU rd, rs, rt
DSUB	Doubleword Subtract	DSUB rd, rs, rt
DSUBU	Doubleword Subtract Unsigned	DSUBU rd, rs, rt
Shift instruction	op | rs | rt | rd | sa | funct	
DSLL	Doubleword Shift Left Logical	DSLL rd, rt, sa
DSRL	Doubleword Shfit Right Logical	DSRL rd, rt, sa
DSRA	Doubleword Shift Right Arithmetic	DSRA rd, rt, sa
DSLLV	Doubleword Shift Left Logical Variable	DSLLV rd, rt, rs
DSRLV	Doubleword Shift Right Logical Variable	DSRLV rd, rt, rs
DSRAV	Doubleword Shift Right Arithmetic Variable	DSRAV rd, rt, rs
DSLL32	Doubleword Shift Left Logical + 32	DSLL32 rd, rt, sa
DSRL32	Doubleword Shift Right Logical + 32	DSRL32 rd, rt, sa
DSRA32	Doubleword Shift Right Arithmetic +32	DSRA32 rd, rt, sa
Multiplication/division instruction	op | rs | rt | rd | sa | funct	
DMULT	Doubleword Multiply	DMULT rs, rt
DMULTU	Doubleword Multiply Unsigned	DMULTU rs, rt
DDIV	Doubleword Divide	DDIV rs, rt
DDIVU	Doubleword Divide Unsigned	DDIVU rs, rt

Table 6-4. CPU Instruction Set: MIPS IV

Instruction	Description	Format
3-operand type instruction	op | rs | rt | rd | sa | funct	
MOVN	Move Conditional On Not Zero	MOVN rd, rs, rt
MOVZ	Move Conditional On Zero	MOVZ rd, rs, rt
Prefetch instruction	op | base | hint | offset	
PREF	Prefetch	PREF hint, offset (base)

6.3 FPU Instruction Set List

All the FPU instructions are 32 bits long and located at a word boundary.

Tables 6-5 through 6-8 list the FPU instruction set.

Table 6-5. FPU Instruction Set: MIPS I

Instruction	Description	Format
Load/store instruction	op | base | ft | offset	
LWC1	Load Word To FPU	LWC1 ft, offset (base)
SWC1	Store Word From FPU	SWC1 ft, offset (base)
Transfer instruction	COP1 | sub | rt | fs | 0	
MTC1	Move Word To FPU	MTC1 rt, fs
MFC1	Move Word From FPU	MFC1 rt, fs
CTC1	Move Control Word To FPU	CTC1 rt, fs
CFC1	Move Control Word From FPU	CFC1 rt, fs
Conversion instruction	COP1 | fmt | 0 | fs | fd | funct	
CVT.S.fmt	Floating-point Convert To Single Floating-point Format	CVT.S.fmt fd, fs
CVT.D.fmt	Floating-point Convert To Double Floating-point Format	CVT.D.fmt fd, fs
CVT.W.fmt	Floating-point Convert To Single Fixed-point Format	CVT.W.fmt fd, fs
Operation instruction	COP1 | fmt | ft | fs | fd | funct	
ADD.fmt	Floating-point Add	ADD.fmt fd, fs, ft
SUB.fmt	Floating-point Subtract	SUB.fmt fd, fs, ft
MUL.fmt	Floating-point Multiply	MUL.fmt fd, fs, ft
DIV.fmt	Floating-point Divide	DIV.fmt fd, fs, ft
ABS.fmt	Floating-point Absolute Value	ABS.fmt fd, fs
MOV.fmt	Floating-point Move	MOV.fmt fd, fs
NEG.fmt	Floating-point Negate	NEG.fmt fd, fs
Compare instruction	COP1 | fmt | ft | fs | cc | 0 | funct	
C.cond.fmt	Floating-point Compare	C.cond.fmt cc, fs, ft
FPU branch instruction	COP1 | BC | cc | 0 | offset	
BC1T	Branch On FPU True	BC1T cc, offset
BC1F	Branch On FPU False	BC1F cc, offset

Table 6-6. FPU Instruction Set: MIPS II

Instruction	Description	Format
Load/store instruction	op | base | ft | offset	
LDC1	Load Doubleword To FPU	LDC1 ft, offset (base)
SDC1	Store Doubleword From FPU	SDC1 ft, offset (base)
Conversion instruction	COP1 | fmt | 0 | fs | fd | funct	
ROUND.W.fmt	Floating-point Round To Single Fixed-point Format	ROUND.W.fmt fd, fs
TRUNC.W.fmt	Floating-point Truncate To Single Fixed-point Format	TRUNC.W.fmt fd, fs
CEIL.W.fmt	Floating-point Ceiling To Single Fixed-point Format	CEIL.W.fmt fd, fs
FLOOR.W.fmt	Floating-point Floor To Single Fixed-point Format	FLOOR.W.fmt fd, fs
Operation instruction	COP1 | fmt | ft | fs | fd | funct	
SQRT.fmt	Floating-point Square Root	SQRT.fmt fd, fs
FPU branch instruction	COP1 | BC | cc | 0 | offset	
BC1TL	Branch On FPU True Likely	BC1TL cc, offset
BC1FL	Branch On FPU False Likely	BC1FL cc, offset

Table 6-7. FPU Instruction Set: MIPS III

Instruction	Description	Format
Transfer instruction	COP1 | sub | rt | fs | 0	
DMTC1	Doubleword Move To FPU	DMTC1 rt, fs
DMFC1	Doubleword Move From FPU	DMFC1 rt, fs
Conversion instruction	COP1 | fmt | 0 | fs | fd | funct	
CVT.S.fmt	Floating-point Convert To Single Floating-point Format	CVT.S.fmt fd, fs
CVT.D.fmt	Floating-point Convert To Double Floating-point Format	CVT.D.fmt fd, fs
CVT.L.fmt	Floating-point Convert To Long Fixed-point Format	CVT.L.fmt fd, fs
ROUND.L.fmt	Floating-point Round To Long Fixed-point Format	ROUND.L.fmt fd, fs
TRUNC.L.fmt	Floating-point Truncate To Long Fixed-point Format	TRUNC.L.fmt fd, fs
CEIL.L.fmt	Floating-point Ceiling To Long Fixed-point Format	CEIL.L.fmt fd, fs
FLOOR.L.fmt	Floating-point Floor To Long Fixed-point Format	FLOOR.L.fmt fd, fs

Table 6-8. FPU Instruction Set: MIPS IV

Instruction	Description	Format
Load index instruction	op | base | index | 0 | fd | funct	
LWXC1	Load Word Indexed To Floating-point	LWXC1 fd, index (base)
LDXC1	Load Doubleword Indexed To Floating-point	LDXC1 fd, index (base)
Store index instruction	op | base | index | fs | 0 | funct	
SWXC1	Store Word Indexed From Floating-point	SWXC1 fs, index (base)
SDXC1	Store Doubleword Indexed From Floating-point	SDXC1 fs, index (base)
Conversion instruction	COP1 | fmt | 0 | fs | fd | funct	
RECIP.fmt	Reciprocal Approximation	RECIP.fmt fd, fs
RSQRT.fmt	Reciprocal Square Root Approximation	RSQRT.fmt fd, fs
Multiplication instruction (1)	COP1 | fmt | ft | fs | fd | funct	
MSUB.fmt	Floating-point Multiply Subtract	MSUB.fmt fd, fr, fs, ft
NMSUB.fmt	Floating-point Negative Multiply Subtract	NMSUB.fmt fd, fr, fs, ft
MADD.fmt	Floating-point Multiply Add	MADD.fmt fd, fr, fs, ft
NMADD.fmt	Floating-point Negative Multiply Add	NMADD.fmt fd, fr, fs, ft
MOVN.fmt	Floating-point Move Conditional On Not Zero	MOVN.fmt fd, fs, ft
MOVZ.fmt	Floating-point Move Conditional On Zero	MOVZ.fmt fd, fs, ft
Operation instruction (2)	COP1 | fmt | cc | 0 | fs | fd | funct	
MOVF.fmt	Floating-point Move Conditional On FPU False	MOVF.fmt fd, fs, cc
MOVT.fmt	Floating-point Move Conditional On FPU True	MOVT.fmt fd, fs, cc
Compare instruction	COP1 | fmt | ft | fs | cc | 0 | funct	
C.cond.fmt	Floating-point Compare	C.cond.fmt cc, fs, ft
FPU branch instruction	COP1 | BC | cc | 0 | offset	
BC1T	Branch On FPU True	BC1T cc, offset
BC1F	Branch On FPU False	BC1F cc, offset
BC1TL	Branch On FPU True Likely	BC1TL cc, offset
BC1FL	Branch On FPU False Likely	BC1FL cc, offset
Conditional transfer instruction	op | rs | cc | tf | rd | funct	
MOVF	Move Conditional On FPU False	MOVF rd, rs, cc
MOVT	Move Conditional On FPU True	MOVT rd, rs, cc
Prefetch instruction	op | base | index | hint | 0 | funct	
PREFX	Prefetch Indexed	PREFX hint, index (base)

6.4 Delay of Instruction

(1) Delay of integer instructions

Table 6-9 shows execution delay of the integer instructions.

For details of each instruction, refer to **VR5000, VR10000 User's Manual – Instruction**.

Table 6-9. Integer Operation Instruction Delay Time

Instruction Type	Execution Unit	PClk	Repeat Rate	Remark
ADD, SET, SUB, Logical	ALU1, ALU2	1	1	
MFHI, MTHI, MFLO, MTLO		1	1	
Shift, LUI	ALU1	1	1	
Conditional Branch		1	1	
Conditional Move		1	1	
MULT	ALU2	5/6	6	Delay of LO/HI
MULTU		6/7	7	Delay of LO/HI
DMULT		9/10	10	Delay of LO/HI
DMULTU		10/11	11	Delay of LO/HI
DIV, DIVU		34/35	35	Delay of LO/HI
DDIV, DDIVU		66/67	67	Delay of LO/HI
Load (except for CP1 instruction)	Load/store	2	1	In the case of cache hit
Store		—	1	In the case of cache hit

(2) Delay of floating-point instructions

Table 6-10 shows the execution delay of the floating-point instruction.

For details of each instruction, refer to **VR5000, VR10000 User's Manual – Instruction**.

Table 6-10. Floating-Point Instruction Delay Time

Instruction Type	Execution Unit	PClk	Repeat Rate	Remark
MTC1, DMTC1	ALU1	3	1	
ADD, SUB, ABS, NEG, ROUND, TRUNC, CEIL, FLOOR, C.cond	Fp adder	2	1	
CVT.S.W, CVT.S.L		4	2	Average value of repeat rate
CVT (other than above)		2	1	
MUL	Fp multiplier	2	1	
MFC1, DMFC1		2	1	
Conditional MOVE/CVT.S.L		2	1	
DIV.S, RECIP.S		12	14	
DIV.D, RECIP.D		19	21	
SQRT.S		18	20	
SQRT.D		33	35	
RSQRT.S		30	20	
RSQRT.D		52	35	
MADD	Fp adder + Fp multiplier	2/4	1	"2" if other MADD instruction uses operation result
LWC1, LDC1, LWXC1, LDXC1	Load/store	3	1	In the case of cache hit

7. ELECTRICAL SPECIFICATIONS

(1) μPD30700RS-180 and 30700RS-200

Absolute Maximum Ratings (T_A = 25 °C)

Parameter	Symbol	Condition	Rating	Unit
Supply voltage	V_{DD}		–0.5 to +3.8	V
Input voltage	V_I		–0.5 to V_{DD} + 0.3	V
		Pulse of less than 10 ns	–1.5 to V_{DD} + 0.3	V
Storage temperature	T_{stg}		–40 to +125	°C

Cautions 1. Do not short-circuit two or more outputs at the same time.

2. If any of the parameters exceeds the absolute maximum ratings, even momentarily, the quality of the product may be impaired. The absolute maximum ratings are values that may physically damage the product(s). Use the product(s) with these rated values never exceeded. The specifications and conditions shown in DC Characteristics and AC Characteristics below are the range in which the product(s) operate normally and the quality of the product is guaranteed.

Operating Case Temperature (V_{DD} = 3.3 V ±0.165 V)

Parameter	Symbol	Condition	Rating	Unit
Operating case temperature	T_C		0 to 70	°C

DC Characteristics (T_C = 0 to 70 °C, V_{DD} = 3.3 V ±0.165 V)

(a) Common to CMOS/TTL and HSTL

Parameter	Symbol	Condition	MIN.	MAX.	Unit
Input capacitance	C_{in}			5	pF
Output capacitance	C_{out}			7	pF
Power consumption	P_D	200 MHz (V_{DD} = 3.3 V)		30	W
		180 MHz (V_{DD} = 3.3 V)		27	W
Input leakage power	I_{LI}			±10	μA
I/O leakage current	I_{LIO}			±10	μA

(b) CMOS/TTL

Parameter	Symbol	Condition	MIN.	MAX.	Unit
Output supply voltage[Note 1]	V_{DDQ}	$V_{DDQ} = V_{DD}$	3.135	3.465	V
Input supply voltage[Note 2]	V_{REF}		1.2	1.6	V
High-level output voltage	V_{OH}	V_{DD} = MIN., I_{OH} = –4 mA	2.4		V
Low-level output voltage	V_{OL}	V_{DD} = MAX., I_{OL} = 4 mA		0.4	V
High-level input voltage	V_{IH}		2.0	V_{DD} + 0.3	V
Low-level input voltage	V_{IL}		–0.5	+0.8	V

Notes 1. V_{DDQ} is applied to the V_{DD}QSC and V_{DD}QSys pins.

2. V_{REF} is applied to the V_{ref}SC and V_{ref}Sys pins.

(c) HSTL

Parameter	Symbol	Condition	MIN.	MAX.	Unit
Output supply voltage[Note 1]	V_{DDQ}		1.4	1.6	V
Input supply voltage[Note 2]	V_{REF}		0.65	0.75	V
High-level output threshold voltage[Note 3]	V_{OH}	I_{OH} = –4 mA	V_{DDQ}/2 + 0.3		V
Low-level output threshold voltage[Note 3]	V_{OL}	I_{OL} = 4 mA		V_{DDQ}/2 – 0.3	V
High-level differential input threshold voltage 1[Note 4]	V_{IH}		V_{REF} + 0.1	V_{DD} + 0.3	V
Low-level differential input threshold voltage 1[Note 4]	V_{IL}		–0.3	V_{DD} – 0.1	V
High-level differential input threshold voltage 2[Note 5]	V_{DIH}		V_{DIL} + 0.8	V_{DD} + 0.3	V
Low-level differential input threshold voltage 2[Note 5]	V_{DIL}		–0.3	V_{DIH} – 0.8	V

Notes 1. V_{DDQ} is applied to the V_{DD}QSC and V_{DD}QSys pins.

2. V_{REF} is applied to the V_{ref}SC and V_{ref}Sys pins.

3. The V_R10000 supports 1a and 1b of the HSTL specifications of SGI.

4. Applied to the input pins other than SysClk and $\overline{\text{SysClk}}$.

5. Applied to the SysClk and $\overline{\text{SysClk}}$ pins.

AC Characteristics (T_C = 0 to 70 °C, V_{DD} = 3.3 V ±0.165 V)

Clock parameter

Parameter	Symbol	Condition	MIN.	MAX.	Unit
System clock high-level width	t_{CH}	t_{CR}, t_{CF} ≤ 2.0 ns	0.5		ns
System clock low-level width	t_{CL}	t_{CR}, t_{CF} ≤ 2.0 ns	0.5		ns
System clock frequency[Notes 1,2]		200-MHz model	50	200	MHz
		180-MHz model	45	180	MHz
System clock cycle[Notes 1,2]	t_{CP}	200-MHz model	5	20	ns
		180-MHz model	5.56	22.2	ns
Input system clock jitter	t_{ji}			±125	ps
Output system clock jitter[Note 3]	t_{jo}			±500	ps
System clock rise time	t_{CR}			2.0	ns
System clock fall time	t_{CF}			2.0	ns

Notes 1. The operation of the V_R10000 is guaranteed only when PLL operates.

2. The operation is guaranteed when the internal operating frequency is 100 MHz or higher.

3. Changes between clock edges are undefined.

System Interface Parameter

(a) CMOS/TTL

Parameter	Symbol	Condition	MIN.	MAX.	Unit
Data output delay time	t_{DO}			2.0	ns
Data input setup time	t_{DS}		1.0		ns
Data input hold time	t_{DH}		1.0		ns

(b) HSTL

Parameter	Symbol	Condition	MIN.	MAX.	Unit
Data output delay time	t_{DO}			1.5	ns
Data input setup time	t_{DS}		1.0		ns
Data input hold time	t_{DH}		1.0		ns

Secondary Cache Tag Interface Parameter

Applied to SCTag (25:0) and SCTagChk (6:0)

(a) CMOS/TTL

Parameter	Symbol	Condition	MIN.	MAX.	Unit
Data output delay time	t_{SDO}			2.0	ns
Data input setup time	t_{SDS}		1.5		ns
Data input hold time	t_{SDH}		0.5		ns

(b) HSTL

Parameter	Symbol	Condition	MIN.	MAX.	Unit
Data output delay time	t_{SDO}			1.5	ns
Data input setup time	t_{SDS}		1.5		ns
Data input hold time	t_{SDH}		0.5		ns

(2) μPD30700LRS-225 and 30700LRS-250 (preliminary)

Absolute Maximum Ratings (T_A = 25 °C)

Parameter	Symbol	Condition	Rating	Unit
Supply voltage	V_{DD}		–0.5 to +3.3	V
Input voltage	V_I		–0.5 to V_{DD} + 0.3	V
		Pulse of less than 10 ns	–1.5 to V_{DD} + 0.3	V
Storage temperature	T_{stg}		–40 to +125	°C

Cautions 1. Do not short-circuit two or more outputs at the same time.

2. If any of the parameters exceeds the absolute maximum ratings, even momentarily, the quality of the product may be impaired. The absolute maximum ratings are values that may physically damage the product(s). Use the product(s) with these rated values never exceeded. The specifications and conditions shown in DC Characteristics and AC Characteristics below are the range in which the product(s) operate normally and the quality of the product is guaranteed.

Operating Case Temperature (V_{DD} = 2.6 V ±0.1 V)

Parameter	Symbol	Condition	Rating	Unit
Operating case temperature	T_C		0 to 70	°C

DC Characteristics (T_C = 0 to 70 °C, V_{DD} = 2.6 V ±0.1 V)

(a) Common to CMOS/TTL and HSTL

Parameter	Symbol	Condition	MIN.	MAX.	Unit
Input capacitance	C_{in}			5	pF
Output capacitance	C_{out}			7	pF
Power consumption	P_D	250 MHz (V_{DD} = 2.6 V)		20	W
		225 MHz (V_{DD} = 2.6 V)		17	W
Input leakage power	I_{LI}			±10	μA
I/O leakage current	I_{LIO}			±10	μA

(b) CMOS/TTL

Parameter	Symbol	Condition	MIN.	MAX.	Unit
Output supply voltage[Note 1]	V_{DDQ}	$V_{DDQ} = V_{DD}$	2.5	2.7	V
Input supply voltage[Note 2]	V_{REF}		1.2	1.6	V
High-level output voltage	V_{OH}	V_{DD} = MIN., I_{OH} = –4 mA	2.4		V
Low-level output voltage	V_{OL}	V_{DD} = MAX., I_{OL} = 4 mA		0.4	V
High-level input voltage	V_{IH}		2.0	V_{DD} + 0.3	V
Low-level input voltage	V_{IL}		–0.5	+0.8	V

Notes 1. V_{DDQ} is applied to the V_{DD}QSC and V_{DD}QSys pins.

2. V_{REF} is applied to the V_{ref}SC and V_{ref}Sys pins.

(c) HSTL

Parameter	Symbol	Condition	MIN.	MAX.	Unit
Output supply voltage[Note 1]	V_{DDQ}		1.4	1.6	V
Input supply voltage[Note 2]	V_{REF}		0.65	0.75	V
High-level output threshold voltage[Note 3]	V_{OH}	I_{OH} = –4 mA	V_{DDQ}/2 + 0.3		V
Low-level output threshold voltage[Note 3]	V_{OL}	I_{OL} = 4 mA		V_{DDQ}/2 – 0.3	V
High-level differential input threshold voltage 1[Note 4]	V_{IH}		V_{REF} + 1	V_{DD} + 0.3	V
Low-level differential input threshold voltage 1[Note 4]	V_{IL}		–0.3	V_{DD} – 0.1	V
High-level differential input threshold voltage 2[Note 5]	V_{DIH}		V_{DIL} + 0.8	V_{DD} + 0.3	V
Low-level differential input threshold voltage 2[Note 5]	V_{DIL}		–0.3	V_{DIH} – 0.8	V

Notes 1. V_{DDQ} is applied to the V_{DD}QSC and V_{DD}QSys pins.

2. V_{REF} is applied to the V_{ref}SC and V_{ref}Sys pins.

3. The V_R10000 supports 1a and 1b of the HSTL specifications of SGI.

4. Applied to the input pins other than SysClk and $\overline{\text{SysClk}}$.

5. Applied to the SysClk and $\overline{\text{SysClk}}$ pins.

AC Characteristics (T_C = 0 to 70 °C, V_{DD} = 2.6 V ±0.1 V)

Clock parameter

Parameter	Symbol	Condition	MIN.	MAX.	Unit
System clock high-level width	t_{CH}	t_{CR}, t_{CF} ≤ 2.0 ns	0.5		ns
System clock low-level width	t_{CL}	t_{CR}, t_{CF} ≤ 2.0 ns	0.5		ns
System clock frequency[Notes 1, 2]		250-MHz model	62.5	250	MHz
		225-MHz model	56.3	225	MHz
System clock cycle[Notes 1, 2]	t_{CP}	250-MHz model	4	16	ns
		225-MHz model	4.44	17.8	ns
Input system clock jitter	t_{ji}			±125	ps
Output system clock jitter[Note 3]	t_{jo}			±500	ps
System clock rise time	t_{CR}			2.0	ns
System clock fall time	t_{CF}			2.0	ns

Notes 1. The operation of the V_R10000 is guaranteed only when PLL operates.

2. The operation is guaranteed when the internal operating frequency is 100 MHz or higher.

3. Changes between clock edges are undefined.

System Interface Parameter

(a) CMOS/TTL

Parameter	Symbol	Condition	MIN.	MAX.	Unit
Data output delay time	t_{DO}			2.0	ns
Data input setup time	t_{DS}		1.0		ns
Data input hold time	t_{DH}		1.0		ns

(b) HSTL

Parameter	Symbol	Condition	MIN.	MAX.	Unit
Data output delay time	t_{DO}			1.5	ns
Data input setup time	t_{DS}		1.0		ns
Data input hold time	t_{DH}		1.0		ns

Secondary Cache Tag Interface Parameter

Applied to SCTag (25:0) and SCTagChk (6:0)

(a) CMOS/TTL

Parameter	Symbol	Condition	MIN.	MAX.	Unit
Data output delay time	t_{SDO}			2.0	ns
Data input setup time	t_{SDS}		1.5		ns
Data input hold time	t_{SDH}		0.5		ns

(b) HSTL

Parameter	Symbol	Condition	MIN.	MAX.	Unit
Data output delay time	t_{SDO}			1.5	ns
Data input setup time	t_{SDS}		1.5		ns
Data input hold time	t_{SDH}		0.5		ns

(3) μPD30710RS-300 (preliminary)

Absolute Maximum Ratings (T_A = 25 °C)

Parameter	Symbol	Condition	Rating	Unit
Supply voltage	V_{DD}		–0.5 to +3.3	V
Input voltage	V_I		–0.5 to V_{DD} + 0.3	V
		Pulse of less than 10 ns	–1.5 to V_{DD} + 0.3	V
Storage temperature	T_{stg}		–40 to +125	°C

Cautions 1. Do not short-circuit two or more outputs at the same time.

2. If any of the parameters exceeds the absolute maximum ratings, even momentarily, the quality of the product may be impaired. The absolute maximum ratings are values that may physically damage the product(s). Use the product(s) with these rated values never exceeded. The specifications and conditions shown in DC Characteristics and AC Characteristics below are the range in which the product(s) operate normally and the quality of the product is guaranteed.

Operating Case Temperature (V_{DD} = 2.6 V ±0.1 V)

Parameter	Symbol	Condition	Rating	Unit
Operating case temperature	T_C		25 to 70	°C

DC Characteristics (T_C = 25 to 70 °C, V_{DD} = 2.6 V ±0.1 V)

(a) Common to CMOS/TTL and HSTL

Parameter	Symbol	Condition	MIN.	MAX.	Unit
Input capacitance	C_{in}			5	pF
Output capacitance	C_{out}			7	pF
Power consumption	P_D	300 MHz (V_{DD} = 2.6 V)		30	W
Input leakage power	I_{LI}			±10	μA
I/O leakage current	I_{LIO}			±10	μA

(b) CMOS/TTL

Parameter	Symbol	Condition	MIN.	MAX.	Unit
Output supply voltage[Note 1]	V_{DDQ}	$V_{DDQ} = V_{DD}$	2.5	2.7	V
Input supply voltage[Note 2]	V_{REF}		1.2	1.6	V
High-level output voltage	V_{OH}	V_{DD} = MIN., I_{OH} = –4 mA	2.4		V
Low-level output voltage	V_{OL}	V_{DD} = MAX., I_{OL} = 4 mA		0.4	V
High-level input voltage	V_{IH}		2.0	V_{DD} + 0.3	V
Low-level input voltage	V_{IL}		–0.5	+0.8	V

Notes 1. V_{DDQ} is applied to the V_{DD}QSC and V_{DD}QSys pins.

2. V_{REF} is applied to the V_{ref}SC and V_{ref}Sys pins.

(c) HSTL

Parameter	Symbol	Condition	MIN.	MAX.	Unit
Output supply voltage[Note 1]	V_{DDQ}		1.4	1.6	V
Input supply voltage[Note 2]	V_{REF}		0.65	0.75	V
High-level output threshold voltage[Note 3]	V_{OH}	I_{OH} = –4 mA	V_{DDQ}/2 + 0.3		V
Low-level output threshold voltage[Note 3]	V_{OL}	I_{OL} = 4 mA		V_{DDQ}/2 – 0.3	V
High-level differential input threshold voltage 1[Note 4]	V_{IH}		V_{REF} + 0.1	V_{DD} + 0.3	V
Low-level differential input threshold voltage 1[Note 4]	V_{IL}		–0.3	V_{DD} – 0.1	V
High-level differential input threshold voltage 2[Note 5]	V_{DIH}		V_{DIL} + 0.8	V_{DD} + 0.3	V
Low-level differential input threshold voltage 2[Note 5]	V_{DIL}		–0.3	V_{DIH} – 0.8	V

Notes 1. V_{DDQ} is applied to the V_{DD}QSC and V_{DD}QSys pins.

2. V_{REF} is applied to the V_{ref}SC and V_{ref}Sys pins

3. The V_R12000 supports 1a and 1b of the HSTL specifications of SGI.

4. Applied to the input pins other than SysClk and $\overline{\text{SysClk}}$.

5. Applied to the SysClk and $\overline{\text{SysClk}}$ pins.

AC Characteristics (T_C = 25 to 70 °C, V_{DD} = 2.6 V ±0.1 V)

Clock parameter

Parameter	Symbol	Condition	MIN.	MAX.	Unit
System clock high-level width	t_{CH}	t_{CR}, t_{CF} ≤ 2.0 ns	0.5		ns
System clock low-level width	t_{CL}	t_{CR}, t_{CF} ≤ 2.0 ns	0.5		ns
System clock frequency[Notes 1, 2]		300-MHz model	30	300	MHz
System clock cycle[Notes 1, 2]	t_{CP}	300-MHz model	3.33	33.3	ns
Input system clock jitter	t_{ji}			±125	ps
Output system clock jitter[Note 3]	t_{jo}			±500	ps
System clock rise time	t_{CR}			2.0	ns
System clock fall time	t_{CF}			2.0	ns

Notes 1. The operation of the V_R12000 is guaranteed only when PLL operates.

2. The operation is guaranteed when the internal operating frequency is 100 MHz or higher.

3. Changes between clock edges are undefined.

System Interface Parameter

(a) CMOS/TTL

Parameter	Symbol	Condition	MIN.	MAX.	Unit
Data output delay time	t_{DO}			2.0	ns
Data input setup time	t_{DS}		1.0		ns
Data input hold time	t_{DH}		1.0		ns

(b) HSTL

Parameter	Symbol	Condition	MIN.	MAX.	Unit
Data output delay time	t_{DO}			1.5	ns
Data input setup time	t_{DS}		1.0		ns
Data input hold time	t_{DH}		1.0		ns

Secondary Cache Tag Interface Parameter

Applied to SCTag (25:0) and SCTagChk (6:0)

(a) CMOS/TTL

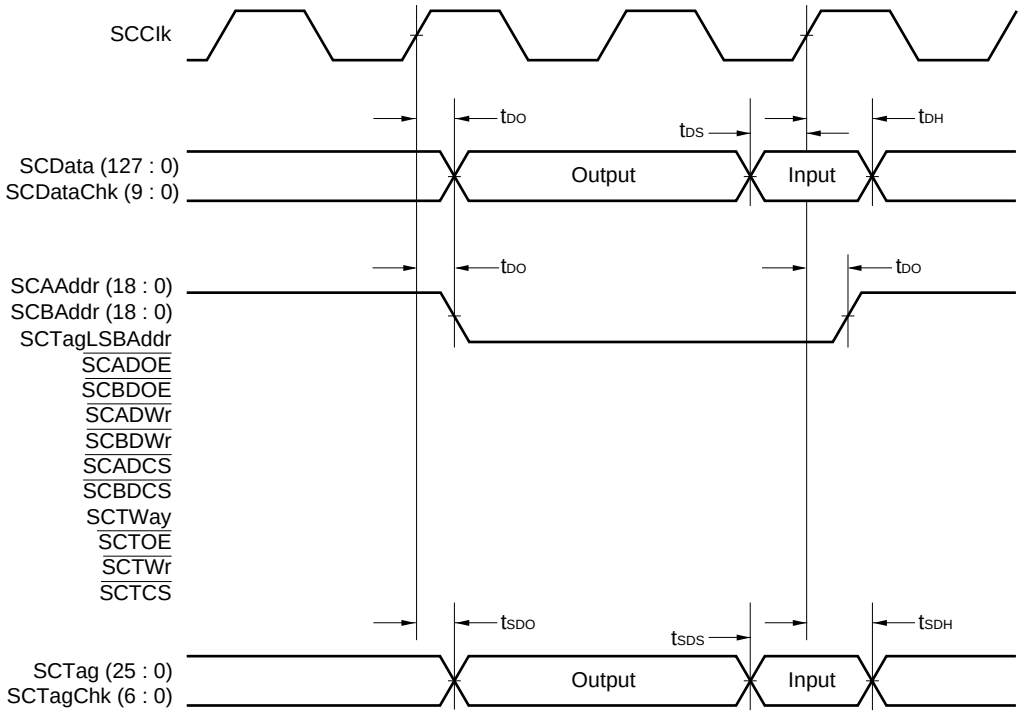
Parameter	Symbol	Condition	MIN.	MAX.	Unit
Data output delay time	t_{SDO}			2.0	ns
Data input setup time	t_{SDS}		1.5		ns
Data input hold time	t_{SDH}		0.5		ns

(b) HSTL

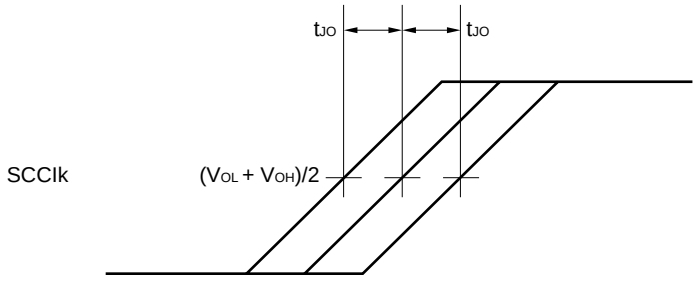
Parameter	Symbol	Condition	MIN.	MAX.	Unit
Data output delay time	t_{SDO}			1.5	ns
Data input setup time	t_{SDS}		1.5		ns
Data input hold time	t_{SDH}		0.5		ns

Timing Chart

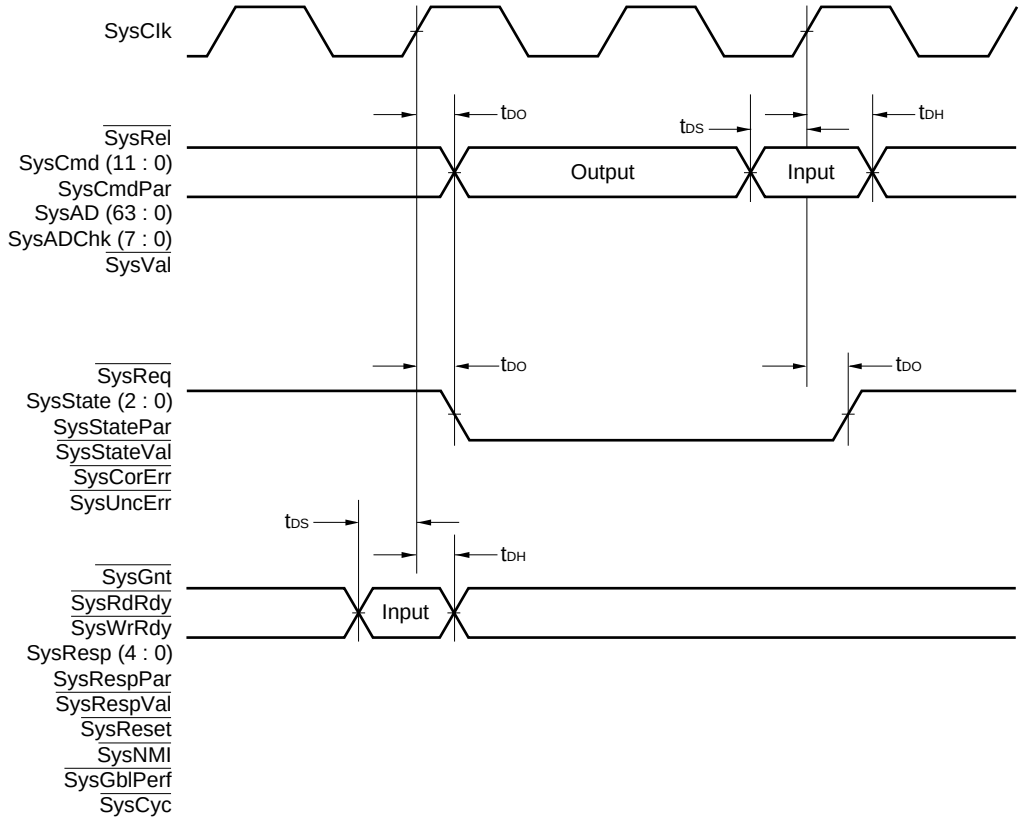
Secondary Cache Interface Timing



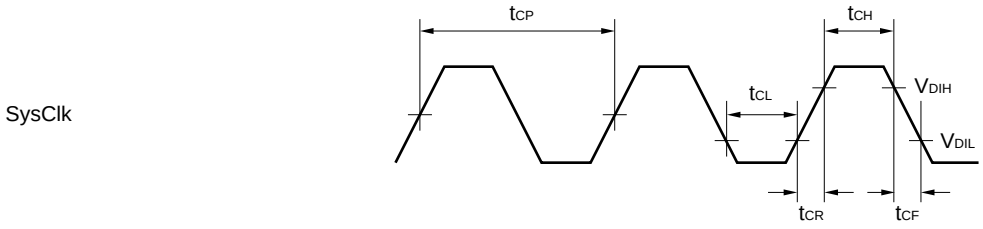
Secondary cache clock jitter



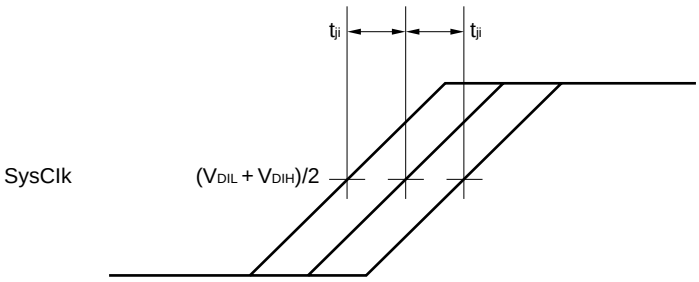
System Interface Timing



System Clock



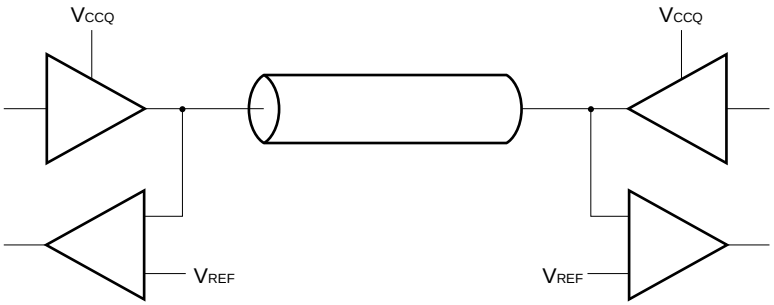
System Clock Jitter



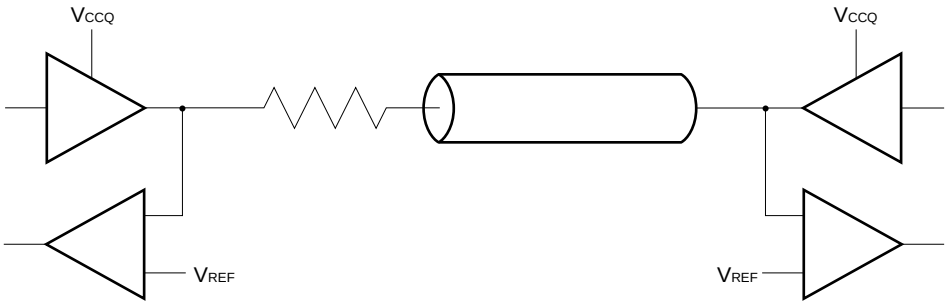
8. PUSH-PULL OUTPUT BUFFER CIRCUIT

The configuration of the push-pull output buffer circuit is shown below.

Push-pull output buffer circuit (without load of termination)

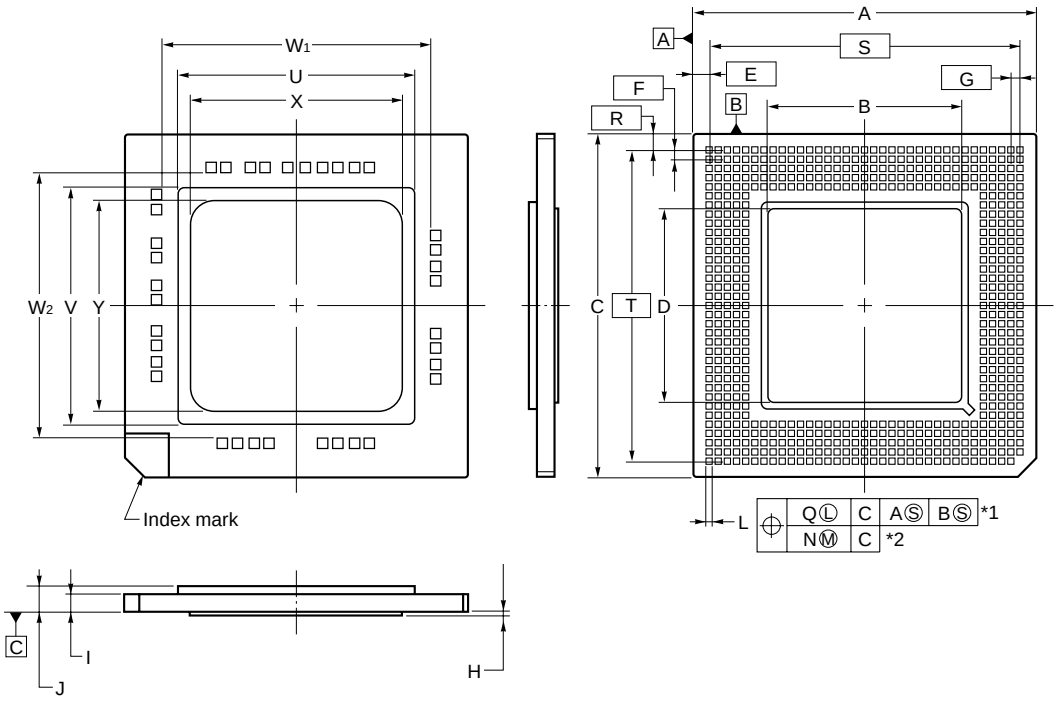


Push-pull output buffer circuit (with load of termination)



9. PACKAGE DRAWING

599 PIN CERAMIC LGA



NOTE

*1 Each land centerline is located within 0.30 mm (0.012 inch) of its true position (T.P.) at least material condition.

*2 Each land centerline is located within 0.20 mm (0.008 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	47.50±0.25	1.870±0.010
B	29.00	1.142
C	47.50±0.25	1.870±0.010
D	29.00	1.142
E	2.16	0.085
F	1.27 (T.P.)	0.050 (T.P.)
G	1.27 (T.P.)	0.050 (T.P.)
H	0.70 MAX.	0.028 MAX.
I	2.54±0.25	0.100±0.010
J	3.81±0.38	0.150±0.015
L	□0.76±0.13	$\square 0.030^{+0.005}_{-0.006}$
N	0.20	0.008
Q	0.30	0.012
R	2.16	0.085
S	43.18	1.700
T	43.18	1.700
U	32.54	1.281
V	32.54	1.281
W_1	37.00	1.457
W_2	37.00	1.457
X	30.00	1.181
Y	30.00	1.181

X599RS-50A

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note: Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note: No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS device behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note: Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

Regional Information

Some information contained in this document may vary from country to country. Before using any NEC product in your application, please contact the NEC office in your country to obtain a list of authorized representatives and distributors. They will verify:

- Device availability
- Ordering information
- Product release schedule
- Availability of related technical literature
- Development environment specifications (for example, specifications for third-party tools and components, host computers, power plugs, AC supply voltages, and so forth)
- Network requirements

In addition, trademarks, registered trademarks, export restrictions, and other legal issues may also vary from country to country.

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Related Documents: VR10000, VR12000 User's Manual (U10278E)
VR5000, VR10000 User's Manual - Instruction (U12754E)

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