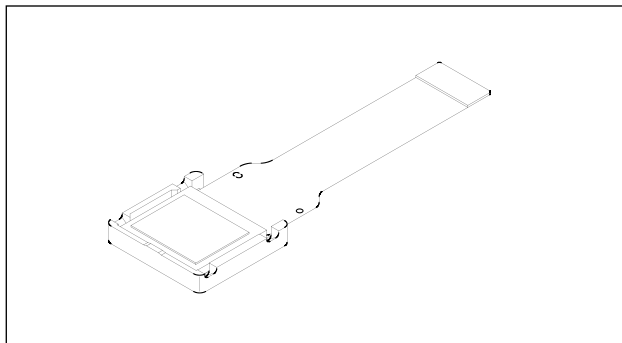


1.1cm (0.44 Type) NTSC/PAL Color LCD Panel

Description

The LCX032ANB is a 1.1cm diagonal active matrix TFT-LCD panel addressed by polycrystalline silicon super thin film transistors with built-in peripheral driving circuit. This panel provides full-color representation in NTSC/PAL mode. RGB dots are arranged in a delta pattern featuring high picture quality of no fixed color patterns, which is inherent in vertical stripes and mosaic pattern arrangements.



Features

- The number of active dots: 113,578 (0.44 Type; 1.1cm in diagonal)
- Horizontal resolution: 260 TV lines
- High optical transmittance: 4.8% (typ.)
- High contrast ratio with normally white mode: 200 (typ.)
- Built-in H and V drivers (built-in input level conversion circuit, TTL drive possible)
- High quality picture representation with RGB delta arranged color filters
- Full-color representation
- NTSC/PAL compatible
- Up/down and/or right/left inverse display function
- 4:3 and 16:9 aspect switching function
- Power save mode (Through current reduction by stop of level shifter and scanner during power supply cutoff)

Element Structure

• Dots

Total dots : 537 (H) × 222 (V) = 119,214

Active dots: 521 (H) × 218 (V) = 113,578

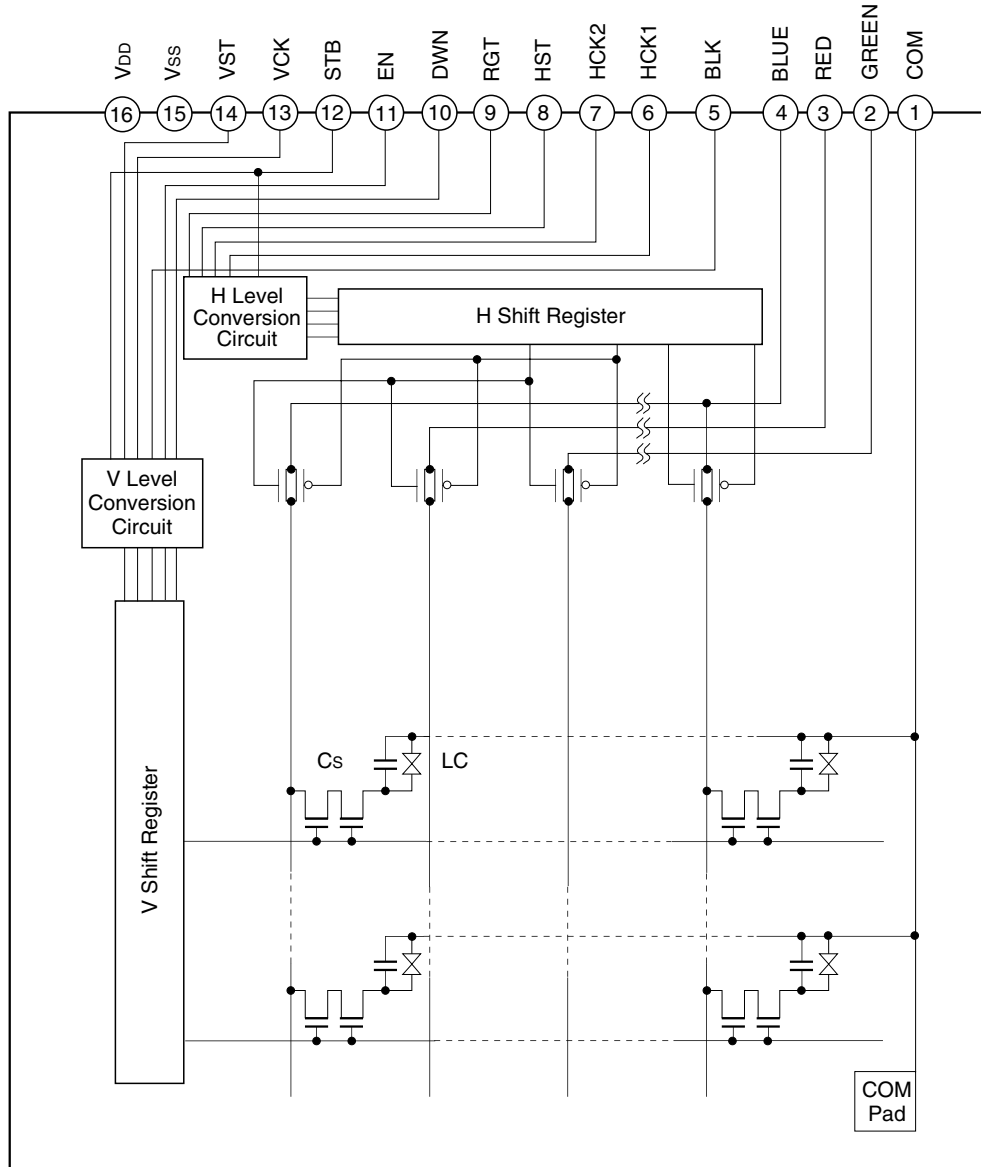
- Built-in peripheral driver using polycrystalline silicon super thin film transistors.

Applications

- Viewfinders
- Super compact liquid crystal monitors etc.

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Block Diagram



Absolute Maximum Ratings ($V_{SS} = 0V$)

| | | | |
|-------------------------------------|---------------------------|-------------|----|
| • H and V driver supply voltages | V_{DD} | -1.0 to +17 | V |
| • Common pad voltage | COM | -1.0 to +17 | V |
| • H driver input pin voltage | HST, HCK1, HCK2 RGT | -1.0 to +17 | V |
| • V driver input pin voltage | VST, VCK, DWN, EN, BLK | -1.0 to +17 | V |
| • Power save mode input pin voltage | STB | -1.0 to +17 | V |
| • Video signal input pin voltage | GREEN, RED, BLUE | -1.0 to +15 | V |
| • Operating temperature | T_{opr} | -10 to +70 | °C |
| • Storage temperature | T_{stg} | -30 to +85 | °C |

Operating Conditions ($V_{SS} = 0V$)

Supply voltage

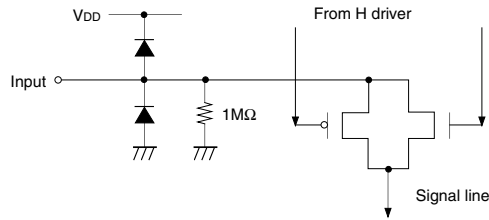
 V_{DD} 11.4 to 14.0 VInput pulse voltage (V_{p-p} of all input pins except video signal input pins) V_{in} 2.6V (more than)**Pin Description**

| Pin No. | Symbol | Description | Pin No. | Symbol | Description |
|---------|--------|--|---------|----------|--|
| 1 | COM | Common voltage of panel | 9 | RGT | Drive direction pulse for H shift register (H: normal, L: reverse) |
| 2 | GREEN | Video signal (G) to panel | 10 | DWN | Drive direction pulse for V shift register (H: normal, L: reverse) |
| 3 | RED | Video signal (R) to panel | 11 | EN | Enable pulse for gate selection |
| 4 | BLUE | Video signal (B) to panel | 12 | STB | For power save mode control (L-power save mode) |
| 5 | BLK | Top/bottom block display pulse | 13 | VCK | Clock pulse for V shift register drive |
| 6 | HCK1 | Clock pulse for H shift register drive | 14 | VST | Start pulse for V shift register drive |
| 7 | HCK2 | Clock pulse for H shift register drive | 15 | V_{SS} | GND (H, V drivers) |
| 8 | HST | Start pulse for H shift register drive | 16 | V_{DD} | Power supply for H and V drivers |

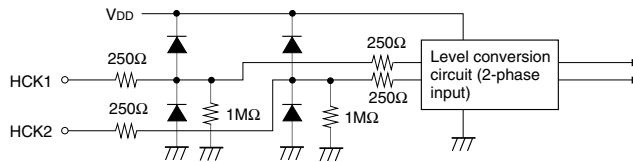
Input Equivalent Circuit

To prevent static charges, protective diodes are provided for each pin except the power supply. In addition, protective resistors are added to all pins except video signal input. All pins are connected to Vss with a high resistance of 1MΩ (typ.). The equivalent circuit of each input pin is shown below: (The resistor value: typ.)

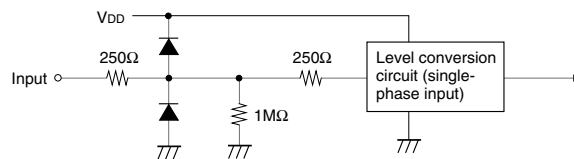
(1) Video signal input



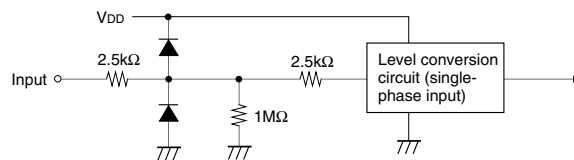
(2) HCK1, HCK2



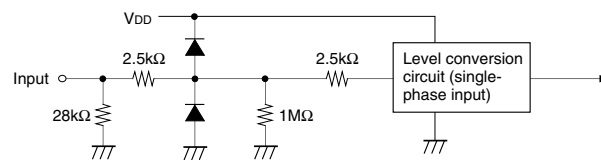
(3) HST



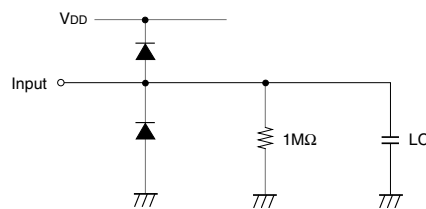
(4) RGT, VST, EN, VCK, DWN, STB



(5) BLK



(6) COM



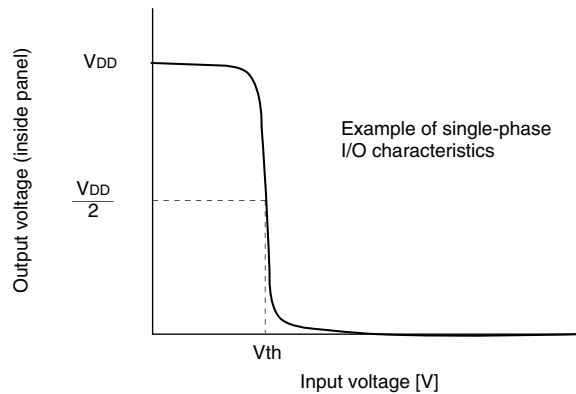
Level Conversion Circuit

The LCX032ANB has a built-in level conversion circuit in the clock input unit located inside the panel. The circuit voltage is stepped up to V_{DD} inside the panel. This level conversion circuit meets the specifications of a 3.0V power supply of the externally-driven IC.

1. I/O characteristics of level conversion circuit

(For a single-phase input unit)

An example of the I/O voltage characteristics of a level conversion circuit is shown in the figure to the right. The input voltage value that becomes half the output voltage (after voltage conversion) is defined as V_{th} . The V_{th} value varies depending on the V_{DD} voltage. The V_{th} values under standard conditions are indicated in the table below. (HST, VST, EN, DWN, STB, RGT, VCK and BLK in the case of a single-phase input)

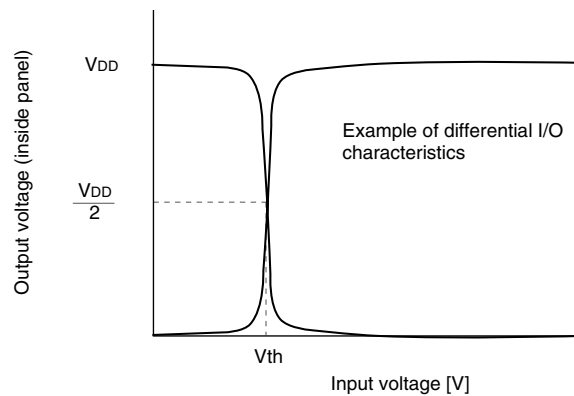


$V_{DD} = 12.0V$

| Item | Symbol | Min. | Typ. | Max. | Unit |
|------------------------|--------|------|------|------|------|
| Vth voltage of circuit | Vth | 0.35 | 1.50 | 2.60 | V |

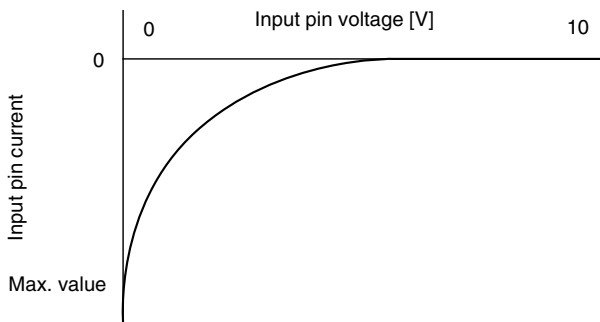
(For a differential input unit)

An example of I/O voltage characteristics of a level conversion circuit for a differential input is shown in the figure to the right. Although the characteristics, including those of the V_{th} voltage, are basically the same as those for a single-phased input, the two-phased input phase is defined. (Refer to clock timing conditions.)

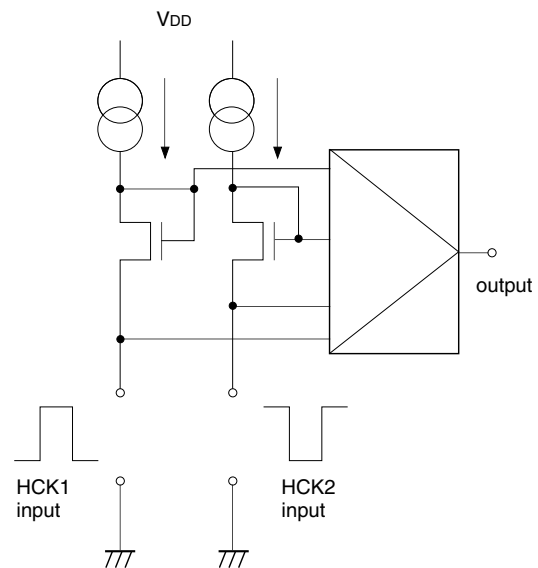


2. Current characteristics at the input pin of level conversion circuit

A slight pull-in current is generated at the input pin of the level conversion circuit. (The equivalent circuit is shown to the right.) The current volume increases as the voltage at the input pin decreases, and is maximized when the pin is grounded. (Refer to electrical characteristics.)



Pull-in current characteristics at the input pin



Level conversion equivalent circuit

2. Clock timing conditions (Ta = 25°C, Input voltage = 3.0V, VDD = 12.0V)

| | Item | Symbol | Min. | Typ. | Max. | Unit |
|-------------------|-------------------------------|--------|------|------|------|------|
| HST | Hst rise time | trHst | | | 30 | ns |
| | Hst fall time | tfHst | | | 30 | |
| | Hst data set-up time | tdHst | -170 | 135 | 200 | |
| | Hst data hold time | thHst | -455 | -135 | -50 | |
| HCK | Hckn* ² rise time | trHckn | | | 30 | |
| | Hckn* ² fall time | tfHckn | | | 30 | |
| | Hck1 fall to Hck2 rise time | to1Hck | -15 | 0 | 15 | |
| | Hck1 rise to Hck2 fall time | to2Hck | -15 | 0 | 15 | |
| VST | Vst rise time | trVst | | | 100 | μs |
| | Vst fall time | tfVst | | | 100 | |
| | Vst data set-up time | tdVst | -50 | 32 | 50 | |
| | Vst data hold time | thVst | -50 | -32 | -20 | |
| VCK | Vck rise time | trVck | | | 100 | ns |
| | Vck fall time | tfVck | | | 100 | |
| EN | En rise time | trEn | | | 100 | |
| | En fall time | tfEn | | | 100 | |
| | En fall to Vck rise/fall time | toVck | 100 | 3000 | 3500 | |
| | Vck rise/fall to En rise time | tdVck | 100 | 500 | 1000 | |
| BLK* ³ | Blk rise time | trBlk | | | 100 | ms |
| | Blk fall time | tfBlk | | | 100 | |
| | Blk pulse width | twBlk | | 1.0 | | ns |
| | Blk fall to En rise time | tdEnb | 600 | 700 | 800 | |

*² Hckn means Hck1, Hck2. (fHckn = 1.84MHz, fVckn = 7.865kHz)

*³ BLK pulse is used only for 16:9 mode. For 4:3 mode, connect to Vss.

<Horizontal Shift Register Driving Waveform>

| Item | | Symbol | Waveform | Conditions |
|------|-----------------------------|--------|----------|--|
| HST | Hst rise time | trHst | | <ul style="list-style-type: none"> • Hckn*2 duty cycle 50% to1Hck = 0ns to2Hck = 0ns |
| | Hst fall time | tfHst | | |
| | Hst data set-up time | tdHst | | <ul style="list-style-type: none"> • Hckn*2 duty cycle 50% to1Hck = 0ns to2Hck = 0ns |
| | Hst data hold time | thHst | | |
| HCK | Hckn*2 rise time | trHckn | | <ul style="list-style-type: none"> • Hckn*2 duty cycle 50% to1Hck = 0ns to2Hck = 0ns tdHst = 135ns thHst = -135ns |
| | Hckn*2 fall time | tfHckn | | |
| | Hck1 fall to Hck2 rise time | to1Hck | | <ul style="list-style-type: none"> • tdHst = 135ns thHst = -135ns |
| | Hck1 rise to Hck2 fall time | to2Hck | | |

<Vertical Shift Register Driving Waveform>

| Item | | Symbol | Waveform | Conditions |
|------|-------------------------------|--------|----------|---|
| VST | Vst rise time | trVst | | <ul style="list-style-type: none"> • VCK duty cycle 50% |
| | Vst fall time | tfVst | | |
| | Vst data set-up time | tdVst | | <ul style="list-style-type: none"> • VCK duty cycle 50% |
| | Vst data hold time | thVst | | |
| VCK | Vck rise time | trVck | | <ul style="list-style-type: none"> • VCK duty cycle 50% tdVst = 32μs thVst = -32μs |
| | Vck fall time | tfVck | | |
| EN | En rise time | trEn | | <ul style="list-style-type: none"> • VCK duty cycle 50% |
| | En fall time | tfEn | | |
| | En fall to Vck rise/fall time | toVck | | <ul style="list-style-type: none"> • VCK duty cycle 50% |
| | Vck rise/fall to En rise time | tdVck | | |
| BLK | Blk rise time | trBlk | | |
| | Blk fall time | tfBlk | | |
| | Blk pulse width | twBlk | | |
| | Blk fall to En rise time | tdEnb | | |

*4 Definitions: The right-pointing arrow ($\bullet \rightarrow$) means +.
 The left-pointing arrow ($\leftarrow \bullet$) means -.
 The black dot at an arrow (\bullet) indicates the start of measurement.

Electrical Characteristics

(Ta = 25°C, VDD = 12.0V, Input voltage = 3.0V)

1. Horizontal drivers

| Item | Symbol | Min. | Typ. | Max. | Unit | Condition |
|------------------------------------|--------|------|------|------|------|------------|
| Input pin capacitance | HCKn | | 5 | 10 | pF | |
| | HST | | 5 | 10 | pF | |
| Input pin current | HCK1 | -500 | -250 | | μA | HCK1 = GND |
| | HCK2 | -500 | -250 | | μA | HCK2 = GND |
| | HST | -300 | -100 | | μA | HST = GND |
| | RGT | -100 | -25 | | μA | RGT = GND |
| | STB | -100 | -25 | | μA | STB = GND |
| Video signal input pin capacitance | Csig | | 50 | | pF | |

2. Vertical drivers

| Item | Symbol | Min. | Typ. | Max. | Unit | Condition |
|-----------------------|--------------------------------|------|------|------|------|---------------------------------|
| Input pin capacitance | VCK | | 5 | 10 | pF | |
| | VST | | 5 | 10 | pF | |
| | VST EN DWN VCK BLK | -100 | -25 | | μA | VST, EN, DWN, VCK, BLK = GND |

3. Total power consumption of the panel

| Item | Symbol | Min. | Typ. | Max. | Unit |
|---|--------|------|------|------|------|
| Total power consumption of the panel (NTSC) | PWR | | 30 | 50 | mW |
| Power consumption during power save | | | 0.6 | | mW |

4. VCOM input resistance

| Item | Symbol | Min. | Typ. | Max. | Unit |
|-------------------------------------|--------|------|------|------|------|
| VCOM – Vss input resistance | Rcom | 0.5 | 1 | 1.2 | MΩ |
| Video signal – Vss input resistance | Rsig | 0.5 | 1 | 1.2 | MΩ |

Electro-optical Characteristics

(Ta = 25°C, NTSC mode)

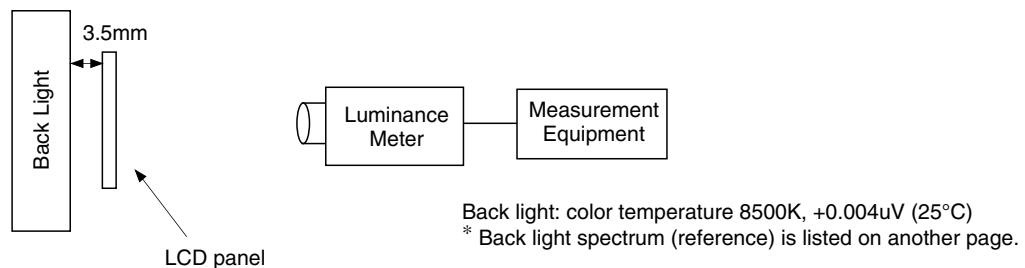
| Item | | | Symbol | Measurement method | Min | Typ. | Max. | Unit |
|------------------------------------|--|---------|---------------------|--------------------|-------|-------|-------|---------------|
| Contrast ratio | V _{DD} = 12.0V V _{sig} = 6.0 ± 4.0V | 60°C | CR _{4.060} | 1 | 70 | 200 | — | — |
| | | 25°C | CR _{4.025} | | 70 | 200 | — | |
| Optical transmittance | | 60°C | T | 2 | 3.8 | 4.8 | — | % |
| Chromaticity | R | X | R _x | 3 | 0.580 | 0.620 | 0.660 | CIE standards |
| | | Y | R _y | | 0.300 | 0.340 | 0.380 | |
| | G | X | G _x | | 0.250 | 0.290 | 0.330 | |
| | | Y | G _y | | 0.550 | 0.590 | 0.630 | |
| | B | X | B _x | | 0.105 | 0.140 | 0.175 | |
| | | Y | B _y | | 0.070 | 0.110 | 0.150 | |
| V-T characteristics | V ₉₀ | 25°C | V ₉₀₋₂₅ | 4 | 1.1 | 1.6 | 2.2 | V |
| | | 60°C | V ₉₀₋₆₀ | | 1.0 | 1.5 | 2.1 | |
| | V ₅₀ | 25°C | V ₅₀₋₂₅ | | 1.5 | 2.0 | 2.5 | |
| | | 60°C | V ₅₀₋₆₀ | | 1.5 | 1.9 | 2.5 | |
| | V ₁₀ | 25°C | V ₁₀₋₂₅ | | 2.2 | 2.5 | 3.2 | |
| | | 60°C | V ₁₀₋₆₀ | | 2.1 | 2.4 | 3.1 | |
| Half tone color reproduction range | | R vs. G | V _{50RG} | 5 | — | -0.10 | -0.25 | V |
| | | B vs. G | V _{50BG} | | — | 0.10 | 0.45 | |
| Response time | ON time | 0°C | ton0 | 6 | — | 30 | 100 | ms |
| | | 25°C | ton25 | | — | 20 | 40 | |
| | OFF time | 0°C | toff0 | | — | 65 | 150 | |
| | | 25°C | toff25 | | — | 20 | 60 | |
| Flicker | | 60°C | F | 7 | — | — | -40 | dB |
| Image retention time | | 60 min. | YT60 | 8 | — | — | 20 | s |

<Electro-optical Characteristics Measurement>

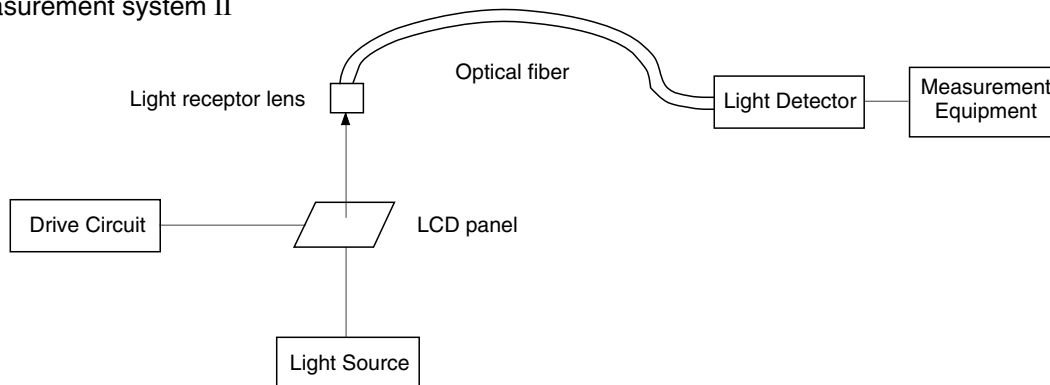
Basic measurement conditions

- (1) Driving voltage
 $V_{DD} = 12.0V$
 $V_{VC} = 6.0V, V_{COM} = 5.7V$
- (2) Measurement temperature
 $25^{\circ}C$ unless otherwise specified.
- (3) Measurement point
 One point in the center of screen unless otherwise specified.
- (4) Measurement systems
 Two types of measurement system are used as shown below.
- (5) RGB input signal voltage (V_{sig})
 $V_{sig} = 6.0 \pm V_{AC}$ [V] (V_{AC} : signal amplitude)

* Measurement system I



* Measurement system II

**1. Contrast Ratio**

Contrast Ratio ($CR_{4.0}$) is given by the following formula (1).

$$CR_{4.0} = \frac{L_{4.0} \text{ (White)}}{L_{4.0} \text{ (Black)}} \dots(1)$$

$L_{4.0}$ (White): Surface luminance of the TFT-LCD panel at $V_{DD} = 12.0V$, $V_{VC} = 6.0V$, $V_{COM} = 5.7V$ and the RGB signal amplitude $V_{AC} = 0.5V$.

$L_{4.0}$ (Black): Surface luminance of the panel at $V_{AC} = 4.0V$.

2. Optical Transmittance

Optical Transmittance (T) is given by the following formula (2).

$$T = \frac{L \text{ (White)}}{\text{Luminance of Back Light}} \times 100 \text{ [\%] ... (2)}$$

L (White) is the same expression as defined in the "Contrast Ratio" section.

3. Chromaticity

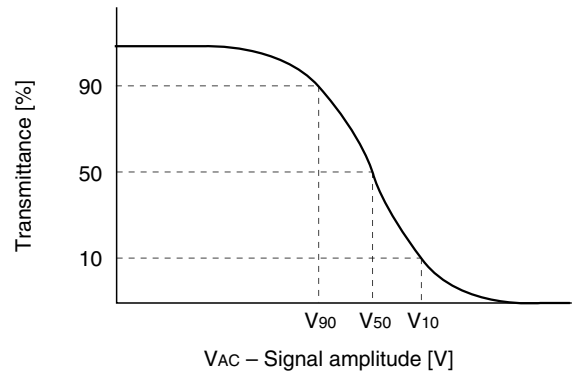
Chromaticity of the panels are measured by System I. Raster modes of each color are defined by the representations at the input signal amplitude conditions shown in the table below. System I uses Chromaticity of x and y on the CIE standards here.

| | | Signal amplitudes (V _{AC}) supplied to each input | | |
|--------|---|---|---------|---------|
| | | R input | G input | B input |
| Raster | R | 0.5 | 4.0 | 4.0 |
| | G | 4.0 | 0.5 | 4.0 |
| | B | 4.0 | 4.0 | 0.5 |

(Unit: V)

4. V-T Characteristics

V-T characteristics, the relationship between signal amplitude and the transmittance of the panels, are measured by System II. V₉₀, V₅₀ and V₁₀ correspond to the each voltage which defines 90%, 50% and 10% of transmittance respectively. (Transmittance at V_{AC} = 0.5V is 100%.)

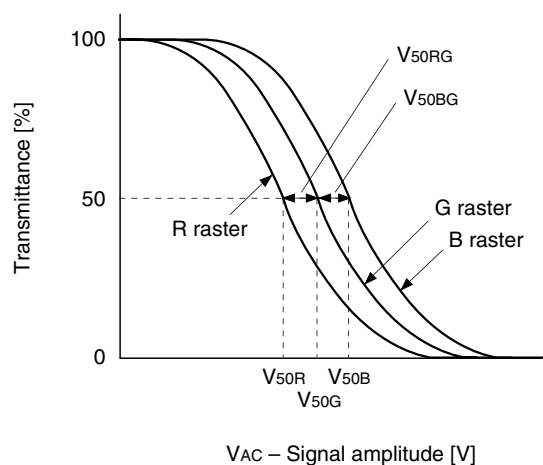


5. Half Tone Color Reproduction Range

Half tone color reproduction range of the LCD panels is characterized by the differences between the V-T characteristics of R, G and B. The differences of these V-T characteristics are measured by System II. System II defines signal voltages of each R, G, B raster modes which correspond to 50% of transmittance, V_{50R}, V_{50G} and V_{50B} respectively. V_{50RG} and V_{50BG}, the voltage differences between V_{50R} and V_{50G}, V_{50B} and V_{50G}, are simply given by the following formulas (3) and (4) respectively.

$$V_{50RG} = V_{50R} - V_{50G} \text{ ... (3)}$$

$$V_{50BG} = V_{50B} - V_{50G} \text{ ... (4)}$$



6. Response Time

Response time t_{on} and t_{off} are defined by the formulas (5) and (6) respectively.

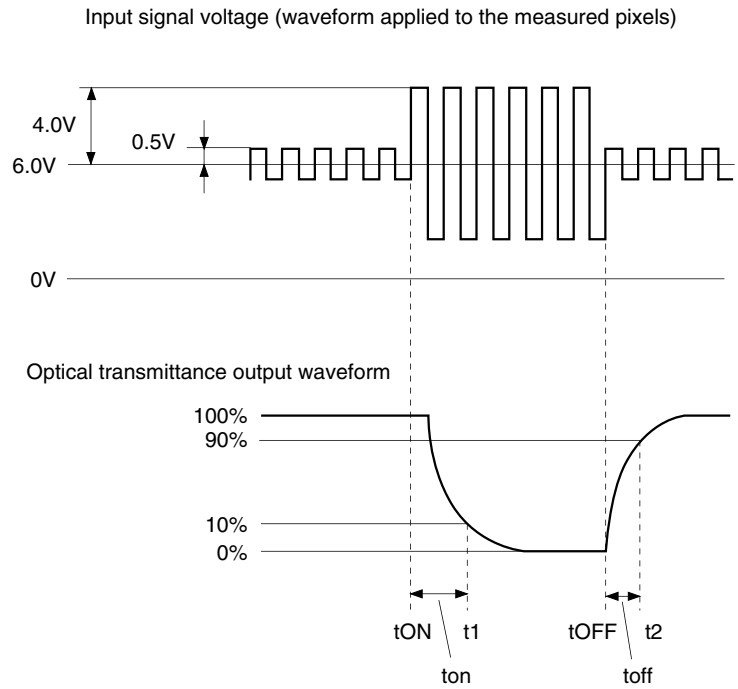
$$t_{on} = t_1 - t_{ON} \dots(5)$$

$$t_{off} = t_2 - t_{OFF} \dots(6)$$

t_1 : time which gives 10% transmittance of the panel.

t_2 : time which gives 90% transmittance of the panel.

The relationships between t_1 , t_2 , t_{ON} and t_{OFF} are shown in the right figure.



7. Flicker

Flicker (F) is given by the formula (7). DC and AC (NTSC: 30Hz, rms, PAL: 25Hz, rms) components of the panel output signal for gray raster* mode are measured by a DC voltmeter and a spectrum analyzer in System II.

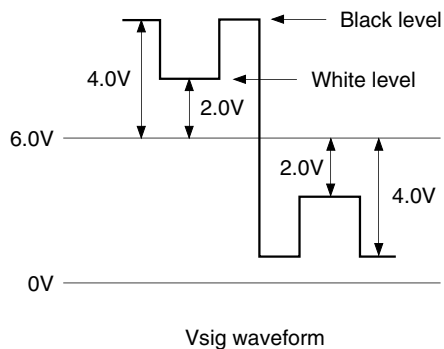
$$F \text{ (dB)} = 20 \log \left\{ \frac{\text{AC component}}{\text{DC component}} \right\} \dots(7)$$

* R, G, B input signal condition for gray raster mode is given by $V_{sig} = 6.0 \pm V_{50}$ (V) where: V_{50} is the signal amplitude which gives 50% of transmittance in V-T characteristics.

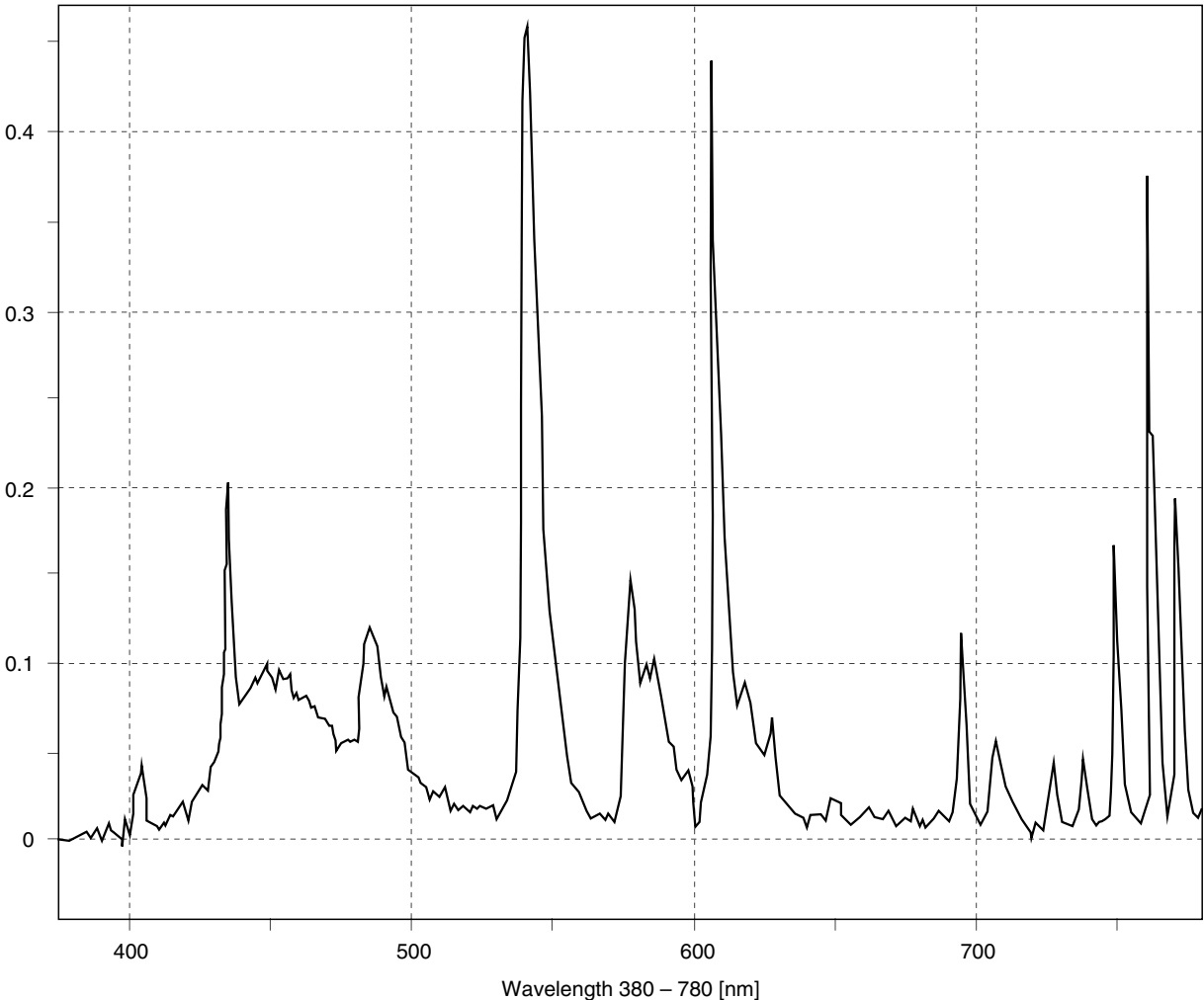
8. Image Retention Time

Apply the monoscope signal to the LCD panel for 60 minutes and then change this signal to the gray scale of $V_{sig} = 6.0 \pm V_{AC}$ (V_{AC} : 3 to 4V), judging by sight at V_{AC} that hold the maximum image retention, measure the time till the residual image becomes indistinct.

* Monoscope signal conditions:
 $V_{sig} = 6.0 \pm 4.0$ or 6 ± 2.0 (V)
 (shown in the right figure)
 $V_{COM} = 5.7V$



Example of Back Light Spectrum (Reference)

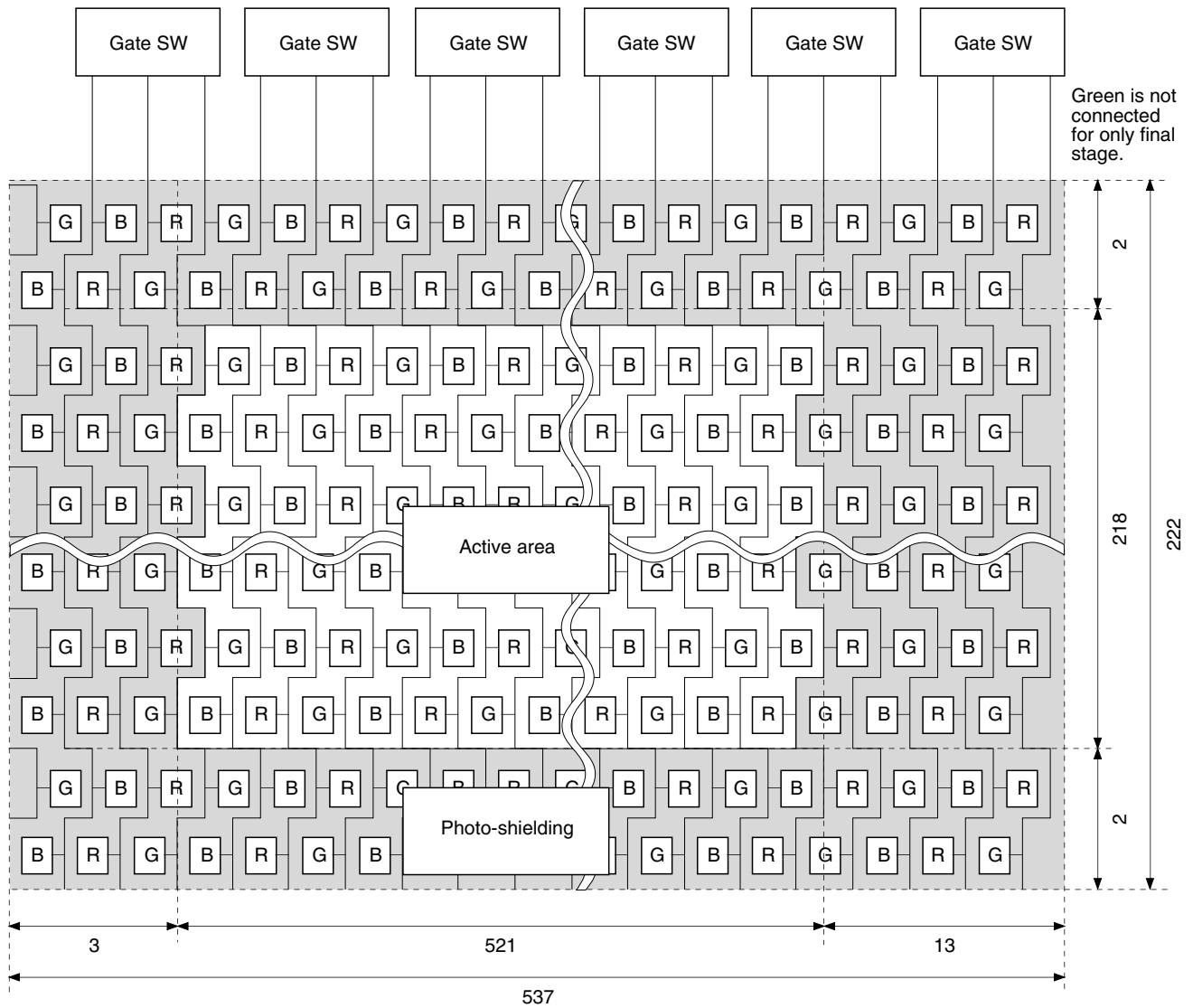


Description of Operation

1. Color Coding

Color filters are coded in a delta arrangement.

The shaded area is used for the dark border around the display.



2. LCD Panel Operations

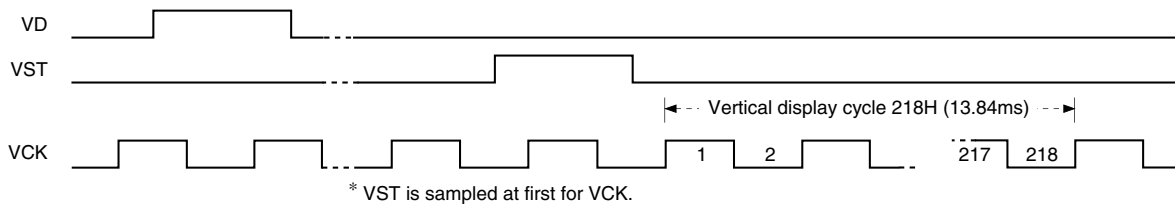
- Through current of the level shifter during power supply cutoff can be reduced by STB pin. (power save mode)
Power save mode is set at STB = Low level.
- A vertical driver, which consists of vertical shift registers, enable-gates and buffers, applies a selected pulse to every 218 gate lines sequentially in every horizontal scanning period. A vertical shift register scans the gate lines from the top to bottom of the panel at DWN = High level.
- The selected pulse is delivered when the enable pin turns to High level. PAL mode images are displayed by controlling the enable and VCK pin. The enable pin should be High when not in use.
- A horizontal driver, which consists of horizontal shift registers, gates and CMOS sample-and-hold circuits applies selected pulses to every 521 signal electrodes sequentially in a single horizontal scanning period.
- Vertical and horizontal drivers address one pixel and then turn on Thin Film Transistors (TFTs; two TFTs) to apply a video signal to the dot. The same procedures lead to the entire 218×521 dots to display a picture in a single vertical scanning period.
- Pixel dots are arranged in a delta pattern, where sets of RGB pixels are positioned with 1.5-dot shifted against adjacent horizontal line. 1.5-dot shift of a horizontal driver output pulse against horizontal synchronized signal is required to apply a video signal to each dot properly. 1H reversed displaying mode is required to apply video signal to the panel.
- The video signal shall be input with polarity-inverted system in every horizontal cycle.
- Timing diagrams of the vertical and the horizontal right-direction scanning (RGT = High level) display cycle are shown below:

- This LCD panel provides the following functions.
 - Right/left inverse mode
 - Up/down inverse mode

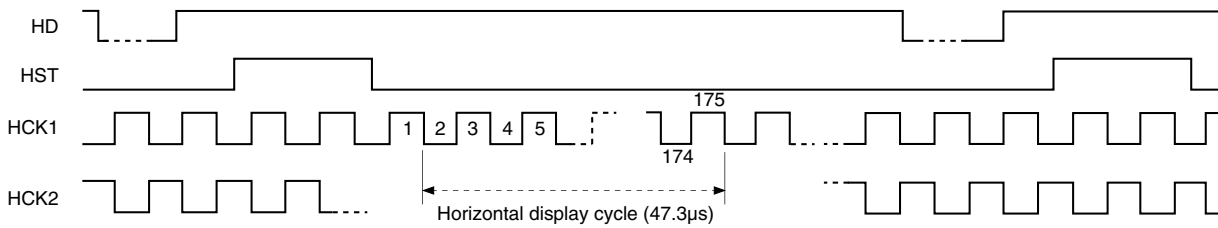
These modes are controlled by two signals, RGT and DWN.

| | | | |
|-----|------------|-----|-----------|
| RGT | Mode | DWN | Mode |
| H | Right scan | H | Down scan |
| L | Left scan | L | Up scan |

(1) Vertical display cycle



(2) Horizontal display cycle (right scan)



* HST is sampled at first for HCK1.

The horizontal display cycle consists of $521/3 = 174$ clock pulses because of RGB simultaneous sampling.

* Refer to Description of Operation "3. RGB Simultaneous Sampling."

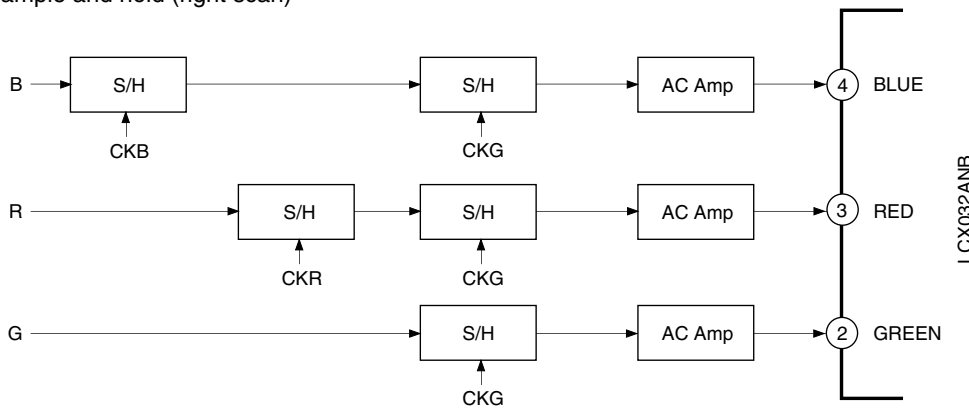
3. RGB Simultaneous Sampling

Horizontal driver samples R, G and B signal simultaneously, which requires the phase matching between R, G and B signals to prevent horizontal resolution from deteriorating. Thus phase matching between each signal is required using an external signal delaying circuit before applying video signal to the LCD panel.

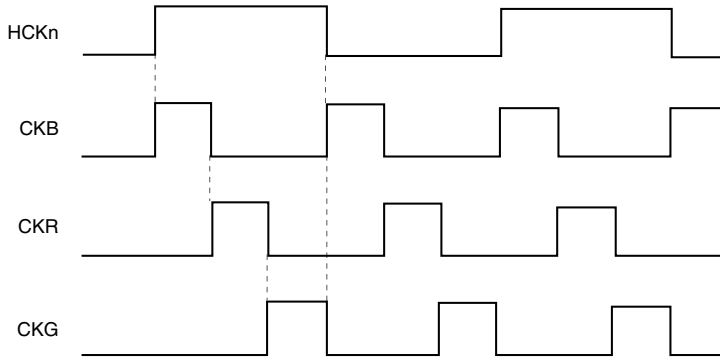
Two methods are applied for the delaying procedure: Sample and hold and Delay circuit. These two block diagrams are as follows.

The LCX032ANB has the right/left inverse function. The following phase relationship diagram indicates the phase setting for the right scan (RGT = High level). For the left scan (RGT = Low level), the phase setting shall be inverted between B and G signals.

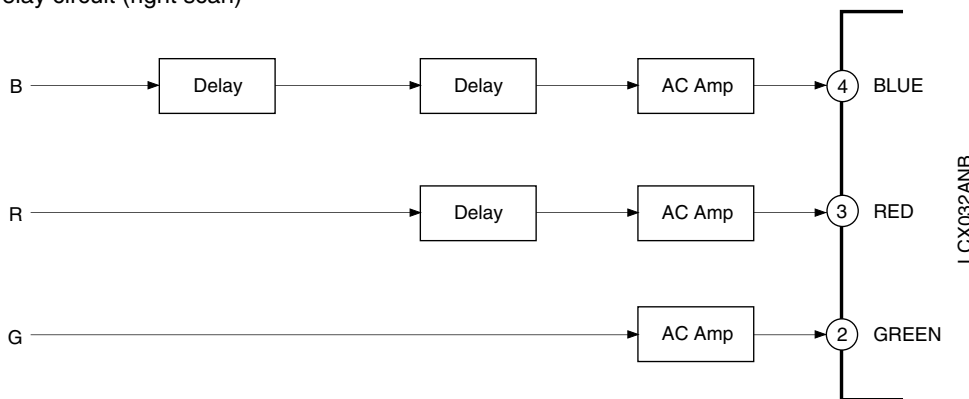
(1) Sample and hold (right scan)



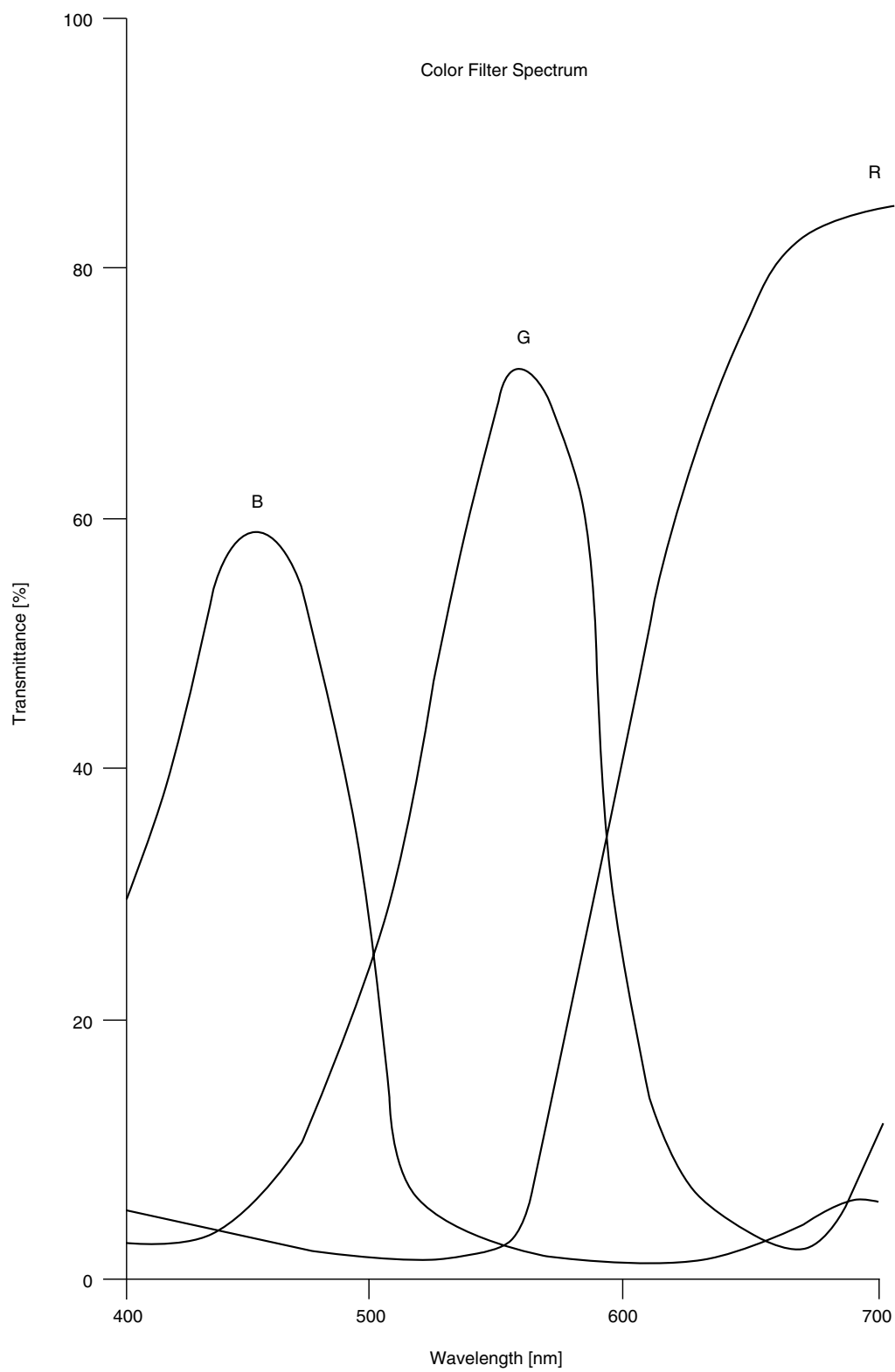
<Phase relationship of delaying sample-and-hold pulses> (right scan)



(2) Delay circuit (right scan)

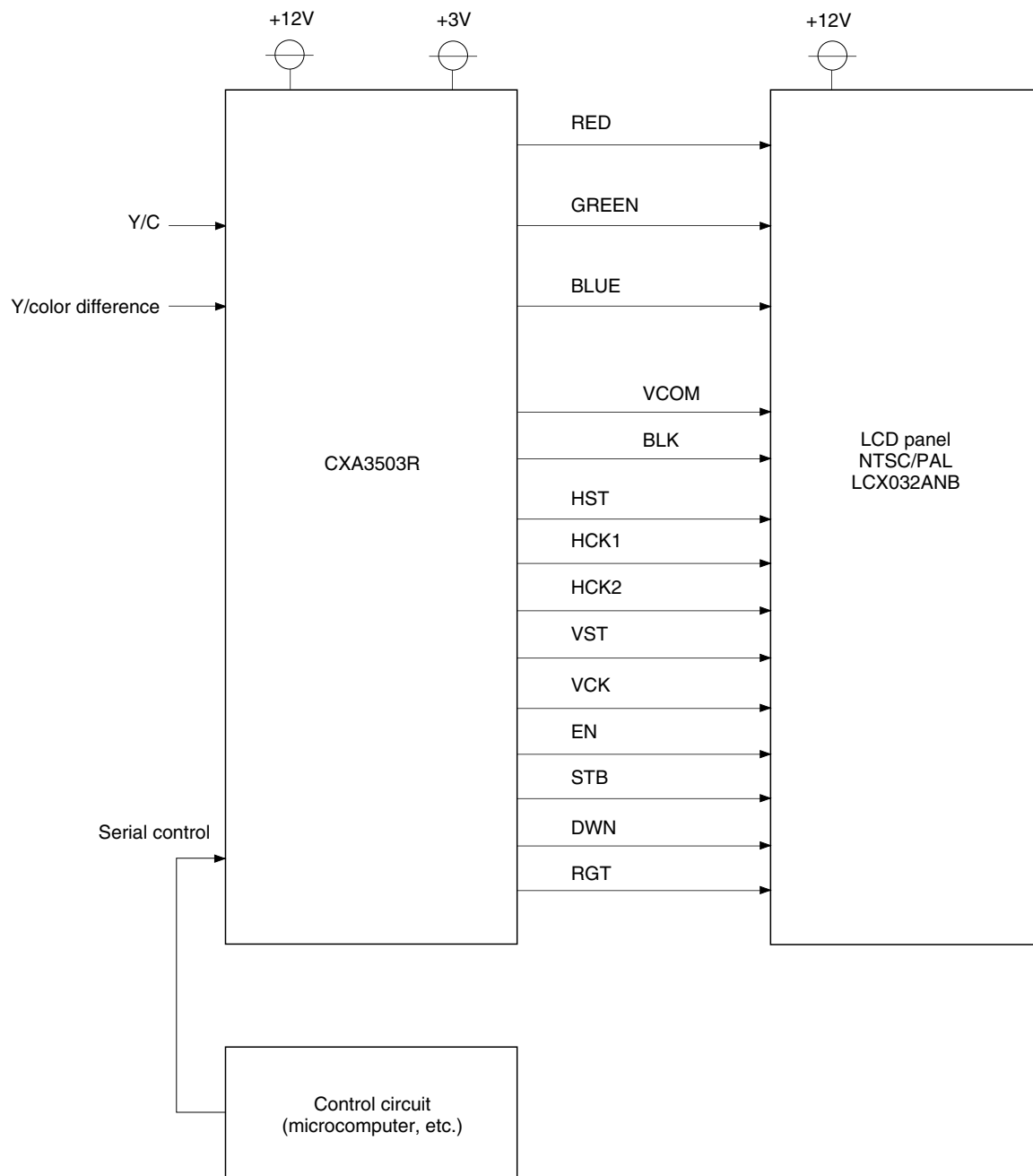


Example of Color Filter Spectrum (Reference)



Color Display System Block Diagram

An example of single-chip display system is shown below.



Notes on Handling**(1) Static charge prevention**

Be sure to take following protective measures. TFT-LCD panels are easily damaged by static charge.

- a) Use non-chargeable gloves, or simply use bare hands.
- b) Use an earth-band when handling.
- c) Do not touch any electrodes of a panel.
- d) Wear non-chargeable clothes and conductive shoes.
- e) Install conductive mat on the working floor and working table.
- f) Keep panels away from any charged materials.
- g) Use ionized air to discharge the panels.

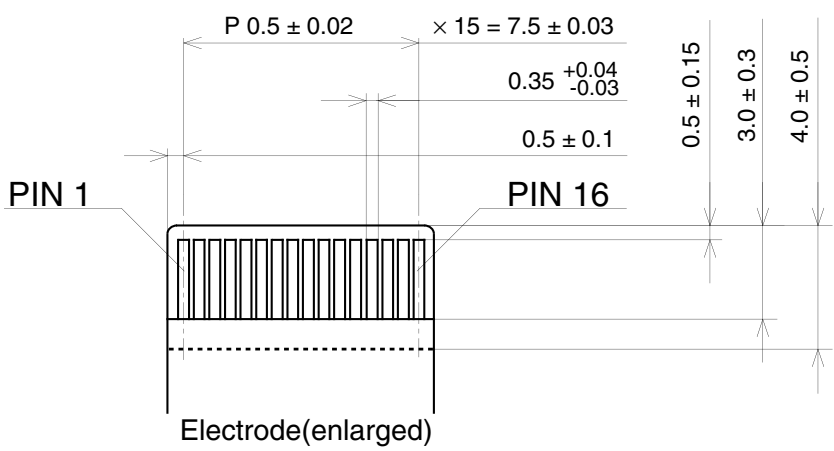
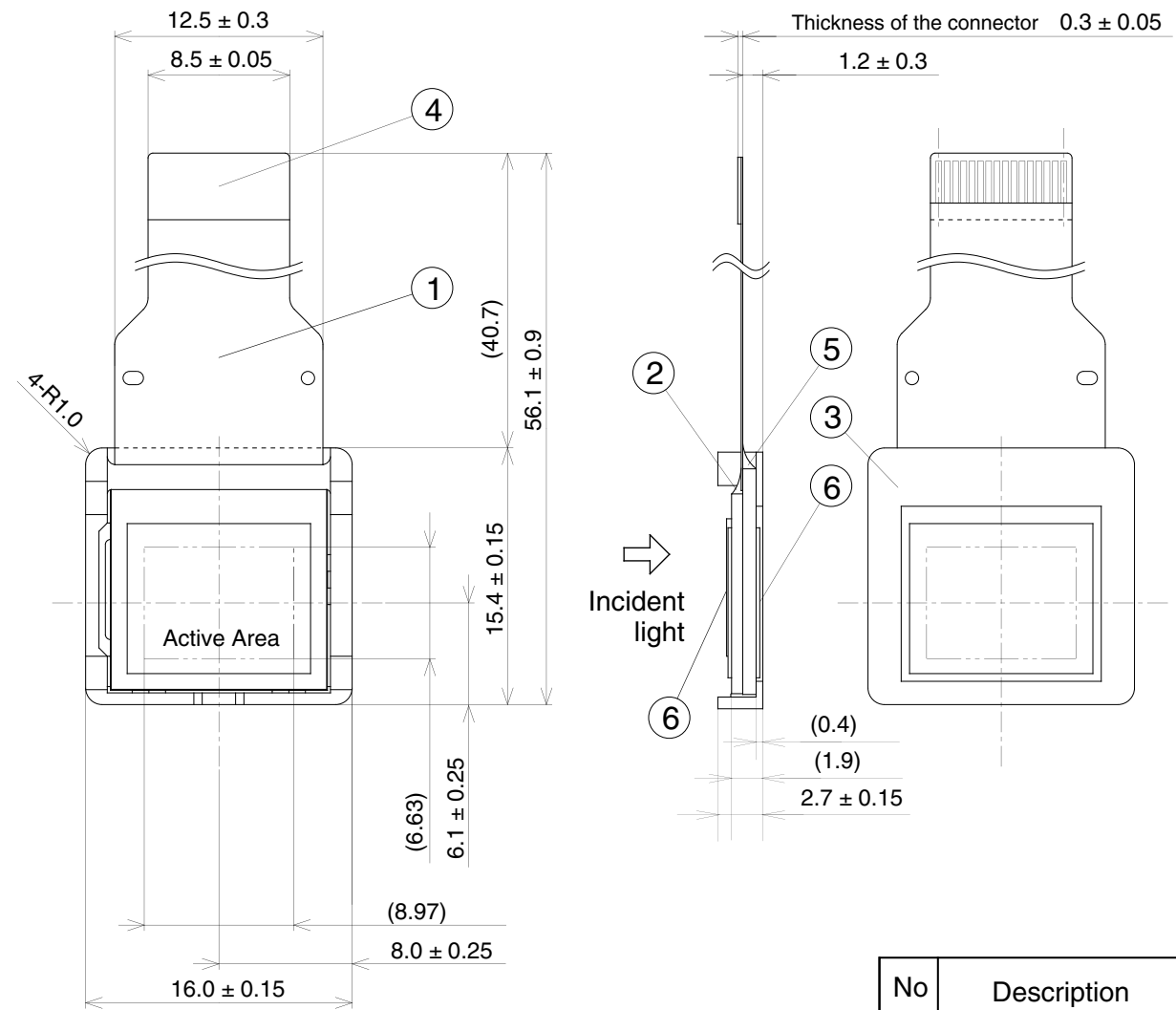
(2) Protection from dust and dirt

- a) Operate in clean environment.
- b) When delivered, a surface of a panel (Polarizer) is covered by a protective sheet. Peel off the protective sheet carefully not to damage the panel.
- c) Do not touch the surface of a panel. The surface is easily scratched. When cleaning, use a clean-room wiper with isopropyl alcohol. Be careful not to leave stain on the surface.
- d) Use ionized air to blow off dust at a panel.

(3) Other handling precautions

- a) Do not twist or bend the flexible PC board especially at the connecting region because the board is easily deformed.
- b) Do not drop a panel.
- c) Do not twist or bend a panel or a panel frame.
- d) Keep a panel away from heat source.
- e) Do not dampen a panel with water or other solvents.
- f) Avoid to store or to use a panel in a high temperature or in a high humidity, which may result in panel damages.

Package Outline Unit: mm



| No | Description |
|----|----------------------|
| 1 | F P C |
| 2 | Molding material |
| 3 | Outside frame |
| 4 | Reinforcing board |
| 5 | Reinforcing material |
| 6 | Polarizing film |

Mass 0.9g