MT88V32

8 x 4 High Performance Video Switch Array

Preliminary Information

ISSUE 1 August 1993

Ordering Information
MT88V32AP 44 Pin PLCC
-40° to 85°C

Features

- 32 bidirectional CMOS "T" switches in an 8×4 non-blocking array
- Break-before-make switching configuration
- Fast setup & hold times for switch programming
- 3dB bandwidth of 200MHz
- Low feedthrough and crosstalk, better than -80dB at 5MHz
- Very low differential gain and phase errors
- 12Vpp bipolar signal capability
- On-state resistance 75Ω (max) for V_{DD}=+5V, V_{EE}=-7V
- Switch control through 2-stage latches
- Orthogonal Xi and Yi pin connections for optimized PCB layout
- Latch readback capability for monitoring

Applications

- High-end video routing and switching
- Medical instrumentation
- Automatic test equipment (ATE)
- Multi-media communication

Description

The MT88V32 is a digitally programmable (TTL levels) 8×4 crosspoint switch that is designed to control wide-band analog (video) signal.

Each of the 32 nodes of the switching matrix has a T-switch, see Fig.1. This grounds the nodes of all open connections, which greatly reduces feedthrough noise. In order to reduce crosstalk, individual analog signal lines are isolated by interleaving them with ground lines.

The two stage programmable latch system allows the state of all switching nodes to be updated simultaneously. The next state of the switch is written into the first stage of the latches through individual write cycles. These changes will not affect the current state of the switch. The $\overline{\text{STROBE2}}$ control input is used to load the state of all first stage latches to the second stage latches, which updates the complete matrix. Therefore, all 32 switching nodes are updated simultaneously.

The MT88V32 supports separate analog (V_{EE}) and digital (V_{DD}) voltage references. This allows the user to select an optimum analog signal bias point.

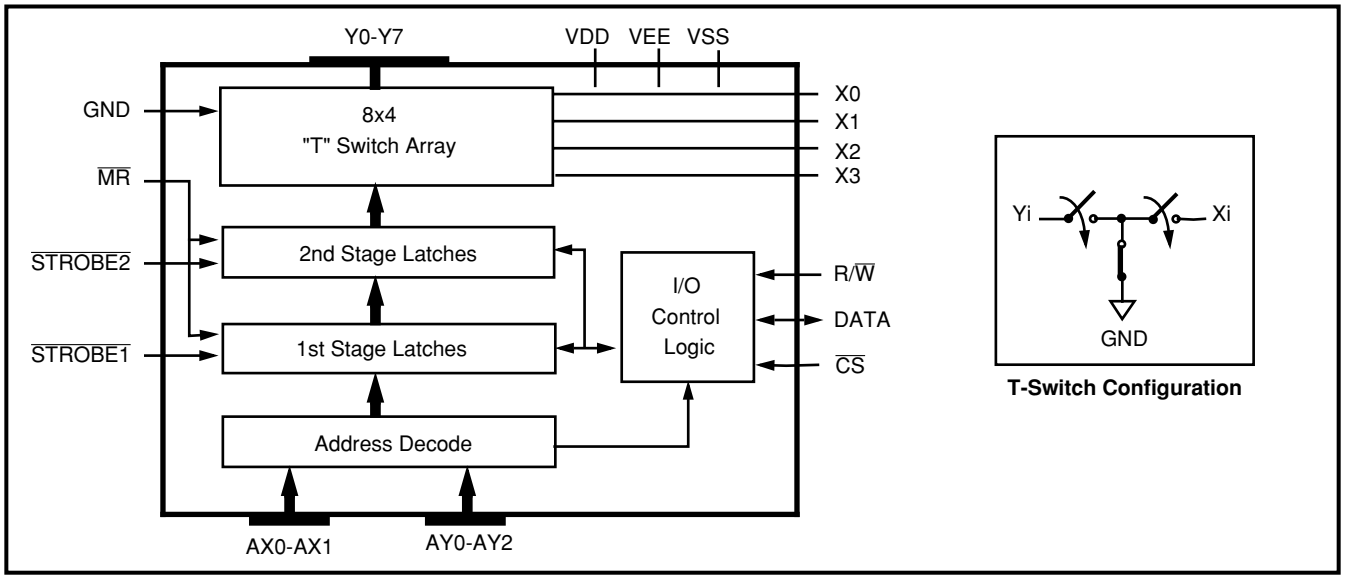


Figure 1 - Functional Block Diagram

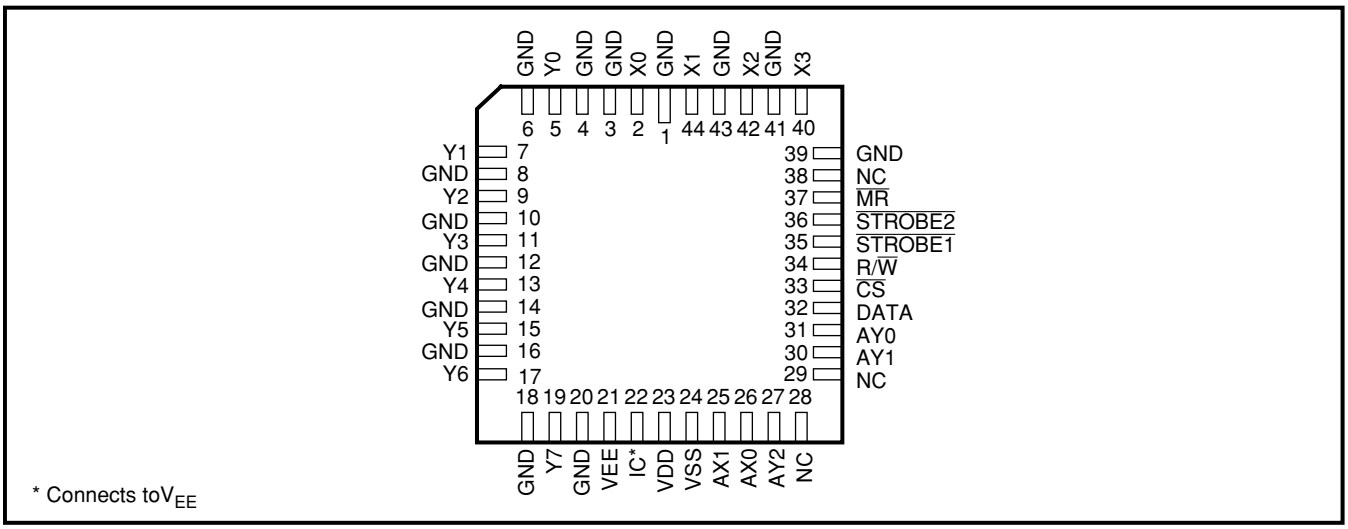


Figure 2 - Pin Connections

Pin Description

Pin #*	Name	Description
1, 3, 4, 6, 8, 10, 12, 14, 16, 18, 20, 39, 41, 43	GND	**Analog Ground.** Connect to system ground for crosstalk noise isolation. Pins 3 and 39 are not bonded internally.
2, 44, 42, 40	X0, X1, X2, X3	**Analog Lines (input/output)**.
5, 7, 9, 11, 13, 15, 17, 19	Y0, Y1, Y2, Y3 Y4, Y5, Y6, Y7	**Analog Lines (input/output)**.
21	V_{EE}	**Negative Analog Power Supply.**
22	IC	**Internal Connection.**
23	V_{DD}	**Positive Power Supply.**
24	V_{SS}	**Digital Ground Reference.**
25, 26	AX1,AX0	**X0-X3 I/O Address Select (inputs).**
27, 30,31	AY2-AY0	**Y0-Y7 I/O Address Select (inputs).**
28, 29	NC	**No Connection.**
32	DATA	**DATA (input/output)**. When input, a logic high will close the selected switch and a logic low will open the selected switch. When output, a logic high indicates a closed switch and a logic low indicates an opened switch.
33	$\overline{CS}$	**Chip Select (input).** Active low.
34	R/$\overline{W}$	**READ/WRITE Control (input).** When high the DATA pin is an output (for reading from second stage latch); when low the DATA pin is an input (for writing to first stage latch).
35	$\overline{STROBE1}$	**STROBE 1 (input).** Modifies memory content of first stage latch as determined by the addess and data lines, but does not change the switch array configuration of entire switch array. Active low.
36	$\overline{STROBE2}$	**STROBE 2 (input).** Transfers memory content of first stage latch to the second stage latch and hence, changes the configuration of entire switch array. Active low.
37	$\overline{MR}$	**MASTER RESET (input).** Used to reset the first and second stage latches. Active low.
38	NC	**No Connection.**

Functional Description

The state of the MT88V32 8 X 4 switching matrix is updated through a simple parallel processor interface. This interface provides access to 32 two stage latches, which determines the state (open/close) of each switching array node. Each latch (or node) is addressed by the AX0-AX1 and AY0-AY2 inputs as per Table 2, and the DATA input will determine if the connection is to be made (DATA=1) or opened (DATA=0).

The second stage of the two stage latches controls the current state of each switching node. The value held in the first stage is the input to the second stage. This allows the device to be programmed in two ways. That is, individual switching nodes may be updated one at a time, or all nodes may be updated at once.

To update one node at a time the $\overline{\text{STROBE2}}$ input should be held low. This makes the second stage latches transparent and the matrix immediately reflects the state of the first stage latches. A write cycle example follows:

1) $\overline{\text{STROBE2}}$ is low,
2) $\overline{\text{CS}}$ and R/$\overline{\text{W}}$ are low, $\overline{\text{MR}}$ is high,
3) AX0-AX1 and AY0-AY2 as per Table 2,
4) DATA input high to close or low to open, and
5) $\overline{\text{STROBE1}}$ toggled from high-to-low-to-high.

These steps (one write cycle) may be repeated for each switch state change. This can also be accomplished by holding $\overline{\text{STROBE1}}$ low and toggling $\overline{\text{STROBE2}}$. See Figure 14 for timing.

To update all nodes simultaneously all switch state changes must be written into the first stage latches. This is accomplished by holding $\overline{\text{STROBE2}}$ high and performing steps 2) through 5) above for each switching node that is to be changed. Writing to the first stage latches only will not affect the switching state of the matrix. When the changes have been made all the switches of the matrix may be updated simultaneously by toggling the $\overline{\text{STROBE2}}$ input from high-to-low-to high.

When $\overline{\text{STROBE2}}$ is used to update the state of the MT88V32 all switch “breaks” are completed before any switch “makes” occur. There is approximately 10ns delay between “breaks” and “makes”.

Both the first and second stage latches will be cleared when the master reset ($\overline{\text{MR}}$) is taken from high-to-low. This will open all the switch nodes. The operation of $\overline{\text{MR}}$ is independent of $\overline{\text{CS}}$, AX0-AX1, AY0-AY2 and R/$\overline{\text{W}}$.

The status of each switching array node (second stage latch) can be read through the bidirectional DATA pin. A read cycle example follows:

1) $\overline{\text{CS}}$ is low, R/$\overline{\text{W}}$ and $\overline{\text{MR}}$ are high,
2) AX0-AX1 and AY0-AY2 as per Table 2, and
3) DATA output high for closed or low for open.

$\overline{\text{MR}}$	R/$\overline{\text{W}}$	$\overline{\text{CS}}$	DATA	$\overline{\text{STROBE1}}$	$\overline{\text{STROBE2}}$	DATA
1 1	0 0	1 0	0 1	$1\rightarrow 0$ $1\rightarrow 0$	1 1	No Change to 1st stage latch. 1st stage latch is loaded with data.
1 1	0 0	0 0	0 $1\rightarrow 0\rightarrow 1$	0 0	1 1	1st stage latch is transparent. Selected latch is cleared and set again (i.e., output follows input).
1 1	0 0	0 x	1 x	$0\rightarrow 1$ 1	1 $1\rightarrow 0$	1st stage latch output is frozen. Output of 1st stage latch is transferred to output of 2nd stage latches.
1 1	0 0	x 0	x x	1 0	$0\rightarrow 1$ 0	2nd stage latch output is frozen. Both 1st stage and 2nd stage latches are transparent.
1	1	0	0	x	x	DATA becomes an output and reflects the contents of the 2nd stage latch addressed by AX0-AX1 and AY0-AY2.
0	1	1	1	1	1	All crosspoints opened (data in 1st and 2nd stage latches are cleared).

Table 1 - Truth Tables

Note: x = don’t care, 0 = logic "0" state, 1 = logic "1" state
A logic 1 on DATA input closes a connection.
A logic 0 on DATA input opens a connection.

AX1	AX0	AY2	AY1	AY0	Switch Connections
0	0	0	0	0	Y0 to X0
0	0	0	0	1	Y1 to X0
0	0	0	1	0	Y2 to X0
0	0	0	1	1	Y3 to X0
0	0	1	0	0	Y4 to X0
0	0	1	0	1	Y5 to X0
0	0	1	1	0	Y6 to X0
0	0	1	1	1	Y7 to X0
0 ↓ 0	1 ↓ 1	0 ↓ 1	0 ↓ 1	0 ↓ 1	Y0 to X1 ↓ Y7 to X1
1 ↓ 1	0 ↓ 0	0 ↓ 1	0 ↓ 1	0 ↓ 1	Y0 to X2 ↓ Y7 to X2
1 ↓ 1	1 ↓ 1	0 ↓ 1	0 ↓ 1	0 ↓ 1	Y0 to X3 ↓ Y7 to X3

Table 2 - Address Decode Truth Table

It should be noted that the $\overline{\text{STROBE1}}$ function is disabled during a read cycle. See Fig. 15 for timing.

The MT88V32 can operate from a dual rail power supply (V_{DD} and V_{EE}) or a single rail power supply (V_{SS}=V_{EE}=0V) as per the recommended operating conditions. For minimum on-state resistance the supply voltages should be V_{DD}=5.0 V_{DC}, V_{SS}=0 V_{DC} and V_{EE}=-7 V_{DC}. The analog input signal should be biased at -2.0 V_{DC} to achieve minimum differential phase and gain error (see AC Electrical Characteristics - Crosspoint Performance).

Applications

Figure 3 illustrates examples of how to connect the signal lines of the MT88V32 to various interfaces. Input buffers allow the incoming signals to be scaled and biased to the optimum operating range of the MT88V32 (i.e., differential phase error, differential gain error and R_{ON}). Buffers will also allow a more precise input impedance to be implemented. For low grade video applications, signal lines may be connected directly, as long as the ultimate source and terminating impedances are matched.

Output buffers may be used to provide signal gain and impedance matching for external connections. Additionally, they may be used to isolate parasitic device capacitance in multiple stage switching applications where high frequency roll-off is critical. Crosstalk, as well as differential phase and gain error can be minimized by designing a low source impedance (e.g., 10 ohms), and a high terminating impedance (e.g., 10k) at each stage. If successive switching stages are not buffered, then a resistor to ground (R) should be present between the switches. Selection of R is based on the following compromise:

1) as R is decreased to approach the source and terminating resistance values signal loss will increase and crosstalk will decrease, and
2) as R increases signal loss will decrease and crosstalk will increase.

It is recommended that the power supply rails of the MT88V32 be decoupled with 0.1µF ceramic Z5U and 10µF dipped tantalum capacitors. These capacitors should be as close to the device as possible. The signal pins of the MT88V32 are interleaved with analog ground lines. This allows the circuit designer to run ground tracks on both sides of each signal line to improve crosstalk immunity.

The 8x4 bidirectional CMOS T-switch configuration is a modular switching element in a convenient package size. The inherent flexibility of this device permits the designer to build large switching matrices, see analog switch application notes.

A_5	A_4	A_3	A_2	A_1	A_0	D_0	Function
0 ↓ 0	0 ↓ 1	0 ↓ 1	0 ↓ 1	0 ↓ 1	0 ↓ 1	1/0 ↓ 1/0	Y0 to X0 ↓ ↓ Y7 to X3
1	X	X	X	X	0	X	$\overline{\text{MR}}$
1	X	X	X	X	1	X	$\overline{\text{STB2}}$

Table 3 - Address Decoding for the Processor Interfaces

Note: x = undefined, 1/0 -1 = make, 0 = break

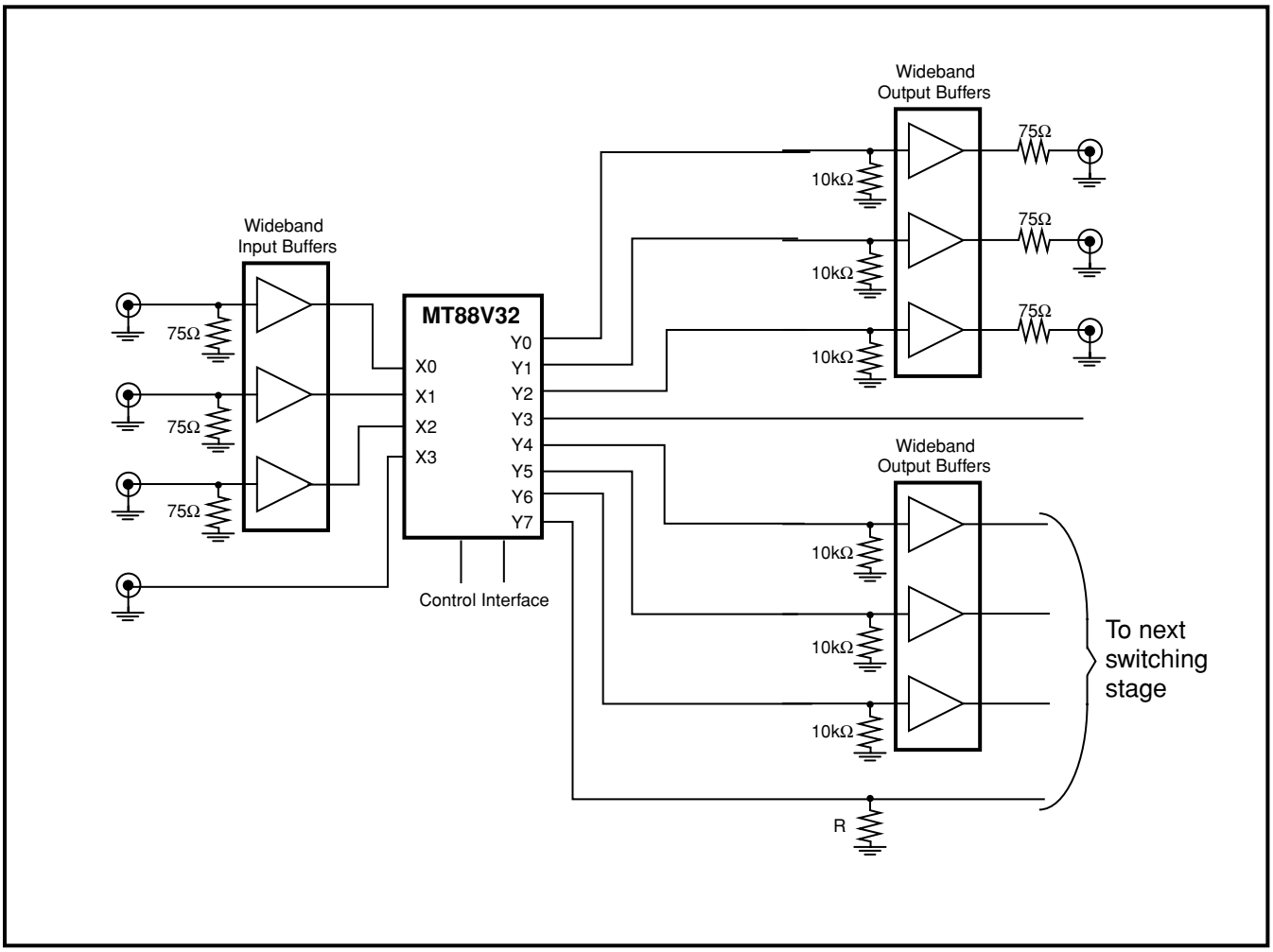


Figure 3 - High Frequency Switching Applications

Figures 4, 5 and 6 show methods of interfacing the MT88V32 to Motorola and Intel microcontrollers. The address decoding for these configurations is in Table 3.

Video Signal Terminology

1) Component Video - separate red (R), blue (B), green (G), and synchronization signals.

2) Composite Video - contains luminance (brightness), chrominance (colour), and synchronization signal components in a single waveform.

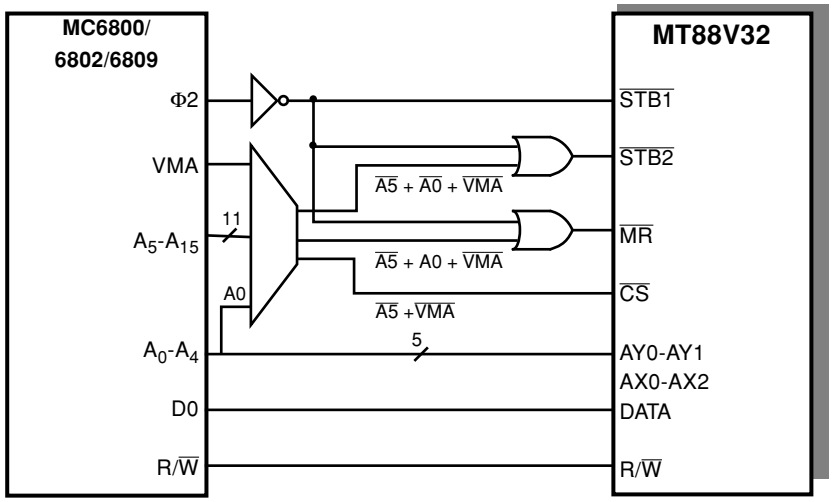
3) Synchronization signal - horizontal sync pulses are negative going excursions of the composite video signal that occur every 63.5 µsec. Their function is to align the horizontal sweep.

   Vertical synchronization is achieved during the vertical blanking interval, which is about 1200 µsec or 20 horizontal scan intervals long. It consists of a number of vertical synchronization and equalization pulses.

4) Luminance - is the black to white brightness component of a composite video signal. Its range is from reference white (maximum amplitude) to reference black (minimum amplitude).

5) Chrominance - rides on the luminance signal and determines the hue (phase) and brightness (amplitude) of the colour component of a composite video signal.

6) Colour burst - is about 9 (minimum 8) cycles of a 3.578545 MHz reference signal, which is transmitted with every horizontal sweep of the composite video signal. A phase comparison



Notes: for the MC6802 Φ2 will be E.
for the MC6809 Φ2 will be E and VMA will be the OR'ed product of Q and E.

Figure 4 - Motorola Non-multiplexed Processor Interface

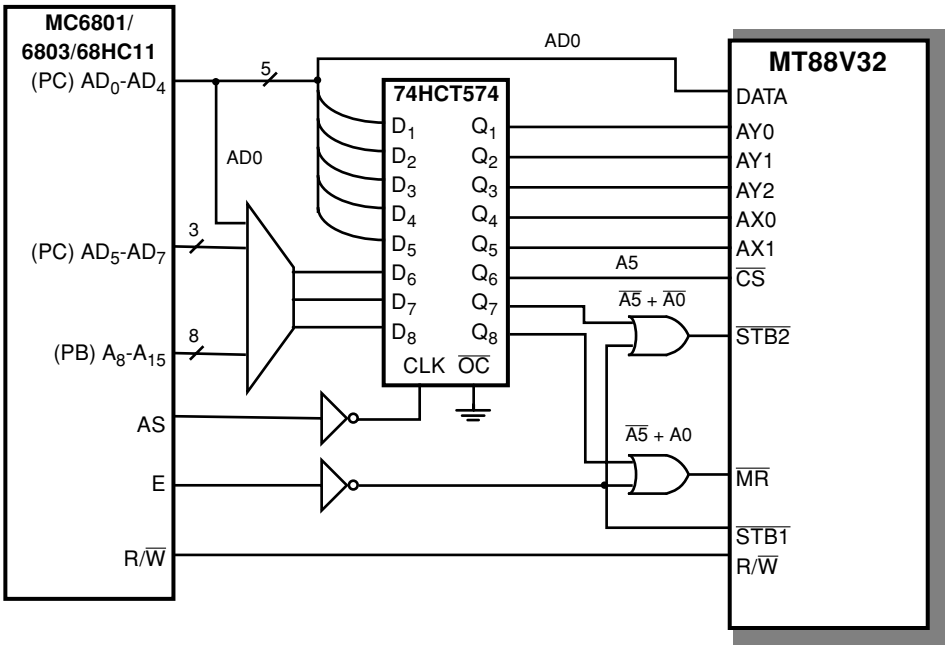


Figure 5 - Motorola Multiplexed Processor Interface

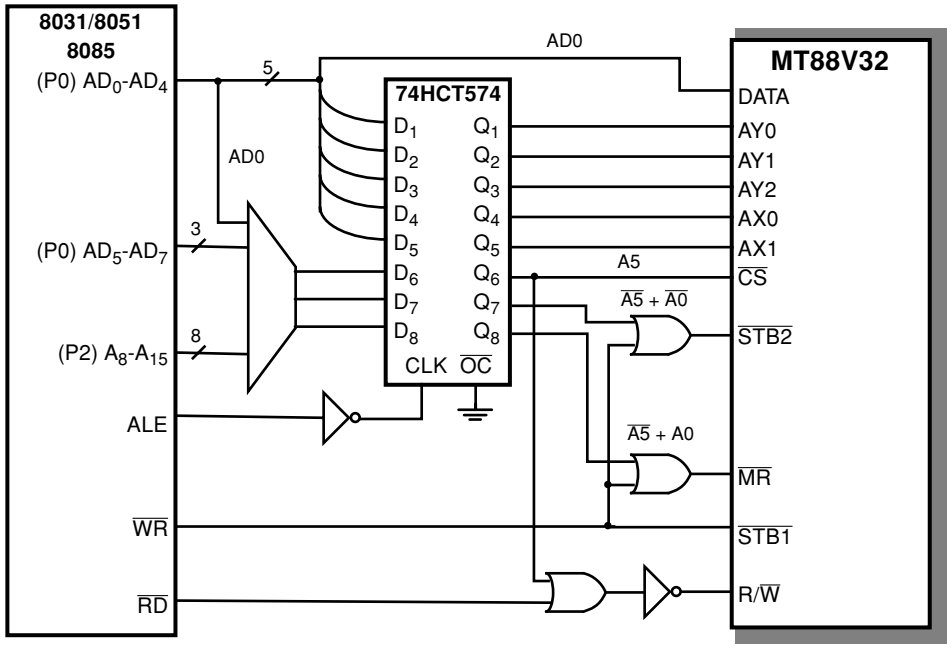


Figure 6 - Intel Processor Interface

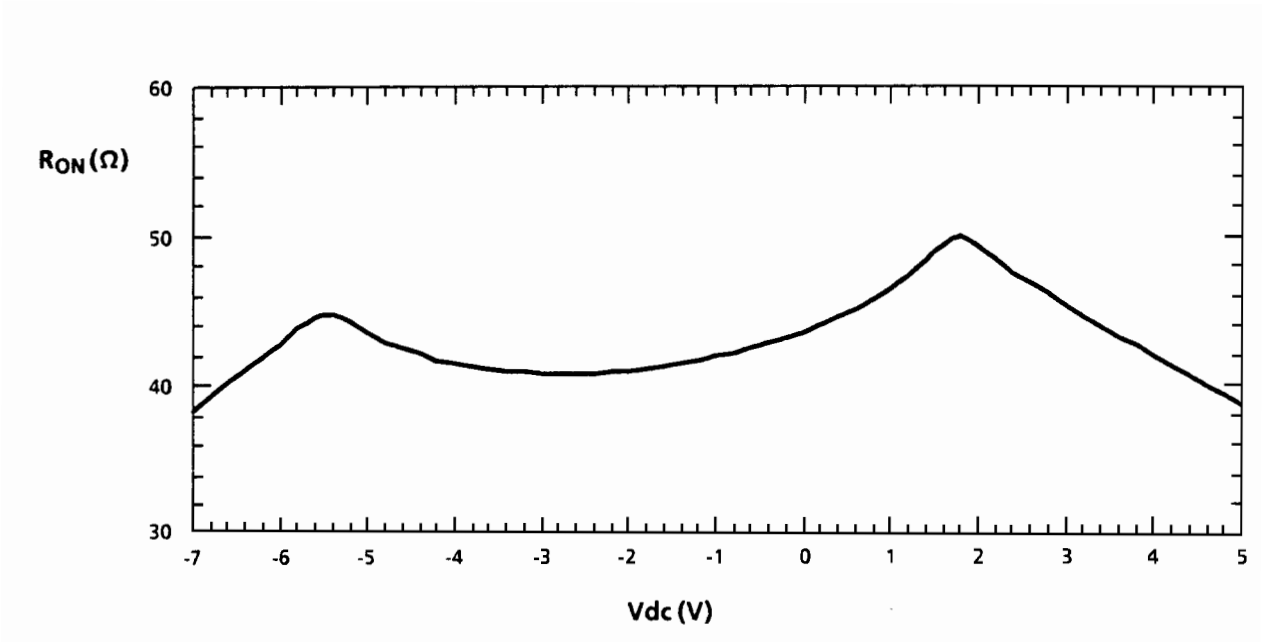


Figure 7 - Typical On-state Resistance (R_{ON}) vs. DC Bias (Vdc) @ V_{DD}=+5V, V_{EE}=-7V

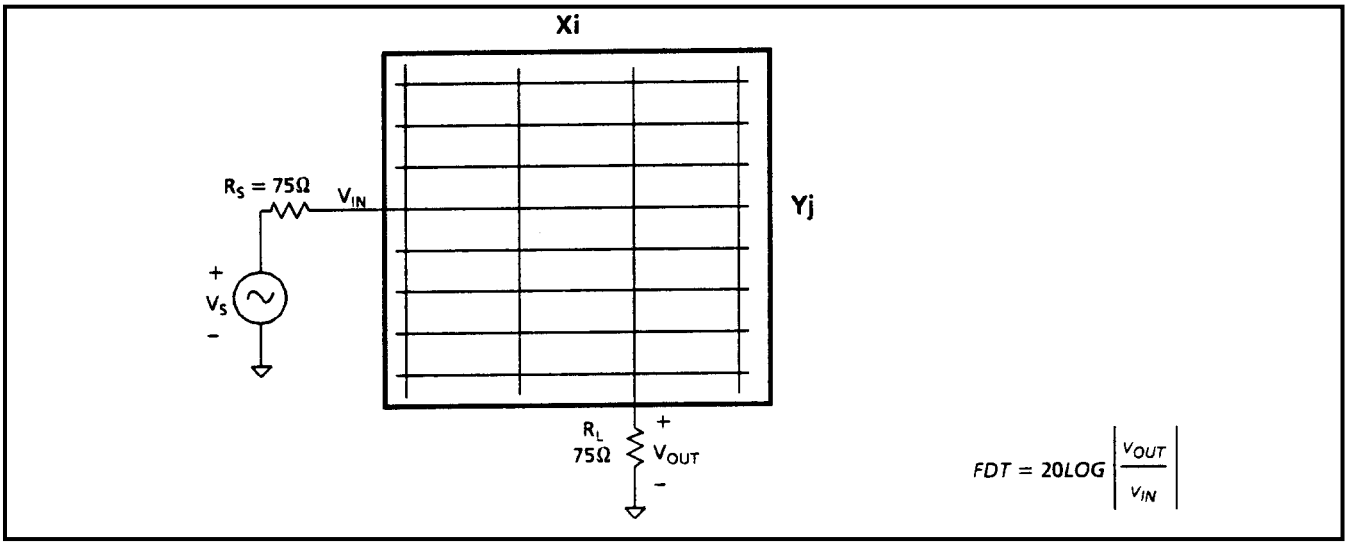


Figure 8 - Single Channel Feedthrough (all crosspoints open)

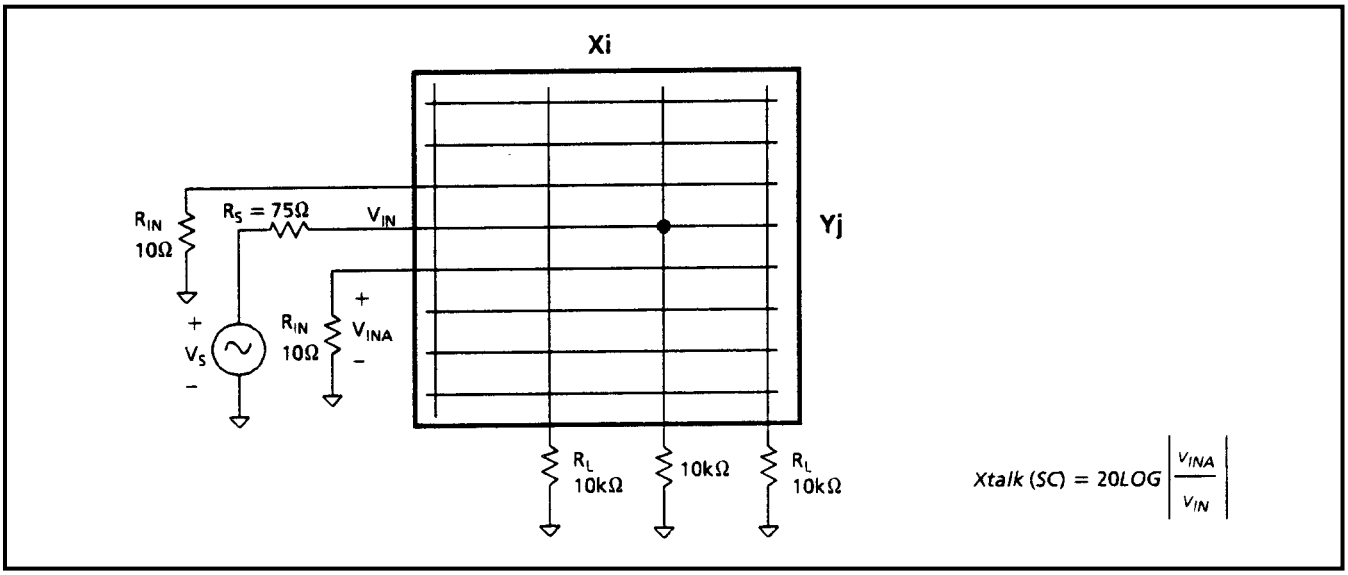


Figure 9 - Single Channel Crosstalk (one crosspoint closed)

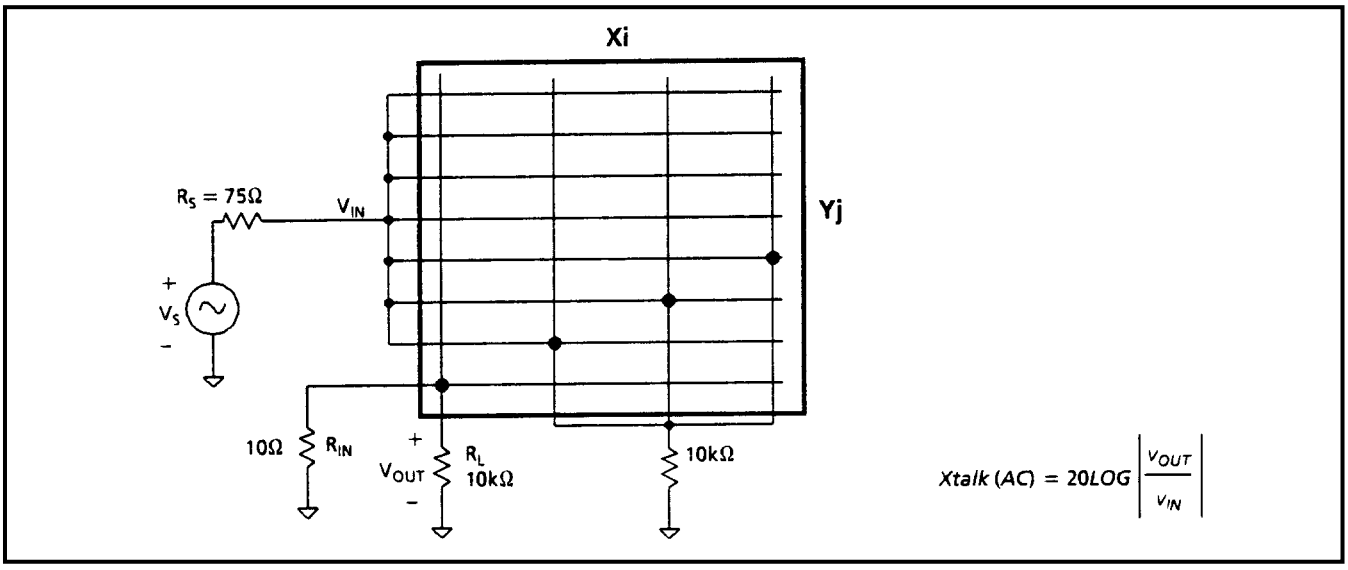


Figure 10 - All Channel Crosstalk (all crosspoints closed)

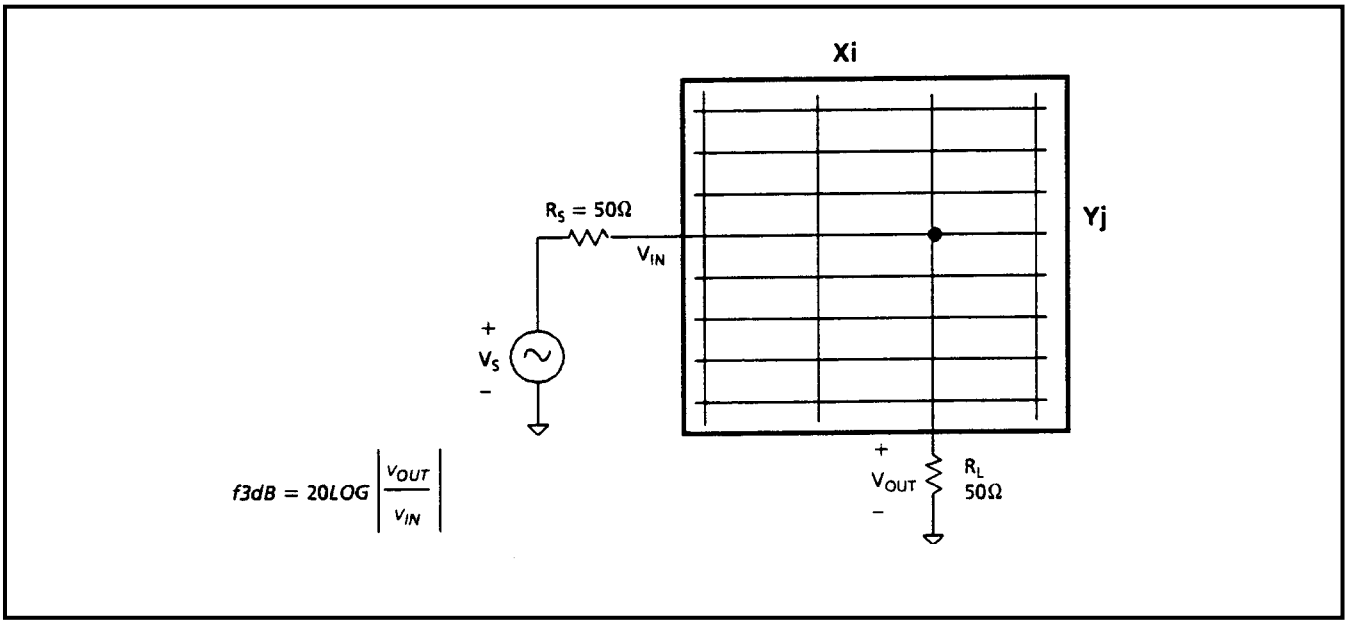


Figure 11 - 3dB Frequency Response

between this reference signal and the chrominance signal determines colour hue.

7) Differential Phase Error - (measured in degrees) is a phase change in the chrominance signal due to a change in luminance amplitude.

8) Differential Gain Error - (measured in percentage) is a change in amplitude of the chrominance signal due to a change in luminance amplitude.

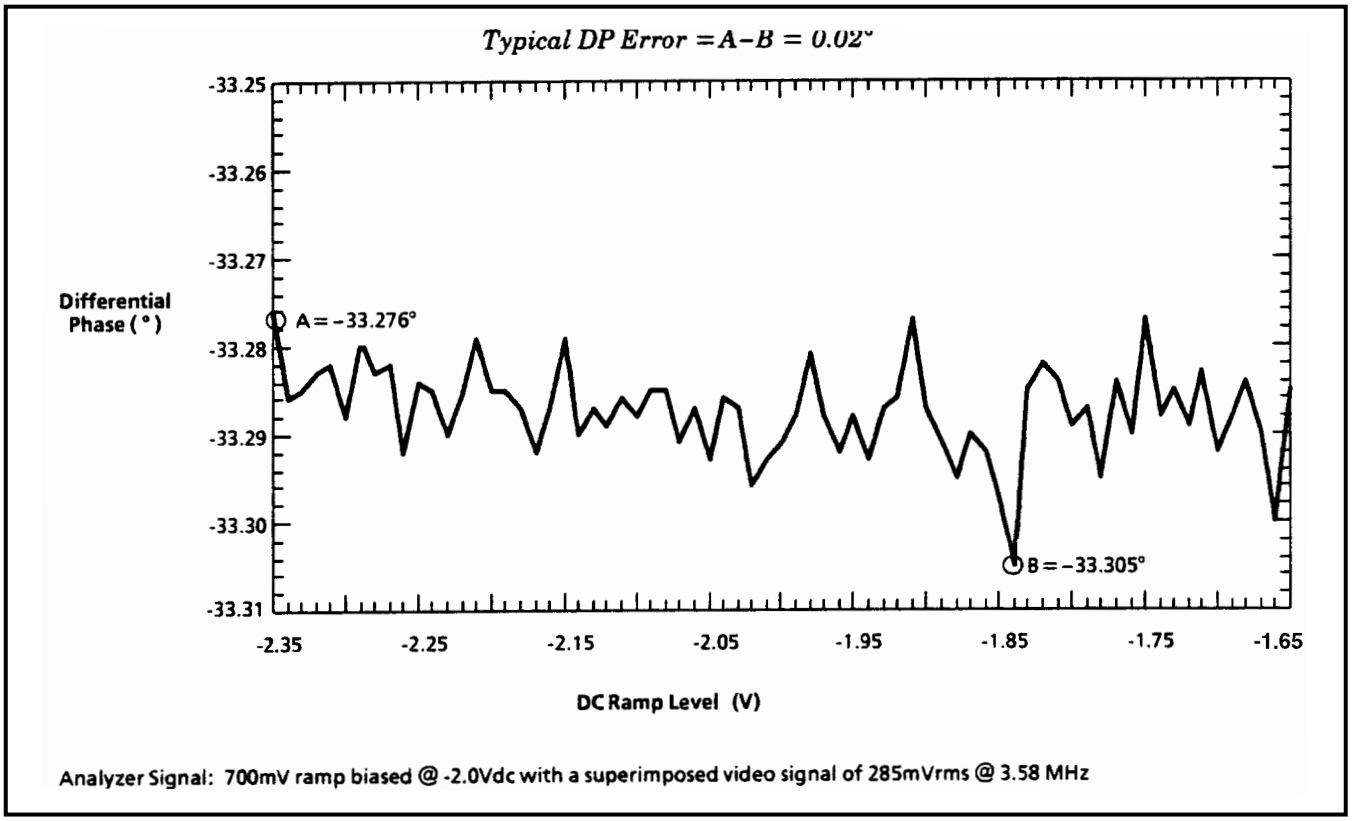


Figure 12 - Typical Differential Phase vs. Ramp Voltage

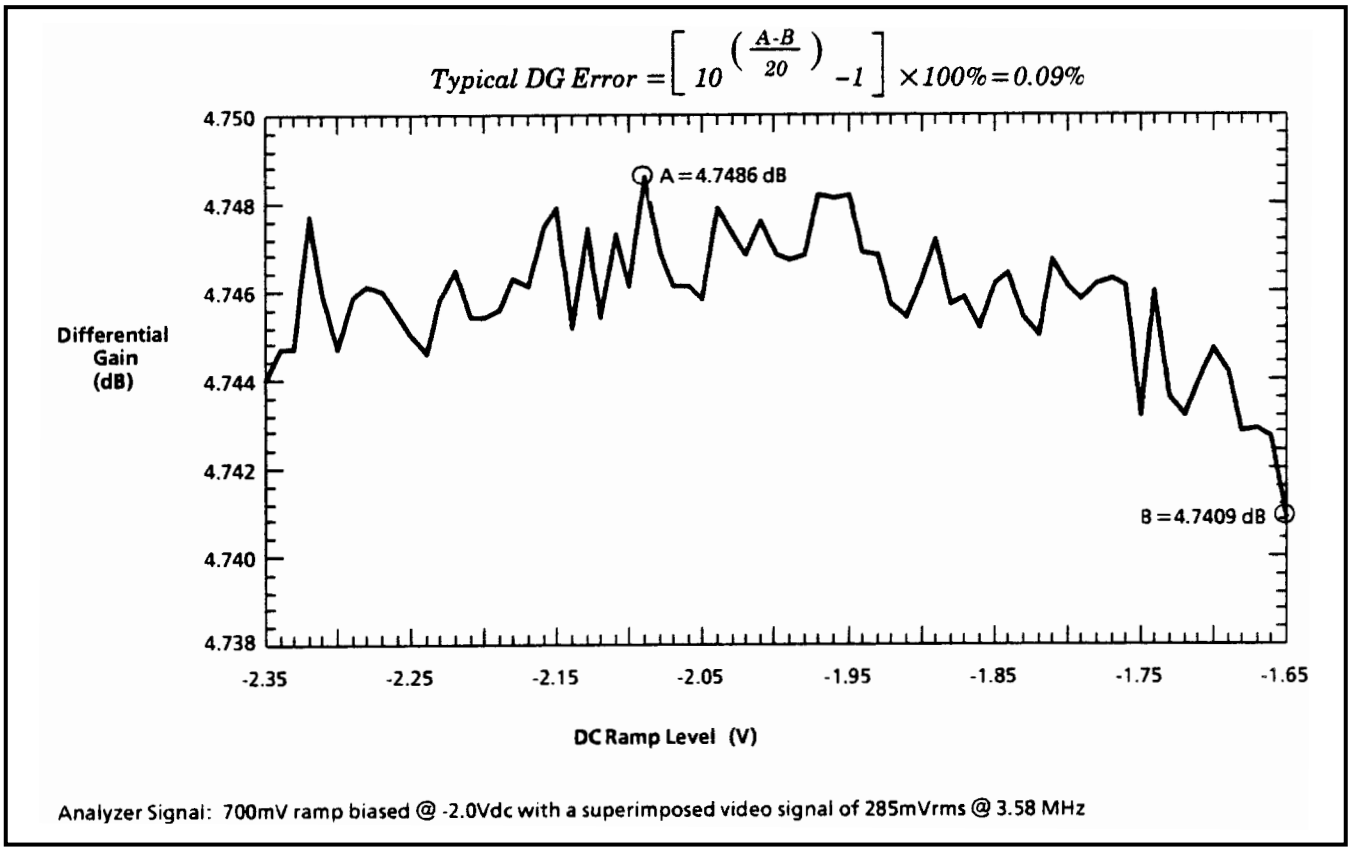


Figure 13 - Typical Differential Gain vs. Ramp Voltage

Absolute Maximum Ratings*- Voltages are with respect to V_{SS} unless otherwise stated.

	Parameter	Symbol	Min	Max	Units
1	Supply Voltage V_{DD} to V_{SS}		-0.3	15	V
	V_{DD} to V_{EE}		-0.3	15	V
	V_{SS} to V_{EE}		-0.3	15	V
	GND to V_{SS}		V_{EE} -0.3	V_{DD}+0.3	V
2	Analog Input Voltage	V_{IN}	V_{EE}-0.3	V_{DD}+0.3	V
3	Digital Input Voltage	V_{IND}	V_{SS}-0.3	V_{DD}+0.3	V
4	Continuous Current (any analog I/O terminal)			±15	mA
5	Storage Temperature		-65	+150	°C
6	Operating Temperature		-40	+85	°C
7	Package Power Dissipation			600	mW

* Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied.

Recommended Operating Conditions - Voltages are with respect to 0V unless otherwise stated.

	Characteristics	Sym	Min	Typ	Max	Units	Test Conditions
1	Supply Voltage V_{DD}-V_{EE}		4.5	12	13.2	V	
	V_{EE}-V_{SS}		-8.5		0	V	
		V_{DD}	4.5	5.0	13.2	V	V_{EE}=V_{SS}=0V
		V_{EE}	-8.5	-7.0	0	V	V_{DD}=4.5V, V_{SS}=0V
2	Analog Input Voltage	V_{IN}	V_{EE}		V_{DD}	V	
3	Digital Input Voltage	V_{IND}	V_{SS}		V_{DD}	V	
4	Analog Ground	GND	V_{EE}	0	V_{DD}	V	

DC Electrical Characteristics† - Analog Switch Characteristics

Voltages are with respect to V_{DD}=+5V, V_{EE} =-7V, V_{SS}=0V unless otherwise stated.

	Characteristics	Sym	25°C		85°C	Units	Test Conditions
			Typ‡	Max	Max		
1	On-state Resistance	R_{ON}					V_{IN}=V_{DC}=(V_{DD}+V_{EE})/2
	V_{EE}=-7V		50	65	75	Ω	
	V_{EE}=-5V		60	75	85	Ω	IV_{Xi}-$V_{Yj}I$ = 0.4V
	V_{EE}=0V		140	185	220	Ω	See Figure 7.
2	Difference in on-state resistance between switches	ΔR_{ON}	6	10	10	Ω	IV_{Xi}-$V_{Yj}I$ = 0.4V V_{IN}=V_{DC}=(V_{DD}+V_{EE})/2
3	Off-state leakage current	I_{OFF}	±10		±200	nA	V_{IN}=V_{DD} or V_{EE}
4	On-state leakage current	I_{ON}	±10		±200	nA	V_{IN}=V_{DD} or V_{EE}

† DC Electrical Characteristics are over recommended temperature range & recommended power supply voltages.
‡ Typical figures are at 25°C and are for design aid only; not guaranteed and not subject to production testing.

DC Electrical Characteristics† - Power Supplies - Voltages are with respect to V_{DD}=+5V, V_{EE} =-7V, V_{SS}=0V, $\overline{MR}$ = 0.8V unless otherwise stated.

	Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1	Positive Supply Current	I_{DD}		1	100	µA	V_{IND}=V_{DD} or V_{SS}
				0.4	1.5	mA	V_{IND}=2.4V
				5	15	mA	V_{DD}=12V, V_{SS}=V_{EE}=0V, V_{IND}=3.4V
2	Negative Supply Current	I_{EE}		1	100	µA	V_{IND}=V_{DD} or V_{SS}
				1	100	µA	V_{IND}=2.4V
				1	100	µA	V_{DD}=12V, V_{SS}=V_{EE}=0V, V_{IND}=3.4V

† DC Electrical Characteristics are over recommended temperature range & recommended power supply voltages.
‡ Typical figures are at 25°C and are for design aid only; not guaranteed and not subject to production testing.

DC Electrical Characteristics† - Digital Input/Output

Voltages are with respect to V_{DD}=5V, V_{EE}=-7V, V_{SS}=0V, unless otherwise stated.

	Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1	Input logic "1" level	V_{IH}	2			V	
		V_{IH}	3.3			V	$V_{EE}=V_{SS}=0$, V_{DD}=12V
2	Input logic "0" level	V_{IL}			0.8	V	
		V_{IL}			0.8	V	$V_{EE}=V_{SS}=0$, V_{DD}=12V
3	Input leakage (digital pins)	I_{LEAK}		±1	±10	µA	$V_{IND}=V_{DD}$ or V_{SS}
4	Data output high voltage	V_{OH}	2.4		V_{DD}	V	I_{OH}=7mA@V_{OH}=2.4V
5	Data output high current	I_{OH}	7	20		mA	source V_{OH}=2.4V
6	Data output low voltage	V_{OL}	V_{SS}		0.4	V	I_{OL}=2mA@V_{OL}=0.4V
7	Data output low current	I_{OL}	2	5		mA	sink V_{OL}=0.4V
8	Data high impedance leakage	I_{OZ}		1	10	µA	V_O=0 to V_{DD}

† DC Electrical Characteristics are over recommended temperature range and recommended power supply voltages.
‡ Typical figures are at 25°C and are for design aid only; not guaranteed and not subject to production testing.
Algebraic convention is adopted in this data sheet where the most negative value is a minimum and the most positive value is a maximum.

AC Electrical Characteristics† - Crosspoint Performance

- Voltages are with respect to V_{DD}=+5V, V_{DC}=0, V_{EE}=-7V, V_{SS}=0V, unlesss otherwise stated. Also applicable for $V_{EE}=V_{SS}=0$, V_{DD}=+12V, $V_{DC}=(V_{DD}+V_{EE})/2$.

	Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1	On-state Xi capacitance❩①	$C_{Xi\ (on)}$			56	pF	1 Xi to 1 Yi
2	On-state Yi capacitance❨②	$C_{Yi\ (on)}$			56	pF	1 Yi to 1 Xi
3	Off-state Xi capacitance❨②	$C_{Xi\ (off)}$			30	pF	
4	Off-state Yi capacitance❨②	$C_{Yi\ (off)}$			15	pF	
5	Break-before-Make interval	t_{open}		10		ns	
6	Single channel feedthrough (all crosspoints open) (see Fig. 8)	FDT		-80 -62		dB dB	R_S= R_L=75Ω V_{IN}=0.6Vpp @ 5MHz V_{IN}=0.6Vpp @ 15MHz
7	Single channel feedthrough (all crosspoints closed) (See Fig. 9)	X_{talk} (sc)		-85 -68		dB dB	R_{IN}= 10Ω, R_L= 10kΩ V_{IN}=0.6Vpp @ 5MHz V_{IN}=0.6Vpp @ 15MHz
		X_{talk} (sc)		-70 -50		dB dB	R_{IN}= 75Ω, R_L= 10kΩ V_{IN}=0.6Vpp @ 5MHz V_{IN}=0.6Vpp @ 15MHz
8	All channel crosstalk (all crosspoints closed) (See Fig. 10)	X_{talk} (ac)		-55		dB	R_{IN}= 10Ω, R_L= 10kΩ V_{IN}=0.6Vpp @ 5MHz
9	Frequency Response (see Fig.11)	f_{3dB}		200		MHz	R_S= R_L=50Ω
10	Differential Phase Error	DP		0.05		°	See Note❩①, R_S= 50Ω, R_L= 75Ω
11	Differential Gain Error	DG		0.11		%	See Note①❩, R_S= 50Ω, R_L= 75Ω

† Timing is over recommended temperature range.
‡ Typical figures are at 25°C and are for design aid only; not guaranteed and not subject to production testing.

Notes:

❩① Valid for V_{EE}=-7V, V_{DD}=+5V and V_{DC}=-2.0V. Error will increase slightly if input is biased differently.
Input test signal: 700mV ramp biased @ -2.0Vdc with a superimposed video signal of 285Vrms @ 3.58 MHz.

❨② Guaranteed by design and characterization and not subject to production testing.

AC Electrical Characteristics† - Timing Characteristics

- Voltages are with respect to V_{DD}=+5V, V_{EE}=-7V, V_{SS}=0V, R_L=1kΩ, C_L=50pF unless otherwise stated. Also applicable for V_{EE}=V_{SS}=0, V_{DD}=+12V.

	Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1	DATA to $\overline{\text{STROBE1}}$ setup	t_{ds1}	20			ns	t_{dh1} = 20ns min.
2	DATA to $\overline{\text{STROBE1}}$ hold	t_{dh1}	10			ns	t_{ds1} = 30ns min.
3	$\overline{\text{CS}}$ to $\overline{\text{STROBE1}}$ setup	t_{css1}	20			ns	
4	$\overline{\text{CS}}$ to $\overline{\text{STROBE1}}$ hold	t_{csh1}	20			ns	
5	ADDRESS to $\overline{\text{STROBE1}}$ setup	t_{ass1}	20			ns	
6	ADDRESS to $\overline{\text{STROBE1}}$ hold	t_{ash1}	20			ns	
7	$\overline{\text{STROBE1}}$ pulse width	t_{spw1}	75			ns	
8	$\overline{\text{STROBE2}}$ pulse width	t_{spw2}	75			ns	
9	R/$\overline{\text{W}}$ to $\overline{\text{STROBE1}}$ setup	t_{rwss1}	20			ns	
10	R/$\overline{\text{W}}$ to $\overline{\text{STROBE1}}$ hold	t_{rwsh1}	10			ns	
11	RESET pulse width	t_{rpw}	75			ns	
12	$\overline{\text{CS}}$ to High Z	t_{rpw}	10			ns	
13	$\overline{\text{CS}}$ to DATA output valid	t_{csov}			200	ns	
14	$\overline{\text{STROBE2}}$ to $\overline{\text{STROBE1}}$ setup	t_{s2s1}	0			ns	
15	$\overline{\text{STROBE1}}$ to $\overline{\text{STROBE2}}$ setup	t_{s1s2}	0			ns	
16	$\overline{\text{MR}}$ to switch OPEN delay 50% $\overline{\text{MR}}$ to10% Output	t_{rst}			300	ns	
17	R/$\overline{\text{W}}$ to DATA output valid	t_{rwov}			150	ns	
18	Address to DATA output valid	t_{aov}			200	ns	
19	R/$\overline{\text{W}}$ to High Z	t_{rwz}	10			ns	
20	Address to High Z	t_{az}	10			ns	
21	$\overline{\text{STROBE2}}$ to switch status delay 50% strobe to10% output change tstrobe2(on) tstrobe2(off)	 t_{son} t_{soff}		 100 100	 300 300	 ns ns	

† Timing is over recommended temperature range with V_{IH}=5V, V_{IL}=0V, V_{OH}=2.4V, V_{OL}=0.8V, R_L=3kΩ (DATA) and R_L=1kΩ (analog).
‡ Typical figures are at 25°C and are for design aid only; not guaranteed and not subject to production testing.

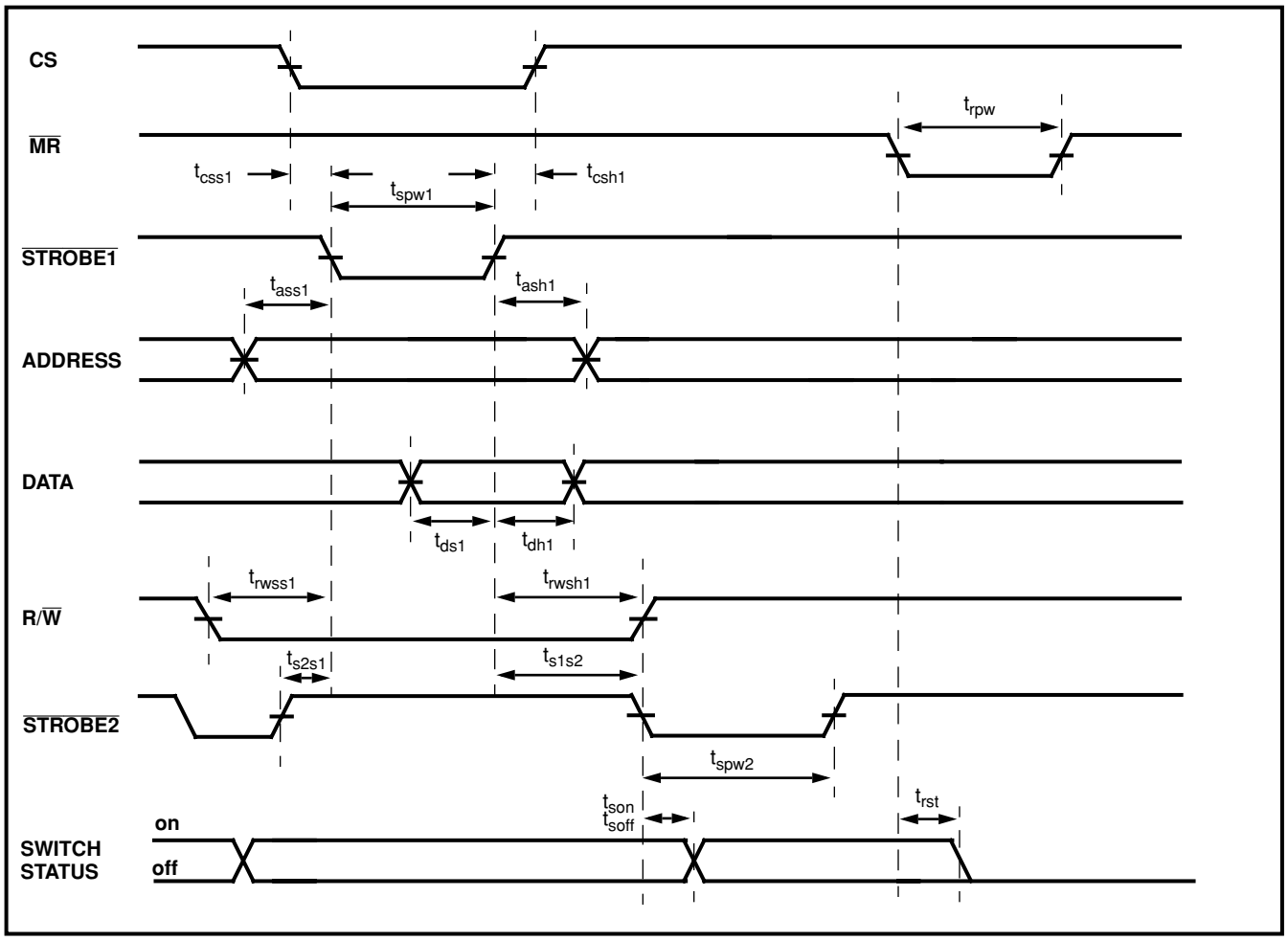
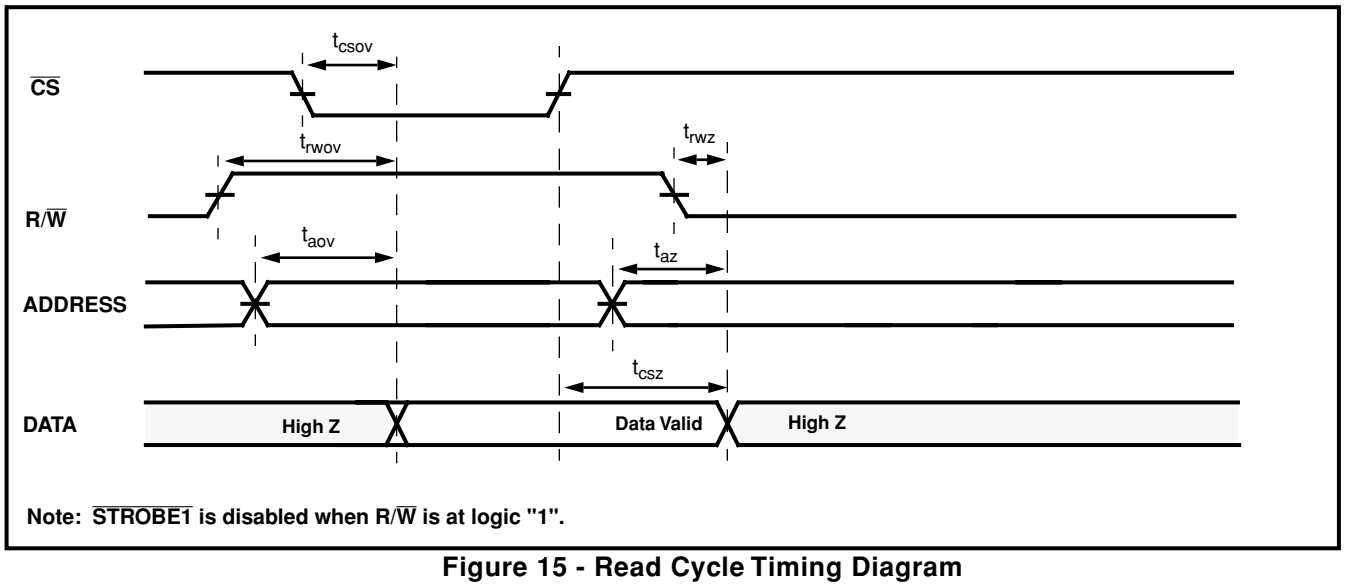
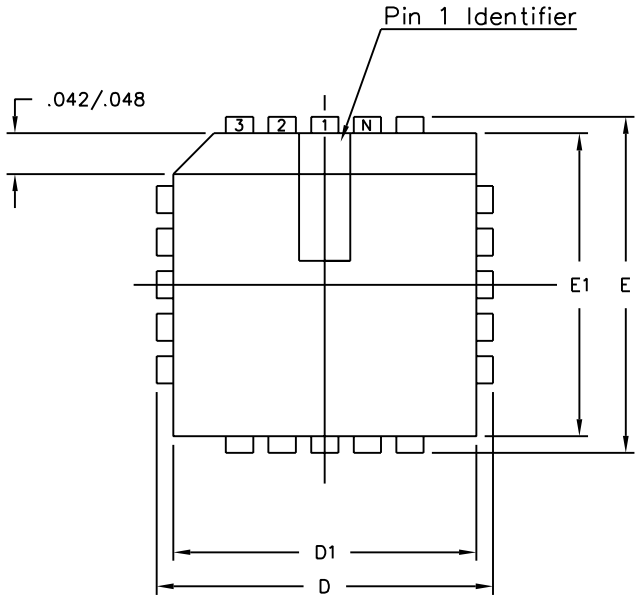


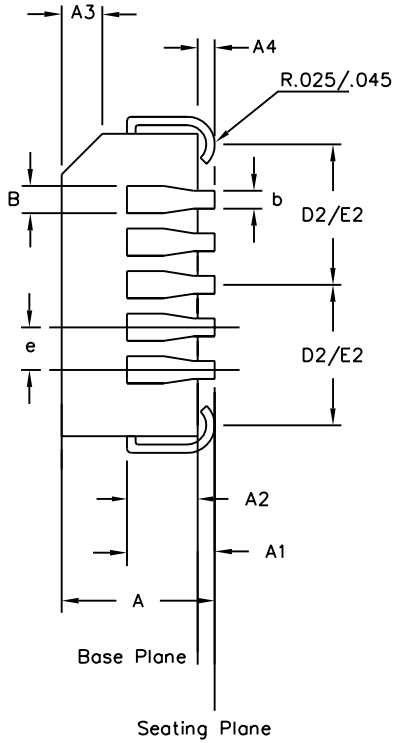
Figure 14 - Write Cycle Timing Diagram



Note: STROBE1 is disabled when R/W is at logic "1".

Figure 15 - Read Cycle Timing Diagram





Symbol	Control Dimensions in inches		Altern. Dimensions in millimetres	
	MIN	MAX	MIN	MAX
A	0.165	0.180	4.19	4.57
A1	0.090	0.120	2.29	3.05
A2	0.062	0.083	1.57	2.11
A3	0.042	0.056	1.07	1.42
A4	0.020	–	0.51	–
D	0.685	0.695	17.40	17.65
D1	0.650	0.656	16.51	16.66
D2	0.291	0.319	7.39	8.10
E	0.685	0.695	17.40	17.65
E1	0.650	0.656	16.51	16.66
E2	0.291	0.319	7.39	8.10
B	0.026	0.032	0.66	0.81
b	0.013	0.021	0.33	0.53
e	0.050 BSC		1.27 BSC	
	Pin features			
ND	11			
NE	11			
N	44			
Note	Square			
Conforms to JEDEC MS-018AC Iss. A				

Notes:
1. All dimensions and tolerances conform to ANSI Y14.5M–1982
2. Dimensions D1 and E1 do not include mould protrusions. Allowable mould protrusion is 0.010" per side. Dimensions D1 and E1 include mould protrusion mismatch and are determined at the parting line, that is D1 and E1 are measured at the extreme material condition at the upper or lower parting line.
3. Controlling dimensions in Inches.
4. "N" is the number of terminals.
5. Not To Scale
6. Dimension R required for 120° minimum bend.

ISSUE	1	2	3	
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