ANALOG DEVICES

T-51-10-12   **12-Bit Video Analog-to-Digital Converter**
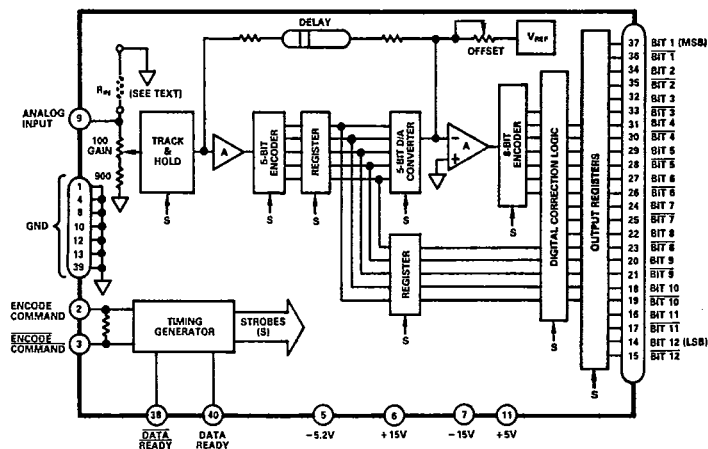
CAV-1220

FEATURES
12-Bit Resolution
20MHz Word Rate
Single 35-In² PC Board
ECL Compatible
No External Support Circuits

APPLICATIONS
Radar Digitizing
Medical Instrumentation
Digital Signal Processing
Spectrum Analysis
Transient Analysis

CAV-1220 FUNCTIONAL BLOCK DIAGRAM

3

GENERAL DESCRIPTION

The Analog Devices model CAV-1220 A/D converter is an outstanding combination of 12-bit resolution, 20MHz word rates, and small size. The unit is capable of solving a multitude of high-speed digitizing problems. Its design is based on concepts pioneered in the MOD-1020 and MOD-1205 A/D converters; and taken to an even higher level of achievement in the CAV-1210.

It is pin-for-pin compatible with the other units in the MOD and CAV series of A/D converters. But it *doubles* the word rate of its predecessor CAV-1210, making it possible for system designers to offer options or upgrade their high-resolution systems without new layouts.

This remarkable converter includes a track-and-hold, along with encoding and timing circuits. The CAV-1220 is an ideal choice for the designer who needs state-of-the-art performance in high-resolution, ultra-high speed A/D conversion.

For radar applications, 12-bits of resolution increase the dynamic

range of the converter, making it possible to detect weaker signals than would be possible with lower resolution characteristics. The high-word rates enhance ranging resolution, thereby increasing system effectiveness.

In imaging applications, the CAV-1220 increases the contrast and/or color resolution of systems in which it is used. Its high-word rates increase spatial resolution; and this combination of high resolution and high speed can materially improve system performance.

All digital inputs and outputs are ECL compatible; optimum analog input impedance can be selected by the user. The unit requires only an encode command and external power supplies for operation. The CAV-1220 is repairable and backed by Analog Devices' limited one-year warranty.

SPECIFICATIONS (typical @ +25°C with nominal power supplies unless otherwise noted) T-51-10-12

Parameter	Units	CAV-1220
RESOLUTION (FS = Full Scale)	Bits (% FS)	12 (0.024)
LSB WEIGHT		
2.048V p-p FS	mV	0.5
ACCURACY		
(Including Linearity) @ dc	% FS ± 1/2LSB	0.0125
Monotonicity		Guaranteed
Nonlinearity vs. Temperature	ppm/°C (max)	10 (15)
Offset vs. Temperature	ppm/°C (max)	220 (250)
Gain Error	% FS	2
Adjustable to Zero with On-Card Potentiometer		
Gain vs. Temperature	ppm/°C, max	150
DYNAMIC CHARACTERISTICS		
In-Band Harmonics[1]		
540kHz Input	dB Below FS, min	70
2.3MHz Input	dB Below FS, min	65
9.3MHz Input	dB Below FS, min	50
Conversion Time[2]	ns (max)	1 Clock Period + 155ns (±10)
Conversion Rate	MHz, max	20
Aperture Uncertainty (Jitter)	ps, rms max	25
Effective Aperture Delay Time[3]	ns (max)	2.5 (±2.5)
Signal to Noise Ratio (SNR)[4]	dB, (min)	66 (65)
Noise Power Ratio (NPR)[5]	dB	52
Transient Response[6]	ns	100
Overvoltage Recovery[7]	ns	200
Input Bandwidth		
Small Signal, 3dB[8]	MHz	40
Large Signal, 3dB[9]	MHz	35
Two-Tone Linearity (@ Input Frequencies)[10]		
(60kHz; 62kHz)	dB Below FS	70
(2.496MHz; 2.498MHz)	dB below FS	65
(4.996MHz; 4.998MHz)	dB below FS	60
ANALOG INPUT		
Voltage Range[11]		
Operating	V, FS	± 1.024
Maximum Without Damage	V, max	± 2
Input Type		Bipolar
Impedance	Ω	1000
Offset[12]	mV	Adjustable to Zero with On-Card Potentiometer
ENCODE COMMAND INPUT[13]		
Logic Levels, ECL-Compatible	V	"0" = −1.7
(Balanced Input)	V	"1" = −0.9
Impedance	Ω, max	100
Rise and Fall Times	ns, max	5
Width		
Min	ns	10
Max		70% of Encode Command Period
Frequency[14]	MHz	dc to 20
DIGITAL OUTPUT		
Format	Data Bits	12 Parallel; NRZ
	Data Ready and	
	Data Ready	2; RZ
Logic Levels, ECL-Compatible	V	"0" = −1.7
(Balanced Output)	V	"1" = −0.9
Drive (Line-to-Line)	Ω, min	75
Time Skew	ns, max	5
Coding		Binary (BIN); 2's Complement (2SC)
DATA READY OUTPUT		
Logic Levels, ECL-Compatible	V	"0" = −1.7
(Balanced Output)	V	"1" = −0.9
Drive (Line-to-Line)	Ω, min	75
Rise and Fall Time	ns, max	5
Duration	ns (max)	22 (±3)
POWER REQUREMENTS[15]		
+15V ±5%	mA (max)	174 (192)
−15V ±5%	mA (max)	157 (173)
+5V ±5%	mA (max)	174 (192)
−5.2V ±5%	A (max)	2.78 (3.06)
Power Consumption	W (max)	20.3 (22.3)
TEMPERATURE RANGE		
Operating	°C	0 to +70
Storage	°C	−55 to +85
Cooling Air Requirements	LFPM	500
	(Linear Feet Per Minute)	
CONSTRUCTION		
Single Printed Circuit Card	Inches	7.0 × 5.0 × 0.5

For Applications Help, Call Computer Labs Division @ (919) 668-9511.

OUTLINE DIMENSIONS
Dimensions shown in inches and (mm).
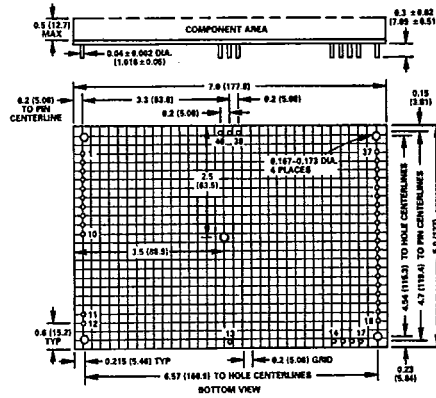
PIN DESIGNATIONS

PIN	FUNCTION	PIN	FUNCTION
1	GROUND	40	DATA READY
2	ENCODE COMMAND	39	GROUND
3	ENCODE COMMAND	38	DATA READY
4	GROUND	37	BIT 1 (MSB)
5	−5.2V	36	BIT 1 (MSB)
6	+15V	35	BIT 2
7	−15V	34	BIT 2
8	GROUND	33	BIT 3
9	ANALOG INPUT	32	BIT 3
10	GROUND	31	BIT 4
11	+5V	30	BIT 4
12	GROUND	29	BIT 5
13	GROUND	28	BIT 5
14	BIT 12 (LSB)	27	BIT 6
15	BIT 12 (LSB)	26	BIT 6
16	BIT 11	25	BIT 7
17	BIT 11	24	BIT 7
18	BIT 10	23	BIT 8
19	BIT 10	22	BIT 8
20	BIT 9	21	BIT 9

NOTES
[1] In-Band Harmonics expressed in terms of spurious in-band signals and harmonics generated at 20MHz encode rate.
[2] Measured from leading edge Encode Command to trailing edge Data Ready; use trailing edge to strobe output data into external circuits (see text).
[3] See text for description of Effective Aperture Delay Time.
[4] Rms signal to rms noise ratio with full-scale 540kHz analog input (see Figure 3).
[5] Dc to 8.2MHz white noise bandwidth with slot frequency of 3.886MHz; and encode rate of 20MHz.
[6] For full-scale step input, 12-bit accuracy attained in specified time.
[7] Recovers to 12-bit accuracy in specified time after 2 × FS input overvoltage.
[8] With analog input 40dB below FS.
[9] With FS analog input. (Large-signal bandwidth flat within 0.2dB, dc to 10MHz).
[10] Both frequencies applied at level 7dB below full scale.
[11] Standard bipolar input is adjustable ±5% with on-card potentiometer (see text and Figure 2). Unipolar 0 to +2V input range is available on special order; consult factory for details.
[12] Adjustable ±15mV without performance degradation (see text and Figure 2).
[13] Digital "0" to digital "1" transition initiates encoding.
[14] Encode rate specified by customer; see Ordering Information. Units operated outside ±10% of specified frequency (up to maximum 20MHz) must be returned to factory for recalibration. For operation at word rates below 500kHz, consult factory.
[15] ±15V must be equal and opposite within 200mV and track over temperature.

Specifications subject to change without notice.

THEORY OF OPERATION

Refer to the block diagram of the CAV-1220.

Analog input signals to be digitized are applied to a track-and-hold (T/H) amplifier, which is normally operating as a buffer amplifier in the "track" mode, following all changes in analog input as they occur. The user of the CAV-1220 determines the point at which the analog signal is to be digitized by applying an Encode Command.

The leading edge of the ECL-compatible encode command causes the track-and-hold to switch momentarily to the "hold" mode of operation, "freezing" the analog input signal long enough to begin the digitizing process. The instant this switching action occurs is affected by one of the parameters of the CAV-1220, called out as Effective Aperture Delay Time in the Specifications table.

Basically, effective aperture delay time is a measure of the difference between the converter's digital and analog delays $(t_d - t_a)$ and can assume a zero, positive, or negative value depending on the comparative lengths of the two delays. In the CAV-1220, the analog delay (t_a) is less than the digital delay (t_d), and causes effective aperture delay to be typically 2.5ns.

The "held" value of analog signal at the output of the T/H is applied to a 5-bit encoder. It is also applied to an analog delay circuit, whose time delay is equal to the interval required for the first step of the digitizing/reconstruction process.

The digitized signal is applied to a 5-bit D/A converter which has 12-bit accuracy. Via registers, the same digital signal is directed to the digital correction logic circuits. The stored data will represent Bits 1–5 of the 12-bit digital output of the CAV-1220.

The reconstructed output of the D/A converter becomes one input to an operational amplifier; its other input is the delayed analog signal from the delay line. The output of the wideband, fast-settling op amp represents the residue which remains after a 5-bit digital representation of the analog input has been subtracted from that input.

This residue, or error, signal is encoded by a second encoder and is applied as 8-bit digital information to the digital correction logic circuits which contain Bits 1–5.

The correction circuits combine the 5-bit and 8-bit bytes of data to compensate for possible nonlinearities and other errors to assure the final 12-bit output of the CAV-1220 is 12-bit accurate.

Expressed in its simplest terms, the digital correction logic circuits use the information in the 8-bit signal to determine what modifications of Bits 1-5 may be necessary. The value of the MSB in the 8-bit byte establishes whether the 5-bit data are passed "as is" or whether they are increased by a value of binary "1". The remaining bits (2-8) of the 8-bit byte become Bits 6-12 of the CAV-1220 digital output.

Digitally corrected subranging (DCS), the innovative technique described here, helps compensate for a wide range of potential errors which could otherwise be avoided only if the CAV-1220 design included expensive, high precision components.

The use of 13 bits to obtain an accurate 12 bits of output cannot prevent gain error, track/hold droop error, linearity error, offset error, or any of the other inherent characteristics of "real-world" A/D converters. But DCS can, and does, help nullify their effects and makes it economically feasible to accomplish high-speed, high-resolution digitizing of analog signals.
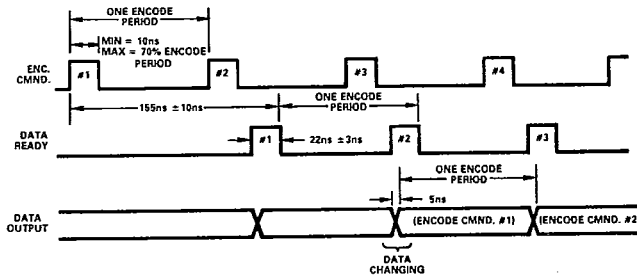

Figure 1. CAV-1220 Timing Diagram

CAV-1220 TIMING

Refer to Figure 1, the CAV-1220 Timing Diagram.

The intervals shown represent a continuous update rate of approximately 10MHz, which is considerably below the maximum capabilities of the CAV-1220. But that frequency helps illustrate the "pipeline delay" characteristic of the converter.

At this word rate, spacing between encode commands is approximately 100 nanoseconds; and three encode commands have occurred before the data associated with the first command are valid. In Figure 1, this pipeline delay has a total time of approximately 255 nanoseconds (155ns + 100ns). This interval will be different at other word rates, but will always include 155ns; depending upon the update rate, either more or fewer encode commands may occur before the first data are available.

After the initial delay, valid data will be available at the word rate dictated by encode commands. Note the spacing between

Encode Command #1 and Encode Command #2 is equal to one encode period. This is the same spacing as that between Data Ready #1 and Data Ready #2; and is also the spacing between the first and second groups of valid data.

System timing can be adjusted as necessary to take into account the pipeline delay effects and assure that the data of interest are strobed out of the converter at the appropriate time.

Figure 1 also illustrates why the trailing edge of the Data Ready pulse is recommended as the strobe for output data. Typically, data begin changing 5ns after the leading (rising) edge of each Data Ready pulse; they will be fully settled at the time of the trailing (falling) edge and available for use in external circuits.

Another possibility for strobing the output data is to use the DATA READY pulse. Its leading edge occurs at the same time as the trailing edge of the DATA READY signal, but is a rising edge, which may facilitate its use as a strobe.

ANALOG INPUT IMPEDANCE

Refer again to the block diagram of the CAV-1220 and note the resistor shown in dashed lines and designated as R$_{IN}$.

This resistor value is chosen by the user to allow the analog input impedance of the CAV-1220 to be matched to the characteristic impedance of the analog signal source.

Without an added resistor, the input impedance of the unit is 1,000Ω; this is the series total of the GAIN control and the 900Ω resistor shown in the block diagram.

When a resistor is added, it is in parallel with the internal impedance of the CAV-1220; various values of resistors can be used to obtain standard impedances:

Desired Input Impedance	Value for R$_{IN}$
50 ohms	52.3 ohms
75 ohms	80.6 ohms
93 ohms	102 ohms
100 ohms	110 ohms

For an input impedance (Z) different from those shown above, the correct resistor value can be established with the equation:

$$\frac{1}{R_{IN}} = \frac{1}{Z} - \frac{1}{1k}$$

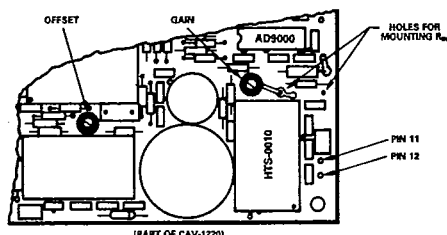The physical location of R$_{IN}$ is shown in Figure 2.

Figure 2. CAV-1220 Adjustment Controls

OFFSET AND GAIN ADJUSTMENTS

The design and manufacture of the CAV-1220 A/D converter are innovative and precise, and have resulted in a high-performance converter which is virtually adjustment-free. This elimination of variable controls helps make the unit less susceptible to performance degradation caused by vibration, shock, or inadvertent and/or incorrect adjustment.

Despite the complexity of the circuits required to obtain high-resolution digitizing at high speeds, there are only two control settings used in the unit. Factory adjustments during final calibration use selected fixed resistors to assure optimum performance without a need for "tweaking" by the user.

Only OFFSET and GAIN controls are available, and even these are sealed at the factory before shipment. In those rare instances where they may require readjustment, the procedure outlined below is one which should be used.

Refer to Figure 2, the CAV-1220 Adjustment Controls.

When adjusting offset and gain of the CAV-1220 in the system, the OFFSET control should be adjusted first. The adjustment sequence is:

1. Apply to the analog input a precise (±0.25mV) dc level corresponding to midscale of the desired input range. (For standard units with ±1V range, this is 0V input.)

2. Adjust OFFSET control while observing MSB (Bit 1); adjust for MSB "toggling" between digital "0" and digital "1".

3. Apply a precise (±0.25mV) dc level corresponding to the most negative excursion of the desired input range. (For standard units, this is −1V input.)   *T-51-10-12*

4. Adjust GAIN control while observing LSB (Bit 12); adjust for output of Bits 1–11 solid "0" with LSB "toggling".

5. Apply a precise (±0.25mV) dc level corresponding to the most positive excursion of the desired input range. (For standard units, this is +1V input.)

6. Check digital output to assure Bits 1–11 are solid "1" with LSB "toggling".

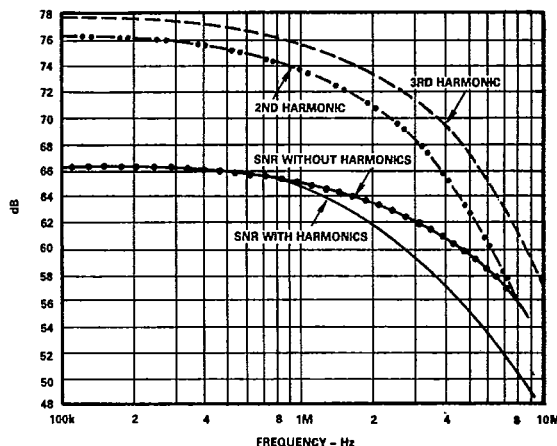7. Adjust OFFSET and GAIN controls alternately as necessary to obtain analog input range to tolerance of ±1/2LSB.

Figure 3. CAV-1220 SNR and Harmonics

DYNAMIC PERFORMANCE

Figure 3 shows typical performance on some of the dynamic characteristics which play an important role in the performance of systems using the CAV-1220 A/D converter.

The A/D was calibrated in final test for an encode rate of 20MHz. As shown, signal-to-noise ratio (SNR) with harmonics is typically 66dB at an input frequency of 100kHz; and remains greater than 50dB for full-scale inputs of 8MHz. As expected, SNR without harmonics is better and is typically 56dB at 8MHz.

The level of 2nd and 3rd harmonics at a word rate of 20MHz is also depicted; in these characteristics, too, the CAV-1220 displays exceptional performance.

ORDERING INFORMATION

For standard CAV-1220 units, order by model number CAV-1220-XXX; XXX is specified by the customer to indicate the desired optimized word rate. The decimal place is assumed (but not shown) between the second and third places. CAV-1220-150, for example, indicates final calibration and optimum performance at 15MHz.

Optimum performance will be achieved within a band of frequencies approximately ±10% around the selected word rate; but the maximum rate of 20MHz must be considered. If later applications require word rates beyond the limits of the original optimum frequency, the unit must be returned to the factory for calibration; there is a nominal charge for this service.

Mating sockets for the CAV-1220 converters are model number MSB-2 (thru hole) or MSB-3 (closed end). These are individual solder-type pin sockets for mounting the A/D on PC boards.