MICRO NETWORKS

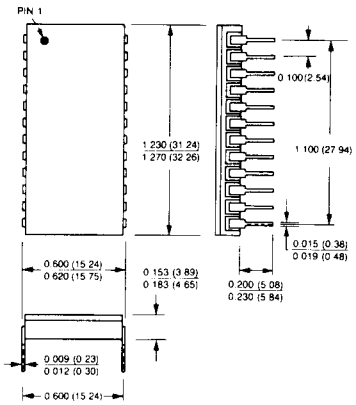
MN4000

40nsec 12-Bit LINEAR
T/H AMPLIFIER

FEATURES

- ±0.024% FSR Maximum Gain Linearity Error
- 40nsec Full Scale Acquisition Time (to 0.01%FSR)
- Low 30mVp-p T/H Transient
- Fast 25nsec T/H Transient Settling Time
- 50MHz Small Signal Bandwidth
- Functionally Compatible with Industry Standard −0010/0025
- DESC SMD 5962-90856 Listed
- Full Mil Operation −55°C to +125°C
- MIL-H-38534 Screening Optional. MIL-STD-1772 Qualified Facility

24-PIN SIDE BRAZED DIP



Dimensions in Inches (millimeters)

DESCRIPTION

The MN4000 is a very high-speed (40nsec signal acquisition to ±0.01%FSR), high-resolution (±0.024%FSR maximum gain linearity error), unity-gain, non-inverting track-hold (T/H) amplifier. The MN4000 is suitable for applications where high-speed performance is required in conjuction with high-resolution.

The MN4000 is packaged in a small, 24-pin, hermetically sealed, side-brazed DIP and maintains an established, industry-standard pinout making it a functionally compatible, performance upgrade in applications utilizing −0010/0025 type devices.

The MN4000 is available fully specified for either 0°C to +70°C or −55° to +125°C (H, H/B and H/B CH models) operation. For military/aerospace or harsh-environment commercial/industrial applications, the MN4000 H/B is available environmentally stress screened. Consult factory for availability of MN4000 H/B CH. Additionally, the MN4000 is listed on DESC SMD 5962-90856.

APPLICATIONS

High-Speed Signal Processing
RADAR and IF Processors
Instrumentation Systems
EW and ECM Systems
Video Digitizers
Communications Systems
Subranging A/D Converters

MN4000

MICRO NETWORKS
324 Clark St., Worcester, MA 01606 (508) 852-5400

MN4000 40nsec 12-Bit LINEAR T/H AMPLIFIER

ABSOLUTE MAXIMUM RATINGS

Operating Temperature Range:	−55°C to +125°C
Specified Temperature Range:	
MN4000	0°C to +70°C
MN4000H, H/B	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
± 15V Supply (± V_{CC}, Pins 22, 3)	± 18 Volts
+5V Supply (± V_{DD}, Pin 9)	−0.5 to +6.5 Volts
−5.2V Supply (± V_{CC}, Pin 4)	+0.5 to −6.5 Volts
Analog Input (Pin 13)	± 2 Volts
Digital Input (Pin 5)	0 to −3 Volts

ORDERING INFORMATION

PART NUMBER **MN4000H/BCH**

Standard device is specified for 0°C to +70° operation.
Add "H" suffix for specified −55°C to +125°C operation.
Add "/B" suffix to "H" model for environmental stress screening.
Add "CH" to H/B models for 100% screening according to MIL-H-38534. Consult factory for availability of "CH" devices.

SPECIFICATIONS (T_A = +25°C, Supply Voltages ± 15V, +5V and −5.2V unless otherwise indicated) (Note 1)

ANALOG INPUT/OUTPUT	MIN.	TYP.	MAX.	UNITS
Input/Output Voltage Range (Note 2)	± 1			Volts
Input Impedance (Note 2)	10			kΩ
Output Current (Note 2)	± 25			mA
Output Impedance (Note 2)		0.25	0.5	Ω
DIGITAL INPUT				
Logic Levels: Logic "1"	−0.8			Volts
Logic "0"			−1.8	Volts
Logic Currents: Logic "1" (V_{IH} = −0.8V)			± 500	μA
Logic "0" (V_{IL} = −1.8V)			± 500	μA
TRANSFER CHARACTERISTICS				
Gain		+1		V/V
Gain Error: Initial (+25°C)		±0.25	±0.5	%FSR
Over Temperature		± 1	± 2	%FSR
Gain Linearity Error		±0.012	±0.024	%FSR
Input Offset Voltage: Intial (+25°C)		±1	±5	mV
Over Temperature		±10	± 15	mV
Pedestal: Initial (+25°C)		±2	±7	mV
Over Temperature		±10	± 15	mV
DYNAMIC CHARACTERISTICS				
Acquisition Time: 2V Step to ± 0.1% (± 2mV)		30	50	nsec
2V Step to ± 0.01% (± 0.2mV, Note 2)		40	60	nsec
Track-to-Hold Transient: Height (Peak to Peak)		20	30	mVp-p
Settling Time (to ± 2mV)		25	30	nsec
Aperture Delay Time			5	nsec
Aperture Jitter (Note 2)			± 20	ps (rms)
Slew Rate (V_{IN} = −1V to +1V Step) (Note 2)	200	250		V/μsec
Small Signal Bandwidth (V_{IN} = 1V AC p-p) (Note 2)	50	60		MHz
Large Signal Bandwidth (V_{IN} = 2V p-p) (Note 2)		40		MHz
Feedthrough Attenuation (V_{IN} = 2V p-p @ 5 MHz)	60	72		dB
Droop Rate: Initial (+25°C)		50	200	μV/μsec
Over Temperature			20	mV/μsec
Harmonic Distortion (Track Mode, V_{IN} = ± 1V, 5MHz)		−72		dB
POWER SUPPLY REQUIREMENTS				
Power Supply Range: +V_{CC} Supply	+14.55	+15	+15.45	Volts
−V_{CC} Supply	−14.55	−15	−15.45	Volts
+V_{DD} Supply	+4.75	+5	+5.25	Volts
−V_{EE} Supply	−5.0	−5.2	−5.7	Volts
Current Drain: +V_{CC} Supply		+8	+10	mA
−V_{CC} Supply		−8	−10	mA
+V_{DD} Supply		+50	+70	mA
−V_{EE} Supply		−50	−70	mA
Power Supply Rejection Ratio: +V_{CC} Supply		± 8	± 15	mV/V
−V_{CC} Supply		± 8	± 15	mV/V
+V_{DD} Supply		± 8	± 15	mV/V
−V_{EE} Supply		± 8	± 15	mV/V
Power Consumption		750	1014	mW

SPECIFICATION NOTES:
1. R_L = 100Ω, C_L = 50pF.
2. These parameters are listed for reference only and are not tested.

APPLICATIONS INFORMATION

LAYOUT CONSIDERATIONS — The MN4000 is a high-resolution high-speed device and requires that careful attention be paid to layout, grounding and bypassing in order to achieve specified accuracy and speed performance. Coupling between analog input and digital signals should be minimized to avoid noise pickup. Care should be taken to avoid long analog runs in parallel with the digital lines. In addition, particular attention must be paid to the device's external hold capacitor connection. Pin 20 should be isolated from digital signals and it is recommended that the pin be shielded by ground.

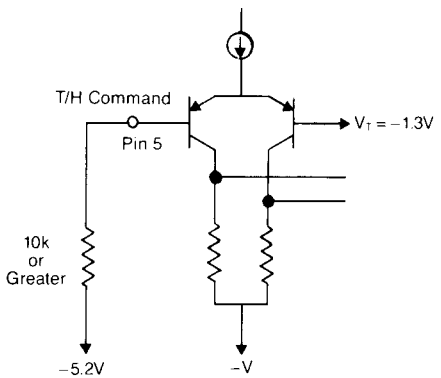
The units five ground pins (pins 7, 11, 18, 19, and 21) should be tied together at the device and connected to system analog ground preferably through a large, low-impedance analog ground plane beneath the device.

If p.c. card ground runs must be run separately, wide conductor runs should be employed with 0.01uF ceramic capacitors interconnecting them as close to the device as possible.

Power supply connections should be as short and direct as possible, and all power supplies should be decoupled with high-frequency bypass capacitors to ground. It is recommended that 1μF tantalum capacitors in parallel with 0.01μF ceramic, surface-mount chip capacitors be located as close to the device pins as possible.

TRACK-HOLD COMMAND — A Logic "0" applied to the Track-Hold (T/H) Command input (pin 5) drives the device into the track (sample) mode. In this mode, the MN4000 operates as a unity gain amplifier (follower) and its output tracks (follows) the applied analog input signal. A Logic "1" applied to the T/H Command (pin 5) drives the MN4000 into the hold mode holding the output of the device constant at the level present when the hold command was given.

The MN4000's T/H Command input is illustrated below. This input is compatible with ECL logic devices. However, precautions should be taken in certain test circuits where the T/H Command input is not driven with standard ECL logic devices (burn-in and life test circuits for example). Care should be taken to avoid exceeding the absolute maximum ratings when hardwiring this input to negative supply voltages. In these cases when the T/H Command input is connected to a voltage supply, we recommend the use of a series 10kΩ or greater resistor as shown below.



MN4000 ACQUISITION TIME — The MN4000's signal acquisition time is specified for full scale steps settling to a specified limit (± 0.1%FSR for 10-bit applications and ± 0.01%FSR for 12-bit applications). It is important to note, for the purpose of comparision, that Micro Networks specifies this parameter from the edge of the applied T/H Command to the point where the T/H output has settled to within the specified band. The acquisition time of the MN4000 includes the gate delay of the switch, output amplifier delay, effects of slew rate and the actual settling of the output signal. For further discussion of acquisition time and other T/H amplifier related specifications, refer to the data book tutorial section labeled Track and Hold Amplifiers.

DRIVING CAPACITIVE LOADS — Care must be taken to optimize the performance of the MN4000 in circuit applications with high capacitive loading at the megahertz frequencies these devices are designed to handle. In particular, the series inductance of the wire or p.c. card run connecting the MN4000 to its capacitive load is no longer insignificant. In order to obtain the quickest settling at the load in response to a driving function at the T/H output, it will be necessary to add a series resisitor such that the resulting RLC circuit is critically damped. The value of the damping resisitor will depend upon the length of the wire (or run) and the load capacitance.

Critical damping occurs in a series RLC circuit when the resonant radian frequency (ωo) equals the exponential damping coefficient (α).

Since $\omega_o = 1/\sqrt{LC}$

and $\alpha = R/2L$

it follows that $R = 2\sqrt{L/C}$

Where R is required value of series resistance, L is the wire (or run) inductance and C is the load capacitance. In making calculations, an inductance of 23nHy/in. can be assumed for straight, solid wire of AWG 20 to 28, or p.c. runs of 100 to 600mil² cross-sectional area. This value should also serve as a good starting point for experimentation if other shapes or wire sizes are used. Bear in mind that critical damping only guaranteed best settling for a given combination of L and C. There will still be practical limits on the values these can assume if settling is to be accomplished in a reasonable time.

The voltage at the load capacitor will be the form

$$V(t) = A\{1-(\alpha t + 1)e^{-\alpha t}\}$$

in response to a step of amplitude A at the T/H output. For settling to 0.1%, v(t) = 0.999A and, from the equation above, $\alpha t = 9.23$. Since $\alpha = \omega o = 1/\sqrt{LC}$, it follows that the settling to ± 0.01% of the step size occurs at the $t = 9.23\sqrt{LC}$.

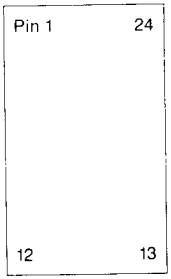
As an example, assume C_{LOAD} = 200pF and that it is 2.2 inches from the T/H ouput. This corresponds to a wire inductance of L=23nHy/in. × 2.2in.=51nHy. For critical damping, $R=2\sqrt{L/C}$ =32Ω. This resistor should be a carbon or other non-inductive type, and its length will count as part of the inductance to be damped. With C and L as above the settling time to ± 0.1% will be

$$t=9.23\sqrt{LC} = 30nsec.$$

The actual settling time in any given situation will be somewhat longer than predicted above due to the effects of the settling time of the T/H itself. A very good approximation of the overall settling time can be obtained by assuming the two components add as the square root of the sum of their squares. In the above example, assuming 30nsec settling time for the T/H to ± 0.1%, this would mean $\sqrt{30^2+30^2}$, or about 42nsec total settling from the time a step is applied to the input of the T/H to the time voltage seen be the A/D settles to ± 0.1% of its final value.

For 12-bit applications the calculations are as shown above where settling is specified to ± 0.01% and settling occurs at $11.75\sqrt{LC}$.

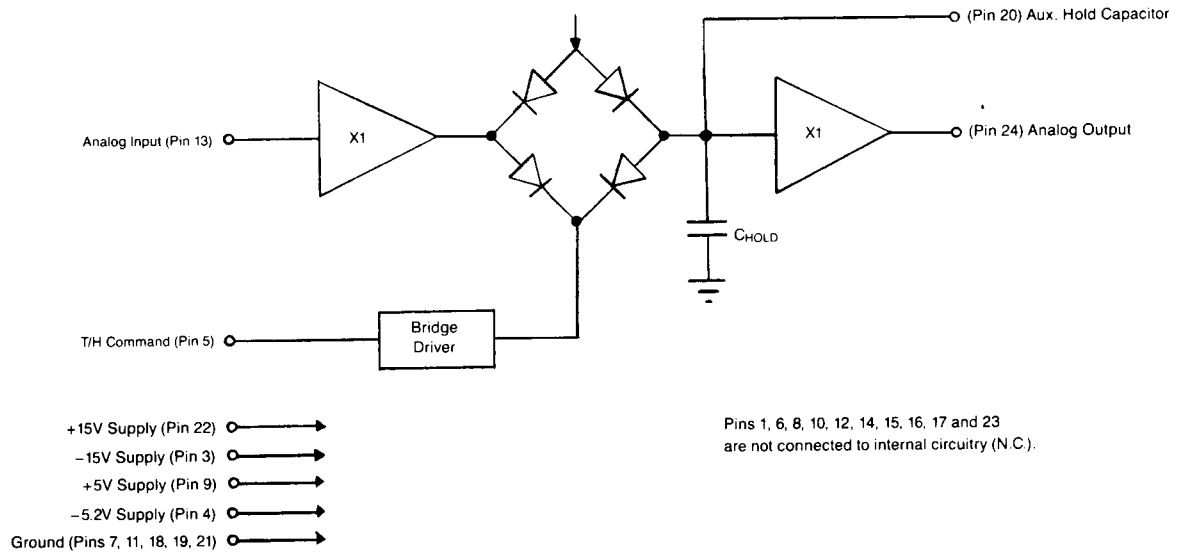
PIN DESIGNATIONS



1	N.C.	24	Analog Output
2	N.C.	23	N.C.
3	−15V Supply	22	+15V Supply
4	−5.2V Supply	21	Ground
5	Hold Command	20	Aux Hold Capacitor
6	N.C.	19	Ground
7	Ground	18	Ground
8	N.C.	17	N.C.
9	+5V Supply	16	N.C.
10	N.C.	15	N.C.
11	Ground	14	N.C.
12	N.C.	13	Analog Input

Notes:
"No Connects" (N.C.) are not connected to internal circuitry.

BLOCK DIAGRAM



Pins 1, 6, 8, 10, 12, 14, 15, 16, 17 and 23 are not connected to internal circuitry (N.C.).