QS7785CF/QS7785PF

QSound Multi-Speaker System

Device Specifications - Preliminary Information

Overview:

The QS7785 is a 3D audio processor IC that creates 5 speaker surround sounds from 2 channel stereo source using QSurround™ technology developed and licensed by QSound Labs, Inc. This chip synthesizes and outputs surround sounds from 2 channel stereo signal for surround speakers as well as an enhanced stereo sound for front speakers.

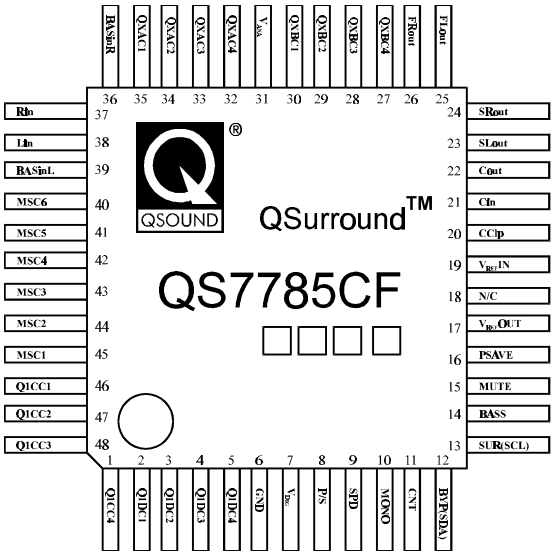
Feature:

- 3D synthesized surround sound for left and right surround speakers
- 3D stereo sound enhancement for left and right front speakers
- Center speaker output
- Parallel and serial digital interface for mode control
  - QS7785CF for I^2C 2 control pins serial interface
  - QS7785PF for 3 control pins serial interface (Data, Clock and Strobe)
- DC 5 to 13 volt supply
- 48-pin QFP packaging

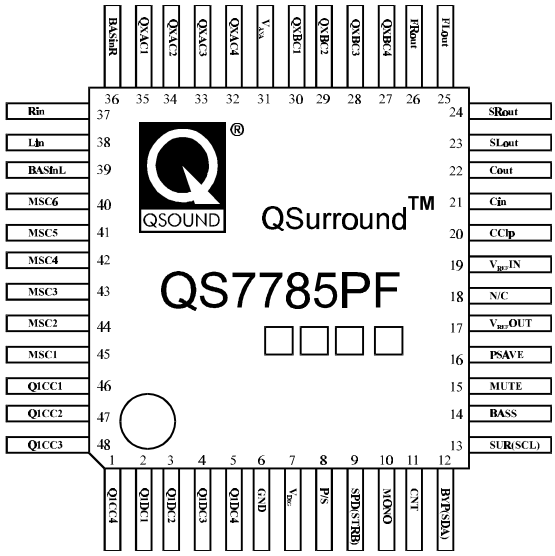
Application:

- Audio systems including TV, AV amps, DVD, VCD, SVCD and VCR
- Resynthesis of multi-speaker output from down-mixed surround source. (DVD etc)
- Car audio
- Computer-based multimedia products, including sound cards, powered loud speakers

Pin Configuration:

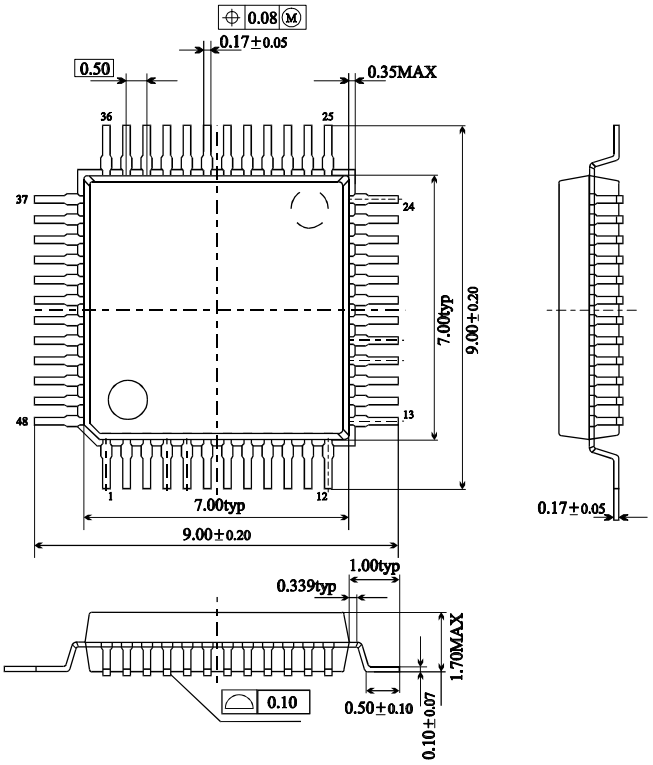


I^2C Serial Interface

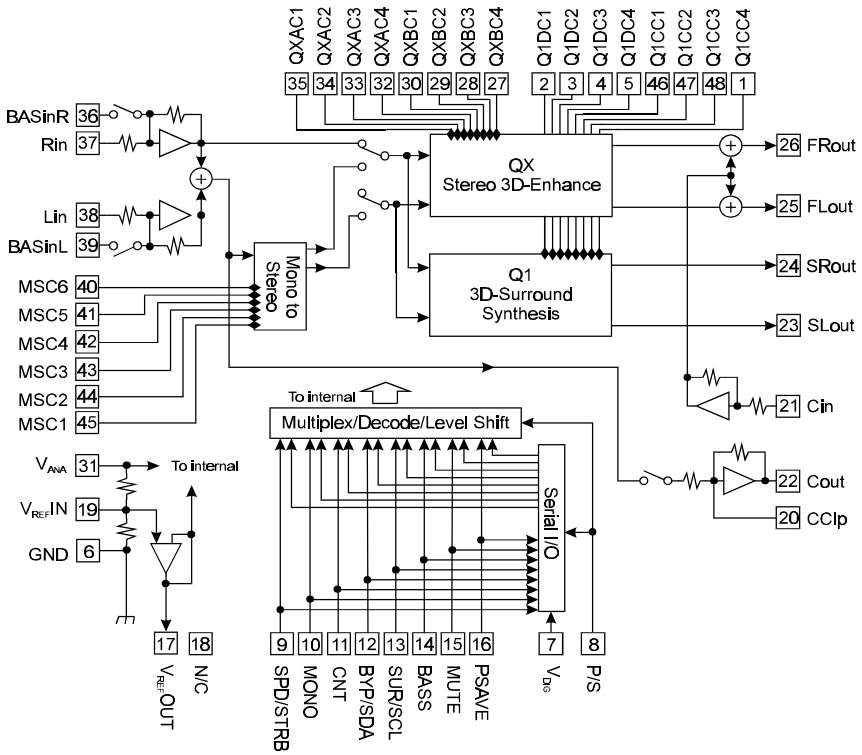


3 Controls Serial Interface

Packaging Dimension:



IC Block Diagram:



Pin Functions:

Number	Name		I/O	Description
	Parallel	Serial		
1	Q1CC4		O	Capacitor
2	Q1DC1		I	Capacitor
3	Q1DC2		I	Capacitor
4	Q1DC3		I	Capacitor
5	Q1DC4		I	Capacitor
6	GND		-	Ground
7	V_{DIG}		-	Digital power supply
8	P/S		I	Interface mode control (H: parallel I/O, L: serial I/O)
9	SPD		I	Front enhancementcontrol (H: high spread, L: low spread)
		STRB	I	Serial data strobe(Not applicable to I^2C of QS7785CF)
10	MONO		I	Monaural to virtual stereo control (See operating mode for detail)
11	CNT		I	Center output control (H: center on, L: center off)
12	BYP		I	Bypass control (See operating mode for detail)
		SDA	I/O	Serial data input (also ACK data output for I^2C of QS7785CF)
13	SUR		I	Surround output control (See operating mode for detail)
		SCL	I	Serial data shift clock
14	BASS		I	Bass boost control (H: on, L: off)
15	MUTE		I	Output mute control (H: mute on, L: mute off)
16	PSAVE		I	Power save control (H: power save on, L: power save off)
17	V_{REF}OUT		O	Buffered reference voltage ($V_{ANA}/2$)
18	N/C (Not used)		-	-
19	V_{REF}IN		-	Signal reference input (Self biased to $V_{ANA}/2$)
20	CClp		I	Capacitor
21	CIN		I	Center signal input to mix with front signal
22	COUT		O	Center signal output
23	SLOUT		O	Surround left signal output
24	SROUT		O	Surround right signal output
25	FLOUT		O	Front left signal output
26	FROUT		O	Front right signal output
27	QXBC4		I	Capacitor
28	QXBC3		I	Capacitor
29	QXBC2		I	Capacitor
30	QXBC1		I	Capacitor
31	V_{ANA}		-	Analog power supply
32	QXAC4		I	Capacitor
33	QXAC3		I	Capacitor
34	QXAC2		I	Capacitor
35	QXAC1		I	Capacitor
36	BASinR		I	Auxiliary right input for the bass boost (Enabled on BASS = H)
37	RIN		I	Right channel signal input
38	LIN		I	Left channel signal input
39	BASinL		I	Auxiliary left input for the bass boost (Enabled on BASS = H)
40	MSC6		I	Capacitor
41	MSC5		I	Capacitor
42	MSC4		I	Capacitor
43	MSC3		I	Capacitor
44	MSC2		I	Capacitor
45	MSC1		I	Capacitor
46	Q1CC1		I	Capacitor
47	Q1CC2		I	Capacitor
48	Q1CC3		I	Capacitor

Electrical Specification:

Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Supply voltage range (analog)	V_{ANA}	-0.3 to 15, and $V_{ANA}>V_{DIG}$-0.3	V
Supply voltage range (digital)	V_{DIG}	-0.3 to 7	V
Input voltage range (analog)	V_{IANA}	-0.3 to V_{ANA} +0.3	V
Input voltage range (digital)	V_{IDIG}	-0.3 to V_{DIG} +0.3	V
Power dissipation	P_D		mW
Storage temperature range	Tstg	-40 to 125	°C
Soldering temperature	T_{SLD}	255	°C
Soldering time	t_{SLD}	10	Sec

Recommended Operating Condition

Parameter	Symbol	Limits	Unit
Operating voltage (analog)	V_{ANA}	5 to 13 and $V_{ANA}\geq V_{DIG}$	V
Operating voltage (digital)	V_{DIG}	4.5 to 5.5	V
Operating temperature range	T_{OPR}	0 to 70	°C

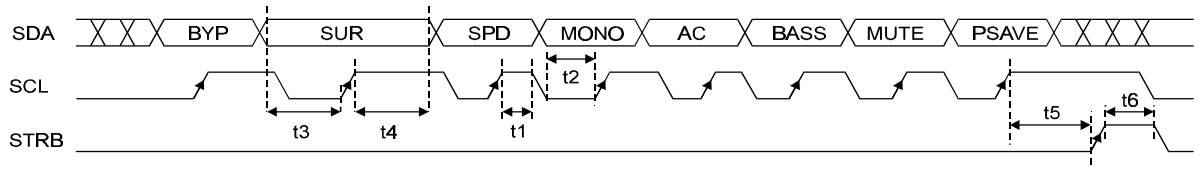
Electrical Chracteristics

(V_{ANA}=9V,V_{DIG}=5V TA=25°C unless otherwise noted)

Parameter	Symbol	Condition	Limits/min	Limits/typ	Limits/max	Unit
Input voltage	V_{IN1}				1.1	V_{RMS}
Analog input impedance1	Z_{AIN1}	L_{IN}, R_{IN}		20		kΩ
Analog input impedance2	Z_{AIN2}	C_{IN}		10		kΩ
Reference voltage out	V_{REFOUT}			V_{ANA}/2		V
HIGH level input voltage	V_{IH}		2.4			V
LOW level input voltage	V_{IL}				0.5	V
HIGH level input current	I_{IH}	$V_{IN}=V_{CC}$				µA
LOW level input current	I_{IL}	V_{IN}=GND				µA
SCL width HIGH	t_1		4.0			µS
SCL width LOW	t_2		4.7			µS
Set-up time, SDA to SCL	t_3		250			nS
Hold time, SCL to SDA	t_4		5.0			µS
Set-up time, SCL to STRB	t_5		250			nS
STRB width HIGH	t_6		5.0			µS
Hold time, SDA to SCL	$t_{HD;STA}$		4.0			µS
Set-up time, SCL to SDA	$t_{SU;STA}$		4.0			µS
Hold time, SCL to SDA	$t_{HD;DAT}$		5.0			µS
Set-up time, SDA to SCL	$t_{SU;DAT}$		250			nS
SCL width HIGH	t_{HIGH}		4.0			µS
SCL width LOW	t_{LOW}		4.7			µS
SCL rise time	t_R				1000	nS
SCL fall time	t_F				300	nS
Operating current (analog)	I_{ANA}				10	mA
Operating current (digital)	I_{DIG}				0.3	mA
Standby current (analog)	$I_{ANASAVE}$				0.1	mA
Standby current (digital)	$I_{DIGSAVE}$				0.035	mA
Signal to Noise Ratio	S/N			96		dB
Frequency Response	F		20		20k	Hz
Total Harmonic Distortion	THD_F	FLIN, SPREAD=HIGH, NO CLIPPING		0.025		%
Total Harmonic Distortion	THD_R	RLIN, Q1=ON, NO CLIPPING		0.025		%

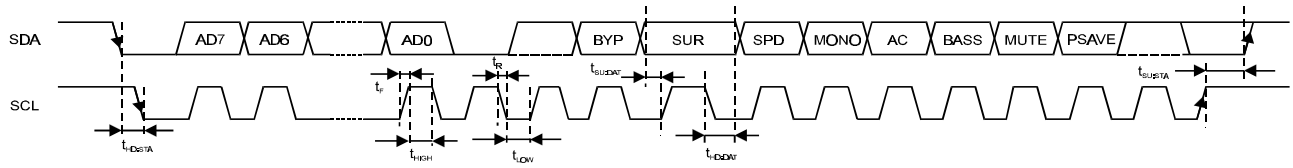
Serial Interface:

Serial interface with 3 control pins (for QS7785PF)



Serial interface with I^{2}C (for QS7785CF)

I2C address is {AD7-AD0} = {10110110}



Operating Mode:

This chip can be set to desired operating mode by control pins for the parallel interface (P/S pin sets to 1) or control bits for the serial interface (P/S pin sets to 0). The control pins or bits configurations are shown in the following table.

Control Pins/Bits				Output Signal	
BYP	**MONO**	**SUR**	**SPD**	**FRout/FLout**	**SRout/SLout**
0	0	0	0	Stereo QX	-
0	0	0	1	Stereo QX+	-
0	0	1	0	Stereo QX	Stereo Q1
0	0	1	1	Stereo QX+	Stereo Q1
0	1	0	0	Mono→Stereo QX	-
0	1	0	1	Mono→Stereo QX+	-
0	1	1	0	Mono→Stereo QX	Mono→Stereo Q1
0	1	1	1	Mono→Stereo QX+	Mono→Stereo Q1
1	0	0	X	Stereo Bypass	-
1	0	1	X	Stereo Bypass	Stereo Bypass
1	1	0	X	-	Stereo Bypass
1	1	1	X	Stereo Bypass	Stereo Q1

Control Pins/Bits					Output Signal
BYP	**MONO**	**SUR**	**SPD**	**CNT**	**Cout**
X	X	X	X	0	-
X	X	X	X	1	(Rin+Lin)/2

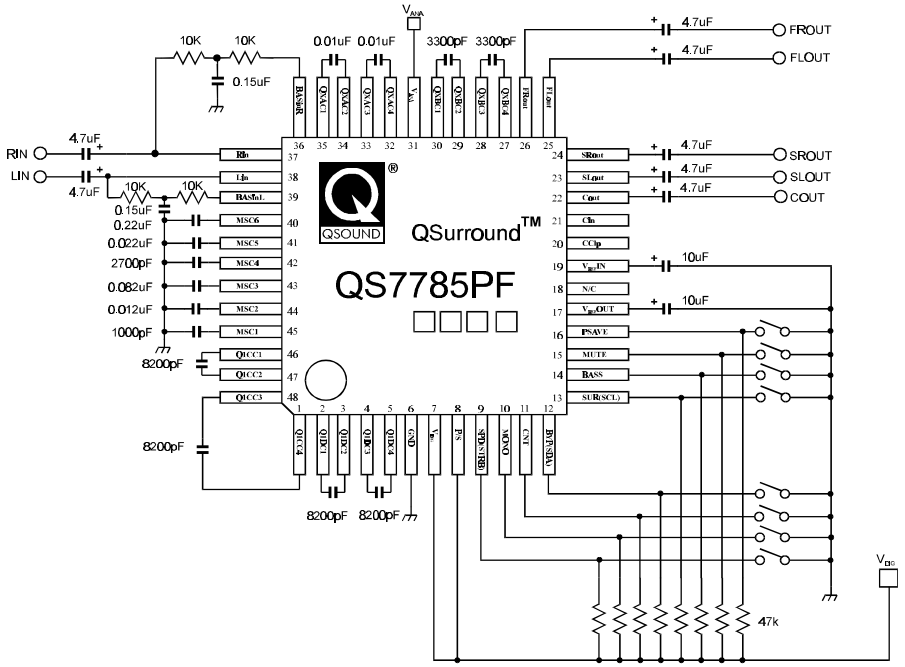
Control Pins/Bits						Output Signal		
BYP	**MONO**	**SUR**	**SPD**	**CNT**	**BASS**	**FRout/FLout**	**SRout/SLout**	**Cout**
X	X	X	X	X	0	Bass Boost OFF	Bass Boost OFF	Bass Boost OFF
X	X	X	X	X	1	Bass Boost ON	Bass Boost ON	Bass Boost ON

Control Pins/Bits								Output Signal		
BYP	**MONO**	**SUR**	**SPD**	**CNT**	**BASS**	**MUTE**	**PSAVE**	**FRout/FLout**	**SRout/SLout**	**Cout**
X	X	X	X	X	X	0	0	Available	Available	Available
X	X	X	X	X	X	1	0	-	-	-
X	X	X	X	X	X	X	1	-	-	-

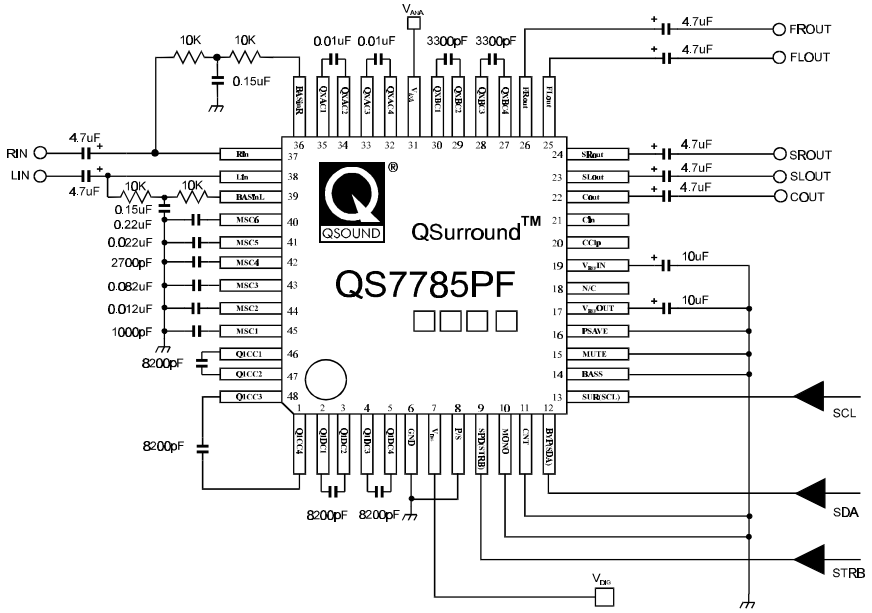
NOTE-1 '_' indicates NO OUTPUT.
NOTE-2 QX+ has higher expansion than QX.
NOTE-3 PSAVE = 1 disables chip. Please refer to the electrical specification for its power consumption.

Application (QS7785PF):

Parallel Interface

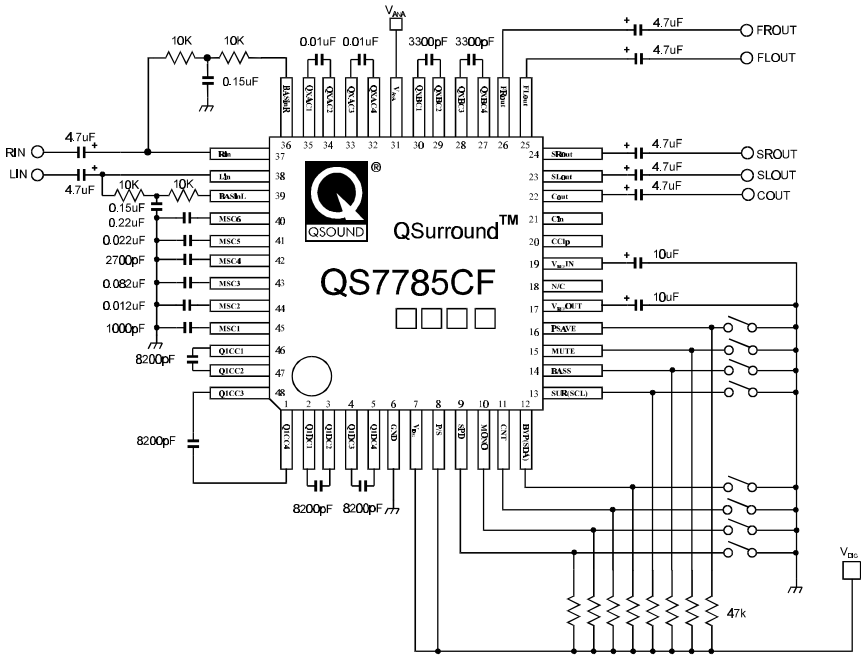


Serial Interface

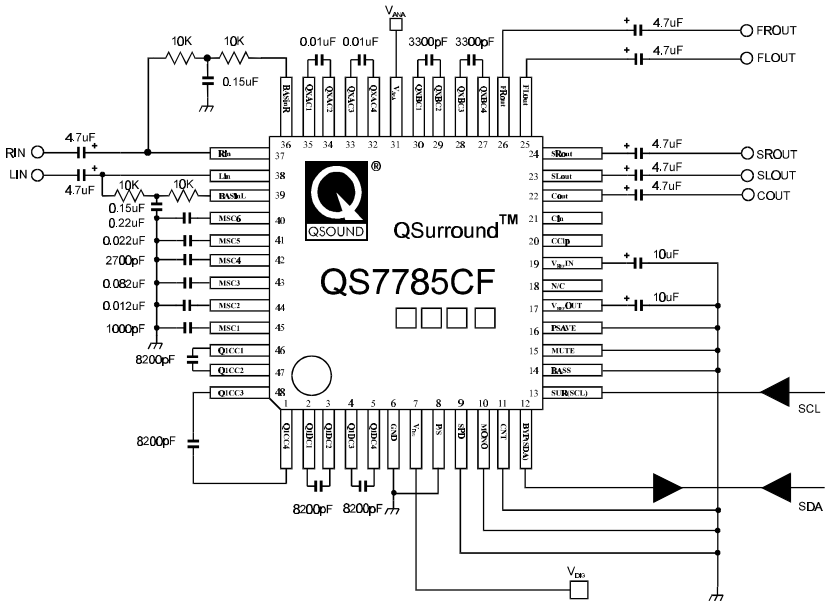


Application (QS7785CF):

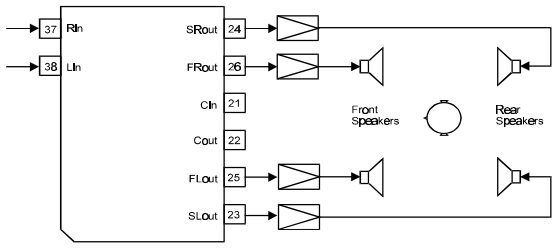
Parallel Interface



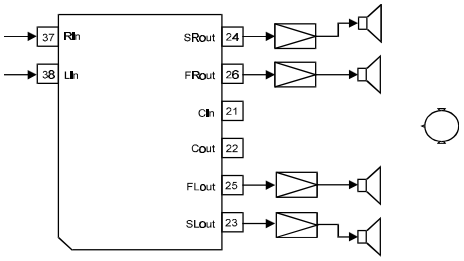
Serial Interface



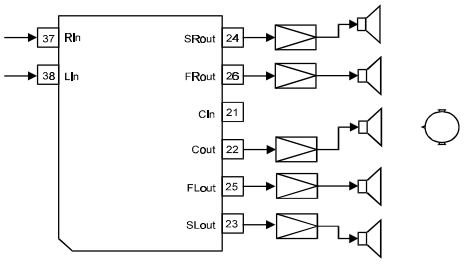
Speaker configuration:
The QS7785 allows the following speaker position.



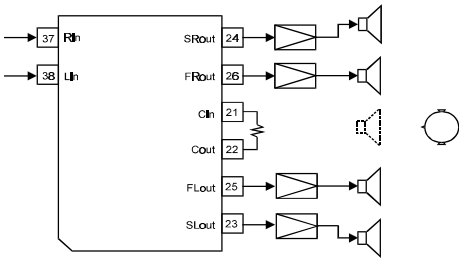
TYPE-A: Two Front speakers In front and two rear speakers In rear



TYPE-B: Front speakers and rear speakers In front

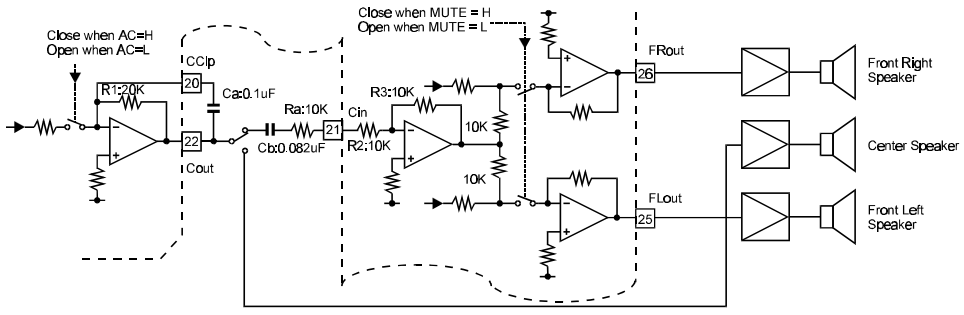


TYPE-C: Front speakers and rear speakers In front with actual center speaker

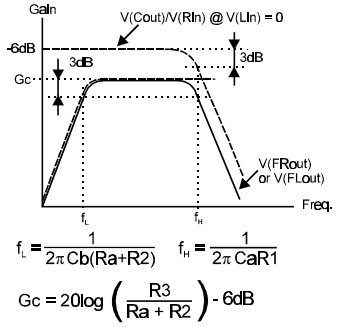


TYPE-D: Front speakers and rear speakers In front with center enhancement

Center control:
The output level of this device is optimized for the speaker layout TYPE-A, two front speakers in front and two rear speakers in rear, shown above. In case of TYPE-B, having four speakers in front, the surround may sound too rich or the center may sound too thin. In such case, either mixing an auxiliary center output, Cout, to two front speakers, TYPE-D, or driving a center speaker from the Cout, TYPE-C, can enhance the center. It may be good idea to filter only voice band of the center signal to enhance a dialog of movies etc. The Cout becomes available by setting AC control to High.



Center output connection

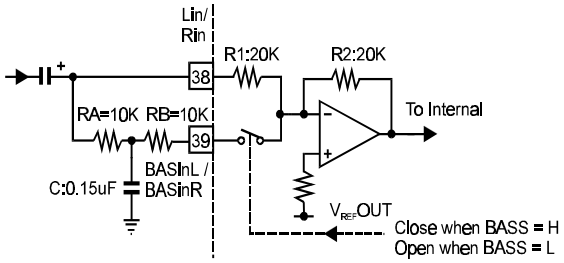


Center output freq. response

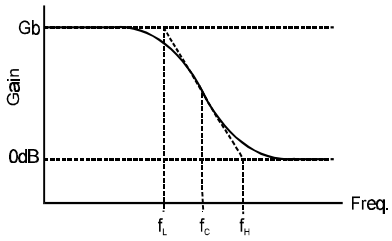
Note) Internal resistance value, R1, R2 and R3, may vary ± 15%

Bass boost:

The signal input of BASinR and BASinL can be used for a bass boosting as shown below. When the BAS control pin is set to H, a low pass filter, consisting of RA, RB and C in the figure below, is connected to the input buffer in parallel to R1.



Bass boost connection
(Gb = 6dB, fc = 300Hz)



Bass boost freq. response

$$Gb = 20\log\left(1 + \frac{R1}{RA + RB}\right)$$

$$f_C = \frac{\sqrt{1 + \frac{R1}{RA + RB}}}{2\pi C \frac{RA \cdot RB}{RA + RB}}$$

$$f_L = f_C \cdot 10^{-\frac{1}{2} \cdot \frac{\log\left(1 + \frac{R1}{RA + RB}\right)}{1 + 2\frac{RA + RB}{R1}}}$$

$$f_H = f_C \cdot 10^{\frac{1}{2} \cdot \frac{\log\left(1 + \frac{R1}{RA + RB}\right)}{1 + 2\frac{RA + RB}{R1}}}$$

Note) Internal resistance value, R1 and R2, may vary ± 15%