

# PUTs

## Planar, TO-18 Hermetic

### FEATURES

- Voltage Ratings: to 100V
- Maximum Peak Current: 150nA
- Valley Current: as low as 25  $\mu$ A
- Low Forward Voltage Drop
- Nano-Amp Leakage
- Hermetically Sealed TO-18 Metal Can

### DESCRIPTION

The Unitorde hermetically sealed TO-18 metal can series of programmable unijunction transistors feature blocking voltages to 100V, the highest available to designers. These PUTs are functionally equivalent to standard unijunction transistors, with the added advantages of programming versatility. External resistors can be added to program  $\eta$ ,  $R_{BB}$ ,  $I_p$  and  $I_v$ , depending upon your design requirements. All units are fully planar passivated. This series features a hermetically sealed TO-18 package for optimum reliability in all environmental conditions. Applications include pulse and timing circuits, SCR trigger circuits, relaxation oscillators, and sensing circuits. For further application information see Unitorde's Application Note U-66.

### ABSOLUTE MAXIMUM RATINGS

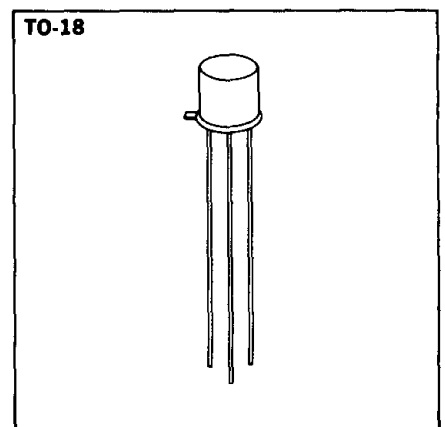
Anode-to-Cathode Forward Voltage, $V_{AK}$	40V
Anode-to-Cathode Reverse Voltage, $V_{AKR}$	40V
Gate-to-Cathode Forward Voltage, $V_{GK}$	40V
Gate-to-Anode Reverse Voltage, $V_{GAR}$	40V
Gate-to-Cathode Reverse Voltage, $V_{GKR}$	5V
Peak Recurrent Forward Current	
10 $\mu$ s 1% Duty Cycle	8A
100 $\mu$ s 1% Duty Cycle	5A
Power Dissipation	
25°C Ambient	400mW
Derating Factor	3.2mW/°C
Storage Temperature Range	-55°C to +150°C
Operating Temperature Range	-55°C to +150°C

### MECHANICAL SPECIFICATIONS

GATE CONNECTED TO CASE

**U13T1-U13T2**

	INCHES	MILLIMETERS
A	.178-.195 DIA.	4.52-4.95 DIA.
B	.170-.210	4.31-5.33
C	.5 MIN.	12.70 MIN.
D	.209-.230 DIA.	5.31-5.84 DIA.
E	.017 ± .002 DIA. .001 DIA.	.432 ± .051 .025
F	.020 MAX.	.508 MAX.
G	.100 ± .010 DIA.	2.54 ± .254 DIA.
H	.041 ± .005	1.04 ± .127
J	.028-.048	.711-1.22



**ELECTRICAL SPECIFICATIONS (at 25°C unless noted)**

Test	Symbol	Fig.	U13T1		U13T2		Units	Test Conditions
			Min.	Max.	Min.	Max.		
Peak Current	$I_p$	1	—	5	—	1.0	$\mu A$	$R_G = 10k, V_s = 10V$ $R_G = 1 \text{ Meg.}$
			—	2	—	0.15	$\mu A$	
Valley Current	$I_v$	1	70	—	25	—	$\mu A$	$R_G = 10k, V_s = 10V$ $R_G = 1 \text{ Meg.}$
			—	50	—	25	$\mu A$	
Offset Voltage	$V_T$	1	0.2	0.6	0.2	0.6	V	$R_G = 10k, V_s = 10V$ $R_G = 1 \text{ Meg.}$
			0.2	1.6	0.2	0.6	V	
Gate-to-Anode Leakage	$I_{GAO}$	2	—	10	—	10	nA	$T = 25^\circ C, V_s = \text{rating}$
Gate-to-Cathode Leakage	$I_{GKS}$	3	—	100	—	100	nA	$V_s = \text{rating}$
Forward Voltage	$V_F$	4	—	1.5	—	1.5	V	$I_F = 50mA$
Pulse Output Voltage	$V_o$	5	6	—	6	—	V	
Pulse Output Rate of Rise	$t_r$	5	—	80	—	80	nS	

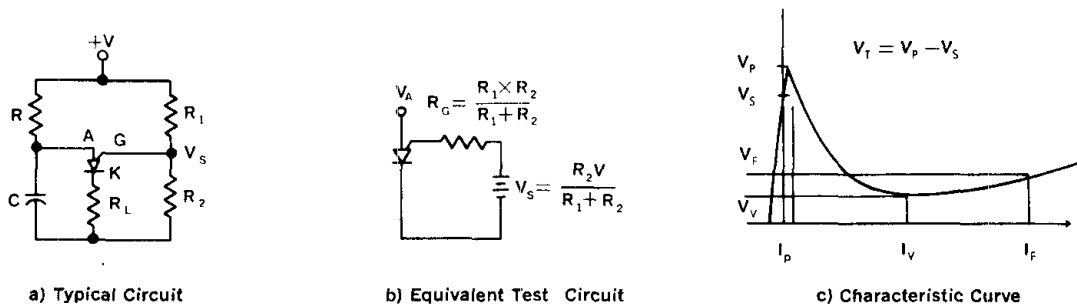


Figure 1

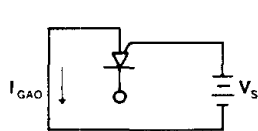


Figure 2

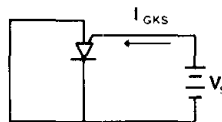


Figure 3

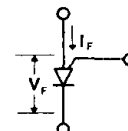


Figure 4

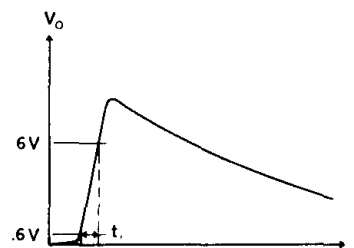
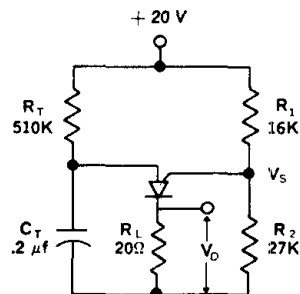


Figure 5