National Semiconductor

Not Intended For New Designs

T-46-23-31

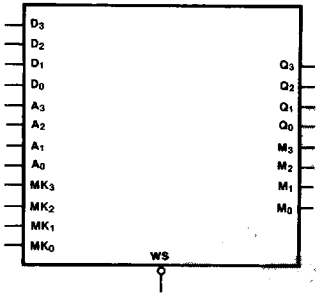
100142
4 x 4-Bit Content Addressable Memory

General Description

The 100142 is a 4 word by 4-bit Content Addressable Memory (CAM). Reading is accomplished when an address select input (A_0, A_7, A_2, A_3) is LOW and the write strobe input ($\overline{WS}$) is HIGH. The corresponding stored word appears on the data outputs (Q_0–Q_3). Writing can be performed to individual bits of a word or to the whole word. (A LOW on an address select input enables a 4-bit word.) A LOW on a bit mask input (MK_0, MK_1, MK_2, MK_3) enables a bit within all four 4-bit words. Write data is presented on the data inputs (D_0, D_1, D_2, D_3) and is latched into the addressed bit latch when the write strobe input ($\overline{WS}$) is LOW. Hence, the bit mask inputs are used to selectively store data bit-wise within an addressed word. During writing, the data input word is simultaneously compared to each of the stored memory words. A search/compare is performed by placing a LOW on the bit mask inputs and presenting a data pattern to the data inputs. Corresponding to the bit mask inputs, the match outputs (M_0–M_3) go LOW if a data bit of the pattern matches the respective stored bit. A HIGH on any bit mask input forces a LOW on the respective match output. Each input has a 50 kΩ (typical) pull-down resistor to V_{EE}.

Ordering Code: See Section 6

Logic Symbol



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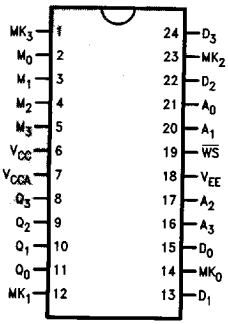
Pin Names	Description
MK_0–MK_3	Data Mask Inputs
A_0–A_3	Address Inputs
D_0–D_3	Data Inputs
$\overline{WS}$	Write Strobe Input
M_0–M_3	Match Outputs
Q_0–Q_3	Data Outputs

Connection Diagrams

24-Pin DIP



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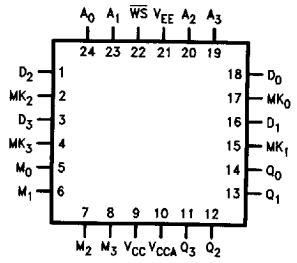
24-Pin Quad Cerpak



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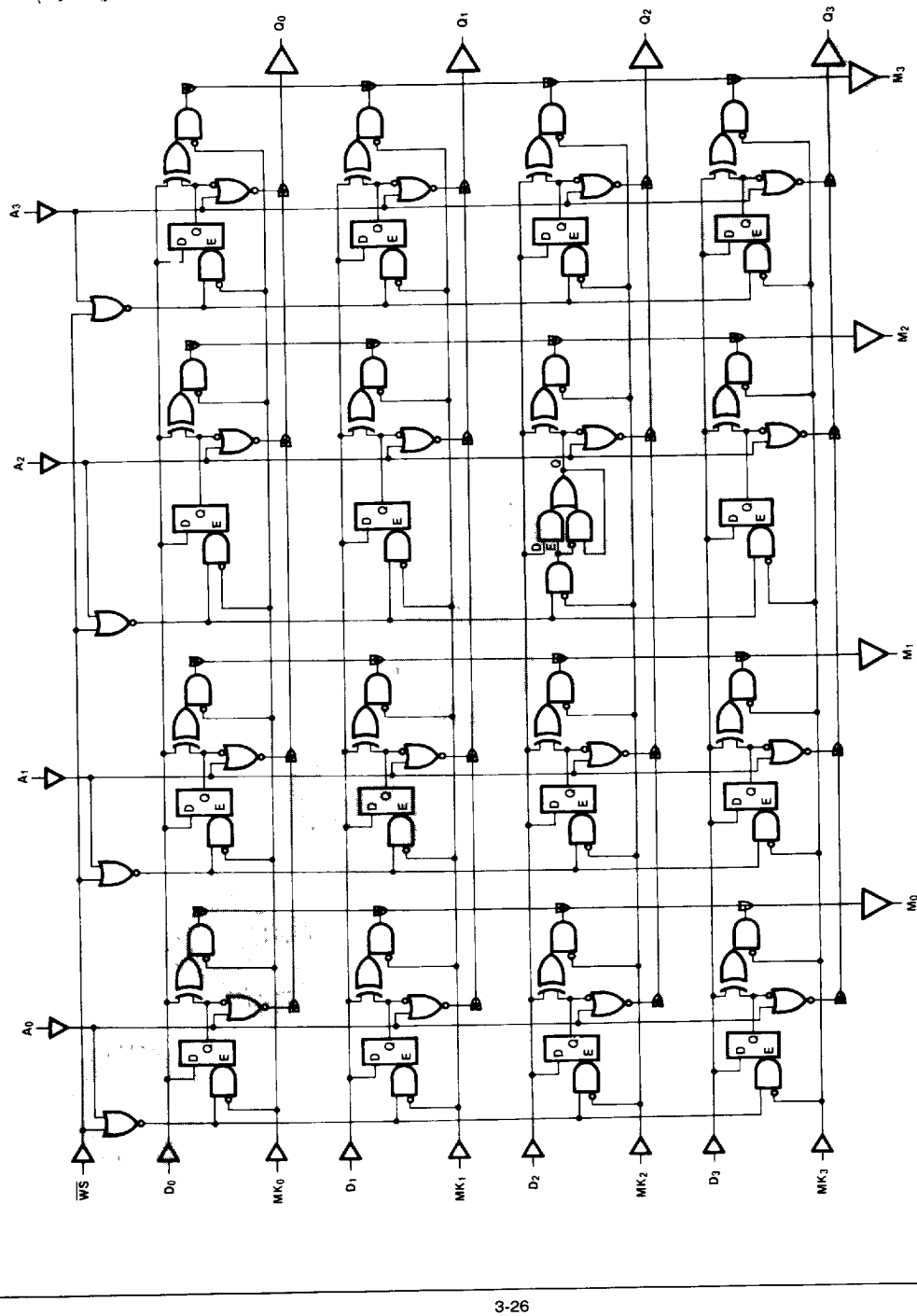
Logic Diagram



Truth Table

Operation	Inputs				Flip-Flop	Outputs	
	$\overline{WS}$	A_i	D_j	MK_j	Q_{ij}	M_i	Q_j
	$\overline{WS}$	A_0 A_1 A_2 A_3	D_0 D_1 D_2 D_3	MK_0 MK_1 MK_2 MK_3		M_0 M_1 M_2 M_3	Q_0 Q_1 Q_2 Q_3
Write Disabled	X X	H L	X X	X H	NC NC	X L	L $Q_{ij}n-1$
Write	L L	L L	H L	L L	H L	L L	H L
Read	H H	L L	X X	X X	H L	X X	H L
Match Masked	H	X	X	H	NC	L	X
Match Not Satisfied	H H H H	L H H L	H H L L	L L L L	L L H H	H H H H	L L L H
Match Satisfied	H H H H	L H H L	H H L L	L L L L	H H L L	L L L L	H L L L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
NC = No Change from Previous State
$\overline{WS}$ = Write Strobe
A_i = Address for ith Word
D_j = Data for jth Bit

MK_j = Data Mask for jth Bit
H = Mask
Q_{ij} = Cell State for ith Word, jth Bit
M_i = Match Output of ith Word
L = True
Q_j = Data Output of jth Bit
Q_{n-1} = Previous Cell State

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Absolute Maximum Ratings

Above which the useful life may be impaired. (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Maximum Junction Temperature (T_J)	+150°C
Case Temperature under Bias (T_C)	0°C to +85°C
V_{EE} Pin Potential to Ground Pin	−7.0V to +0.5V
Input Voltage (DC)	V_{EE} to +0.5V
Output Current (DC Output HIGH)	−50 mA
Operating Range (Note 2)	−5.7V to −4.2V

DC Electrical Characteristics

V_{EE} = −4.5V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions (Note 4)	
V_{OH}	Output HIGH Voltage	−1025	−955	−880	mV	V_{IN} = $V_{IH\ (Max)}$ or $V_{IL\ (Min)}$	Loading with 50Ω to −2.0V
V_{OL}	Output LOW Voltage	−1810	−1705	−1620			
V_{OHC}	Output HIGH Voltage	−1035			mV	V_{IN} = $V_{IH(Min)}$ or $V_{IL\ (Max)}$	Loading with 50Ω to −2.0V
V_{OLC}	Output LOW Voltage			−1610			
V_{IH}	Input HIGH Voltage	−1165		−880	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	−1810		−1475	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.50			μA	V_{IN} = $V_{IL\ (Min)}$	

DC Electrical Characteristics

V_{EE} = −4.2V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions (Note 4)	
V_{OH}	Output HIGH Voltage	−1020		−870	mV	V_{IN} = $V_{IH\ (Max)}$ or $V_{IL\ (Min)}$	Loading with 50Ω to −2.0V
V_{OL}	Output LOW Voltage	−1810		−1605			
V_{OHC}	Output HIGH Voltage	−1030			mV	V_{IN} = $V_{IH\ (Min)}$ or $V_{IL\ (Max)}$	Loading with 50Ω to −2.0V
V_{OLC}	Output LOW Voltage			−1595			
V_{IH}	Input HIGH Voltage	−1150		−870	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	−1810		−1475	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.50			μA	V_{IN} = $V_{IL\ (Min)}$	

DC Electrical Characteristics

V_{EE} = −4.8V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions (Note 4)	
V_{OH}	Output HIGH Voltage	−1035		−880	mV	V_{IN} = $V_{IH\ (Max)}$ or $V_{IL\ (Min)}$	Loading with 50Ω to −2.0V
V_{OL}	Output LOW Voltage	−1830		−1620			
V_{OHC}	Output HIGH Voltage	−1045			mV	V_{IN} = $V_{IH\ (Min)}$ or $V_{IL\ (Max)}$	Loading with 50Ω to −2.0V
V_{OLC}	Output LOW Voltage			−1610			
V_{IH}	Input HIGH Voltage	−1165		−880	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	−1830		−1490	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.50			μA	V_{IN} = $V_{IL\ (Min)}$	

Note 1: Absolute maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Parametric values specified at −4.2V to −4.8V.

Note 3: The specified limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.

Note 4: Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

DC Electrical Characteristics

V_{EE} = −4.2V to −4.8V unless otherwise specified, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C

Symbol	Parameter	Min	Typ	Max	Units	Conditions
I_{IH}	Input HIGH Current All Inputs			200	μA	V_{IN} = $V_{IH\ (Max)}$
I_{EE}	Power Supply Current	−288	−190	−114	mA	Inputs Open

Ceramic Dual-In-Line Package AC Electrical Characteristics

V_{EE} = −4.2V to −4.8V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = 0°C		T_C = +25°C		T_C = +85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_{AD}	Address to Data Out	1.20	4.40	1.20	4.30	1.20	4.50	ns	*Figures 2* and *3*
t_{DM}	Data In to Match Out Time	1.60	3.70	1.60	3.60	1.60	3.80	ns	
t_{MM}	Mask In to "Enable Partial" Match Out Time	1.20	3.90	1.20	3.90	1.20	4.00	ns	*Figure 5*
t_{DD}	Data In to New Data Out	1.70	4.40	1.70	4.40	1.70	4.60	ns	
t_{WD}	Write to New Data Out	2.50	5.40	2.50	5.20	2.30	5.10	ns	
t_{AM}	Address to Match	2.50	4.60	2.50	4.60	2.50	4.90	ns	*Figure 2*
t_{MD}	Mask to Data	2.20	4.90	2.20	4.80	2.20	5.00	ns	
t_{WSM}	$\overline{WS}$ to Match	2.80	4.90	2.80	4.80	2.80	5.10	ns	
t_W	Write Pulse Width	1.30		1.30		1.30		ns	
t_{AS}	Address Setup before Write Time	1.40		1.40		1.40		ns	
t_{AH}	Address Hold after Write Time	1.40		1.40		1.40		ns	
t_{DS}	Data In Setup before Write Time	0.60		0.60		0.60		ns	*Figure 1*
t_{DH}	Data In Hold after Write Time	1.10		1.10		1.10		ns	
t_{MH}	Mask In Hold Write Time	2.50		2.50		2.50		ns	
t_{MS}	Mask In Setup Write Time	1.10		1.10		1.10		ns	
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.50	2.30	0.50	2.30	0.50	2.30	ns	*Figure 2*

Cerpak AC Electrical Characteristics

V_{EE} = −4.2V to −4.8V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = 0°C		T_C = +25°C		T_C = +85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_{AD}	Address to Data Out	1.20	4.20	1.20	4.10	1.20	4.30	ns	*Figures 2* and *3*
t_{DM}	Data In to Match Out Time	1.60	3.50	1.60	3.40	1.60	3.60	ns	
t_{MM}	Mask In to "Enable Partial" Match Out Time	1.20	3.70	1.20	3.70	1.20	3.80	ns	*Figure 5*
t_{DD}	Data In to New Data Out	1.70	4.20	1.70	4.20	1.70	4.40	ns	
t_{WD}	Write to New Data Out	2.50	5.20	2.50	5.00	2.30	4.90	ns	
t_{AM}	Address to Match	2.50	4.40	2.50	4.40	2.50	4.70	ns	*Figure 2*
t_{MD}	Mask to Data	2.20	4.70	2.20	4.60	2.20	4.80	ns	
t_{WSM}	$\overline{WS}$ to Match	2.80	4.70	2.80	4.60	2.80	4.90	ns	
t_W	Write Pulse Width	1.20		1.20		1.20		ns	
t_{AS}	Address Setup before Write Time	1.30		1.30		1.30		ns	
t_{AH}	Address Hold after Write Time	1.30		1.30		1.30		ns	
t_{DS}	Data In Setup before Write Time	0.50		0.50		0.50		ns	*Figure 1*
t_{DH}	Data In Hold after Write Time	1.00		1.00		1.00		ns	
t_{MH}	Mask In Hold Write Time	2.40		2.40		2.40		ns	
t_{MS}	Mask In Setup Write Time	1.00		1.00		1.00		ns	
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.50	2.20	0.50	2.20	0.50	2.20	ns	*Figure 2*

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Switching Waveforms

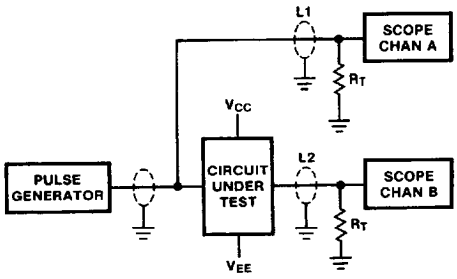

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FIGURE 1. AC Test Circuit

Note:

V_{CC}, V_{CCA} = +2V, V_{EE} = −2.5V
L1, L2 and L3 = equal length 50Ω impedance lines
R_T = 50Ω terminator internal to scope
Decoupling 0.1 μF from GND to V_{CC} and V_{EE}
All unused outputs are loaded with 50Ω to GND
C_L = Fixture and stray capacitance ≤ 3 pF

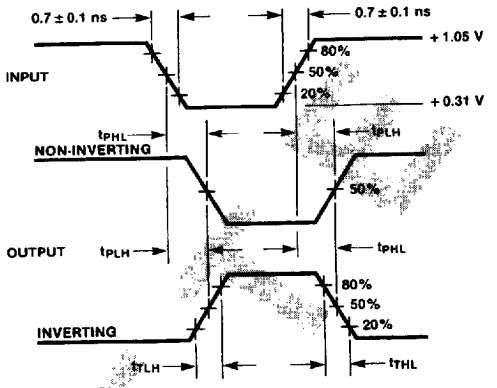

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FIGURE 2. Output Rise and Fall Times and Waveforms

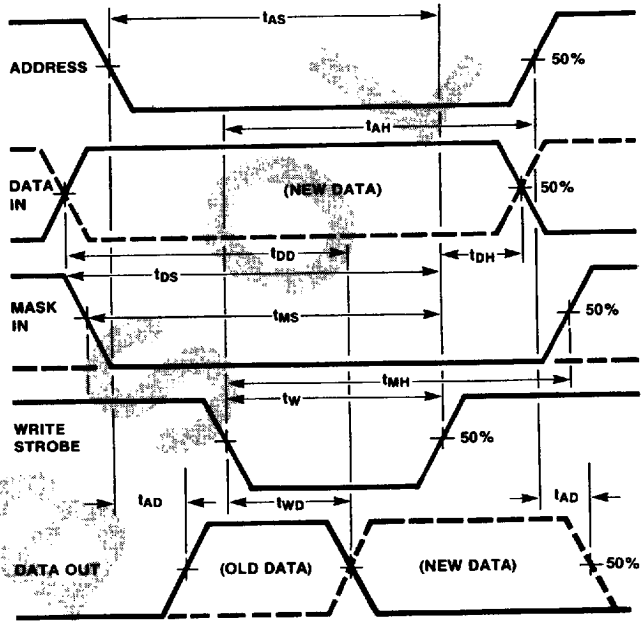

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FIGURE 3. Write Mode and Read/Write Mode Waveforms

Switching Waveforms (Continued)

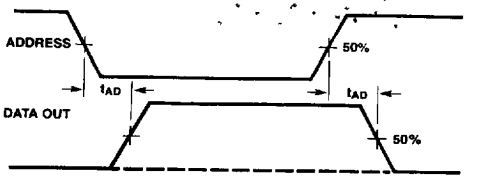

FIGURE 4. Read Mode Waveforms

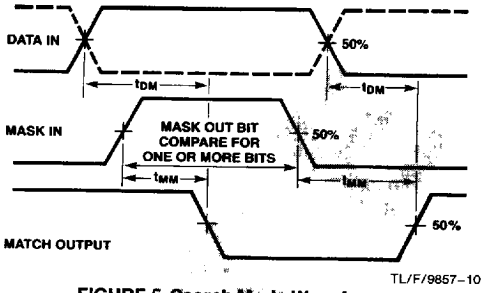

FIGURE 5. Search Mode Waveforms

Application

The 100142 is an ideal choice for the register file unit of a bit-slice processor. *Figure 5* shows the configuration of four 100145s into a 16 x 16 register file. The write enbles (WE_1, WE_2) and output enables (OE_1, OE_2) are configured to allow access to one array of sixteen 16-bit registers or two arrays of sixteen 8-bit registers. Simultaneous read and write addressing is made possible with separate buses. Also, reading and then writing to the same address is easily and efficiently done by tying one write enable to an output enable.

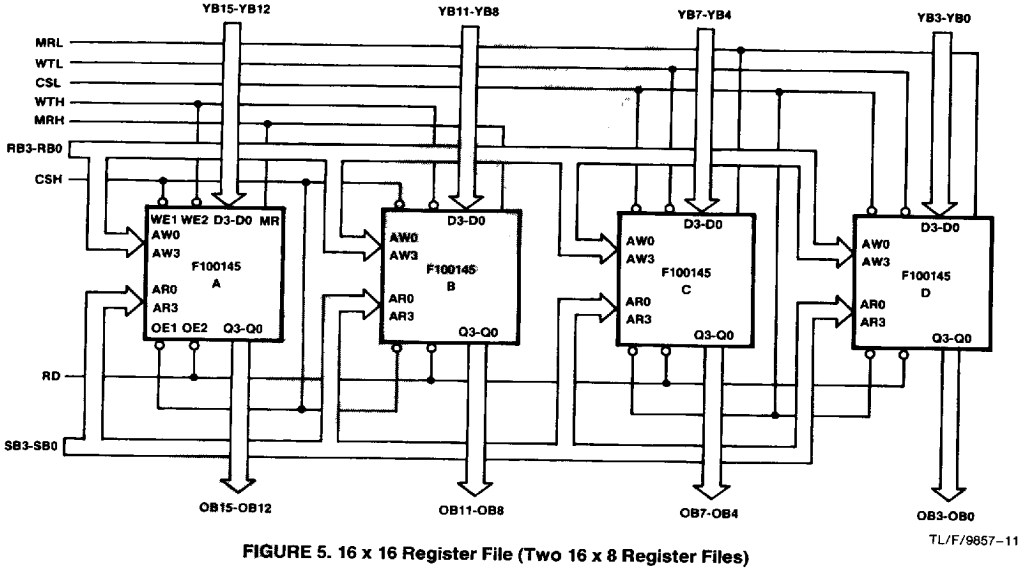

FIGURE 5. 16 x 16 Register File (Two 16 x 8 Register Files)