CIRRUS LOGIC®

CL-CR3430

Preliminary Product Bulletin

FEATURES

- **General**
  - — High-performance CD-ROM decoder supports disc speeds up to 45× (6750 Kbytes/sec.)
  - — CD-DSP data transfer rate:
    - Up to 45× drive speed with concurrent ECC correction with no C2 pointers
    - Up to 36× drive speed with concurrent ECC correction with C2 pointers
  - — Supports Ultra DMA: capable of synchronous DMA data transfer rates up to 33.3 Mbytes/sec.
  - — Supports 16-bit DRAM interface
  - — Firmware compatible with all Cirrus Logic CD-ROM decoders (CL-CR3410/'15/'20) and CD-R/RW encoder/decoder devices (CL-CR3460/'3560)
  - — Fully compatible with the ATAPI Specification SFF-8020, Revision 1.2
  - — Improved testability using scan methodology
  - — 128-pin SQFP package
- **CD-ROM DSP Interface**
  - — Supports Sony-Philips® CD-ROM, CD-I, and CD-DA™ (CD-Digital Audio) formats
  - — Supports CD-TEXT Mode format
  - — Supports various compact disc DSP controllers
  - — Supports programmable pseudo-sync-mark insertion for CD-ROM sector synchronization
  - — Supports automatic target sector header search for CD-ROM

(cont.)

High-Performance
45× ATAPI CD-ROM Decoder

OVERVIEW

The CL-CR3430 is the newest addition to the Cirrus Logic family of high-performance ATAPI CD-ROM decoders, supporting disc speeds up to 45×. In addition, it also supports the latest addition to the ATA interface specification, Ultra DMA/33, allowing host speeds up to 33.3 Mbytes/sec.

This device is firmware compatible with all Cirrus Logic CD-ROM and CD-R/RW products, allowing customers to upgrade quickly and efficiently. In a system, the CL-CR3430 is configured with an external buffer memory (8- or 16-bit DRAM), a local microcontroller, and system RAM and ROM to create a complete CD-ROM solution.

Other performance features include support for 16-bit-wide DRAMs. This feature allows the CL-CR3430 to support PIO Mode 4 without turning on IOCHRDY.

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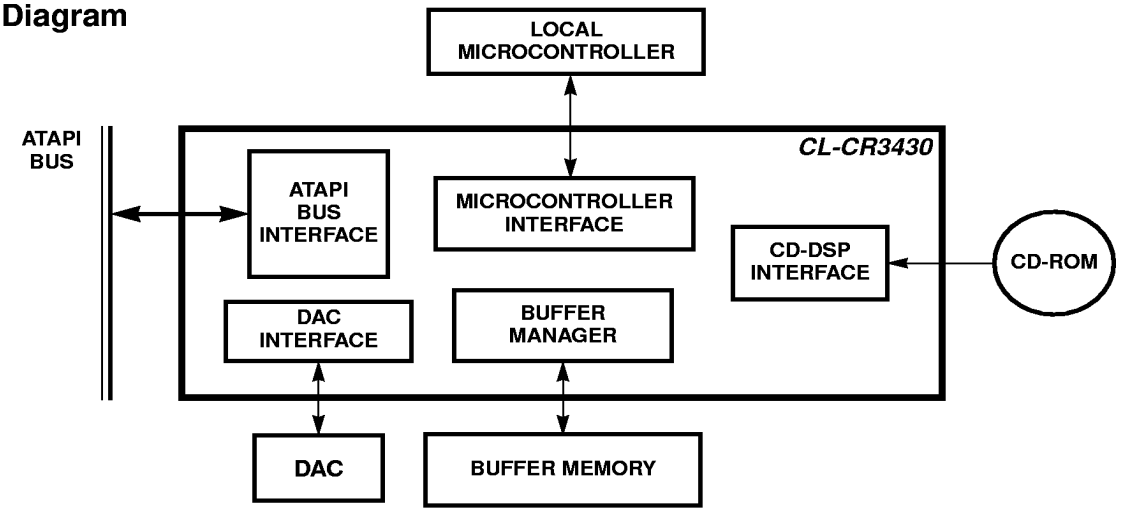
Functional Block Diagram



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FEATURES (cont.)

- — Sector header validity check is done in hardware during data transfer
- — Realtime CD-ROM layered ECC correction with up to 64 programmable sets of P/Q-word corrections per sector
- — Supports realtime subcode error correction in CD-DA (CD-Digital Audio) mode
- — Supports Philips® subcode interface

■ **Audio DAC Interface**

- — Supports ADB for CD-DA audio play mode
- — Supports buffer streaming during the Disc-to-DAC data transfer
- — Supports various DACs

■ **ATAPI Host Interface**

- — Supports Synchronous Ultra DMA/33 data transfer protocol with data rate up to 33.3 Mbytes/sec.
- — Supports ATA PIO Modes 3 and 4 transfers without IOCHRDY and supports DMA Modes 1 and 2
- — FIFOs synchronize buffer RAM access with the host bus and the DSP data transfer
- — Hardware implementation of:
  - ATAPI packet command
  - ATAPI reset command
- — Supports any host speed with programmable and auto wait-state generation
- — True realtime hardware/software ATAPI compatibility
- — All ATAPI command and control registers contained in the CL-CR3430 register set
- — Direct interface to ATAPI bus with programmable 4- or 12-mA drivers
- — Can daisy-chain two ATA- or ATAPI-embedded drives

■ **Buffer Manager**

- — Supports 8- and 16-bit DRAM
- — Dual-port circular buffer control with access-priority resolver
- — Supports streaming operation
- — Direct addressing of up to 4 Mbytes of DRAM
- — Supports variable buffer segmentation
- — Programmable timing control for DRAM
- — Host overrun control

■ **Microcontroller Interface**

- — Supports high-speed Intel®- and Motorola®-type microcontrollers
- — Supports nonmultiplexed and multiplexed address and data buses
- — Interrupt- or polled-microcontroller interface
- — Three-level power-down capability when idle and automatic power-up when command is received

OVERVIEW (cont.)

The built-in ADB (audio data buffering) interface eliminates slowing the motor down from 45× to 1× for digital audio data. This feature is especially useful in CAV (constant angular velocity) designs where motor speed remains constant regardless of the data type, either audio or data, read from the disc.

The CL-CR3430 includes support for CD-TEXT mode, a new subcode format. In this mode, the subcode R-W data is stored in the buffer without de-interleaving and de-scrambling, allowing storage of short messages such as song titles.

The CL-CR3430 supports realtime layered ECC correction, which is programmable for up to 64 P/Q-word corrections per sector. Also, subcode R-W correction is supported in the CD-DA (CD-Digital Audio) mode.

The CL-CR3430 DSP interface supports many CD-ROM DSPs from various manufacturers. It includes three types of interface signals: the main data channel signals, subcode channel signals, and serial DSP programming signals.

The ATAPI host interface is designed for compliance with ATAPI Specification SFF-8020, Revision 1.2. The ATAPI Command and Control Block registers are contained in the CL-CR3430 register set, allowing both host and local microcontroller accesses. The CL-CR3430 supports some ATAPI protocols in hardware without microcontroller intervention (such as ATAPI packet and ATAPI reset commands).

The buffer manager controls the flow of data between the host and DSP interfaces. These interfaces store and retrieve data to/from the external buffer memory using interleaved access cycles. The actual buffer memory is implemented with DRAMs. The buffer manager can be programmed to provide all the necessary address and control signals for RAM devices with varying access times and memory configurations.

ADVANTAGES

Unique Features	*Benefits*
■ CD-DSP data transfer rates up to 45× disc speed	❒ Supports CD-ROM speeds above the current industry requirements.
■ Supports Ultra DMA/33 transfer rate of 33.3 Mbytes/sec., and ATA PIO Modes 3 and 4, DMA Modes 1 and 2 transfer rates up to 16.6 Mbytes/sec.	❒ Enables transfer rates of the highest performance systems.
■ Implements ADB (audio data buffering) interface in CD-DA audio play mode	❒ No need to slow motor speed anywhere from 45× to 1× for audio data in CAV implementations.
■ Register-compatible with Cirrus Logic CD-ROM and CD-R/RW products	❒ Preserves existing firmware base, resulting in quicker time to market.
■ Supports Sony-Philips® CD-ROM, CD-I, CD-TEXT, and CD-DA™ (CD-Digital Audio) formats	❒ Can be used in all implementations of CD technology.
■ Supports automatic target sector header search for CD-ROM ■ Sector header validity check is done in hardware during data transfer	❒ Improves performance and reduces firmware requirements.
■ Realtime subcode error correction in CD-DA mode ■ Realtime CD-ROM layered ECC error correction with up to 64 programmable sets of P/Q-word corrections per sector	❒ Exceeds advanced ECC requirements of state-of-the-art CD-ROM designs for a variety of media/performance combinations.
■ Automated ATAPI packet and reset commands	❒ Improves system performance and lowers firmware overhead.

System Block Diagram