FS511

18-bit ADC with 1 low noise OPAMP.

Data Sheet

FS511-DS-12_EN

Rev. 1.2

Table of Contents

1. General Description

The FS511 is a high-resolution analog-to-digital converter (ADC) chip. The core of this chip is an 18-bit resolution ΔΣADC. Besides the ΔΣADC, FS511 consists of switching circuits, operational amplifier, digital filter, crystal oscillation circuits, digital control logic, and microprocessor interface. Under 5V working voltage, this chip consumes 1.2mA power.

2. Features

- **Delta-Sigma ADC, 18-bit high-resolution 10Hz output rate (Programmable).**
- **Linearity Error: ±0.005%FS**
- **Voltage operation ranges from 4.5V to 6V.**
- **4MHz crystal oscillator.**
- **Operation current is less than 1.2mA; sleep mode current is about 1μA.**
- **SPI Interface to Micro-Processor**
- **Package: 20-pin DIP, 20-pin SOP.**

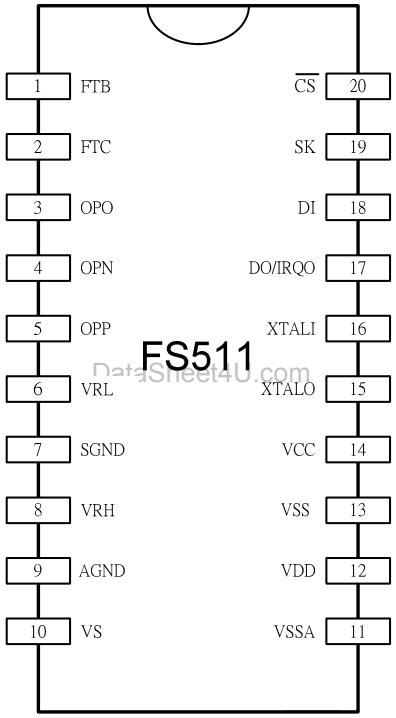
3. Applications

- **Electronics Weigh Scale**
- **Sensor or Transducer measurement application**
- **Others**

4. Ordering Information

Product Number	Description	Package Type
FS511-PI	DIP20 Pb free package part number.	DIP20 (Pb free package)
FS511-PHB	SOP20 Pb free package part number.	SOP20 (Pb free package)

5. Pin Configuration

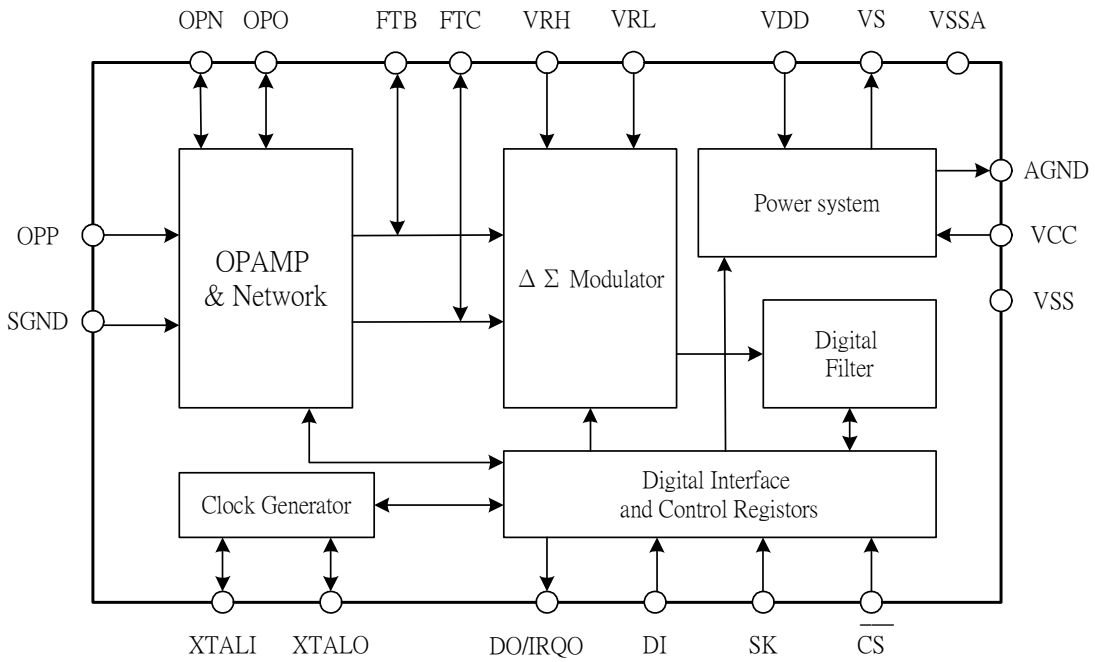


6. Pin Description

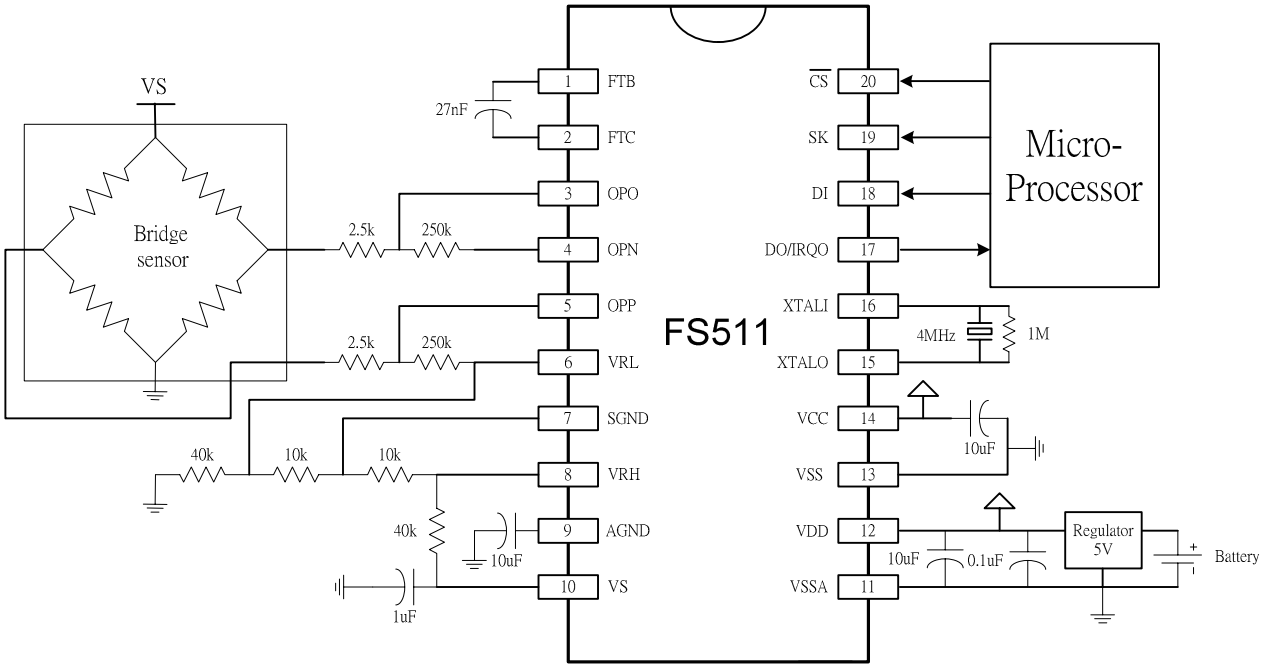
Name	Attribute	Pin No	Description
FTB	AIO	1	ADC Pre-Filter Capacitor Connection and input high
FTC	AIO	2	ADC Pre-Filter Capacitor Connection and input low
OPO	AIO	3	OPAMP Output
OPN	AIO	4	OPAMP Negative Input
OPP	AIO	5	OPAMP Positive Input
VRL	AIO	6	Input Reference Voltage low of the ADC
SGND	AI	7	Signal Ground
VRH	AI	8	Input Reference Voltage high of the ADC
AGND	APIO	9	Analog Ground
VS	APO	10	Voltage source
VSSA	API	11	Analog Negative Power Supply
VDD	PI	12	Positive Power Supply
VSS	API	13	Digital Negative Power Supply
VCC	DPO	14	Power Supply for Digital Signal
XTALO	DO	15	4MHz Oscillator Output
XTALI	DI	16	4MHz Oscillator Input
SDO/IRQO	DO	17	SPI Data Output or interrupt request output
SDI	DI	18	SPI Data Input
SCLK	DI	19	SPI Clock Input
/CS	DIO	20	Chip select of Digital Interface

Notations: D stands for Digital. A stands for Analog. P stands for Power. O stands for Output. I stands for Input. For example: DIO means “Digital Input/Output”.

7. Functional Block Diagram



8. Typical Application Circuit



9. Absolute Maximum Ratings

Parameter	Rating	Unit
Supply Voltage to Ground Potential	-0.3 to 10	V
Applied Input/Output Voltage	-0.3 to VDD+0.3	V
Ambient Operating Temperature Range	-40 to +85	℃
Storage Temperature Range	-55 to +150	℃
Soldering Temperature (10 Sec)	260	℃
ESD Tolerance	Human body Model (HBM): ≧2KV Machine Model (MM): ≧200V	

10. Electrical Characteristics

DC Characteristics (VDD=5V, T_A=25℃, unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Analog-to-Digital Converter					
Zero Input Reading	VIN=0V, Vref=500mV , CYS=01	-15		15	μV
Linearity (Max. deviation from best straight line fit)	VIN= ± 0.9 Vref, Vref=500mV , CYS=01	-25		25	μV
Input Common-Mode Rejection Ratio	VCM=AGND ± 1V, VIN=0.25V, Vref=500mV			150	μV/V
Noise (p-p Value not Exceeding 95% of Time)	VIN=0V, 500mV Scale		5	10	μV
Rollover Error (Difference in reading for equal positive and negative inputs near Full Scale)	-VIN=+VIN=500.00mV	0	10	50	μV
Scale Factor Temperature Coefficient	VIN=500.00mV, -10℃<TA<+50℃		10		ppm/℃
Current Consumption			0.7	1.2	mA
Instrumentation Amplifier					
Input Offset Voltage without chopper	Rs<100Ω		1		mV
Input Offset Voltage with chopper	Rs<100Ω		30		μV
Input Referred Noise without chopper	Rs=100Ω, 0.1Hz~1Hz		1		μVpp
Input Referred Noise with chopper	Rs=100Ω, 0.1Hz~1Hz		0.3		μVpp
Input Bias Current	[2]		100	300	pA

PARAMETER	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Input Common-Mode Voltage Range		2		3	V
Current Consumption			200	300	μA
General Electrical Characteristics					
VDD Operating Current	Enable ADC, OPAMP		1	2	mA
Sleep Current	Disable OSC, AGND		1	5	μA
VS switch resister			20		Ω
Digital Output High	IOUT=-1mA		4.7		V
Digital Output Low	IOUT=1mA		0.3		V
Digital Input High		3.5			V
Digital Input Low				1.5	V

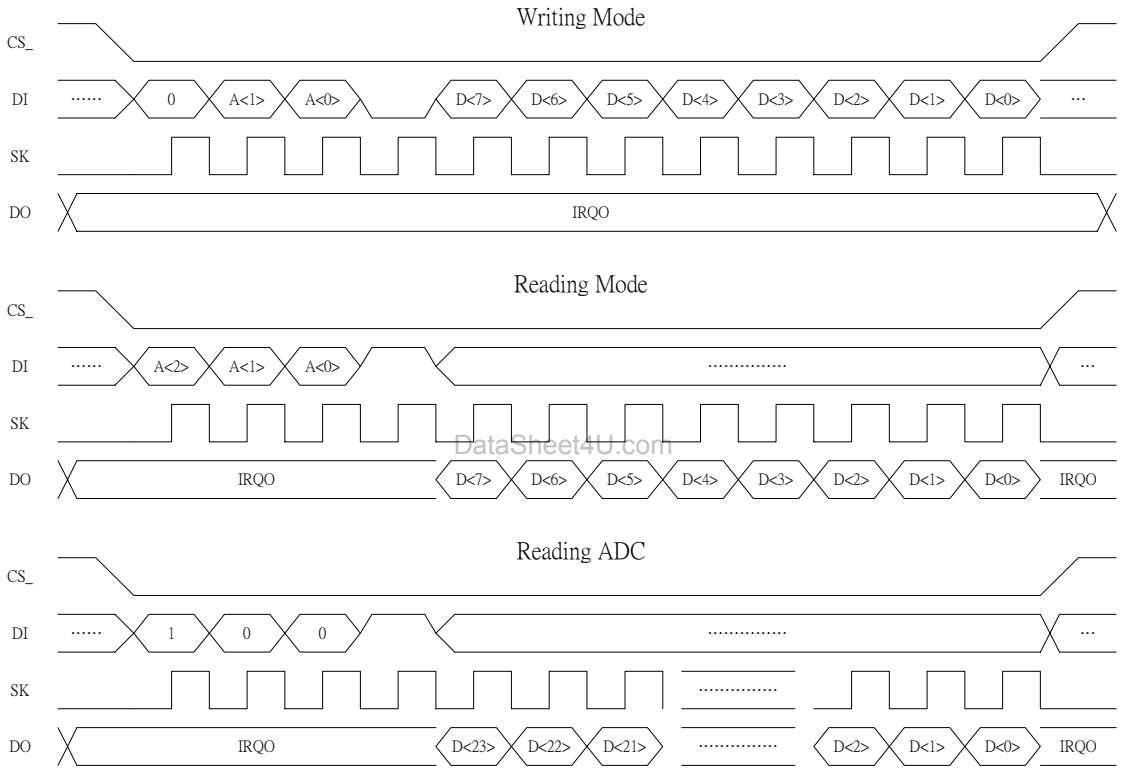
[1] These parameters are guaranteed by design and are tested only by sampling while mass production.

[2] While a voltage source with large output impedance is measured by an instrumentation amplifier having input bias current, an additional input offset voltage will be introduced. However, this offset voltage could be cancelled by mirrored offset cancellation technique.

11.Function Description

11.1 Microprocessor Interface

FS511 can be directly connected to any microprocessor by pins of CS_, SK, DI, DO/IRQO. It can access the read/write of the control registers, handle interrupts, and access the measure registers.



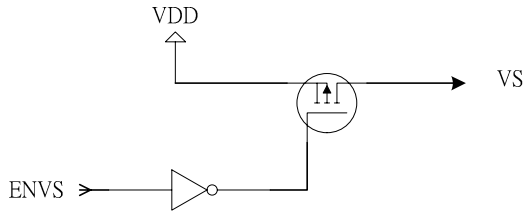
If ADC Data converse complete, IRQO will be high to Low.

11.2 Power System

11.2.1 Analog power (VDD, VSSA) and Digital power (VCC, VSS)

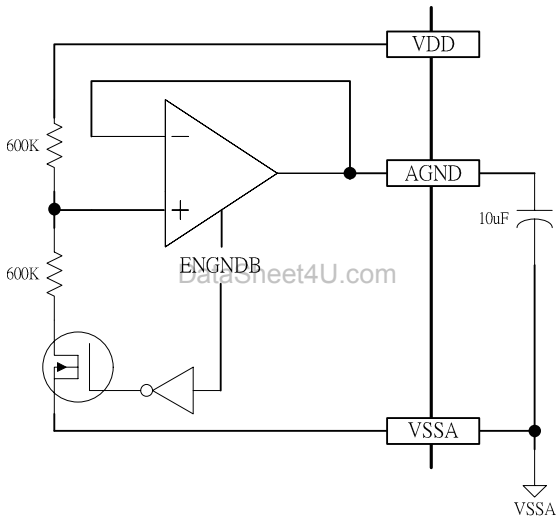
ADC, OPAMP and analog circuit used Analog power (VDD, VSSA). VDD typically is 5V.
Digital Interface and Digital circuit used Digital power (VCC, VSS).

11.2.2 Switch-able Power Output



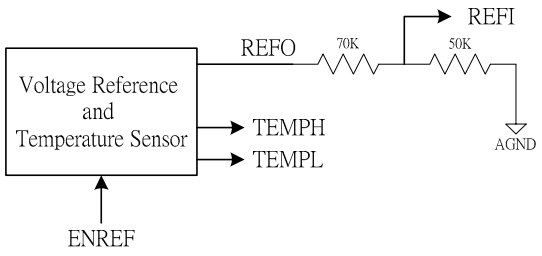
Terminals of VS is the switch-able power output of VDD. The PMOS switch is controlled by ENVS control signal. When ENVS = 1, the switch is short.

11.2.3 AGND Generator



AGND is analog common voltage. When ENGNDB=0, analog common voltage generator will active.

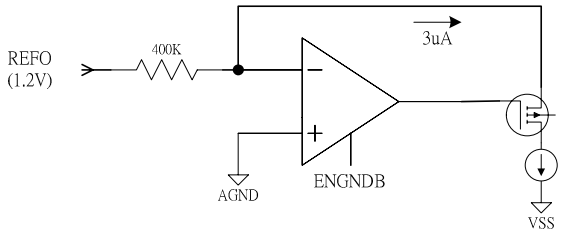
11.2.4 Bandgap Voltage Reference and Temperature sensor



REFO is low temperature coefficient bandgap voltage reference output. When ENBAND=1, the circuit will active. The output voltage to AGND is about 1.2V. Typical temperature coefficient is 100ppm/℃.

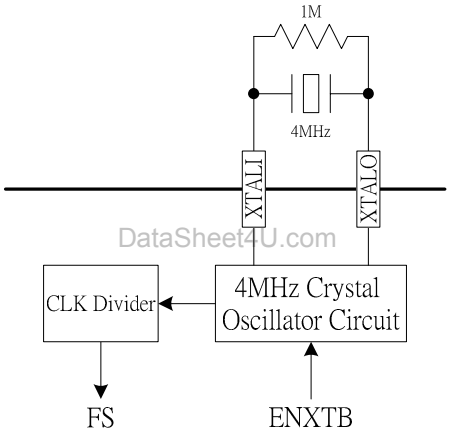
{TEMPH, TEMPL} is proportion to ambient temperature. You can select them to ADC input and transfer to digital code. (Typical 500uV±50uV/℃)

11.2.5 Bias Current Source Generator



The bias current for all the analog circuits of FS511. If the embedded op amp works, REFO will be pulled to AGND by the feedback; there are 1.2V in resistor 400K, and 3uA bias current can be obtained.

11.3 Clock Generator



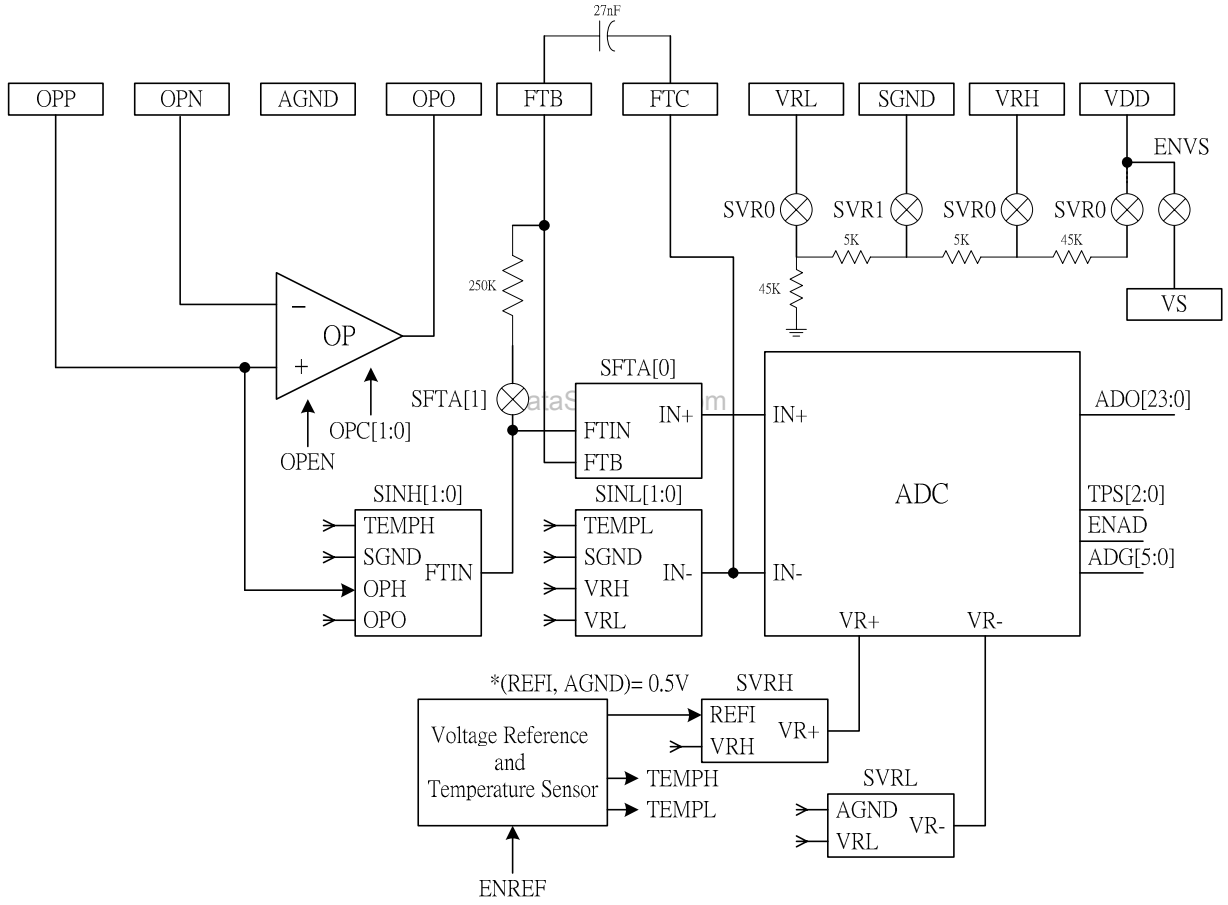
We connect a 4MHz crystal oscillator to the clock generator to generate a 4MHz clock frequency. A frequency divider is used to divide the clock signal to generate a signal FS, and the ADC uses this FS signal to do data conversion.

ENXTB	ENAD	FS
L	H	83.33 kHz
H	L	0, (L)

11.4 Function Network

Adress	Name		7	6	5	4	3	2	1	0
0	NETA[7:0]	R/W	SINL[1:0]		SINH[1:0]		SFTA[1:0]		SOPL[1:0]	
1	NETB[7:0]	R/W	OPEN	OPC[1:0]		ENREF	SVR1	SVR0	SVRL	SVRH
2	NETC[7:0]	R/W	ENAD	CPVR	ADG[5:0]					
3	NETD[7:0]	R/W	ENXTB	ENVS	CYS[1:0]		ENGNDB	TPS[2:0]		

4	ADCO[23:0]	R



11.4.1 Analog Multiplex:

1. Low Pass Filter Input:

SINH[1:0]	00	01	10	11
Select	OPO	OPH	SGND	TEMPH

2. ADC Negative Input:

SINL[1:0]	00	01	10	11
Select	VRL	VRH	SGND	TEMPL

3. Low Pass Filter Output, ADC Positive Input:

SFTA[0]	0	1
Select	FTB	FTIN

4. External Filter Control: SFTA[1]=1, FTIN and FTB short; SFTA[1]=0, FTIN and FTB open.

5. Internal Reference Voltage Control: SVR0=1, (VRH,VRL) = 1V (at VDD=5V). SVR1=1, SGND=1/2(VRH,VRL).

6. ADC Reference Voltage Negative Input:

SVRL	0	1
Select	VRL	AGND

7. ADC Reference Voltage Positive Input:

SVRH	0	1
Select	VRH	REFI

8. OPAMP Reference voltage Input:

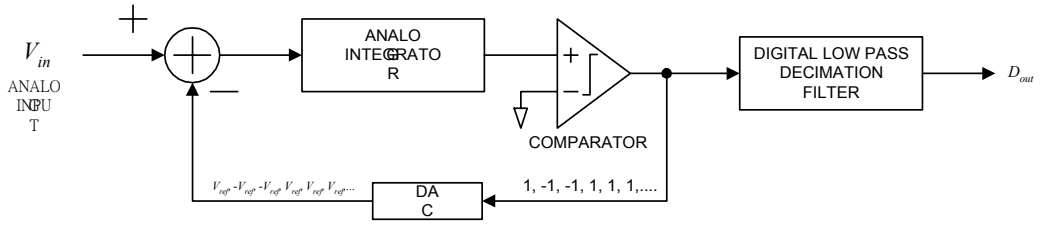
SOPL[1:0]	00	01	10	11
Select	VRL	VRH	SGND	AGND

11.4.2 OPAMP

1. OPEN is the OPAMP enable control signal.
2. OPC [1:0] can set OPAMP input operation mode as follows, 00: +Offset, 01: -Offset, 2KHz chopper frequency, 11: 1KHz Chopper frequency.

11.4.3 The Operation of the Delta-Sigma (ΔΣ) Modulator ADC

This high resolution ADC is designed by the technology of delta-sigma (ΔΣ) modulator. The continuous analog signals are sampled by a very high sampling rate that is much higher than the bandwidth of the input signal. The delta-sigma modulator converts the input signal to a series of 1-bit codes. These 1-bit codes are then fed to the digital filter to filter out the high frequency quantization noise to find high resolution digital outputs. This kind of ADC quantizes one bit in the analog part, therefore, it has very good linearity. Because it is in a fully differential configuration, the common mode rejection ratio (CMRR) is very high and can reduce the common mode signals effectively.



The Symbolic Diagram of the Delta-Sigma Analog-to-Digital Converter

The symbolic diagram of the delta-sigma ADC is shown as above. It consists of an analog subtractor, an integrator, a comparator, a 1-bit digital-to-analog converter (DAC), and a low-pass digital filter. The analog signals are continuously sampled and are subtracted by the expected voltage. The difference of the signals is fed into the integrator, and then the signal is compared with a reference voltage to find a digital output. This digital output is converted by the 1-bit DAC to become an analog signal (+Vref or -Vref) and then negatively fed back into the integrator. Due to the infinitive DC gain of the integrator, if the change of the input signal is much slower than the sampling speed, the average voltage obtained by the delta-sigma modulator will be very close to the input signal. In some resolution they can be treated to be the same, therefore, the 1-bit output data from the comparator are equivalent to the ± Vref analog signal values. The digital filter then decimates the 1-bit data to get a very high resolution digital code.
ENAD(ADG<7>) is the enable control signal for the ADC. It is 1 to enable the ADC; it is 0 to turn off the ADC and can save power.

11.4.3.1. Gain Stage Setting

There are four different gain paths to the input of the FS511 ADC, and they are controlled by control register ADG[3:0]. Two different gain paths control the input reference voltage, and they are controlled by control register ADG[5:4]. The gains shown here are not accurate. The accurate gains can be found by careful calibration.

Diagram of FS511Gain Stage Setting

By proper selection of the gain paths, this ADC can be applied to the optimum dynamic range for all the measuring applications. Table shows values of ADG[5:0] for three frequently used applications.

	First Scale	Second Scale	Third Scale
ADG<5:0>	01_0011	11_0111	11_1000
Reference Voltage Gain（G_{REFi}）	×1.0	×1.25	×1.25
Input Voltage Gain（G_{SIGi}）	×1.0	×1.25	×0.1

Table: FS511 ADC Typical Gain Setting

The transfer function for each scale is as follows,

Equation 1

$$D_x = \frac{G_{SIGi}}{G_{REFi}} \times \frac{v_x}{v_{ref}}$$

The gains for the reference voltages and input voltages shown in Table are approximate values. The accurate gains for the reference voltages and input voltages can be found by careful calibration.

11.4.3.2. Digital Filter

In Symbolic Diagram of the Delta-Sigma Analog-to-Digital Converter, the 1-bit output of the comparator should be fed to the digital low pass filter to do decimation to find the high resolution multiple-bit digital output. The transfer function of the FS511 digital filter is:

Equation 2

$$|H(f)| = \frac{1}{N^2}\left(\frac{\sin(N\pi f / f_S)}{\sin(\pi f / f_S)}\right)^2$$

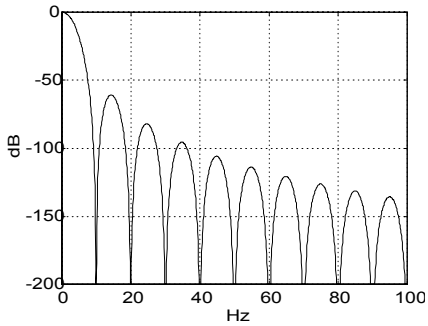
Where N is TAP of the digital filter.

Suppose the sampling rate of the ADC is 83.3KHz, the TAP of the digital filter is 8192. We can find the frequency response diagram of the digital filter as shown in Fig . The first zero is at:

Equation 3

$$f_{Z1} = \frac{f_S}{N} = \frac{83333\ \text{Hz}}{8192} \cong 10\ \text{Hz}$$

The Frequency Response Diagram of FS511 Digital Filter



The zero points fall at multiples of 10Hz. The digital filter will filter out all the signals near the zero points. From above figure., we can find that the noises at 50Hz and 60Hz are suppressed very well. If the sampling rate is 83KHz and the TAP of the filter is 16384, the first zero-frequency is at 5Hz.

The output rate is selected by TPS [2:0].

TPS [2:0]	TAP (N)	ADC Output Rate and First Zero Frequency（Hz）
111	16384	5
110	8192	10
101	4096	20
100	2048	40
011	1024	80
010	512	160
001	256	320
000	128	640

11.4.3.3. Reading and Calculating of Digital-to-Analog Converter

Due to the manufacture process drift, there is an offset voltage in the FS511 ADC such that an offset value is existed in the ADC output. In order to eliminate the offset value, FS511 provides three operation modes, which can be set by CYS <1:0> of control register NETD. The ADO output and calculation are different in different operation modes, and they are described in the following subsection.

ADC Output ADO
Set CYS<1:0>=00, the ADC inputs are short circuited, and we can find the negative offset voltage of the ADC from ADO[23:0].

Set CYS<1:0>=11, we can find the equivalent voltage of the input signal from ADO[23:0].

Set CYS<1:0>=01, and the ADO[23:0] output is the value of an ideal ADC. This mode is suitable for high resolution measurement.

When CYS<1:0>≠01, the output rate of ADO[23:0] is the first zero frequency, f_{Z1}, of COMB as described in Equation 3. When CYS<1:0> =01, the output rate equals $f_{Z1}/2$.

11.4.3.4. The Conversion of the Digital Codes and Equivalent Voltage

The output of the FS511 ADC is ADO[23:0], which is a 24-bit 2's complement number. ADO[23:0] is the sign bit; 0 represents a positive number, and 1 represents a negative number. The decimal point lies in between ADO[22] and ADO[21].

If ADO[23:0]=0010_1000_0000_0000_0000_0000, the equivalent floating point number is:

$$\begin{aligned} ADO &= 00.10\_1000\_0000\_0000\_0000\_0000 \\ &= 1\times 2^{-1} + 0\times 2^{-2} + 1\times 2^{-3} + 0\times 2^{-4} + 0\times 2^{-5} + ... + 0\times 2^{-22} \\ &= 0.5 + 0.125 = 0.625 \end{aligned}$$

Equation 4

If ADO[23:0]=1101_1111_1111_1111_1111_1111, the equivalent floating point number is:

$$\begin{aligned} ADO &= 11.01\_1111\_1111\_1111\_1111\_1111 \\ &= -(00.10\_0000\_0000\_0000\_0000\_0001) \\ &= -(1\times 2^{-1} + 0\times 2^{-2} + 0\times 2^{-3} + 0\times 2^{-4} + ... + 1\times 2^{-22}) \\ &= -0.5000002384 \end{aligned}$$

Equation 5

From Equation 1, if gain G' equals 1 and reference voltage V_{ref} =1.00000V, the value of ADO, 0010_1000_0000_0000_0000_0000, can be used to calculate the measured voltage as:

$$v_x = \frac{V_{ref}}{G'} \times D_x = \frac{1.00000\ \text{V}}{1} \times 0.625 = 0.62500\ \text{V}$$

。

If ADO=1101_1111_1111_1111_1111_1111, the measured voltage can be calculated:

$$v_x = \frac{V_{ref}}{G'} \times D_x = \frac{1.00000\ \text{V}}{1} \times -0.5000002384 = -0.50000\ \text{V}$$

。

However, due to the manufacture process drift G' is not exactly equal to 1, and there will be around $\pm 1\%$ offset. Similarly the reference voltage source and resistors may affect the reference voltage V_{ref}, and make V_{ref} not to be exact 1.00000V. Therefore, we have to calibrate the ADC.

11.4.3.5. Other Control Setting

CPVR is the enhancement mode for resistance measuring. It is set to 1 to improve the linearity when measuring resistance.

12. Application sample

Example Network setting:

Mode	NETA	NETB	NETC	NETD
ADC	88h	00h	93h	57h
OPAMP+ADC	88h	E0h	93h	57h

Demo Assembly code for Digital Interface:

```
;============================
; FS511_RW.ASM      version 0.0
; FS511 Read/Write use FS9822
; Edit by Jong            2003/6/27
;============================
Addr_bf     EQU EAH
RW_bf       EQU AL
Rd_cnt1     EQU counter0
Rd_cnt2     EQU counter1
CS_         EQU 3       ; Port3 bit 3
SK_         EQU 2       ; Port3 bit 2
DI_         EQU 1       ; Port3 bit 1
DO_         EQU 0       ; Port3 bit 0
FS511_PT        EQU PT3
FS511_PTEN      EQU PT3EN
FS511_PTPU      EQU PT3PU
Status      EQU 4
Work        EQU 5
C           EQU 1
;--------------------------------------------
; user define macro
;--------------------------------------------
dly     macro
        nop
        endm
cs_0 macro
        bcf    FS511_PT,3
        dly
        endm
cs_1 macro
        bsf    FS511_PT,3
        dly
        endm
sk_0 macro
        bcf    FS511_PT,2
        dly
        endm
sk_1 macro              ; 3.2us
        bsf    FS511_PT,2
        dly
        endm
di_0 macro
        bcf    FS511_PT,1
        dly
        endm
di_1 macro
        bsf    FS511_PT,1
        dly
        endm
sk_pls      macro
        sk_1
        sk_0
        endm

Wr511 macro d1,d2
        movlfd1,Addr_bf
        movlfd2,RW_bf
        call   _511W
        endm
Rd511 macro d1
        movlfd1,Addr_bf
        call   _511R
        endm
;--------------------------------------------
; Initial of port
;--------------------------------------------
511_ini:
        bsf    FS511_PTEN,CS_
        bsf    FS511_PTEN,SK_
        bsf    FS511_PTEN,DI_
        bcf    FS511_PTEN,DO_
        bsf    FS511_PTPU,DO_
        bsf    FS511_PT,CS_
        return



;--------------------------------------------
; FS511 Register Write sub function
```

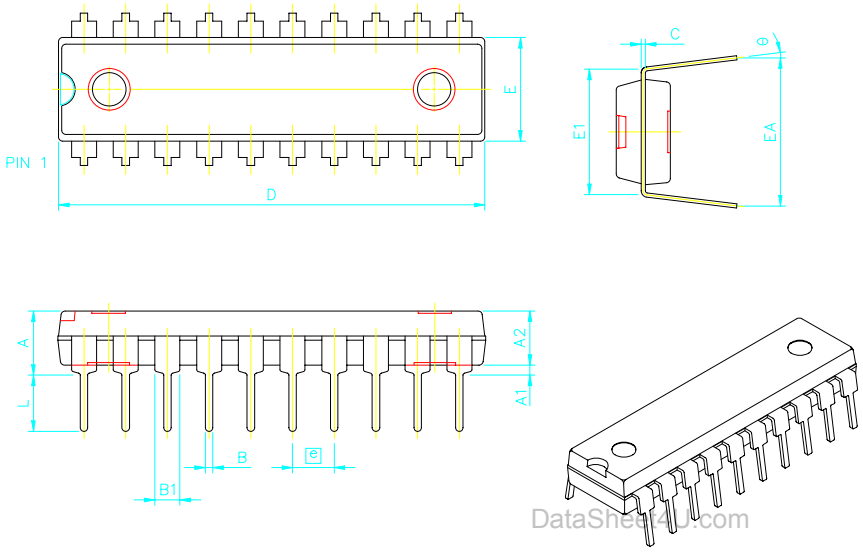
```
; use Addr_bf as address Buffer
; use RW_bf as Write Data buffer
;-----------------------------------------
_511W:
        cs_0
        di_0            ; 0
        sk_pls
        di_0            ;
        btfsc addr_bf,1 ;A<1>
        di_1            ;
        sk_pls
        di_0            ;
        btfsc addr_bf,0  ;A<0>
        di_1              ;
        sk_pls
        di_0            ;WR
        sk_pls
Send_data:
        bsf   RD_cnt1,3
        clrf  Status,C
 SendLoop:
        rlf   RW_bf,1
        di_0            ;
        btfsc Status,C  ;D<x>
        di_1            ;
        sk_pls
 SendLoopDec:
        decfsz      rd_Cnt1,1
        goto  SendLoop
        di_0
        cs_1
        return
;-----------------------------------------
; FS511 Register Read function
; use Addr_bf as address Buffer
; use RW_bf, ~+1, ~+2 as Read Data buffer
;-----------------------------------------
_511R:
        cs_0
        di_0            ;
        btfsc addr_bf,2 ;A<2>
        di_1            ;
        sk_pls
        di_0            ;
        btfsc addr_bf,1 ;A<1>
        di_1            ;
        sk_pls
        di_0            ;
        btfsc addr_bf,0 ;A<0>
        di_1            ;
        sk_pls
        di_1            ;RD
        sk_pls
        call  Get_data
        btfsc addr_bf,2
        call  Get_adc
        movwf     RW_bf
        cs_1
        di_0
        return

Get_data:
        clrf  work        ; rd_tmp
        bsf   rd_cnt1,3
 GetLoop:
        clrf  Status,C
        rlf   work,1
        btfsc FS511_PT,0
        bsf   work,0
        sk_pls
        decfsz      rd_Cnt1,1
        goto  GetLoop
        return

Get_adc:
        movwf     RW_bf+2
        call  Get_data
        movwf     RW_bf+1
        call  Get_data
        return
```

13. Package Information

13.1 Package Outline, DIP20

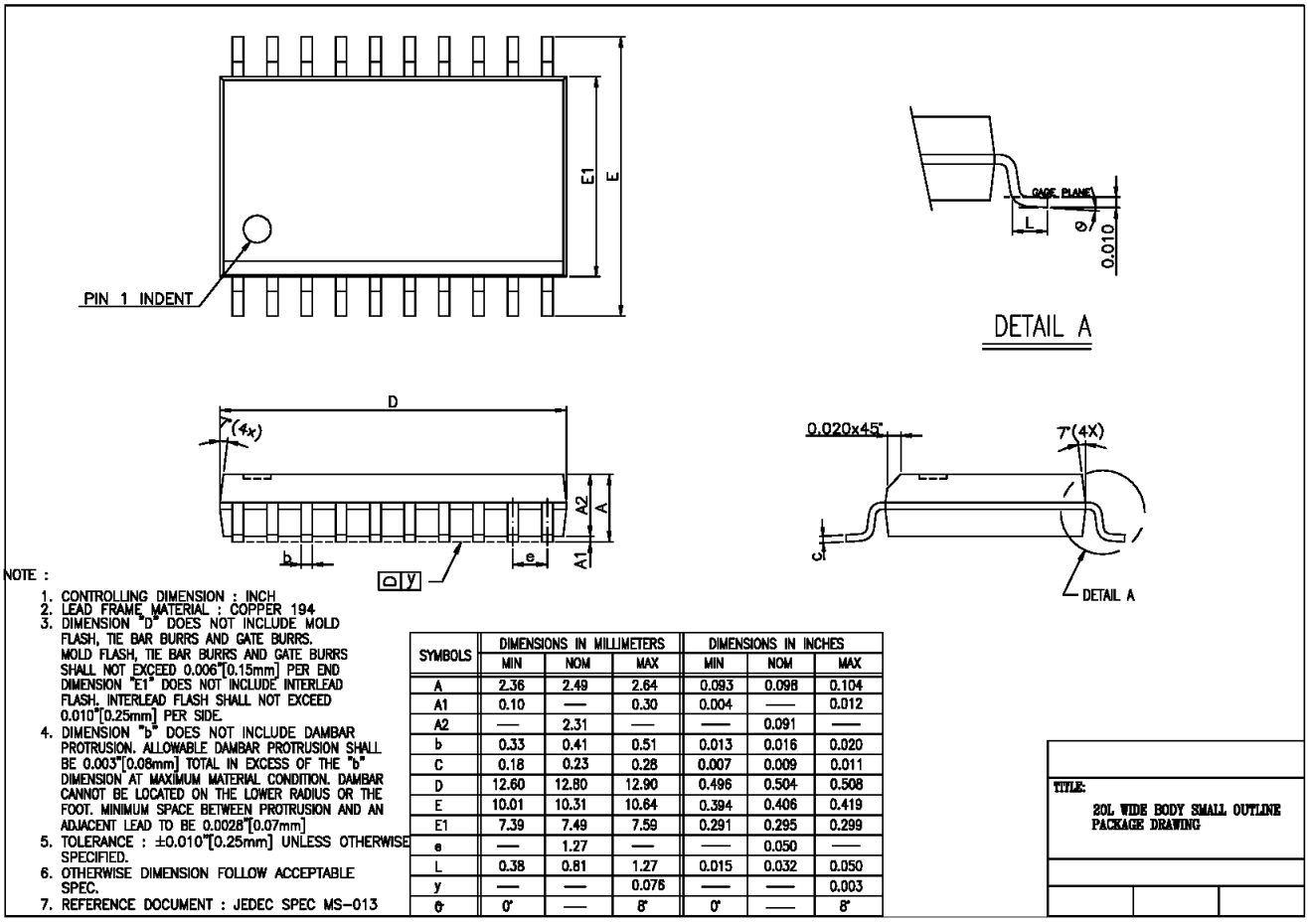


SYMBOL	DIMENSION IN INCH	DIMENSION IN MM
A	0.170 MAX.	4.318 MAX.
A1	0.015 MIN.	0.381 MIN.
A2	0.130±0.005	3.302±0.127
B	0.018 TYP.	0.457 TYP.
B1	0.060 TYP.	1.524 TYP.
C	0.010 NOM.	0.254 NOM.
D	1.026±0.005	26.060±0.127
E	0.252±0.005	6.401±0.127
E1	0.300±0.010	7.62±0.254
EA	0.355±0.020	9.017±0.508
e	0.100 TYP.	2.540 TYP.
L	0.130±0.010	3.302±0.254
θ	0°~15°	0°~15°

NOTE:
1.DIMENSION D & E DOES NOT INCLUDE FLASH.

DIP20

13.2 Package Outline, SOP20



NOTE :

1. CONTROLLING DIMENSION : INCH
2. LEAD FRAME MATERIAL : COPPER 194
3. DIMENSION "D" DOES NOT INCLUDE MOLD FLASH, TIE BAR BURRS AND GATE BURRS. MOLD FLASH, TIE BAR BURRS AND GATE BURRS SHALL NOT EXCEED 0.006"[0.15mm] PER END DIMENSION "E1" DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010"[0.25mm] PER SIDE.
4. DIMENSION "b" DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.003"[0.08mm] TOTAL IN EXCESS OF THE "b" DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD TO BE 0.0028"[0.07mm]
5. TOLERANCE : ±0.010"[0.25mm] UNLESS OTHERWISE SPECIFIED.
6. OTHERWISE DIMENSION FOLLOW ACCEPTABLE SPEC.
7. REFERENCE DOCUMENT : JEDEC SPEC MS-013

SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	2.36	2.49	2.64	0.093	0.098	0.104
A1	0.10	—	0.30	0.004	—	0.012
A2	—	2.31	—	—	0.091	—
b	0.33	0.41	0.51	0.013	0.016	0.020
C	0.18	0.23	0.28	0.007	0.009	0.011
D	12.60	12.80	12.90	0.496	0.504	0.508
E	10.01	10.31	10.64	0.394	0.406	0.419
E1	7.39	7.49	7.59	0.291	0.295	0.299
e	—	1.27	—	—	0.050	—
L	0.38	0.81	1.27	0.015	0.032	0.050
y	—	—	0.076	—	—	0.003
θ	0°	—	8°	0°	—	8°

TITLE:
20L WIDE BODY SMALL OUTLINE PACKAGE DRAWING

14. Revision History

Ver.	Date	Page	Description
0.3	unknown	-	Initial version of document.
1.0	2003/12/8	1	Revise "Electrical Characteristics, Micro-process Interface, Power System, Clock Generator, Function Network, Application Note"
		2	18-bit high-resolution 10Hz output rate (Programmable).
		3-4	Revise "Specification Table".
		8	Delete "Bandgap Voltage Reference and Temperature sensor"
		9-10	Deleted Bandgap Voltage Reference and Temperature sensor Network setting.
		15-16	Add "Example Network setting" and " Demo code for Digital interface"
1.1	2004/9/13	All	Reformat and correct the contents
		7	Add "Absolute Maximum Ratings".
		10	Add back "Bandgap Voltage Reference and Temperature sensor"
		12	Add back "Bandgap Voltage Reference and Temperature sensor" network.
		19	Add "Package Information"
1.2	2005/7/31	4	Add SOP20 Pb free package part number.
		20	Add Package Outline, SOP20
		21	Add Revision History