

Structure Silicon Monolithic IC

Product Name Capacitive Sensor Controller for Cellular Phone

Product No **BU21018MWV**

Features

- 1) High- resistive sensor material
- 2) High Speed Sensing
- 3) 3.0 V single power supply
- 4) 36ch sensors
- 5) 2ch reference (1ch only use is possible)
- 6) Automatic program download function for internal CPU

● Absolute maximum ratings

PARAMETER	SYMBOL	RATING	UNIT
Digital applied voltage	DVDD	-0.5 ~ 2.5	V
Analog applied voltage	AVDD	-0.5 ~ 4.5	V
Digital input voltage	Vdi	-0.5 ~ DVDD	V
Analog input voltage	Vai	-0.5 ~ AVDD	V
Storage temperature range	Tstg	-55 ~ 125	°C
Power dissipation	Pd	928*1	mW

(\*1) This is the power dissipation per IC unit. Reduce to 9.28 mW /°C when Ta = 25°C or above.

● Operating conditions

PARAMETER	SYMBOL	RATING	UNIT
Digital power supply	DVDD	1.60 ~ 2.00	V
Analog power supply	AVDD	2.70 ~ 3.60	V
Operating temperature range	Topr	-20 ~ 85	°C

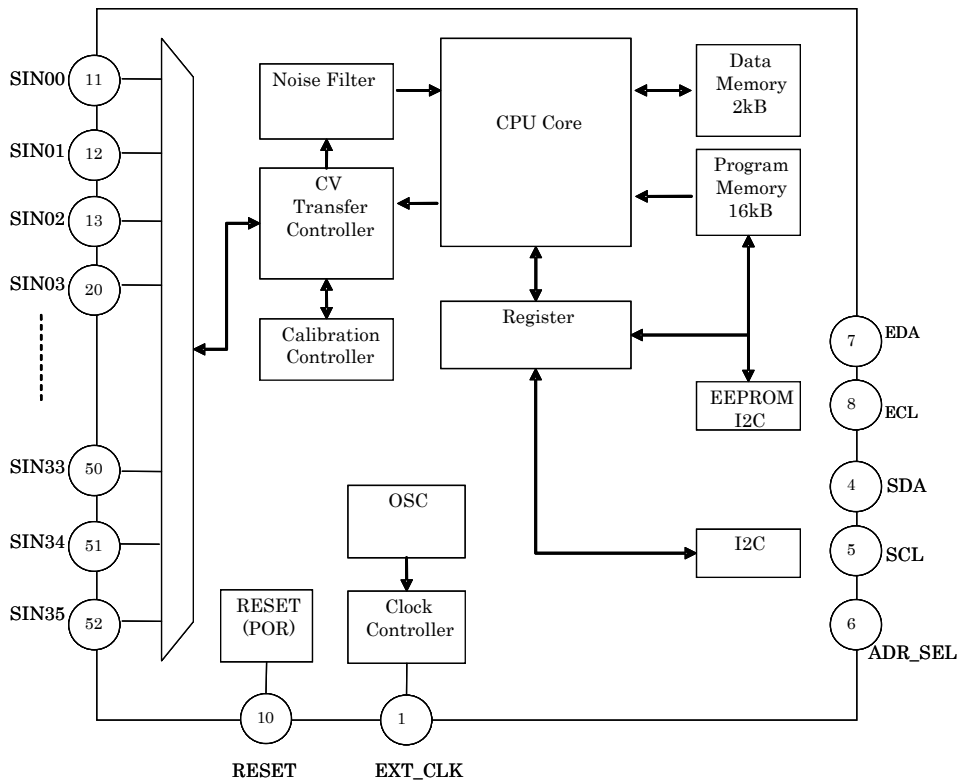
This chip is not designed to protect itself against radioactive rays.

●Electrical characteristics

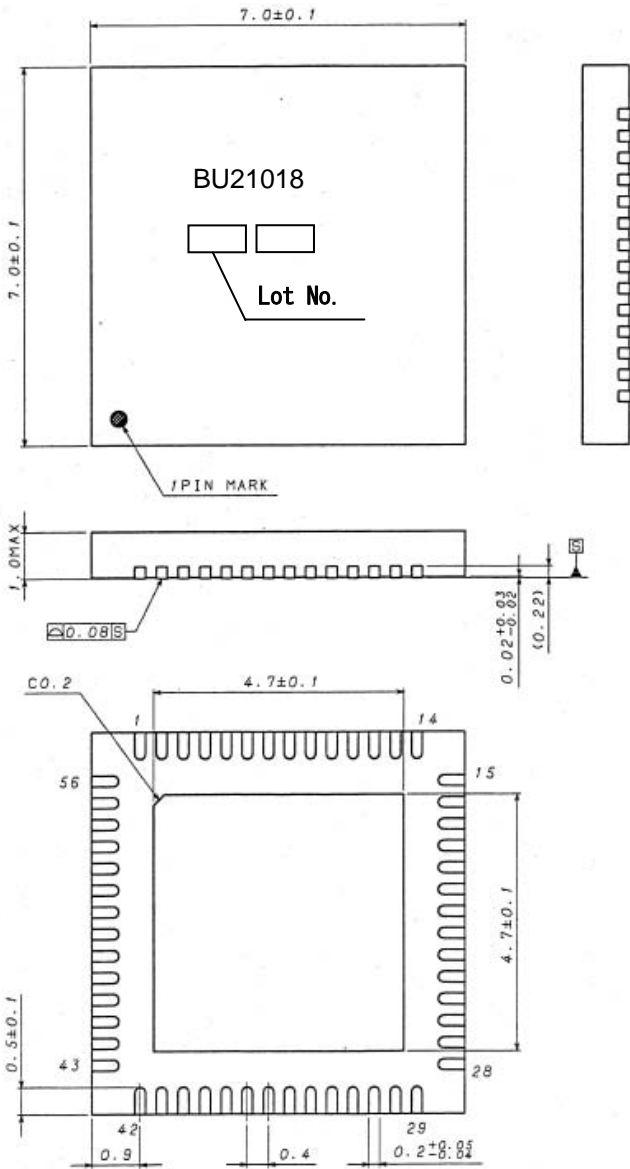
PARAMETER	SYMBOL	RATING			UNIT	CONDITION
		MIN	TYP	MAX		
Digital Low level input voltage	VIL1	-0.4	-	0.25*DVDD	V	
Digital High level input voltage	VIH1	0.7*DVDD	-	DVDD+0.5	V	
Digital Low level output voltage	VOL1	-	-	VSS+0.4	V	$I_{OL}=2.0[mA]$
Analog Low level output voltage	VOL2	-	-	VSS+0.45	V	$I_{OL}=1.0[mA]$
Analog High level output voltage	VOH2	LDO-0.4	-	LDO+0.5	V	$I_{OH}=-0.5[mA]$
OSC Frequency	Freq	21.0	24.0	27.0	MHz	
Digital standby current	Ist1	0	-	10	uA	
Analog standby current	Ist2	0	-	10	uA	
Digital operating current	Idd1	-	3	5.5	mA	
Analog operation current	Idd2	-	1	1.5	mA	

\*Ta = 25°C as long as it doesn't specify it.

●Block diagram



● External measure and View



Package : UQFN056V7070

● Pin description

PIN	NAME	DISCRIPTION
1	EXTCLK	External clock input
2	INT	Interrupt
3	NC	-
4	SDA	I2C:SDA
5	SCL	I2C:SCL
6	ADR_SEL	I2C: Address select "L" (1011100) <sub>2</sub> "H" (1011101) <sub>2</sub>
7	EDA	Automatic program download of EEPROM (SDA)
8	ECL	Automatic program download of EEPROM (SCL)
9	IFSEL	Interface select (Low fix)
10	DVDD	Digital power Connect to LDO pin.
11	SIN00	Sensor
12	SIN01	Sensor
13	SIN02	Sensor
14	LDO	LDO output*1
15	VSS	Ground
16	AVDD	Analog power
17	RESET	Reset "L" Reset "H" Release
18	SREF0	Reference sensor
19	SREF1	Reference sensor
20	SIN03	Sensor
21	SIN04	Sensor
22~50	SIN05~SIN33	Sensor
51	SIN34	Sensor
52	SIN35	Sensor
53	TEST0	Test (Low fix)
54	TEST1	Test (Low fix)
55	TEST2	Test (Low fix)
56	TEST3	Test (Low fix)

\*1 Please do not connect devices other than BU21018MWV.

## ● Cautions on use

## (1) Absolute Maximum Ratings

An excess in the absolute maximum ratings, such as supply voltage, temperature range of operating conditions, etc., can break down devices, thus making impossible to identify breaking mode such as a short circuit or an open circuit. If any special mode exceeding the absolute maximum ratings is assumed, consideration should be given to take physical safety measures including the use of fuses, etc.

## (2) Operating conditions

These conditions represent a range within which characteristics can be provided approximately as expected. The electrical characteristics are guaranteed under the conditions of each parameter.

## (3) Reverse connection of power supply connector

The reverse connection of power supply connector can break down ICs. Take protective measures against the breakdown due to the reverse connection, such as mounting an external diode between the power supply and the IC's power supply terminal.

## (4) Power supply line

Design PCB pattern to provide low impedance for the wiring between the power supply and the GND lines. In this regard, for the digital block power supply and the analog block power supply, even though these power supplies has the same level of potential, separate the power supply pattern for the digital block from that for the analog block, thus suppressing the diffraction of digital noises to the analog block power supply resulting from impedance common to the wiring patterns. For the GND line, give consideration to design the patterns in a similar manner.

Furthermore, for all power supply terminals to ICs, mount a capacitor between the power supply and the GND terminal. At the same time, in order to use an electrolytic capacitor, thoroughly check to be sure the characteristics of the capacitor to be used present no problem including the occurrence of capacity dropout at a low temperature, thus determining the constant.

## (5) GND voltage

Make setting of the potential of the GND terminal so that it will be maintained at the minimum in any operating state.

Furthermore, check to be sure no terminals are at a potential lower than the GND voltage including an actual electric transient.

## (6) Short circuit between terminals and erroneous mounting

In order to mount ICs on a set PCB, pay thorough attention to the direction and offset of the ICs. Erroneous mounting can break down the ICs. Furthermore, if a short circuit occurs due to foreign matters entering between terminals or between the terminal and the power supply or the GND terminal, the ICs can break down.

## (7) Operation in strong electromagnetic field

Be noted that using ICs in the strong electromagnetic field can malfunction them.

## (8) Inspection with set PCB

On the inspection with the set PCB, if a capacitor is connected to a low-impedance IC terminal, the IC can suffer stress.

Therefore, be sure to discharge from the set PCB by each process. Furthermore, in order to mount or dismount the set PCB to/from the jig for the inspection process, be sure to turn OFF the power supply and then mount the set PCB to the jig. After the completion of the inspection, be sure to turn OFF the power supply and then dismount it from the jig. In addition, for protection against static electricity, establish a ground for the assembly process and pay thorough attention to the transportation and the storage of the set PCB.

## (9) Input terminals

In terms of the construction of IC, parasitic elements are inevitably formed in relation to potential. The operation of the parasitic element can cause interference with circuit operation, thus resulting in a malfunction and then breakdown of the input terminal. Therefore, pay thorough attention not to handle the input terminals, such as to apply to the input terminals a voltage lower than the GND respectively, so that any parasitic element will operate. Furthermore, do not apply a voltage to the input terminals when no power supply voltage is applied to the IC. In addition, even if the power supply voltage is applied, apply to the input terminals a voltage lower than the power supply voltage or within the guaranteed value of electrical characteristics.

## (10) Ground wiring pattern

If small-signal GND and large-current GND are provided, it will be recommended to separate the large-current GND pattern from the small-signal GND pattern and establish a single ground at the reference point of the set PCB so that resistance to the wiring pattern and voltage fluctuations due to a large current will cause no fluctuations in voltages of the small-signal GND. Pay attention not to cause fluctuations in the GND wiring pattern of external parts as well.

## (11) External capacitor

In order to use a ceramic capacitor as the external capacitor, determine the constant with consideration given to a degradation in the nominal capacitance due to DC bias and changes in the capacitance due to temperature, etc.

## (12) Rush current

The IC with some power supplies has a capable of rush current due to procedure and delay at power-on. Pay attention to the capacitance of the coupling condensers and the wiring pattern width and routing of the power supply and the GND lines.

## (13) Others

In case of use this LSI, please peruse some other detail documents, we called, Technical note, Functional description, Application note.

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