TDA8035HN

Smart card interface

Rev. 1.0 — 19 April 2011 Product data sheet

1. General description

The TDA8035 is the cost efficient successor of the well established integrated contact smart card reader IC TDA8024. It offers a high level of security for the card performing current limitation, short circuit detection, ESD protection as well as supply supervision. Operating in 3 V supply domain, the current consumption during the standby mode of the contact reader is very low and is therefore the ideal component for a power efficient contact reader.

2. Features and benefits

2.1 Protection of the contact smart card

- Thermal and short-circuit protections on all card contacts
- Vcc regulation:
  - 5 V, 3 V, 1.8 V ± 5 % on 2 × 220 nF multilayer ceramic capacitors with low ESR
  - current spikes of 40 nA/s (Vcc = 5 V and 3 V) or 15 nA/s (Vcc = 1.8 V) up to 20 MHz, with controlled rise and fall times, filtered overload detection approximately 120 mA
- Automatic activation and deactivation sequences initiated by software or by hardware in the event of a short-circuit, card take-off, overheating, falling V_{REG} $V_{DD(INTF)}$,V_{DDP}
- Enhanced card-side ElectroStatic Discharge (ESD) protection of (> 8 kV)
- Supply supervisor for killing spikes during power on and off:
  - threshold internally fixed
  - externally by a resistor bridge

2.2 Easy integration into your contact reader

- SW compatible to TDA8024 and TDA8034
- 5 V, 3 V, 1.8 V smart card supply
- DC/DC converter for Vcc generation separately powered from 2.7 V to 5.5 V supply (VDDP and GNDP)
- Very low power consumption in Deep Shutdown mode
- Three protected half-duplex bidirectional buffered I/O lines (C4, C7 and C8)
- External clock input up to 26 MHz
- Card clock generation up to 20 MHz using pins CLKDIV1 and CLKDIV2 with synchronous frequency changes of f_{XTAL}, $f_{XTAL/2}$, $f_{XTAL/4}$ or $f_{XTAL/8}$
- Non-inverted control of pin RST using pin RSTIN
- Built-in debouncing on card presence contact
- Multiplexed status signal using pin OFFN

- Chip Select digital input for parallel operation of several TDA8035 ICs.

2.2.1 Other

- HVQFN32 package
- Compliant with ISO 7816, NDS and EMV 4.2 payment systems

3. Applications

- Pay TV
- Electronic payment
- Identification
- IC card readers for banking

4. Quick reference data

Table 1. Quick reference data

V_{DDP} = 3.3 V; $V_{DD(INTF)}$ = 3.3 V; f_{Xtal} = 10 MHz; GND = 0 V; T_{amb} = 25 °C; unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Supply						
V_{DDP}	power supply voltage		2.7	3.3	5.5	V
$V_{DD(INTF)}$	interface supply voltage		1.6	3.3	3.6	V
I_{DDP}	power supply current	Deep Shutdown mode; f_{XTAL} = stopped;	-	0.1	3	µA
		Shutdown mode; f_{XTAL} = stopped;	-	300	500	µA
		active mode; V_{CC} = +5 V CLK = $f_{XTAL}/2$; no load	-	-	5	mA
		active mode; CLK = $f_{XTAL}/2$; V_{CC} = +5 V; Icc = 65 mA	-	-	220	mA
		active mode; CLK = $f_{XTAL}/2$; V_{CC} = +3 V; I_{CC} = 65 mA	-	-	160	mA
		active mode; CLK = $f_{XTAL}/2$; V_{CC} = +1.8 V; Icc = 35 mA	-	-	120	mA
$I_{DD(INTF)}$	interface supply current	Deep Shutdown mode; f_{XTAL} = stopped; present card	-	-	1	µA
		Shutdown mode; f_{XTAL} = stopped; present card	-	-	1	µA
Internal supply voltage						
V_{DD}	supply voltage		1.62	1.8	1.98	V
Card supply voltage: pin V_{CC}						

Table 1. Quick reference data *...continued*

V_{DDP} = 3.3 V; $V_{DD(INTF)}$ = 3.3 V; f_{Xtal} = 10 MHz; GND = 0 V; T_{amb} = 25 °C; unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage	5 V card; DC I_{CC} < 65 mA	4.75	5.0	5.25	V
		5 V card; AC current spikes of 40 nAs	4.65	5.0	5.25	V
		3 V card; DC I_{CC} < 65 mA	2.85	-	3.15	V
		3 V card; AC current spikes of 40 nAs	2.76	-	3.24	V
		1.8 V card; DC I_{CC} < 35 mA	1.71	-	1.89	V
		1.8 V card; AC current spikes of 15 nAs	1.66	-	1.94	V
$V_{ripple(p-p)}$	peak-to-peak ripple voltage	from 20 kHz to 200 MHz	-	-	300	mV
I_{CC}	supply current	V_{CC} = 5 V or 3 V	-	-	65	mA
		V_{CC} = 1.8 V	-	-	35	mA
General						
t_{deact}	deactivation time	total sequence	35	90	250	µs
P_{tot}	total power dissipation	T_{amb} = −40 °C to +85 °C	-	-	0.45	W
T_{amb}	ambient temperature		-25	-	+85	°C

5. Ordering information

Table 2. Ordering information

Type number	Package		
	Name	Description	Version
TDA8035HN/C1	HVQFN32	plastic thermal enhanced very thin quad flat package; no leads; 32 terminals; body 5 × 5 × 0.85	SOT617-7

6. Block diagram

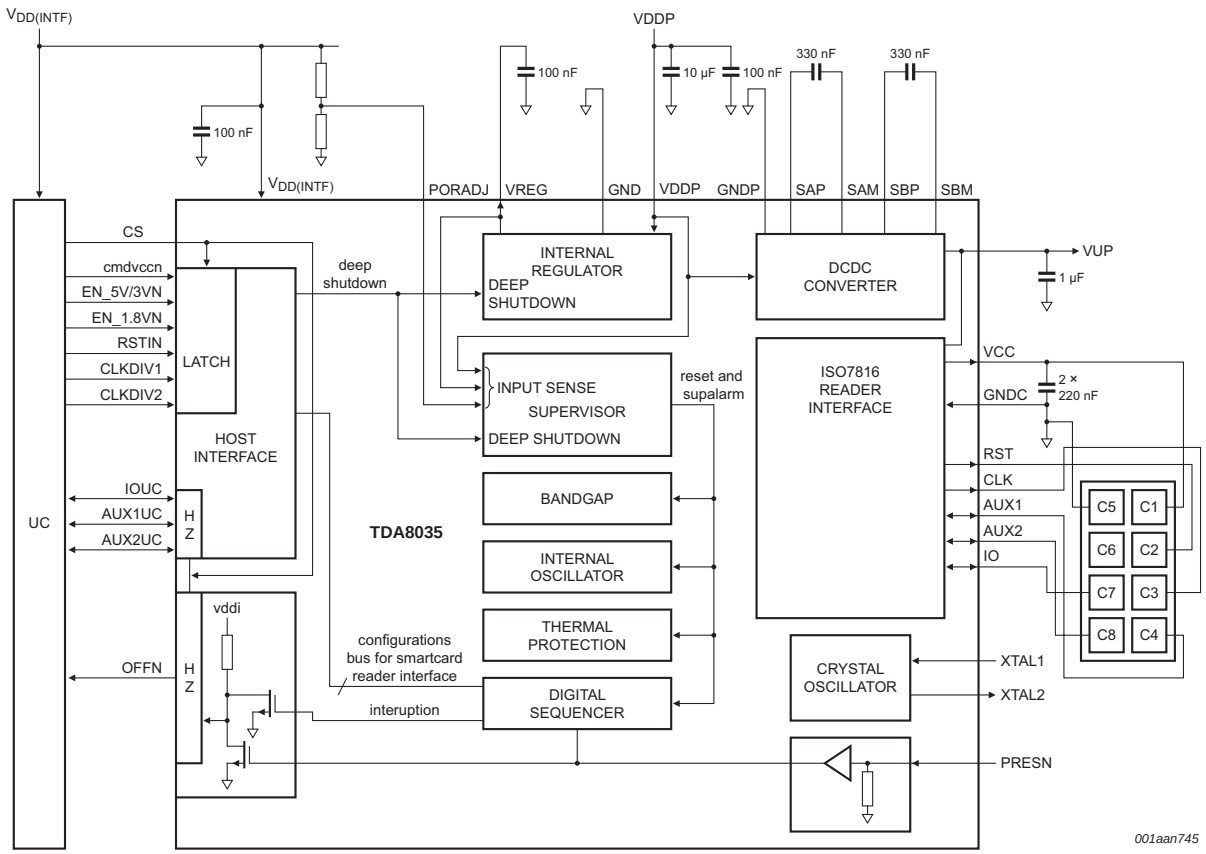


Fig 1. Block diagram

7. Pinning information

7.1 Pinning

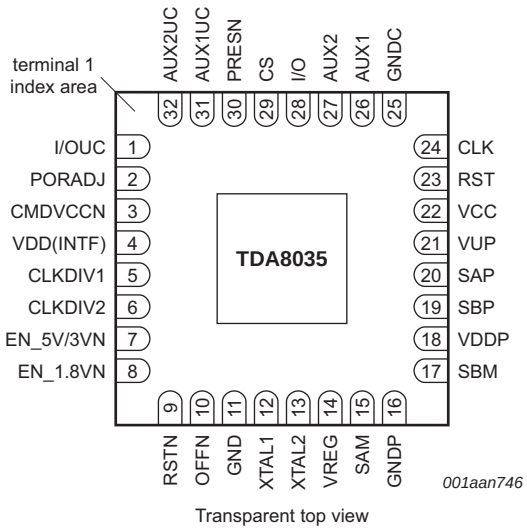


Fig 2. Pin configuration HVQFN32

7.2 Pin description

Table 3. Pin description

Symbol	Pin	Supply	Type	Description
I/OUC	1	$V_{DD(INTF)}$	I/O	host data I/O line (internal 10k pullup resistor to $V_{DD(INTF)}$)
PORADJ	2	$V_{DD(INTF)}$	I	Input for $V_{DD(INTF)}$ supervisor. PORADJ threshold can be changed with an external R bridge
CMDVCCN	3	$V_{DD(INTF)}$	I	start activation sequence input from the host (active LOW)
$V_{DD(INTF)}$	4	$V_{DD(INTF)}$	supply	interface supply voltage
CLKDIV1	5	$V_{DD(INTF)}$	I	control with CLKDIV2 for choosing CLK frequency see Table 4
CLKDIV2	6	$V_{DD(INTF)}$	I	control with CLKDIV1 for choosing CLK frequency see Table 4
EN_5V/3VN	7	$V_{DD(INTF)}$	I	control signal for selecting Vcc = 5 V (HIGH) or Vcc = 3 V (LOW) if EN_1.8 VN = High
EN_1.8 VN	8	$V_{DD(INTF)}$	I	control signal for selecting Vcc = 1.8V (low)
RSTIN	9	$V_{DD(INTF)}$	I	card reset input from the host (active HIGH)
OFFN	10	$V_{DD(INTF)}$	O	NMOS interrupt to the host (active LOW) with 10k internal pull up resistor to $V_{DD(INTF)}$ (See fault detection)
GND	11	-	supply	ground
XTAL1	12	$V_{DD(INTF)}$	I	crystal connection
XTAL2	13	$V_{DD(INTF)}$	O	crystal connection
VREG	14	V_{DDP}	supply	Internal supply voltage
SAM	15	V_{DDP}	I/O	DC/DC converter capacitor ; connected between SAM and SAP; C = 330nF with ESR < 100mΩ
GNDP	16	-	supply	DC/DC converter power supply ground

Table 3. Pin description *...continued*

Symbol	Pin	Supply	Type	Description
SBM	17	V_{DDP}	I/O	DC/DC converter capacitor ; connected between SBM and SBP; C = 330nF with ESR < 100mΩ
V_{DDP}	18	V_{DDP}	supply	Power supply voltage
SBP	19	V_{DDP}	I/O	DC/DC converter capacitor ; connected between SBM and SBP; C = 330nF with ESR < 100mΩ
SAP	20	V_{DDP}	I/O	DC/DC converter capacitor ; connected between SAM and SAP; C = 330nF with ESR < 100mΩ
VUP	21	V_{DDP}	I/O	DC/DC converter output decoupling capacitor connected between VUP and GNDP; C = 1uF with ESR < 100mΩ
Vcc	22	Vcc	O	supply for the card (C1)(decouple to GND with 2 × 220nF capacitors with ESR < 100mΩ).
RST	23	Vcc	O	card reset (C2)
CLK	24	Vcc	O	clock to the card (C3)
GNDC	25	-	supply	card signal ground
AUX1	26	Vcc	I/O	auxiliary data line to/from the card (C4)(internal 10 k pull up resistor to Vcc)
AUX2	27	Vcc	I/O	auxiliary data line to/from the card (C8)(internal 10 k pull up resistor to Vcc)
I/O	28	Vcc	I/O	data line to/from the card (C7)(internal 10 k pull up resistor toVcc)
CS	29	$V_{DD(INTF)}$	I	Chip Select input from the host (active High)
PRESN	30	$V_{DD(INTF)}$	I	card presence contact input (active LOW); if PRESN is true, then the card is considered as present. A debouncing feature of 4.05 ms typ. is built in.
AUX1UC	31	$V_{DD(INTF)}$	I/O	auxiliary data line to/from the host (internal 10 k pull up resistor to $V_{DD(INTF)}$)
AUX2UC	32	$V_{DD(INTF)}$	I/O	auxiliary data line to/from the host (internal 10 k pull up resistor to $V_{DD(INTF)}$)

8. Functional description

Remark: Throughout this document the ISO 7816 terminology conventions have been adhered to and it is assumed that the reader is familiar with these.

8.1 Power Supply

Power supply voltage V_{DDP} should be in the range from 2.7 to 5.5 V

All interface signals with the system controller are referenced to $V_{DD(INTF)}$. All card contacts remain inactive during powering up or powering down.

Internal regulator VREG should be in the range of 1.8 V

After powering the device, OFFN remains Low until CMDVCCN is set High and PRESN is Low .

During power off, OFFN falls Low when V_{DDP} is below the threshold voltage falling.

The frequency of the internal oscillator Foscint used for the activation sequences is put in low frequency mode in order to save power consumption as long as CMDVCCN is kept at high level (card not activated).

This device includes DC/DC converter to generate the 5 V, 3 V or 1.8 V card supply voltage (Vcc). The DC/DC converter should be supplied separately by Vddp and Gndp. The DC/DC converter operates as a voltage tripler, doubler or follower according to the respective values of Vcc and Vddp.

The operating mode is as follows (see Figure 3):

- Vcc = 5 V & Vddp > 3.8 V ; voltage doubler
- Vcc = 5 V & Vddp < 3.6 V; voltage tripler
- Vcc = 3 V & Vddp > 3.8 V; voltage follower
- Vcc = 3 V & Vddp < 3.6 V; voltage doubler
- Vcc = 1.8 V & Vddp > 3.8 V; voltage doubler
- Vcc = 1.8 V & Vddp < 3.6 V; voltage tripler

8.2 Voltage supervisor

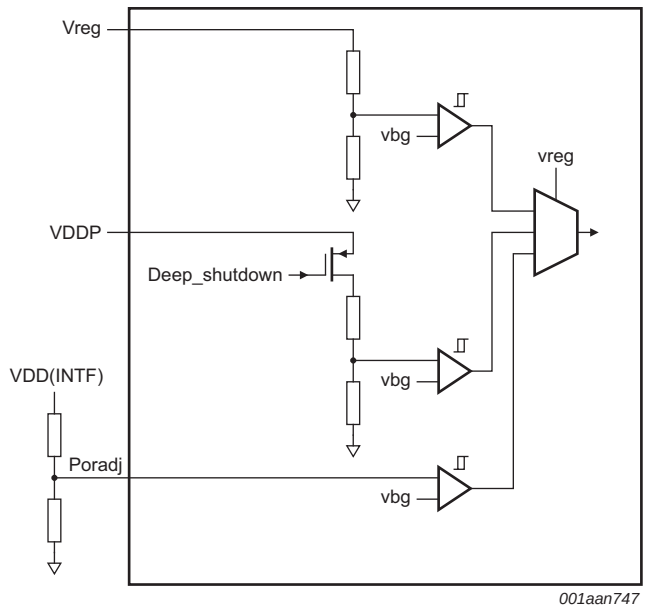


Fig 3. Block voltage supervisor

The voltage supervisor is used as a power on reset, and also as supply drop detection during a card session. The threshold of the voltage supervisor is set internally in the IC for V_{DDP} and V_{REG} whereas it can be adjusted externally for $V_{DD(INTF)}$ using the PORADJ pin. As long as V_{REG} is less than Vth(V_{REG}) + Vhys(V_{REG}), the IC will remain inactive whatever the levels on the command lines are. This also lasts for the duration of tw after V_{REG} has reached a level higher than Vth(V_{REG}) + Vhys(V_{REG}).The outputs of the $V_{DDP,}$ V_{REG} and $V_{DD(INTF)}$ supervisors are combined and sent to a digital controller in order to reset the TDA8035. This defined reset pulse of approximately 5.7 ms (tw=2048 $\times$ 1/(fosc(int)_Low) is used internally for maintaining the IC in a inactive mode during the supply voltage power-on; (see following pictures). When V_{REG} falls below Vth(V_{REG}) or when $V_{DD(INTF)}$falls below Vthextf or when V_{DDP} falls below Vth(VDDP) , a deactivation sequence is performed.

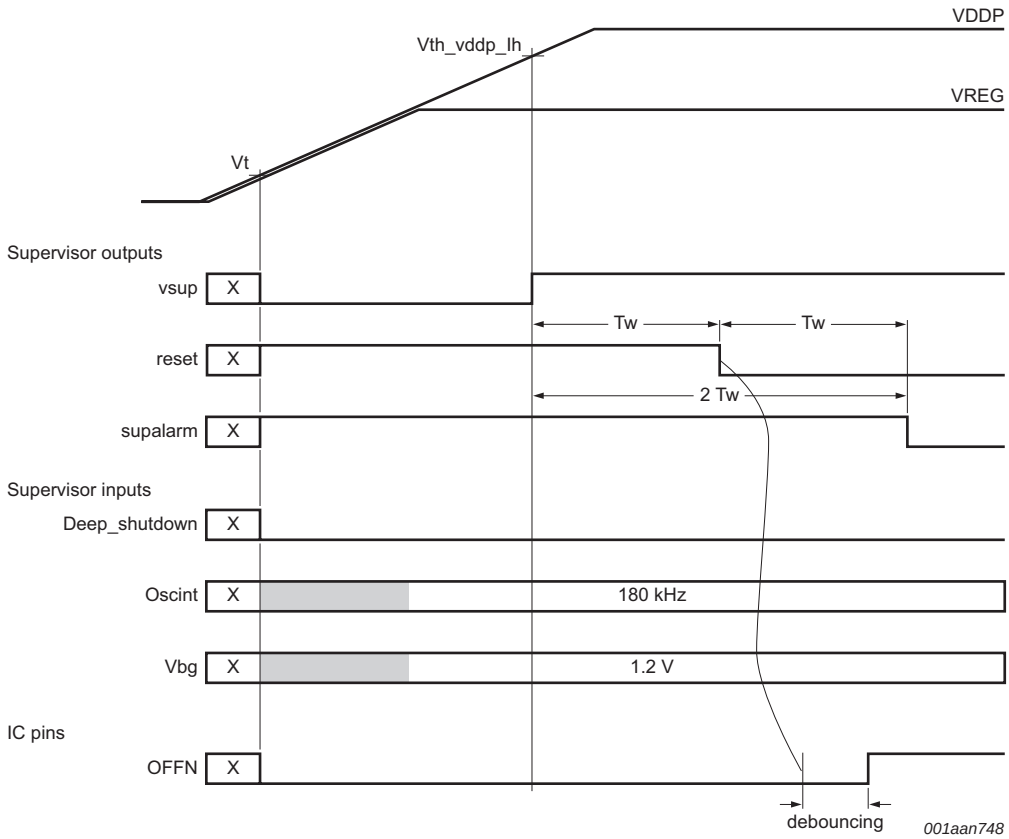


Fig 4. Voltage supervisor

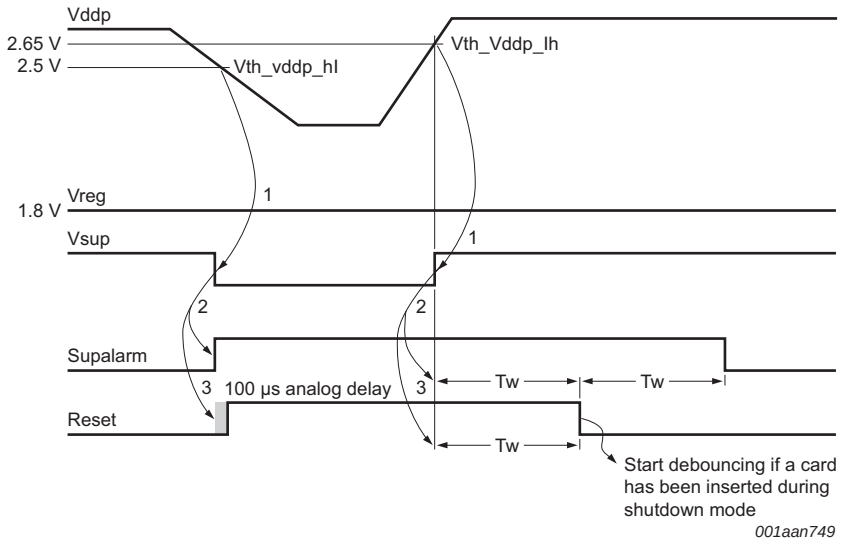


Fig 5. Voltage supervisor

8.3 Clock circuitry

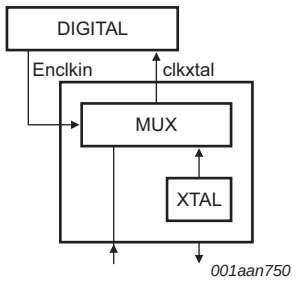


Fig 6. Switch external clock

To generate the card clock CLK, the TDA8035 can either use an external clock provided on XTAL1 pin or a crystal oscillator connected on both XTAL1 and XTAL2 pins. The TDA8035 automatically detects if an external clock is provided on XTAL1. So, there is no need of an extra pin to configure the clock source (external clock or crystal).

The automatic clock source detection is performed on each activation command (CMDVCCN pin falling edge). During a time window defined by the internal oscillator, the presence of an external clock on XTAL1 pin is checked. If a clock is detected, the crystal oscillator is kept stopped, else, the crystal oscillator is started. It is mandatory when an external clock is used, that the clock is applied on XTAL1 before CMDVCCN falling edge signal.

The frequency may be chosen as f_{XTAL}, $f_{XTAL/2}$, $f_{XTAL/4}$ or $f_{XTAL/8}$ via the pins CLKDIV1 and CLKDIV2. (Both selection inputs shall not be changed simultaneously: 10 ns minimum are required between changes on CLKDIV1/CLKDIV2).

The frequency change is synchronous, which means that during transition, no pulse is shorter than 45 % of the smallest period and that the first and last clock pulse around the change has the correct width. When changing dynamically the frequency, the change is effective only 10 periods of XTAL1 after the command.

The duty cycle on pin CLK shall be between 45 % and 55 % :

- When an external clock is used on XTAL1 pin , it should have a duty cycle of 48 % to 52 % when f_{XTAL} is used and rise and fall times shall respect values mentioned on table 7 $t_{r(i)}$, $t_f(i)$. It has to connect a 56 pF serial capacitor .
- CLK frequency is f_{XTAL},$f_{XTAL/2}$, $f_{XTAL/4}$ or $f_{XTAL/8}$:
  It is guaranteed between 45 % and 55 % of the period by the frequency dividers.

Table 4. Clock configuration

CLKDIV1	CLKDIV2	CLK
0	0	$f_{XTAL/8}$
0	1	$f_{XTAL/4}$
1	1	$f_{XTAL/2}$
1	0	f_{XTAL}

8.4 I/O circuitry

The three data lines I/O, AUX1 and AUX2 are identical.

The Idle state is realized by both lines (I/O and I/OUC) being pulled HIGH via a 10 k resistor (I/O to V_{CC} and I/OUC to $V_{DD(INTF))}$.

I/O is referenced to V_{CC}, and I/OUC to $V_{DD(INTF)}$, thus allowing operation with $V_{CC} \neq V_{DD(INTF)}$.

The first side on which a falling edge occurs becomes the master. An anti-latch circuit disables the detection of falling edges on the other line, which becomes a slave.

After a time delay $t_{d(edge)}$, the logic 0 present on the master side is transmitted to the slave side.

When the master side returns to logic 1, the slave side transmits the logic 1 during the time delay tpu, and then both sides return to their Idle states.

This active pull-up feature ensures fast Low to High transitions; it is able to deliver more than 1 mA up to an output voltage of 0.9 V_{CC} on a 80 pF load. At the end of the active pull-up pulse, the output voltage only depends on the internal pull-up resistor, and on the load current.

The current to/from the cards I/O lines is internally limited to 15 mA.

The maximum frequency on these lines is 1.5 MHz.

8.5 CS control

The CS (Chip Select) input allows multiple devices to operate in parallel. When CS is high, the system interface signals operate as described. When CS is low , the signals CMDVCCN, RSTIN, CLKDIV1, CLKDIV2, EN5V/3VN and EN1V8N are latched. I/OUC, AUX1UC and AUX2UC are set to high impedance pull up mode and won't pass data to or from the smart card. OFFN output is tri-stated.

8.6 Shutdown mode and Deep Shutdown mode

After power-on reset, the circuit enters the Shutdown mode if CMDVCCN input pin is to a logic-High. A minimum number of circuits are active while waiting for the micro-controller to start a session.

1. All card contacts are inactive (approximately 200 Ω to GND).
2. I/OUC, AUX1UC and AUX2UC are high impedance (10 k pull-up resistor connected to V_{DDI}).
3. Voltage generators are stopped.
4. Voltage supervisor is active.
5. The internal oscillator runs at its low frequency.

A Deep Shutdown mode can be entered by forcing CMDVCCN input pin to a logic-High state and EN5V/3VN, EN1V8N input pins to a logic-Low state. Deep Shutdown mode can only be entered when the smart card reader is inactive. In Deep Shutdown mode, all circuits are disabled. The OFFN pin follows the status of PRESN pin. To exit Deep Shutdown mode, change the state of one or more of the three control pins. Figure 8 shows the control sequence for entering and exiting.

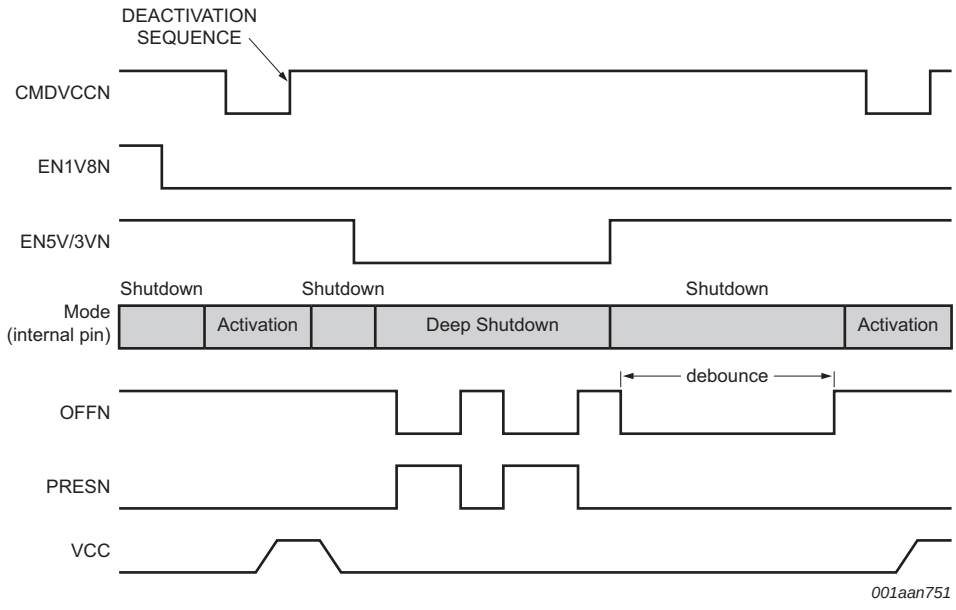


Fig 7. Shutdown mode and Deep Shutdown mode

8.7 Activation sequence

The following sequence then occurs with crystal oscillator (see Figure 8):

T = 64 × Toscint(freq high)

1. CMDVCCN is pulled Low (t0)
2. Crystal oscillator start up time (t0).
3. The internal oscillator changes to its high frequency & DC/DC starts (t1 = t0 + 768 × Tosc_Low)
4. V_{CC} rises from 0 to selected Vcc value (5 V, 3 V, 1.8 V) with a controlled slope ($t_2 = t_1 + 3T/2$)
5. I/O, AUX1 and AUX2 are enabled ($t_3 = t_1 + 10T$) (They were pulled LOW until this moment)
6. CLK is applied to the C3 contact ($t_4 = t_3 + x$) with 200 ns < x < 10 x 1/fXtal
7. RST is enabled ($t_5 = t_1 + 13T$).

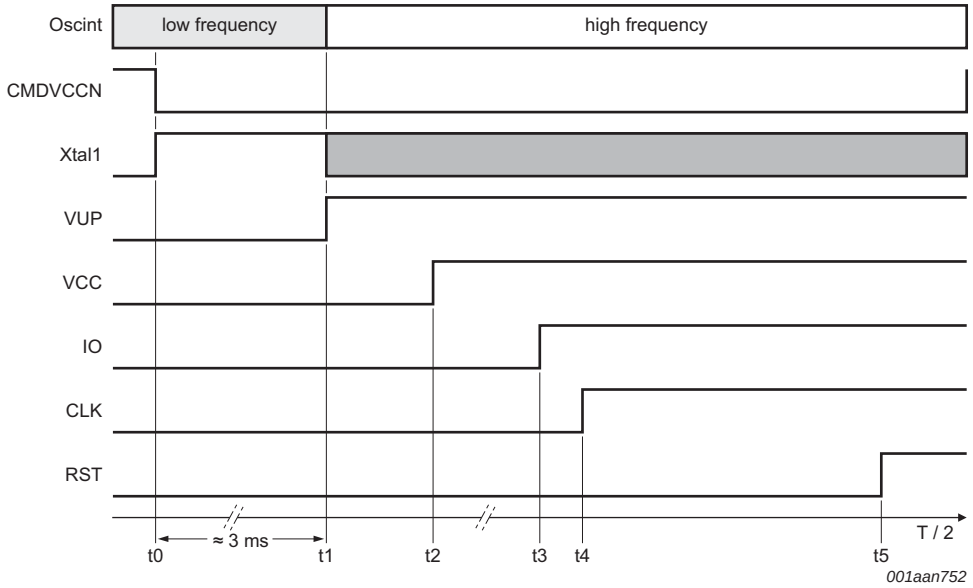


Fig 8. Activation sequence at t3

8.8 Deactivation sequence

When a session is completed, the micro-controller sets the CMDVCCN line to the HIGH state. The circuit then executes an automatic deactivation sequence by counting the sequencer back and ends in the inactive state (see Figure 9):

1. RST goes LOW ($t_{11} = t_{10} + 3T/64$)
2. CLK is stopped LOW ($t_{12} = t_{11} + T/2$)
3. I/O, AUX1 and AUX2 are pulled LOW ($t_{13} = t_{11} + T$)
4. V_{CC} falls to zero ($t_{14} = t_{11} + 3T/2$) (The deactivation sequence is completed when V_{CC} reaches its inactive state)
5. VUP falls to zero ($t_{15} = t_{11} + 7T/2$)
6. $V_{CC} < 0.4$ V ($t_{de} = t_{11} + 3T/2$ + Vcc fall time)
7. All card contacts become low-impedance to GND (I/OUC, AUX1UC and AUX2UC remain pulled up to $V_{DD(INTF)}$ via a 10 kΩ resistor).
8. The internal oscillator goes back to its lower frequency.

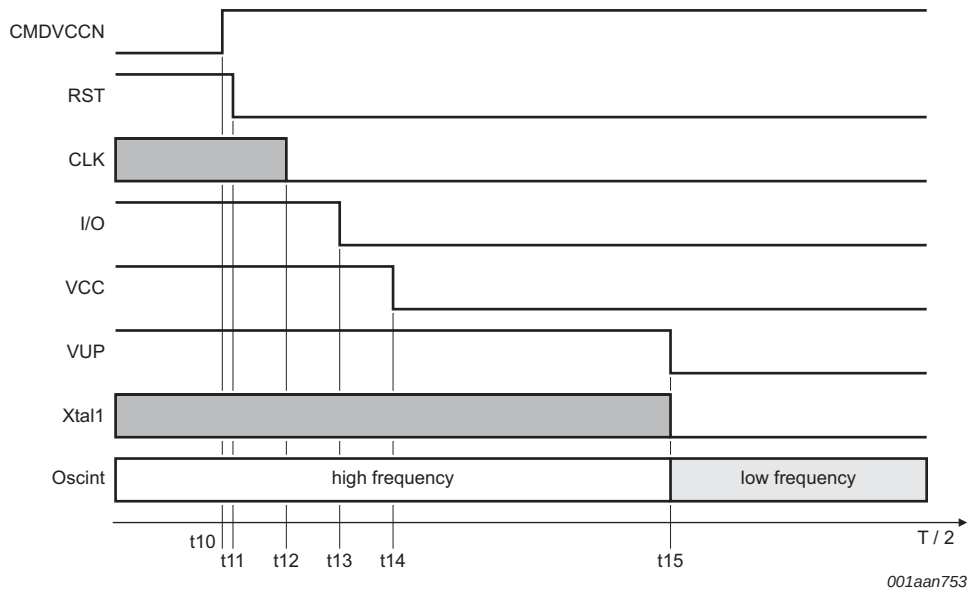


Fig 9. Deactivation sequence

8.9 VCC regulator

V_{CC} buffer is able to continuously deliver up to 65mA at Vcc = 5 V, 65 mA at Vcc = 3 V, 35 mA at Vcc =1.8 V .

It has an internal overload detection at approximately 125 mA.

This detection is internally filtered, allowing spurious current pulses of some ms up to 200 mA to be drawn by the card without causing a deactivation. (The average current value must stay below maximum).

8.10 Fault detection

The following fault conditions are monitored by the circuit:

1. Short-circuit or high current on V_{CC}
2. Card removal during transaction
3. V_{DDP} or $V_{DD(INTF)}$ or Vreg dropping
4. Overheating.

There are two different cases (see Figure 10 on page 16):

1. CMDVCCN High: (outside a card session) then, OFFN is Low if the card is not in the reader, and High if the card is in the reader. A supply voltage drop on V_{DDP} is detected by the supply supervisor, generates an internal power-on reset pulse, but does not act upon OFFN. The card is not powered-up, so no short-circuit or overheating is detected.
2. CMDVCCN Low: (within a card session) then, OFFN falls Low in any of the aforementioned cases. As soon as the fault is detected, an emergency deactivation is automatically performed. When the system controller sets CMDVCCN back to High, it may sense OFFN again after complete deactivation sequence in order to distinguish between a hardware problem or a card extraction (OFFN will then go back High if the card is still present).

Depending on the type of card presence switch within the connector (normally close or normally open), and on the mechanical characteristics of the switch, a bouncing may occur on PRESN signal at card insertion or withdrawal. Consequently, a debounce feature of approximately 4.05 ms (t_{deb} = 1280 × 1/(fosc(int)_Low) is integrated in the device.

Figure 11 on page 16 When the card is inserted, OFFN goes High only at the end of the debouncing time.

When the card is extracted, an automatic deactivation sequence of the card is performed on the first True/False transition on PRESN, and OFFN goes Low .

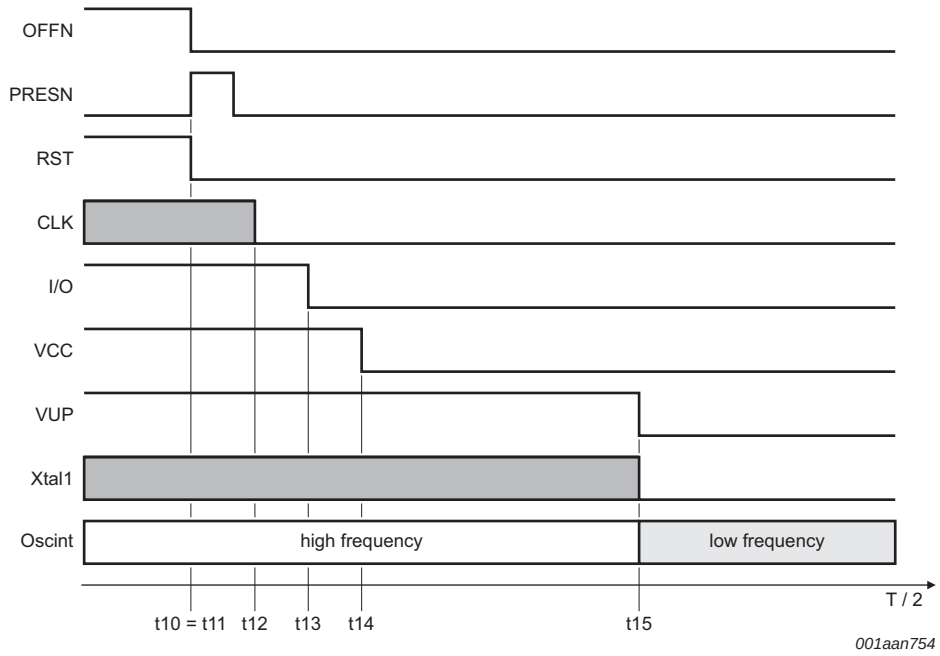


Fig 10. Emergency deactivation sequence (Card extraction)

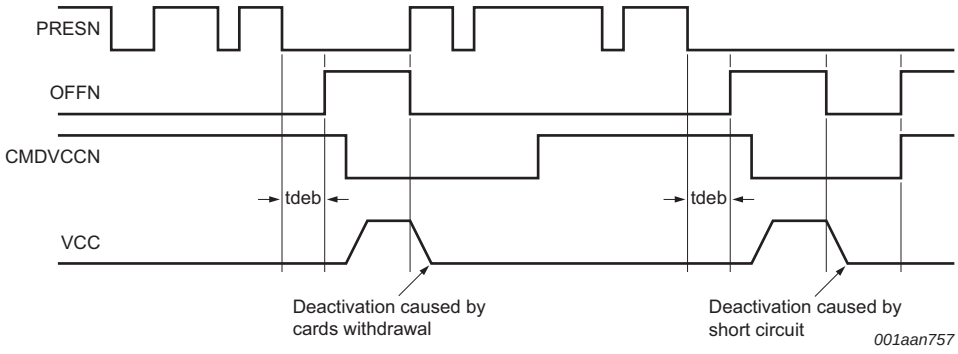


Fig 11. Behavior of OFFN, CMDVCCN, PRESN and Vcc

9. Limiting values

All card contacts are protected against any short with any other card contact.

Stress beyond these levels may cause permanent damage to the device. This is a stress rating only and functional operation of the device under this condition is not implied.

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DDP}	power supply voltage		–0.3	6	V
$V_{DD(INTF)}$	interface supply voltage		–0.3	4.1	V
V_{IH}	High-level input voltage	CS, PRESN, CMDVCCN, CLKDIV2, CLKDIV1, EN_1.8VN, EN_5V/3VN, RSTIN, OFFN, PORADJ, XTAL1, I/OUC, AUX1UC, AUX2UC, V_{DDP}, $V_{DD(INTF)}$	–0.3	4.1	V
		I/O, RST, AUX1, AUX2 and CLK	–0.3	5.75	V
T_{amb}	ambient temperature		–25	+85	°C
T_{stg}	storage temperature		–55	+150	°C
T_j	junction temperature			+125	°C
P_{tot}	total power dissipation	T_{amb} = –40 to +85 °C		0.45	W
V_{ESD}	electrostatic discharge voltage	Human Body Model (HBM) on card pins I/O, RST, V_{CC}, AUX1, CLK, AUX2, PRESN within typical application	–10	+10	kV
		Human Body Model (HBM) on all other pins	–2	+2	kV
		Machine Model (MM) on all pins	–200	+200	V
		Field Charged Device Model (FCDM) on all pins	–500	+500	V

10. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Package name	Parameter	Conditions	Typ	Unit
$R_{th(j-a)}$	HVQFN32	thermal resistance from junction to ambient	in free air with 4 thermal vias on pcb	55	K/W
			in free air without thermal vias on pcb	63	K/W

11. Characteristics

Table 7. Characteristics of IC

V_{DDP} = 3.3 V; $V_{DD(INTF)}$ = 3.3 V; f_{Xtal} = 10 MHz; GND = 0 V; T_{amb}=25 °C; unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Supply voltage						
V_{DDP}	power supply voltage		2.7	3.3	5.5	V
$V_{DD(INTF)}$	interface supply voltage		1.6	3.3	3.6	V
I_{DDP}	power supply current	Deep Shutdown mode; f_{XTAL} = stopped	-	0.1	3	µA
		Shutdown mode; f_{XTAL} = stopped	-	300	500	µA
		active mode; CLK = f_{XTA}/2; V_{CC} = +5 V; no load	-	-	5	mA
		active mode; CLK = f_{XTAL}/2 ; V_{CC} = +5 V; I_{CC} = 65 mA	-	-	220	mA
		active mode; CLK = f_{XTAL}/2 ; V_{CC} = +3 V; Icc = 65 mA	-	-	160	mA
		active mode; CLK=f_{XTAL}/2 ; V_{CC} = +1.8 V; I_{CC} = 35 mA	-	-	120	mA
$I_{DD(INTF)}$	interface supply current	Deep Shutdown mode f_{XTAL} = stopped; present card	-	-	1	µA
		Shutdown mode f_{XTAL} = stopped; present card	-	-	1	µA
$V_{th(VREG)}$	V_{th} threshold voltage	Internal voltage regulator falling	1.38	1.45	1.52	V
$V_{hys(VREG)}$	V_{hys} hysteresis voltage	Internal voltage regulator	90	100	110	mV
$V_{th(VDDP)}$	V_{th} threshold voltage	Pin V_{DDP} falling	2.15	2.25	2.35	V
$V_{hys(VDDP)}$	V_{hys} hysteresis voltage	Pin V_{DDP}	90	100	110	mV
t_W	pulse width		3	6.5	8.9	ms
$V_{th(L)(PORADJ)}$	LOW-level threshold voltage on pin PORADJ	External resistors on PORADJ	0.68	0.86	1.04	V
$V_{hys(PORADJ)}$	V_{hys} hysteresis voltage	Pin PORADJ	30	60	90	mV
I_L	leakage current	Pin PORADJ	–1	-	1	µA
V_{REG}						
V_O	output voltage		1.62	1.8	1.98	V
t_r	rise time	Exit of deep Shutdown mode	-	-	200	µs
VUP (DC/DC converter)						
V_{OH}	output voltage	V_{CC} = 5 V, I_{CC} < 65 mA DC	5.10	5.60	6.10	V
		V_{CC} = 3 V, I_{CC} < 65 mA DC	3.50	3.95	4.40	V
		V_{CC} = 1.8 V, I_{CC} < 35 mA DC	5.10	5.60	6.10	V
Card supply voltage (V_{CC}) (2 ceramic multilayer capacitances with low ESR 220 nF/220nF should be used in order to meet these specs)[1]						

Table 7. Characteristics of IC *...continued*

V_{DDP} = 3.3 V; $V_{DD(INTF)}$ = 3.3 V; f_{xtal} = 10 MHz; GND = 0 V; T_{amb}=25 °C; unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
C_{dec}	decoupling capacitance	connected on V_{CC} (220 nF + 220 nF 10 %)	396	-	484	nF
V_o	output voltage	inactive mode; no load	–0.1	-	+0.1	V
		inactive mode; I_o = 1 mA	–0.1	-	+0.3	V
I_o	output current	inactive mode & at grounded pin V_{CC}	-	-	–1	mA
V_{CC}	supply voltage	active mode; 5 V card; I_{CC} < 65 mA DC	4.75	5.0	5.25	V
		active mode; 3 V card; I_{CC} < 65 mA DC	2.85	3.05	3.15	V
		active mode; 1.8 V card; I_{CC} < 35 mA DC	1.71	1.83	1.89	V
		active mode; current pulses of 40 nAs with I_{CC} < 200 mA, t < 400 ns; 5 V card	4.65	5.0	5.25	V
		active mode; current pulses of 40 nAs with I_{CC} < 200 mA, t < 400 ns; 3 V card	2.76	-	3.20	V
		active mode; current pulses of 15 nAs with I_{CC} < 200 mA, t < 400 ns;1.8 V card	1.66	-	1.94	V
$V_{ripple(p-p)}$	peak to peak ripple voltage	from 20 kHz to 200 MHz	-	-	350	mV
I_{CC}	supply current	V_{CC} = 0 V to 5 V, 3V	-	-	65	mA
		V_{CC} = 0 V to 1.8V	-	-	35	mA
SR	slew rate	5 V card	0.055	0.18	0.8	V/µs
		3 V card	0.040	0.18	0.8	V/µs
		1.8 V card	0.025	0.18	0.8	V/µs
Crystal oscillator (XTAL1 and XTAL2)						
C_{ext}	external capacitance	connected on pins XTAL1/XTAL2 (depending on specification of crystal or resonator used)	-	-	33	pF
f_{XTAL}	crystal frequency		2	-	27	MHz
f_{XTAL1}	External frequency applied on XTAL1	with 56 pF serial capacitor	0	-	27	MHz
V_{IL}	LOW-level input voltage		–0.3	-	0.3 $V_{DD(INTF)}$	V
V_{IH}	HIGH-level input voltage		0.7$V_{DD(INTF)}$	-	$V_{DD(INTF)}$ + 0.3	V

Table 7. Characteristics of IC *...continued*

V_{DDP} = 3.3 V; $V_{DD(INTF)}$ = 3.3 V; f_{Xtal} = 10 MHz; GND = 0 V; T_{amb}=25 °C; unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{r(i)}$, $t_f(i)$	input rise time, input fall times	f_{CLK} = f_{XTAL1} = 20 MHz on external clock	-	-	4	ns
		f_{CLK} = f_{XTAL1} = 10 MHz on external clock	-	-	8	ns
		f_{CLK} = f_{XTAL1} = 5 MHz on external clock	-	-	16	ns
Data lines (pins I/O, I/OUC, AUX1, AUX2, AUXIUC, AUX2UC)						
t_d	delay time	falling edge on pins I/O and I/OUC or I/OUC and I/O	-	-	200	ns
$t_{w(pu)}$	pull-up pulse width		200		400	ns
f_{max}	maximum frequency	on data lines	-	-	1	MHz
C_i	input capacitance	on data lines	-	-	10	pF
Data lines to the card (pins I/O, AUX1, AUX2); (Integrated 10k pull up resistor connected to V_{CC})						
V_o	output voltage	inactive mode; no load	0	-	0.1	V
		inactive mode; I_o= 1 mA	0	-	0.3	V
I_o	output current	inactive mode & at grounded pin I/O	-	-	–1	mA
V_{OL}	LOW-level output voltage	I_{OL} = 1 mA	0	-	0.3	V
		$I_{OL} \geq$ 15 mA	V_{CC} – 0.4	-	V_{CC}	V
V_{OH}	HIGH-level output voltage	No DC load	0.9 V_{CC}	-	V_{CC} + 0.1	V
		I_{OH} < –40 µA 5 V or 3 V	0.75 V_{CC}		V_{CC} + 0.1	V
		I_{OH} < –20 µA 1.8 V card	0.75 V_{CC}		V_{CC} + 0.1	V
		$I_{OH} \geq$ –15 mA	0	-	0.4	V
V_{IL}	LOW-level input voltage		–0.3	-	0.8	V
V_{IH}	HIGH-level input voltage	V_{CC} = +5 V	0.6Vcc	-	V_{CC} + 0.3	V
		V_{CC} = +3 V or 1.8 V	0.7Vcc	-	V_{CC} + 0.3	V
V_{hys}	hysteresis voltage	on I/O	30	75	120	mV
I_{IL}	LOW-level input current	on I/O; V_{IL} = 0	-	-	600	µA
I_{LH}	HIGH-level leakage current	on I/O; V_{IH} = V_{CC}	-	-	10	µA
$t_{r(i)}$, $t_f(i)$	input rise time, input fall time	from V_{IL} max to V_{IH} min	-	-	1.2	µs
$t_{r(o)}$, $t_{f(o)}$	output rise time, output fall time	C_L <= 80 pF; 10 % to 90 % from 0 to V_{CC}	-	-	0.1	µs
R_{pu}	pull-up resistance	connected to V_{CC}	8k	10k	12k	Ω
I_{pu}	pull-up current	V_{OH} = 0.9 V_{CC}, C = 80 pF	–8	–6	–4	mA
Data lines to the system; pins I/OµC, AUX1µC, AUX2µC (Integrated 10k pull up resistor to $V_{DD(INTF)}$)						
V_{OL}	LOW level output voltage	I_{OL} = 1 mA	0	-	0.3	V

Table 7. Characteristics of IC *...continued*

V_{DDP} = 3.3 V; $V_{DD(INTF)}$ = 3.3 V; f_{Xtal} = 10 MHz; GND = 0 V; T_{amb}=25 °C; unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{OH}	HIGH level output voltage	No DC load	0.9 $V_{DD(INTF)}$	-	$V_{DD(INTF)}$ + 0.1	V
		$I_{OH} \leq 40$ µA; V_{DDI}>2V	0.75 $V_{DD(INTF)}$	-	$V_{DD(INTF)}$ + 0.1	V
		$I_{OH} \leq 20$ µA; V_{DDI}<2V	0.75 $V_{DD(INTF)}$	-	$V_{DD(INTF)}$ + 0.1	V
V_{IL}	LOW-level input voltage		–0.3	-	0.3 $V_{DD(INTF)}$	V
V_{IH}	HIGH-level input voltage		0.7 $V_{DD(INTF)}$		$V_{DD(INTF)}$ + 0.3	V
V_{hys}	hysteresis voltage	on I/Ouc	0.05 $V_{DD(INTF)}$	-	0.25 $V_{DD(INTF)}$	V
I_{LH}	HIGH-level input leakage current	$V_{IH} = V_{DDI}$			10	µA
I_{IL}	LOW-level input current	V_{IL} = 0			600	µA
R_{pu}	pull-up resistance	connected to $V_{DD(INTF)}$	8k	10k	12k	Ω
$t_{r(i)}$, t_f(i)	input rise & fall times	from V_{IL} max to V_{IH} min	-	-	1.2	µs
$t_{r(o)}$, $t_{f(o)}$	output rise & fall times	$C_L \leq 30$ pF; 10 % to 90 % from 0 to $V_{DD(INTF)}$	-	-	0.1	µs
I_{pu}	pull up current	V_{OH} = 0.9 V_{DD}, C = 30 pF	–1	-	-	mA
Internal oscillator						
$f_{osc(int)}$	internal oscillator frequency	inactive state : osc(int)_Low	230	315	430	kHz
		active state : osc(int)_High	2.0	2.5	3.0	MHz
Reset output to the card (RST)						
V_o	output voltage	inactive mode; no load	0	-	0.1	V
		inactive mode; I_o= 1 mA	0	-	0.3	V
I_o	output current	inactive mode & at grounded pin RST	-	-	–1	mA
t_d	between RSTIn and RST	RST enabled	-	-	200	ns
V_{OL}	LOW level output voltage	I_{OL}= 200 µA ,V_{CC} = +5 V	0	-	0.3	V
		I_{OL}= 200 µA ,V_{CC} = +3 V or 1.8 V	0	-	0.2	V
		I_{OL} = 20 mA (current limit)	V_{CC} – 0.4	-	V_{CC}	V
V_{OH}	HIGH level output voltage	I_{OH} = –200 µA	0.9 V_{CC}	-	V_{CC}	V
		I_{OH} = –20 mA (current limit)	0	-	0.4	V
tr, tf	rise and fall time	C_L = 100 pF V_{CC} = +5 V and +3 V	-	-	0.1	us
tr, tf	rise and fall time	C_L = 100 pF V_{CC} = +18 V	-	-	0.2	us
Clock output to the card (CLK)						
V_o	output voltage	inactive mode; no load	0	-	0.1	V
		inactive mode; I_o = 1 mA	0	-	0.3	V

Table 7. Characteristics of IC *...continued*

V_{DDP} = 3.3 V; $V_{DD(INTF)}$ = 3.3 V; f_{Xtal} = 10 MHz; GND = 0 V; T_{amb}=25 °C; unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_o	output current	inactive mode & at grounded pin CLK	-	-	–1	mA
V_{OL}	LOW level output voltage	I_{OL} = 200 µA	0	-	0.3	V
		I_{OL} = 70 mA (current limit)	V_{CC} – 0.4	-	V_{CC}	V
V_{OH}	HIGH level output voltage	I_{OH} = –200 µA	0.9 V_{CC}	-	V_{CC}	V
		I_{OH} = –70 mA (current limit)	0	-	0.4	V
t_r	rise time	C_L = 30 pF [2]	-	-	16	ns
t_f	fall time	C_L = 30 pF [2]	-	-	16	ns
f_{CLK}	frequency on pin CLK	operational	0	-	20	MHz
	duty cycle	C_L = 30 pF [2]	45	-	55	%
SR	slew rate	rise and fall; C_L = 30 pF; V_{CC} = +5 V	0.2	-	-	V/ns
		rise and fall; C_L = 30 pF; V_{CC} = +3 V	0.12	-	-	V/ns
		rise and fall; C_L = 30 pF; V_{CC} = +1.8 V	0.072	-	-	V/ns
Control inputs (pins CS, CMDVCCN, CLKDIV1, CLKDIV2, RSTIN, EN_5V/ 3VN, EN_1.8VN) [3]						
V_{IL}	LOW-level input voltage		–0.3	-	0.3 $V_{DD(INTF)}$	V
V_{IH}	HIGH-level input voltage		0.7 $V_{DD(INTF)}$	-	$V_{DD(INTF)}$ + 0.3	V
V_{hys}	hysteresis voltage	on control input	0.05 $V_{DD(INTF)}$	-	0.25 $V_{DD(INTF)}$	V
I_{LL}	LOW-level input leakage current	V_{IL} = 0	-	-	1	µA
I_{LH}	HIGH-level input leakage current	V_{IH} = $V_{DD(INTF)}$	-	-	1	µA
Card presence input (PRESN); PRESN has an integrated pull down resistor [3]						
V_{IL}	LOW-level input voltage		–0.3	-	0.3 $V_{DD(INTF)}$	V
V_{IH}	HIGH-level input voltage		0.7 $V_{DD(INTF)}$	-	$V_{DD(INTF)}$ + 0.3	V
V_{hys}	hysteresis voltage		0.05 $V_{DD(INTF)}$	-	0.1 $V_{DD(INTF)}$	V
I_{LL}	LOW-level input leakage current	V_{IL} = 0	-	-	1	µA
I_{LH}	HIGH-level input leakage current	V_{IH} = $V_{DD(INTF)}$	-	-	5	µA
OFFN output (pin OFFN is an NMOS drain with a 10k pull up resistor to $V_{DD(INTF)}$)						
V_{OL}	LOW level output voltage	I_{OL} = 2 mA	0	-	0.3	V
V_{OH}	HIGH level output voltage	I_{OH} = –15 µA	0.75 $V_{DD(INTF)}$	-		V
R_{pu}	pull-up resistance		8	10	12	kΩ
Protections and limitations						

Table 7. Characteristics of IC *...continued*

V_{DDP} = 3.3 V; $V_{DD(INTF)}$ = 3.3 V; f_{xtal} = 10 MHz; GND = 0 V; T_{amb}=25 °C; unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{sd}	shutdown temperature	at die	-	150	-	°C
I_{Olim}	output current limit	on pin I/O	–15	-	+15	mA
		on pin CLK	–70	-	+70	mA
		on pin RST	–20	-	+20	mA
		on pin V_{CC} = 5 V or 1.8 V	90	125	160	mA
		on pin V_{CC} = 3 V	90	160	260	mA
I_{sd}	shutdown current	on pin V_{CC} = 5 V or 1.8 V	80	115	150	mA
		on pin V_{CC} = 3 V	80	150	250	mA
Timings						
t_{act}	activation time	see Figure 8 on page 13	1847	-	3390	µs
t_{deact}	deactivation time	see Figure 9 on page 14	35	90	250	µs
t_{act}	activation time	time of the window for sending CLK to the card with XTAL1	1992	2690	3653	µs
		$t_{act(start)}$= t3; see Figure 8 on page 13	2055	2766	3749	µs
		$t_{act(end)}$=t5; see Figure 8 on page 13				
t_{deb}	debouncing time	on pin PRESN	2.96	4.05	5.55	ms

[1] To meet these specifications, V_{CC} should be decoupled to CGND using two ceramic multilayer capacitors of low ESR with values of either 220 nF.

[2] The transition time and the duty factor definitions are shown in Figure 12 on page 23.; d=t1/(t1+ t2)

[3] PRESN and CMDVCCN are active LOW; RSTIN is active HIGH; for CLKDIV1 and CLKDIV2 see Table 4.

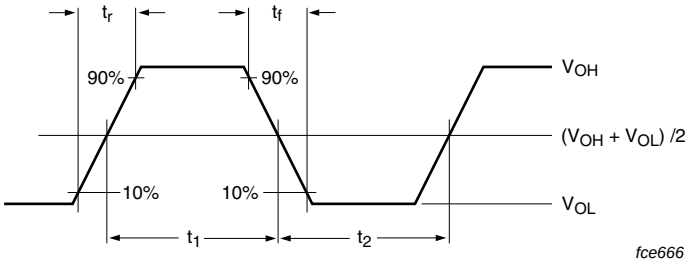
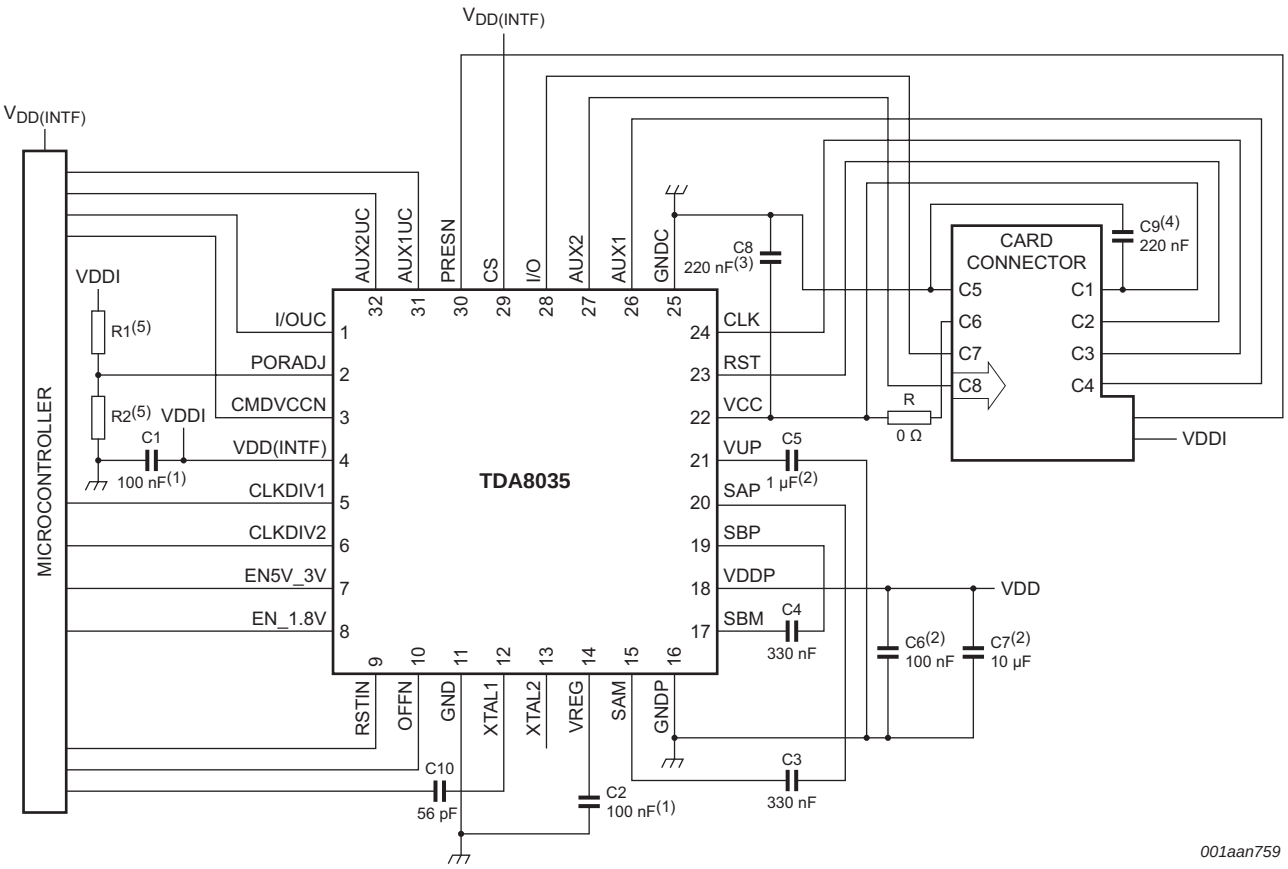


Fig 12. Definition of output and input transition times

12. Application information



(1) Place close to the protected pin with good (low resistive) and straight connection to the main ground.

(2) Place close to the supply pin with good (low resistive) and straight connection to GNDP.

(3) Place close to TDA8035´s VCC pin with good connection to GNDC.

(4) Place close to card connector´s C1 (VCC) pinwidth good connection to GNDC.

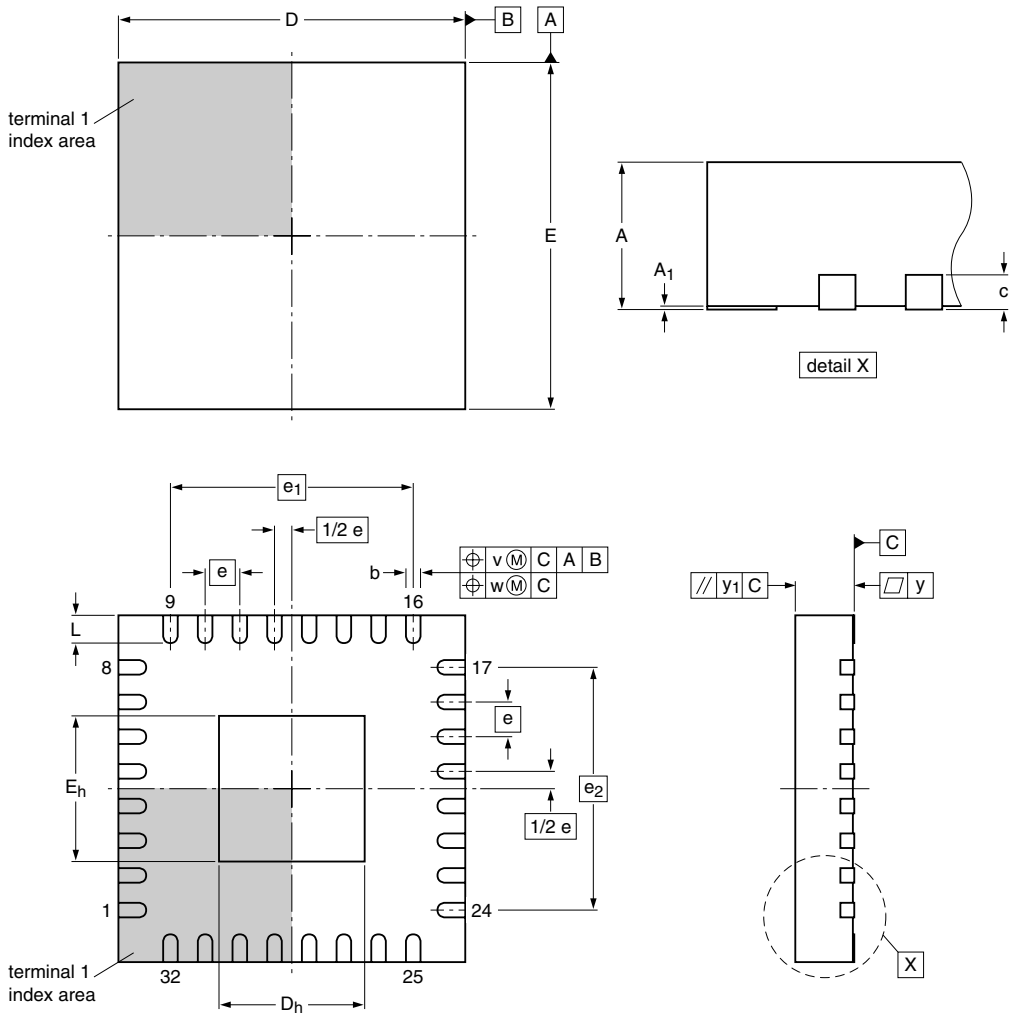
(5) Optional bridge. If not used, R1 must be O Ohm and R2 absent (direct connection to VDDI).

(6) GNDP and GNDC must be connected to the main ground with a straight and low resistive connection

Fig 13. Application diagram

13. Package outline

HVQFN32: plastic thermal enhanced very thin quad flat package; no leads; 32 terminals; body 5 x 5 x 0.85 mm **SOT617-7**



Dimensions

Unit		A	A_1	b	c	$D^{(1)}$	D_h	$E^{(1)}$	E_h	e	e_1	e_2	L	v	w	y	y_1
mm	max	1.00	0.05	0.30		5.1	2.2	5.1	2.2				0.5				
	nom	0.85	0.02	0.21	0.2	5.0	2.1	5.0	2.1	0.5	3.5	3.5	0.4	0.1	0.05	0.05	0.1
	min	0.80	0.00	0.18		4.9	2.0	4.9	2.0				0.3				

Note
1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

sot617-7_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT617-7		- - -	- - -			~~10-02-08~~ 10-02-09

Fig 14. Package outline SOT617-7

14. Soldering

14.1 Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *Data Handbook IC26; Integrated Circuit Packages* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering can still be used for certain surface mount ICs, but it is not suitable for fine pitch SMDs. In these situations reflow soldering is recommended.

14.2 Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, convection or convection/infrared heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferable be kept below 220 °C for thick/large packages, and below 235 °C small/thin packages.

14.3 Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C. A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

14.4 Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

14.5 Package related soldering information

Table 8. Suitability of surface mount IC packages for wave and reflow soldering methods

Package	Soldering method	
	Wave	Reflow[1]
BGA, HBGA, LFBGA, SQFP, TFBGA	not suitable	suitable
HBCC, HLQFP, HSQFP, HSOP, HTQFP, HTSSOP, HVQFN, SMS	not suitable[2]	suitable
PLCC[3], SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended[3][4]	suitable
SSOP, TSSOP, VSO	not recommended[5]	suitable

[1] All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods*.

[2] These packages are not suitable for wave soldering as a solder joint between the printed-circuit board and heatsink (at bottom version) can not be achieved, and as solder may stick to the heatsink (on top version).

[3] If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.

[4] Wave soldering is only suitable for LQFP, QFP and TQFP packages with a pitch (e) equal to or larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.

[5] Wave soldering is only suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

15. Abbreviations

Table 9. Abbreviations

Acronym	Description
ESD	ElectroStatic Discharge

16. Revision history

Table 10. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
TDA8035HN v. 1.0	20110419	Product data sheet	-	-

17. Legal information

17.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

17.2 Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

Product specification — The information and data provided in a Product data sheet shall define the specification of the product as agreed between NXP Semiconductors and its customer, unless NXP Semiconductors and customer have explicitly agreed otherwise in writing. In no event however, shall an agreement be valid in which the NXP Semiconductors product is deemed to offer functions and qualities beyond those described in the Product data sheet.

17.3 Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the *Terms and conditions of commercial sale* of NXP Semiconductors.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors accepts no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

Terms and conditions of commercial sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at http://www.nxp.com/profile/terms, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. NXP Semiconductors hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of NXP Semiconductors products by customer.

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from national authorities.

Quick reference data — The Quick reference data is an extract of the product data given in the Limiting values and Characteristics sections of this document, and as such is not complete, exhaustive or legally binding.

Non-automotive qualified products — Unless this data sheet expressly states that this specific NXP Semiconductors product is automotive qualified, the product is not suitable for automotive use. It is neither qualified nor tested in accordance with automotive testing or application requirements. NXP Semiconductors accepts no liability for inclusion and/or use of non-automotive qualified products in automotive equipment or applications.

In the event that customer uses the product for design-in and use in automotive applications to automotive specifications and standards, customer (a) shall use the product without NXP Semiconductors' warranty of the product for such automotive applications, use and specifications, and (b) whenever customer uses the product for automotive applications beyond NXP Semiconductors' specifications such use shall be solely at customer's own risk, and (c) customer fully indemnifies NXP Semiconductors for any liability, damages or failed product claims resulting from customer design and use of the product for automotive applications beyond NXP Semiconductors' standard warranty and NXP Semiconductors' product specifications.

17.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

18. Contact information

For more information, please visit: **http://www.nxp.com**

For sales office addresses, please send an email to: **salesaddresses@nxp.com**

19. Tables

20. Figures

21. Contents

For more information, please visit: http://www.nxp.com
For sales office addresses, please send an email to: salesaddresses@nxp.com

Date of release: 19 April 2011
Document identifier: TDA8035HN