Features

S422 Encoder Features

- Supports 4:2:2 Profile at Main Level (422P@ML), Main Profile at Main Level (MP@ML), Main Profile at High Level (MP@HL) and Simple Profile at Main Level (SP@ML)
- IPB, IP, IBI picture video compression mode with up to 2B pictures between references
- Real-time encoding up to:
  - 720x512 NTSC in 4:2:2 or 4:2:0 chroma format
  - 720x608 PAL in 4:2:2 or 4:2:0 chroma format
- Conversion of 704x512x60 fps and image sizes to HHR (1/2D1) and SIF sizes
- Field or frame encoding
- Produces compressed data rates up to 50Mb/s
- Supports motion estimation search range up to +/- 101H, +/- 64V
- Selectable MPEG-1 or MPEG-2 encoding format
- Adaptive field or frame motion estimation to half-pel accuracy
- Adaptive field or frame DCT
- Automatic adaptive quantization and rate controls
- Automatic scene change detection
- Support for dynamic GOP encoding
- Supports CBR,VBR and statistical multiplexing encoding
- Outputs picture statistics
- Repeat field detection (3/2 pulldown inversion)
- Includes hardware functions for performance and programmable functions for flexibility
- 8-bit CCIR 656 or 16-bit CCIR 601 input
- 16-bit generic host interface
- Outputs compressed data to FIFO or field memory
- External FIFO feedback for dynamic rate control
- Insertion of user data in encoded stream
- Selectable 8 to 11 bit DC precision
- Frame accurate start/stop
- User-specifiable quantizer tables
- Optimization of luma and chroma encoding utilizing separate quantization tables
- Programmable conversion of 4:2:2 chroma format to 4:2:0 chroma format
- Selectable compression parameters and controls
- Interfaces directly to standard 3.3 V/5.0 V SDRAM/SGRAM/SSRAM
- JTAG for system test
- CMOS 0.27 µm technology packaged in 35 mm plastic ball grid array module with 352 I/Os and 4.4 watts nominal power dissipation.
- Part number: IBM39MPEGS422PBA17C

S420 Encoder Features

- Supports MPEG-2 Main Profile at Main Level (MP@ML) plus extensions, Main Profile at High Level (MP@HL) and Simple Profile at Main Level (SP@ML)
- IPB, IP, IBI and I picture video compression modes with up to 2B pictures between references
- Real-time encoding in 4:2:0 format up to:

  720x480 NTSC

  720x576 PAL
- Conversion of 720x480x60 fps and 720x576x50 fps image sizes to HHR (1/2 D1) and SIF sizes
- Field or frame encoding
- Produces compressed data rates up to 50Mb/s
- Supports motion estimation search range up to +/- 101H, +/- 64V
- Selectable MPEG-1 or MPEG-2 encoding format
- Adaptive field or frame motion estimation to half-pel accuracy
- Adaptive field or frame DCT
- Automatic adaptive quantization and rate controls
- Automatic scene change detection
- Support for dynamic GOP encoding
- Supports CBR,VBR and statistical-multiplexing encoding
- Outputs picture statistics
- Repeat field detection (3/2 pulldown inversion)
- Includes hardware functions for performance and programmable functions for flexibility
- 8-bit CCIR 656 or 16-bit CCIR 601 input
- 16-bit generic host interface

- Outputs compressed data to FIFO or field memory
- External FIFO feedback for dynamic rate control
- Insertion of user data in encoded stream
- Selectable 8 to 11 bit DC precision
- Frame accurate start/stop
- User-specifiable quantizer tables
- Programmable conversion of 4:2:2 chroma format to 4:2:0 chroma format
- Selectable compression parameters and controls
- Interfaces directly to standard 3.3 V/5.0 V SDRAM/SGRAM/SSRAM
- JTAG for system test
- CMOS 0.27µm technology packaged in 35 mm plastic ball grid array module with 352 I/Os and 4.1 watts nominal power dissipation
- Part number: IBM39 MPEGS420 PBA 18C

SI Encoder Features

- Supports MPEG-2 4:2:2 Profile at Main Level (422@ML) plus extensions, Main Profile at High Level (MP@HL) and Simple Profile at Main Level (SP@ML)
- I frame only picture video compression
- Real-time encoding in 4:2:2 format up to:

  720x512 NTSC

  720x608 PAL
- Conversion of 720x512x60 fps and 720x608x50 fps image sizes to HHR (1/2 D1) and SIF sizes
- Field or frame encoding
- Produces compressed data rates up to 50Mb/s
- Selectable MPEG-1 or MPEG-2 encoding format
- Adaptive field or frame motion estimation to half-pel accuracy
- Adaptive field or frame DCT
- Automatic adaptive quantization and rate controls
- Automatic scene change detection
- Supports CBR,VBR and statistical-multiplexing encoding
- Outputs picture statistics
- Repeat field detection (3/2 pulldown inversion)
- Includes hardware functions for performance and programmable functions for flexibility
- 8-bit CCIR 656 or 16-bit CCIR 601 input
- 16-bit generic host interface
- Outputs compressed data to FIFO or field memory
- External FIFO feedback for dynamic rate control
- Insertion of user data in encoded stream
- Selectable 8 to 11 bit DC precision
- Frame accurate start/stop
- User-specifiable quantizer tables

- Programmable conversion of 4:2:2 chroma format to 4:2:0 chroma format
- Selectable compression parameters and controls
- Interfaces directly to standard 3.3 V/5.0 V SDRAM/SGRAM/SSRAM
- JTAG for system test
- CMOS 0.27µm technology packaged in 35 mm plastic ball grid array module with 352 I/Os and 1.7 watts nominal power dissipation
- Part number: IBM39 MPEGSI PBA 18C

Description

MPEGS422 Professional Studio Encoder

MPEGS422 Professional Studio Encoder maintains IBM's leadership position in 4:2:2 profile applications and addresses the special needs of high quality applications. The chip supports MPEG-2 IBP encoding for 4:2:2 Profile at Main Level and compressed data rates up to 50 Mb/s. It maintains this conformance with a search range of +/-101H, +/-64V.

MPEGS420 Professional Broadcast Encoder

IBM's MPEGS420 Professional Broadcast Encoder provides real-time 4:2:0 MPEG-2 encoding at CCIR601 resolution. The MPEG420 offers high performance and functionality at a search range of +/- 101H, +/-64V and data rates up to 50 Mb/s. The MPEGS420 can also be configured by the user for 15Mb/s (or less) compressed data rates, and for a search range of +/-64H, +/-56V. This allows ASRAM to replace SSRAM on the search memory interface. User selectable chrominance down sampling from 4:2:2 and 4:2:0 in either progressive or interlaced mode assures color quality.

MPEGSI Intra-Frame Encoder

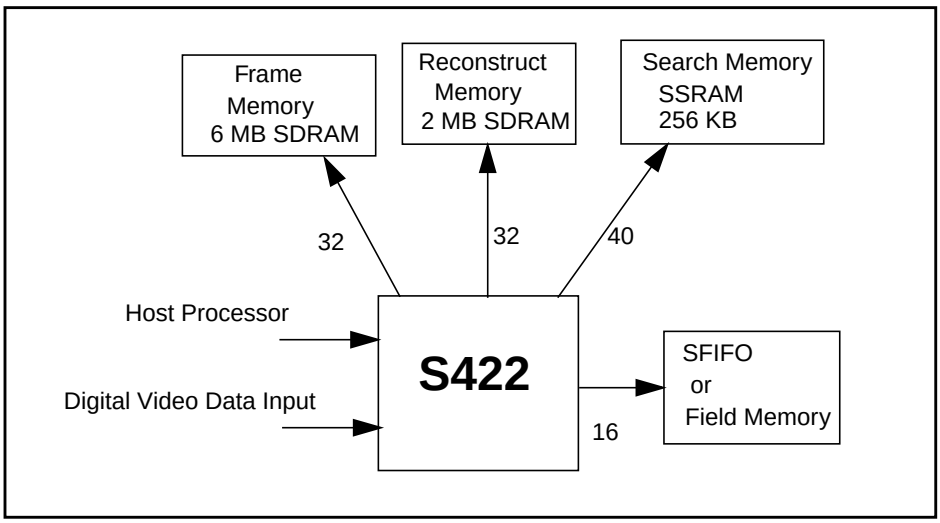
IBM's MPEGSI Intra-Frame Encoder offers the flexibility and editability of an intra-frame bitstream along with the excellent picture achieved through many of the rate control features available on the MPEGS422 product. Image statistics and user-specified encoding functions combine to produce high quality images at rates of up to 50Mb/s. The MPEGSI is a low power solution, well suited for applications with high picture quality and minimal hardware requirements.

Ordering Information

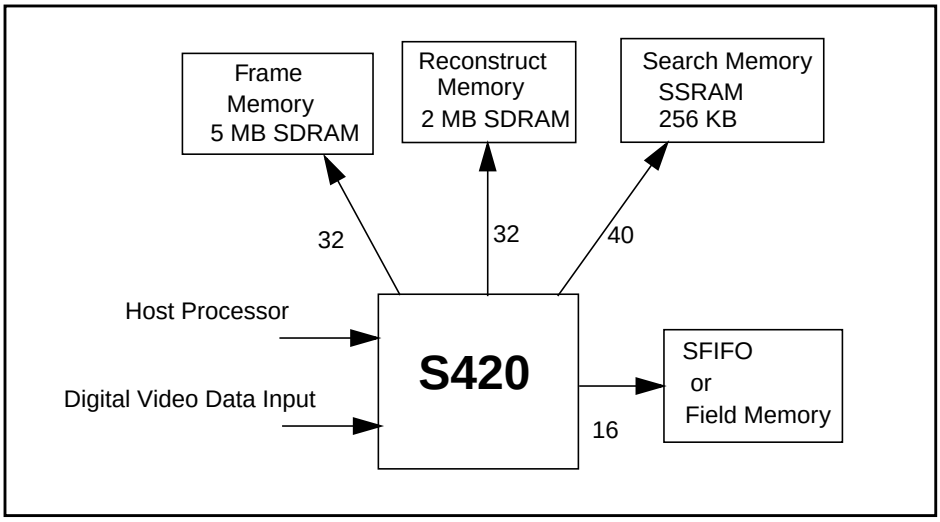
Ordering Information

Part Number	Highest Profile @Level	Clock Frequency	GOP Type	Chroma Output Format	Power(Nominal)
IBM39MPEGS422PBA17C	4:2:2@ML	60 MHz	I,IP,IPB,IPBB,IB,IBB	4:2:2, 4:2:0	4.4W
IBM39MPEGS420PBA18C	MP@ML	57 or 60 MHz	I,IP,IPB,IPBB,IB,IBB	4:2:0	4.1W
IBM39MPEGSIPBA18C	4:2:2@ML	57 or 60 MHz	I	4:2:2, 4:2:0	1.7W

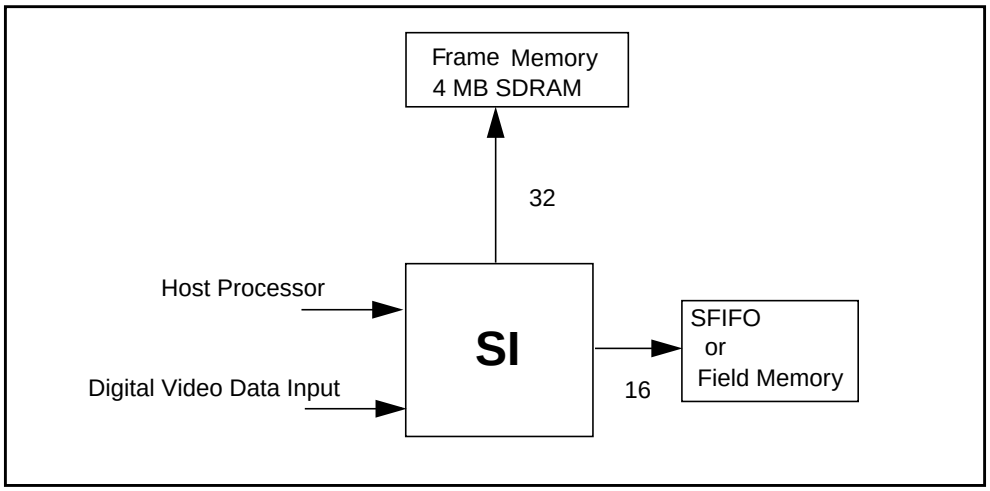
Block Diagrams



Note: Also requires 60 MHz and 27 MHz clocks.



Note: Also requires 57 MHz and 27 MHz clocks.



Note: Also requires 57 MHz and 27 MHz clock.

S422 Encoder Operations and Features

This section, contains operations and features specific to the S422 product. Please refer to Section 8.4, “Basic Register Definitions”, of the MPEG-2 S-Series Encoder User Application Guide, for a detailed description of each host register referenced.

MPEG-2 Support

The MPEG-2 standard defines several syntactic subsets at which compliant encoders and decoders may operate. These subsets were defined to help make the implementation of encoders and decoders more practical. Each subset is defined in terms of a **profile** and a **level**. The profile designation represents the syntactic subset of the MPEG-2 standard supported by a given encoder or decoder implementation, and the level designation provides constraints for various bitstream parameters.

The encoder conforms to the 4:2:2 Profile at Main Level (4:2:2P@ML) specifications provided in the MPEG-2 standard. In addition, the following syntactic subsets of 4:2:2P@HML are supported by the encoder:

- MP@ML (Main Profile at Main Level)
- MP@HL (Main Profile at High Level)
- SP@ML (Simple Profile at Main Level)
- ISO/IEC 11172 (MPEG-1)

The user can choose the syntactic subset based upon the user-specified parameters in effect while encoding a given sequence. For example, Host Register X’23’ enables the user to select the output profile. Also, the user can produce an MPEG-1 compliant bitstream by setting the user-specified parameters listed in Section 7.1.1, “Overview”, of the MPEG-2 S-Series Encoder User Application Guide.

VBV Buffer Size

At chip power on and initialization, the VBV buffer size is set to a default value based on how the following initialization parameters are set by the application:

- MPEG Standard via Host Register X'00', bit 0
- Profile Configuration via Host Register X'23', bits 6 and 5
- Bitrate via Host Register X'01' and Host Register X'02', bits 13 to 12
- DC Precision via Host Register X'28', bits 1 to 0
- SIF Picture Resolution via Host Registers X'07', bits 6 and 1, X'0A', bits 11 to 0, X'15', bits 11 to 0, X'19', bit 0, and command code X'000C' to Host Register X'3E'

For the various combinations of the above parameters, the encoded bitstream VBV size, profile and level fields are set according to the following table.

VBV Size/Profile/Level

VBV Size/Profile/ Table Level	MPEG-1	MPEG-2 / ≤SIF	MPEG-2 / >SIF / ≤15Mbps	MPEG-2 / >SIF / >15Mbps
SP / <11-b DC	INVALID	475,136	1,835,008	9,437,184
SP / 11-b DC	INVALID	9,437,184	9,437,184	9,437,184
MP / <11-b DC	327,680	475,136	1,835,008	9,437,184
MP / 11-b DC	INVALID	9,437,184	9,437,184	9,437,184
422P / <11-b DC	INVALID	9,437,184	9,437,184	9,437,184
422P / 11-b DC	INVALID	9,437,184	9,437,184	9,437,184

Note: Combinations listed as INVALID will cause the encoder to either automatically adjust conflicting parameters to be consistent or hang after initialization.

The VBV buffer size may alternatively be specified by the user via command code X'0005' to Host Register X'3D'

Picture Format

The encoder supports combinations of progressive and interlaced video formats as specified in the Table entitled: “Input/Output Formats,” on page 8.

Input Pixel Interface

The pixel data interface will accept raster scanned digital video data up to

- For NTSC, 720x512 pixels/frame at 30 frames per second
- For PAL, 720x608 pixels/frame at 25 frames per second

Data is accepted at the pixel interface at a nominal rate of 13.5 MHz for a 16 bit YCbCr format, and 27 MHz for 8 bit CCIR 656 format. The encoder will accept pixel data down to 64x64 pixels/frame. The data can be in either 4:2:0 or 4:2:2 format.

Maximum Picture Resolution

The encoder can support various picture widths, for example 720, 704, 608, 544, 352 etc. The encoder retrieves the first n number of pixels from each active input picture line, where n is specified by the user in Host Register X’14’. The encoder will ignore the number of video lines specified by the user in Host Register X’1B’ and subsequently processes the number of video lines specified by the user in Host Register X’15’.

Maximum Video Resolution

		4:2:0 Luminance	**4:2:0 Chrominance**	**4:2:2 Luminance**	**4:2:2 Chrominance**
NTSC	60 fps (1)	720x256	360x128	720x256	360x256
NTSC	30 Fps (2)	720x512	360x256	720x512	360x512
PAL	50 fps (1)	720x304	360x152	720x304	360x304
PAL	25 Fps (2)	720x608	360x304	720x608	360x608
Note: (1) fps = fields per second (2) Fps = frames per second					

4:2:2 to 4:2:0 Chroma Conversion Operation

Input video data can be in either the 4:2:2 or 4:2:0 format. The encoded output format can also be 4:2:2 or 4:2:0. Valid combinations of these formats in and out of the encoder are shown in Table entitled: “Input/Output Formats.” When the video source format is 4:2:2 and the encoded output format is 4:2:0, a conversion from 4:2:2 to 4:2:0 will need to be done. The encoder can internally perform the 4:2:2 to 4:2:0 conversion.

The encoder supports four chroma conversion modes. Host Register X’04’ bits 4-3 are used to select the chroma conversion mode. The choices are: *frame convert, field convert, drop field* and *output convert*. An on-chip 2 tap filter is used in each conversion mode. The contents of Host Register X’04’ bits 4-3 remain effective until changed by the user. This register may be changed on any input picture boundary, during input picture gaps. The encoder allows this parameter to be dynamically changed while encoding is in progress. However, if a change to this parameter is processed between fields of a given input frame, the result is unpredictable. There is no on-chip

provision to prevent this register from being changed between a pair of odd/even fields that make up a frame. In all conversion modes except *drop field*, the filter coefficients are 1/2.

Two adjacent vertical frame pixels are used to produce one chroma pixel in *frame convert* mode.

Two adjacent vertical pixels of the same field are used to produce one chroma pixel in *field convert* mode.

The chroma data in the even field is dropped, and the chroma data in the odd field is used for the entire picture in *drop field* mode.

Field convert mode is used for field encoding and *frame convert* is used for frame encoding in *output convert* mode.

If the user requires a more accurate filter (i.e. a long tap filter), then it is recommended that an external conversion mechanism be used.

Input/Output Formats

Out	In			
	4:2:2 Interlaced	**4:2:0 Interlaced**	**4:2:2 Progressive**	**4:2:0 Progressive**
4:2:2 Field	Real time	Not Supported	Real time	Not Supported
4:2:0 Field	Real time (1)	Real time	Real time (1)	Real time
4:2:2 Frame	Real time	Not Supported	Real time	Not Supported
4:2:0 Frame	Real time (1)	Real time	Real time (1)	Real time
Note: (1) Real time with 2-tap 4:2:2 to 4:2:0 filter				

Active Picture Area

For NTSC, the 525 lines of video are broken into two active picture areas and two vertical blanking intervals. Lines 1-20 are a blanking interval, lines 21 through 262-1/2 are an active picture area, lines 262-1/2 through 282-1/2 are a blanking interval, and lines 282-1/2 through 525 are an active picture area. Line 14 is used for time code information, and line 21 contains closed caption information.

A common implementation uses lines 22-261 (240 lines) from the first active picture area and lines 285-524 (240 lines) from the second active picture area to comprise the 480 lines of a given picture. By starting 12 lines earlier and ending four lines later than normal in each field, a 512-line picture can be created (e.g. lines 10-265 in the digital odd field and lines 273-528 in the digital even field).

For PAL, the 625 lines of video are broken into two active picture areas and two vertical blanking intervals. Lines 624-625 and 1-22 are a blanking interval, lines 23 through 310 are an active picture area, lines 311-312-1/2 and 312-1/2-335 are a blanking interval, and lines 336 through 623 are an active picture area (i.e Lines 23 and 623 are counted as 'full' active lines).

Lines 23-310 (288 lines) from the first active picture area and lines 336-623 (288 lines) from the second active picture area compose the 576 lines of a given picture. By starting 14 lines earlier and extending two lines later than normal in each field, a 608-line picture can be created (e.g. lines 9-312 in the digital odd field and lines 322-625 in the digital even field).

This feature provides the user the flexibility to select the location of the first active picture line by writing to Host Register X'1B'.

Encoder Memory Requirement

The applicable size, type and speed of each external memory is defined in the following table..

Memory Requirement

Memory	Minimum Required Size	Type	Speed
Frame memory	6MB	SDRAM	100MHz
Reconstructed memory	2MB	SDRAM	100MHz
Search memory	256KB	SSRAM	8ns
Compressed data output memory	application dependent	FIFO or Field Memory	10ns

S420 Encoder Operations/Features

This section, contains operations and features specific to the S420 product. Please refer to Section 8.4, “Basic Register Definitions”, of the MPEG-2 S-Series Encoder User Application Guide, for a detailed description of each host register referenced.

MPEG-2 Support

The MPEG-2 standard defines several syntactic subsets at which compliant encoders and decoders may operate. These subsets were defined to make the implementation of encoders and decoders more practical. Each subset is defined in terms of a **profile** and a **level**. The profile designation represents the syntactic subset of the MPEG-2 standard supported by a given encoder or decoder implementation, and the level designation provides constraints for various bitstream parameters.

The encoder conforms to the Main Profile at Main Level (MP@ML) plus extension specifications provided in the MPEG-2 standard. The extension includes up to 50Mb/s and 11 bit DC precision. In addition, the following syntactic subsets of the MPEG-2 standard are supported by the encoder:

- MP @ HL (Main Profile @ High Level)
- SP@ML (Simple Profile at Main Level)
- ISO/IEC 11172 (MPEG-1)

In addition, the encoder can operate beyond the MP@ML specifications by supporting encoded bitrates of up to 50 Mbps and a DC precision of up to 11 bits. When operating beyond the MP@ML specifications (i.e.up to 15 Mbps and 8 to 10 bits DC precision), provisions are made to allow the user to define encoder operations up to Main Profile at High Level (MP@HL).

The user can choose the syntactic subset based upon the user-specified parameters in effect while encoding a given sequence. For example, Host Register X’23’, bits 6 and 5, enable the user to select the output profile. Also, the user can produce an MPEG-1 compliant bitstream by setting the user-specified parameters listed in Section 7.3.1, “Overview”, of the MPEG-2 S-Series Video Encoder User Application Guide.

When the selected bitrate is higher than 15 Mb/s or the selected DC precison is 11 bit, Main Profile and High Level are placed in the output header. Otherwise, Main Profile and Main Level are used.

VBV Buffer Size

At chip power on and initialization, the VBV buffer size is set to a default value based on how the following initialization parameters are set by the application:

- MPEG Standard via Host Register X'00', bit 0
- Profile Configuration via Host Register X'23', bits 6 and 5
- Bitrate via Host Register X'01' and Host Register X'02', bits 13 to 12
- DC Precision via Host Register X'28', bits 1 to 0
- SIF Picture Resolution via Host Registers X'07', bits 6 and 1, X'0A', bits 11 to 0, X'15', bits 11 to 0, X'19', bit 0, and command code X'000C' to Host Register X'3E'

For the various combinations of the above parameters, the encoded bitstream VBV size, profile and level fields are set according to the following table:

S420 VBV Size/Profile/Level

Host Register Parameter Settings	MPEG-1	MPEG-2 / ≤SIF	MPEG-2 / >SIF / ≤15 Mbps	MPEG-2 / >SIF / >15 Mbps
SP / <11-b DC	INVALID	475,136	1,835,008	9,437,184
SP / 11-b DC	INVALID	9,437,184	9,437,184	9,437,184
MP / <11-b DC	327,680	475,136	1,835,008	9,437,184
MP / 11-b DC	INVALID	9,437,184	9,437,184	9,437,184
422P / <11-b DC	INVALID	INVALID	INVALID	INVALID
422P / 11-b DC	INVALID	INVALID	INVALID	INVALID

Note: Combinations listed as INVALID will cause the encoder to either automatically adjust conflicting parameters to be consistent or hang after initialization.

The VBV buffer size may alternatively be specified by the user via command code X'0005' to Host Register X'3D'.

Picture Format

The encoder supports combinations of progressive and interlaced video formats as specified in the Table entitled: “Input/Output Formats,” on page 12.

Input Pixel Interface

The pixel data interface will accept raster scanned digital video data up to:

- For NTSC, 720x480 pixels/frame at 30 frames per second
- For PAL, 720x576 pixels/frame at 25 frames per second

Data is accepted at the pixel interface at a nominal rate of 13.5 MHz for a 16 bit YCbCr format, and 27 MHz for 8 bit CCIR 656 format. The encoder will accept pixel data down to 64x64 pixels/frame. The data can be in either 4:2:0 or 4:2:2 format.

Maximum Picture Resolution

The encoder can support various picture widths, for example 720, 704, 608, 544, 352 etc. The encoder retrieves the first n number of pixels from each active input picture line, where n is specified by the user in Host Register X’14’. The encoder will ignore the number of video lines specified by the user in Host Register X’1B’ and subsequently processes the number of video lines specified by the user in Host Register X’15’.

4:2:2 to 4:2:0 Chroma Conversion Operation

Input video data can be in either the 4:2:2 or 4:2:0 format. The encoded output format must be 4:2:0. Valid combinations of these formats in and out of the encoder are shown in the Table entitled: “Input/Output Formats,” on page 12. When the video source format is 4:2:2, a conversion from 4:2:2 to 4:2:0 will need to be done. The encoder can internally perform the 4:2:2 to 4:2:0 conversion.

The encoder supports four chroma conversion modes. Host Register X’04’ bits 4-3 are used to select the chroma conversion mode. The choices are: *frame convert, field convert, drop field* and *output convert*. An on-chip 2 tap filter is used in each conversion mode. The contents of Host Register X’04’ bits 4-3 remain effective until changed by the user. This register may be changed on any input picture boundary, during input picture gaps. The encoder allows this parameter to be dynamically changed while encoding is in progress. If a change to this parameter is

processed between fields of a given input frame, the result is unpredictable. There is no internal provision to prevent this register from being changed between a pair of odd/even fields that make up a frame. In all conversion modes, except *drop field*, the filter coefficients are 1/2.

Two adjacent vertical frame pixels are used to produce one chroma pixel in *frame convert* mode.

Two adjacent vertical pixels of the same field are used to produce one chroma pixel in *field convert* mode.

The chroma data in the even field is dropped, and the chroma data in the odd field is used for the entire picture in *drop field* mode.

Field convert mode is used for field encoding and *frame convert* is used for frame encoding in the *output convert* mode.

If the user requires a more accurate filter (i.e. a long tap filter), then it is recommended that an external conversion mechanism be used.

Input/Output Formats

Out	In			
	4:2:2 Interlaced	**4:2:0 Interlaced**	**4:2:2 Progressive**	**4:2:0 Progressive**
4:2:0 Field	Real time (1)	Real time	Real time (1)	Real time
4:2:0 Frame	Real time (1)	Real time	Real time (1)	Real time
Note: (1) Real time with 2-tap 4:2:2 to 4:2:0 filter				

Active Picture Area

For NTSC, the 525 lines of video are broken into two active picture areas and two vertical blanking intervals. Lines 1-20 are a blanking interval, lines 21 through 262-1/2 are an active picture area, lines 262-1/2 through 282-1/2 are a blanking interval, and lines 282-1/2 through 525 are an active picture area. Line 14 is used for time code information, and line 21 contains closed caption information.

A common implementation uses lines 22-261 (240 lines) from the first active picture area and lines 285-524 (240 lines) from the second active picture area to comprise the 480 lines of a given picture.

For PAL the 625 lines of video are broken into two active picture areas and two vertical blanking intervals. Lines 624-625 and 1-22 are a blanking interval, lines 23-310 are an active picture area, lines 311-312-1/2 and 312-1/2-335 are a blanking interval, and lines 336-623 are an active picture area. (i.e Lines 23 and 623 are counted as 'full' active lines.)

Lines 23-310 (288 lines) from the first active picture area and lines 336-623 (288 lines) from the second active picture area comprise the 576 lines of a given picture.

A feature is available in the S-Series Encoders that provides the user the flexibility to select the location of the first active picture line by writing to Host Register X'1B'. (See Section 7.28, "Pixel Interface Functional Enhancements", of the MPEG-2 S-Series Encoder User Application Guide for further details.)

Encoder Memory Requirement

The required type and speed of each external memory are defined in the following table.

MPEGS420 Memory Requirement

Memory	Minimum Required Size	Type	Speed
Frame memory	5MB	SDRAM	100MHz
Reconstructed memory	2MB	SDRAM	100MHz
Search memory *	256KB	SSRAM	8ns
Compressed data output memory	application dependent	FIFO or Field Memory	10ns

***Note:** For an alternative memory solution, see section entitled: “Solution for System Cost Reduction”.

Solutions to Help Lower System Expense

The MPEGS420 may be configured by the user to operate at 15 Mb/s (or less) compressed data rate and +/-64H, +/- 56V search range. This configuration allows the use of 192KB industry standard ASRAM with 12 ns access time in place of the previously indicated SSRAM as the Search Memory. This configuration will also lower encoder operating power by 0.3 W.

SI Encoder Operations/Features

This section, describes the encoder operations and features of the MPEGSI product. Please refer to Section 8.4 Basic Register Definitions of the MPEG-2 S-Series Encoder User Application Guide, for a detailed description of each host register referenced.

MPEG-2 Support

The MPEG-2 standard defines several syntactic subsets at which compliant encoders and decoders may operate. These subsets were defined to make the implementation of encoders and decoders more practical. Each subset is defined in terms of a **profile** and a **level**. The profile designation represents the syntactic subset of the MPEG-2 standard supported by a given encoder or decoder implementation, and the level designation provides constraints for various bitstream parameters.

The encoder conforms to the 4:2:2 Profile at Main Level (4:2:2P@ML) specifications provided in the MPEG-2 standard. In addition, the following syntactic subsets of 4:2:2P@ML are supported by the encoder:

- MP@ML (Main Profile at Main Level)
- MP@HL (Main Profile at High Level)
- SP@ML (Simple Profile at Main Level)
- ISO/IEC 11172 (MPEG-1)

The user can choose the syntactic subset based upon the user-specified parameters in effect while encoding a given sequence. For example, Host Register X’23’, bits 6 and 5, enables the user to select the output profile. Also, the user can produce an MPEG-1 compliant bitstream by setting the user-specified parameters listed in Section 7.1.1, “Overview” of the MPEG-2 S-Series Encoder User Application Guide.

VBV Buffer Size

At chip power on and initialization, the VBV buffer size is set to a default value based on how the following initialization parameters are set by the application:

- MPEG Standard via Host Register X'00', bit 0
- Profile Configuration via Host Register X'23', bits 6 and 5
- Bitrate via Host Register X'01' and Host Register X'02', bits 13 to 12
- DC Precision via Host Register X'28', bits 1 to 0
- SIF Picture Resolution via Host Registers X'07', bits 6 and 1, X'0A', bits 11 to 0, X'15', bits 11 to 0, X'19', bit 0, and command code X'000C' to Host Register X'3E'

For the various combinations of the above parameters, the encoded bitstream VBV size, profile and level fields are set according to the following table.

VBV_SI Size/Profile/Level

Host Register Parameter Settings	MPEG-1	MPEG-2 / ≤SIF	MPEG-2 / >SIF / ≤15 Mbps	MPEG-2 / >SIF / >15 Mbps
SP / <11-b DC	INVALID	475,136	1,835,008	9,437,184
SP / 11-b DC	INVALID	9,437,184	9,437,184	9,437,184
MP / <11-b DC	327,680	475,136	1,835,008	9,437,184
MP / 11-b DC	INVALID	9,437,184	9,437,184	9,437,184
422P / <11-b DC	INVALID	9,437,184	9,437,184	9,437,184
422P / 11-b DC	INVALID	9,437,184	9,437,184	9,437,184

Note: Combinations listed as INVALID will cause the encoder to either automatically adjust conflicting parameters to be consistent or hang after initialization.

The VBV buffer size may alternatively be specified by the user via command code X'0005' to Host Register X'3D'.

Picture Format

The encoder supports combinations of progressive and interlaced video formats as specified in the Table entitled: “Input/Output Formats,” on page 17.

Input Pixel Interface

The pixel data interface will accept raster scanned digital video data up to the following:

- For NTSC, 720x512 pixels/frame at 30 frames per second
- For PAL, 720x608 pixels/frame at 25 frames per second

Data is accepted at the pixel interface at a nominal rate of 13.5MHz for a 16 bit YCbCr format, and 27 MHz for 8 bit CCIR 656 format. The encoder will accept pixel data down to 64x64 pixels/frame. The data can be in either 4:2:0 or 4:2:2 format.

Maximum Picture Resolution

The encoder can support various picture widths, for example 720, 704, 608, 544, 352 etc. The encoder retrieves the first n number of pixels from each active input picture line, where n is specified by the user in Host Register X’14’. The encoder will ignore the number of video lines specified by the user in Host Register X’1B’ and subsequently processes the number of video lines specified by the user in Host Register X’15’.

Maximum Video Resolution

		4:2:0 Luminance	4:2:0 Chrominance	4:2:2 Luminance	4:2:2 Chrominance
NTSC	60fps (1)	720x256	360x128	720x256	360x256
NTSC	30Fps (2)	720x512	360x256	720x512	360x512
PAL	50fps (1)	720x304	360x152	720x304	360x304
PAL	25Fps (2)	720x608	360x304	720x608	360x608
Note: (1) fps = fields per second (2) Fps = frames per second					

4:2:2 to 4:2:0 Chroma Conversion Operation

Input video data can be in either the 4:2:2 or 4:2:0 format. The encoded output format can also be 4:2:2 or 4:2:0. Valid combinations of these formats in and out of the encoder are shown in Table . When the video source format is 4:2:2 and the encoded output format is 4:2:0, a conversion from 4:2:2 to 4:2:0 will need to be done. The encoder can internally perform the 4:2:2 to 4:2:0 conversion.

The encoder supports four chroma conversion modes. Host Register X'04' bits 4-3 are used to select the chroma conversion mode. The choices are: *frame convert, field convert, drop field* and *output convert*. An on-chip 2 tap filter is used in each conversion mode. The contents of Host Register X'04' bits 4-3 remain effective until changed by the user. This register may be changed on any input picture boundary, during input picture gaps. The encoder allows this parameter to be dynamically changed while encoding is in progress. If a change to this parameter is processed between fields of a given input frame, the result is unpredictable. There is no internal provision to prevent this register from being changed between a pair of odd/even fields that make up a frame. In all conversion modes, except *drop field*, the filter coefficients are 1/2.

Two adjacent vertical frame pixels are used to produce one chroma pixel in *frame convert* mode.

Two adjacent vertical pixels of the same field are used to produce one chroma pixel in *field convert* mode.

The chroma data in the even field is dropped, and the chroma data in the odd field is used for the entire picture in *drop field* mode.

Field convert mode is used for field encoding and *frame convert* mode is used for frame encoding in the *output convert* mode.

If the user requires a more accurate filter (i.e. a long tap filter), then it is recommended that an external conversion method be used.

Input/Output Formats

Out	In			
	4:2:2 Interlaced	**4:2:0 Interlaced**	**4:2:2 Progressive**	**4:2:0 Progressive**
4:2:2 Field	Real time	*	Real time	*
4:2:0 Field	Real time (1)	Real time	Real time (1)	Real time
4:2:2 Frame	Real time	*	Real time	*
4:2:0 Frame	Real time (1)	Real time	Real time (1)	Real time
Note: (*) Not supported. (1) Real time with 2-tap 4:2:2 to 4:2:0 filter				

Active Picture Area

For NTSC, the 525 lines of video are broken into two active picture areas and two vertical blanking intervals. Lines 1-20 are a blanking interval, lines 21 through 262-1/2 are an active picture area, lines 262-1/2 through 282-1/2 are a blanking interval, and lines 282-1/2 through 525 are an active picture area. Line 14 is used for time code information, and line 21 contains closed caption information.

A common implementation uses lines 22-261 (240 lines) from the first active picture area and lines 285-524 (240 lines) from the second active picture area to comprise the 480 lines of a given picture. By starting 12 lines earlier and ending four lines later than normal in each field, a 512-line picture can be created (e.g. lines 10-265 in the digital odd field and lines 273-528 in the digital even field).

For PAL, the 625 lines of video are broken into two active picture areas and two vertical blanking intervals. Lines 624-625 and 1-22 are a blanking interval, lines 23 through 310 are an active picture area, lines 311-312-1/2 and 312-1/2-335 are a blanking interval, and lines 336 through 623 are an active picture area (i.e Lines 23 and 623 are counted as ’full’ active lines).

Lines 23-310 (288 lines) from the first active picture area and lines 336-623 (288 lines) from the second active picture area compose the 576 lines of a given picture.By starting 14 lines earlier and extending two lines later than normal in each field, a 608-line picture can be created (e.g. lines 9-312 in the digital odd field and lines 322-625 in the digital even field).

A feature is available in the S-Series encoders that provides the user with the flexibility to select the location of the first active picture line by writing to Host Register X’1B’.

Encoder Latency

The delay between the first pixel data input at the video input interface and the availability of the first corresponding compressed video data at the output interface is the encoder latency. The latency is due to the time required to read all pixel data for a frame into the encoder, store it in frame memory, and process the data through the encoder. The encoder latency is not fixed to a specific value and can change based on the encoding parameters (For

example, Host Register X'07', bit 0 - Frame vs. Field Encoding; Host Register X'17', bit 2 - Internal 3:2 Pulldown Inversion Mode) and/or the microcode level being used. The typical time ranges for latency are as follows:

Encoder Latency Summary

Encoding Mode	Typical latency range in non-3:2 pulldown inversion mode	Typical latency range in 3:2 pulldown inversion mode
I-Frames Only	1 Frame	1.5 to 2 Frames

Latency Notes

- The above latency time ranges include internal encoder latency only. Compressed data output buffering and other system latency is not included.
- The time units associated with 1 frame are dependent on the specified frame rate (e.g. for a 1 frame latency with a frame rate of 30 per second, the latency is 33 milliseconds).
- The above latency time ranges do not guarantee a fixed timing relationship between the pixel interface VR signal and HENC_INTRPT. System designers must not rely on such a relationship when using the encoder in a system since it can change based on encoding parameters and/or microcode level.

Encoder Memory Requirement

Two external memories are needed to support the encoder. These include frame memory and compressed data output memory components. The required size, type and speed of each external memory is defined in the following table:

MPEGSI Memory Requirement

Memory	Minimum Required Size	Type	Speed
Frame memory	4MB	SDRAM	100MHz
Compressed data output memory	application dependent	FIFO or Field Memory	10ns

Environmental and Electrical Specifications

This section describes the encoder environmental and electrical specifications.

Environmental Specifications

Operating Ratings/Range of S422

Parameter	Value	Units
Vdd (supply voltage)(maximum)	3.60	Volts
Vdd (Nominal supply voltage)	3.30 ± 5%	Volts
System Clock	60	MHz
Ambient temperature range (operating conditions)	0 - 40	˚C
Operating temperature range (Chip Tj)	0 - 110	˚C
Storage temperature range	-55 to 125	˚C
Air Flow (minimum)	0.5	meters/sec
Power Dissipation (nominal)	4.4	Watts
Power Dissipation (maximum)	4.9	Watts

Notes
• The allowable ambient temperature range specified is based on the module mounted to a 50 x 50 mm 2-signal/2-power plane card with the specified airflow on both sides of card, vertical orientation.

Operating Ratings/Range of S420

Parameter	Value	Units
Vdd (supply voltage)(maximum)	3.60	Volts
Vdd (Nominal supply voltage)	3.30 ± 5%	Volts
System Clock	57	MHz
Ambient temperature range (operating conditions)	0 - 40	˚C
Operating temperature range (Chip Tj)	0 - 110	˚C
Storage temperature range	-55 to 125	˚C
Air Flow (minimum)	0.5	meters/sec
Power Dissipation (nominal)	4.1	Watts
Power Dissipation (maximum)	4.6	Watts

Notes:
- The allowable ambient temperature range specified is based on the module mounted to a 50 x 50 mm 2-signal/2-power plane card with the specified airflow on both sides of card, vertical orientation.
- S420 can also be operated at 60 MHz with an increase in power of less than 5%. This does not change the application conditions shown in this table.

Operating Ratings/Range of S420 (Reduced Search)

Parameter	Value	Units
Vdd (supply voltage)(maximum)	3.60	Volts
Vdd (Nominal supply voltage)	3.30 ± 5%	Volts
System Clock	57	MHz
Ambient temperature range (operating conditions)	0 - 50	˚C
Operating temperature range (Chip Tj)	0 - 110	˚C
Storage temperature range	-55 to 125	˚C
Air Flow (minimum)	0.5	meters/sec
Power Dissipation (nominal)	3.8	Watts
Power Dissipation (maximum)	4.3	Watts

Notes:
- The allowable ambient temperature range specified is based on the module mounted to a 50 x 50 mm 2-signal/2-power plane card with the specified airflow on both sides of card, vertical orientation.
- The operating range is show for reduced search range (+/- 64 H, +/- 56 V) operation.
- For the reduced search configuration, S420 should only be operated at 57 MHz in order to meet the application conditions shown in this table.

Operating Ratings/Range of SI

Parameter	Value	Units
Vdd (supply voltage)(maximum)	3.60	Volts
Vdd (Nominal supply voltage)	3.30 ± 5%	Volts
System Clock	57	MHz
Ambient temperature range (operating conditions)	0 - 70	˚C
Operating temperature range (Chip Tj)	0 - 110	˚C
Storage temperature range	-55 to 125	˚C
Power Dissipation (nominal)	1.7	Watts
Power Dissipation (maximum)	1.9	Watts

Notes:
- The allowable ambient temperature range specified is based on the module mounted to a 50 X 50 mm 2-signal/2-power plane card with natural convection (no air flow).
- SI can also be operated at 60 MHz with an increase in power of less than 5%. This does not change the application conditions shown in this table.

Signal I/O Electrical Specifications

The drivers and receivers have the following voltage level specifications and are compatible with both 3.3 Volt and 5.0 Volt technologies.

DC Electrical Characteristics (in Volts)

Usage	MAUL	MPUL	LPUL	MPDL	LPDL	MADL
Receiver	5.50V	5.50V	2.00V	0.80V	0.00V	-0.60V
Driver	5.50V	3.60V	2.40V	0.40V	0.00V	-0.60V

Definitions
MAUL Maximum Allowable Up Level - Applies to overshoot only - for drivers, implies output is disabled.
MPUL Maximum Positive Up Level - For drivers, implies output is active.
LPUL Least Positive Up Level
MPDL Maximum Positive Down Level
LPDL Least Positive Down Level
MADL Minimum Allowable Down Level - Applies to Undershoot only.

LVTTL Driver Minimum DC Currents at Rated Voltage

Driver Type	V_{high} (V)	I_{high} (mA)	V_{low} (V)	I_{low} (mA)
LVTTL 65 Ω Driver Outputs	2.40	8.0	0.4	5.0
LVTTL 50 Ω Driver Outputs	2.40	11.0	0.4	7.0
LVTTL 35 Ω Driver Outputs	2.40	16.0	0.4	10.0

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Receiver Maximum Input Leakage DC Current Input Specifications

Function	I_{il} (µA)	I_{ih} (µA)
Without pull-up element or pull-down element	0 at V_{in} = LPDL	0 at V_{in} =MPUL
With pull-down element	0 at V_{in} = LPDL	400 at V_{in} =MPUL
With pull-up element	-250 at V_{in} = LPDL	0 at V_{in} =MPUL

Physical Information of S422/S420/SI

Parameter	Value	Unit
Module dimension	35 x 35	mm
Module height	2	mm
Package type	PBGA	
Ball pitch	1.27	mm
Ball diameter	0.9	mm

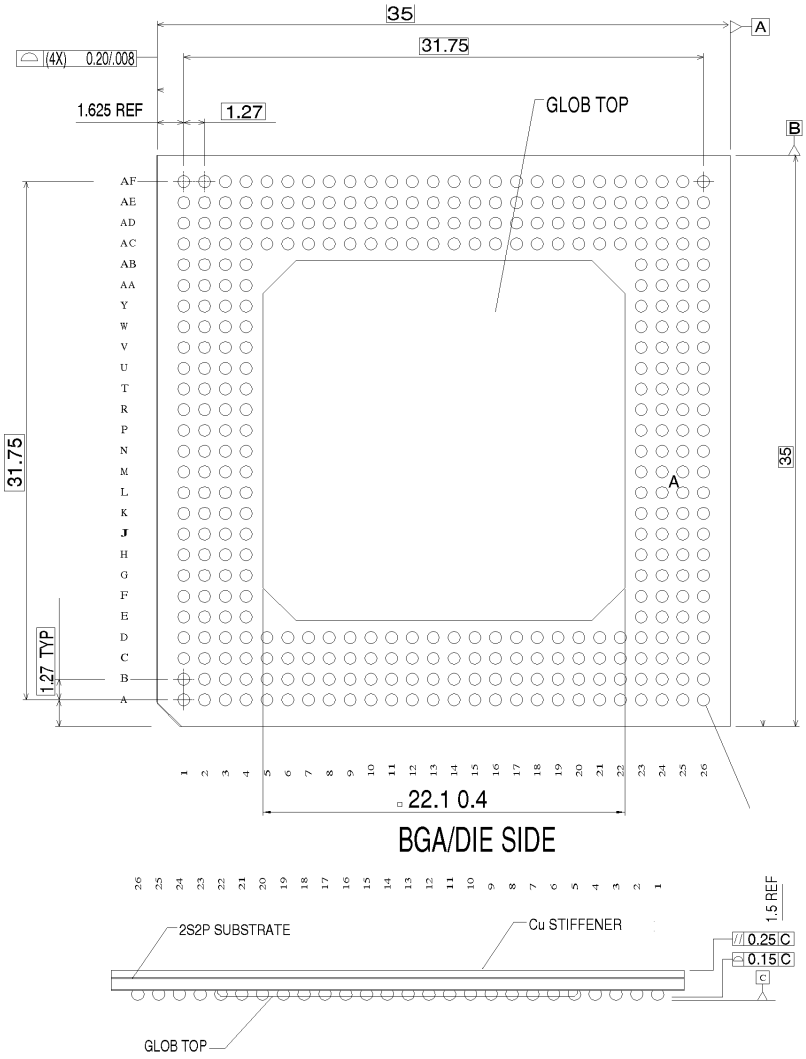
Note: For card design with the S-Series encoders, no heat generating components (such as memory devices, logic chips, etc.) should be put on the backside of the card within the 35 X 35mm. outline of the encoder module. Discrete components such as chip capacitors and resistors are permitted.

Package Usage Summary

Package

Module	Package size (mm)	Total pins	Power pins	Ground pins	N/C	Signal pins
S422	35 x 35	352	16	32	37	267
S420	35 x 35	352	16	32	37	267
SI	35 x 35	352	16	32	169	135

Package specifications (ball side view)



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Revision Log

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April 24, 2001	Initial release (00)
May 31, 2001	Changes subsequent to legal review. Added IBM Confidential Classification. Release (01)
June 18, 2001	Removed IBM Confidential Classification. Release (02).
July 17, 2001	Removed Preliminary Information Disclaimer. Release (02)