

Am27S19/27S19A

Am27S19SA/27LS19

256-Bit (32x8) Bipolar PROM



DISTINCTIVE CHARACTERISTICS

- Ultra high speed
- Highly reliable, ultra-fast programming Platinum-Silicide fuses
- High-programming yield
- Low-current PNP inputs
- High-current open collector and three-state outputs
- Fast chip select

GENERAL DESCRIPTION

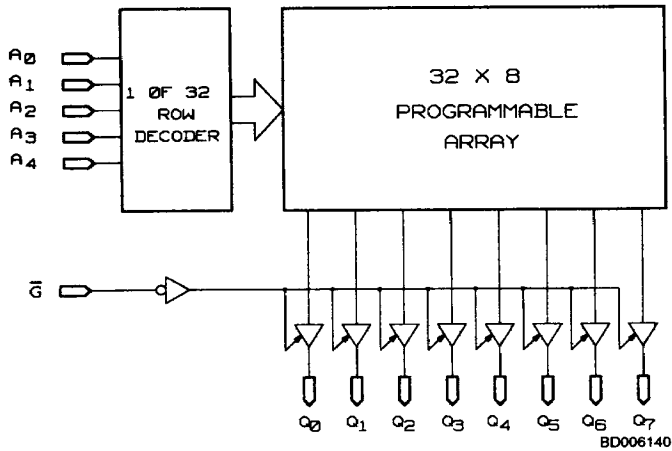
The Am27S19 (32 words by 8 bits) is a Schottky TTL Programmable Read-Only Memory (PROM).

This device is available in three-state (Am27S19) output versions. These outputs are compatible with low-power Schottky bus standards capable of satisfying the requirements of a variety of microprogrammable controls, mapping

functions, code conversions, or logic replacements. Easy word depth expansion is facilitated by an active LOW output enable (\bar{G}).

This device is also available in a low-power version Am27LS19.

BLOCK DIAGRAM



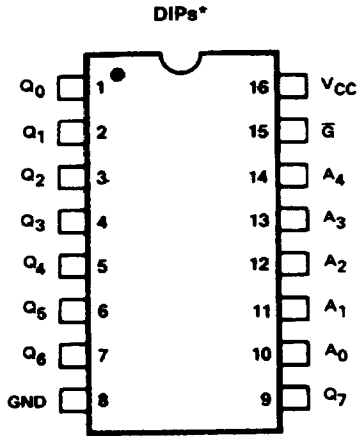
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PRODUCT SELECTOR GUIDE

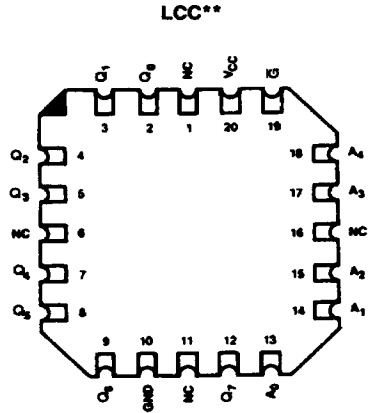
Three-State Part Number	Am27S19SA		Am27S19A		Am27S19		Am27LS19	
Address Access Time	15 ns	20 ns	25 ns	35 ns	40 ns	50 ns	55 ns	70 ns
Operating Range	C	M	C	M	C	M	C	M

Publication # 03209 Rev. E Issue Date: January 1989

CONNECTION DIAGRAMS
Top View



CD000521



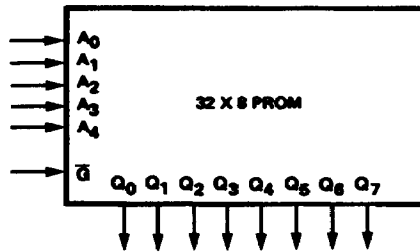
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Note: Pin 1 is marked for orientation.

*Also available in a 16-pin Flatpack. Pinout identical to DIPs.

**Also available in a 16-pin Plastic Leaded Chip Carrier. Pinout identical to LCC.

LOGIC SYMBOL



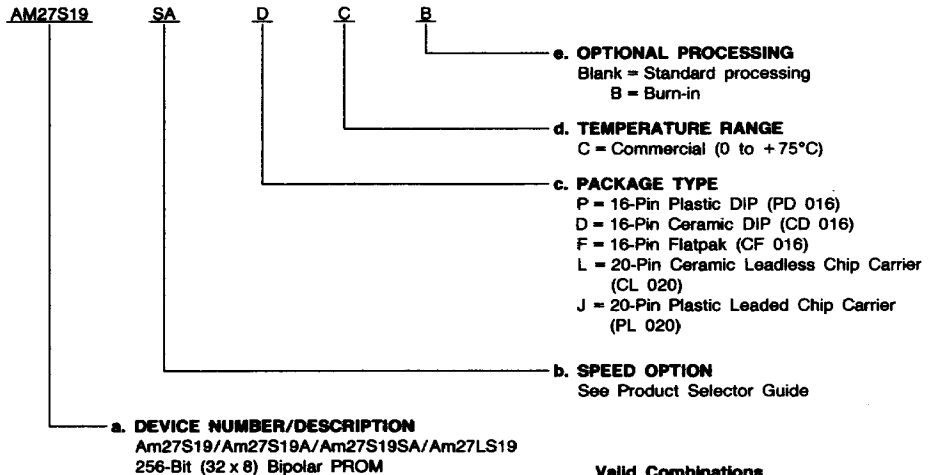
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ORDERING INFORMATION

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

- a. Device Number
- b. Speed Option (if applicable)
- c. Package Type
- d. Temperature Range
- e. Optional Processing



Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

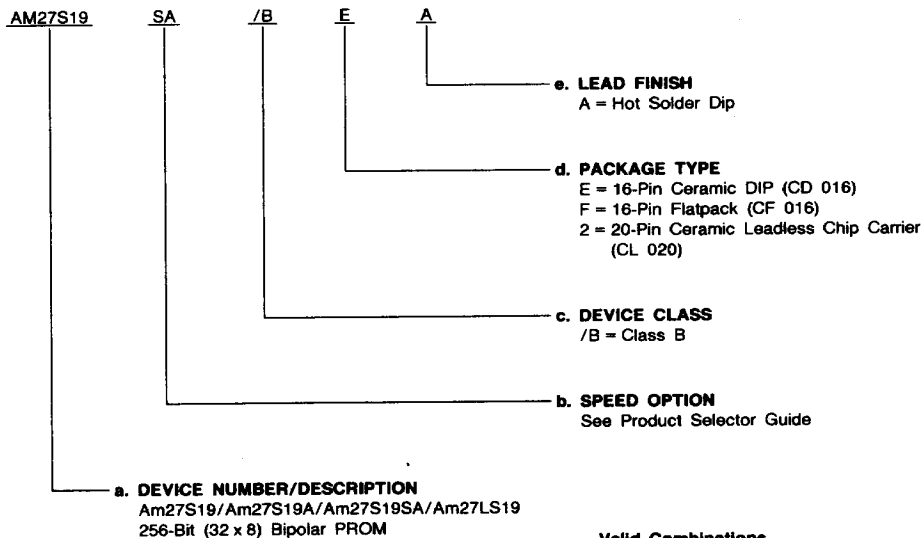
Valid Combinations	
AM27S19	PC, PCB,
AM27S19A	DC, DCB,
AM27S19SA	FC, FCB,
AM27LS19	LC, LCB,
	JC, JCB

MILITARY ORDERING INFORMATION

APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. The order number (Valid Combination) for APL products is formed by a combination of:

- a. **Device Number**
- b. **Speed Option** (if applicable)
- c. **Device Class**
- d. **Package Type**
- e. **Lead Finish**



Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check for newly released valid combinations.

Valid Combinations	
AM27S19	
AM27S19A	/BEA,
AM27S19SA	/BFA,
AM27LS19	/B2A

Group A Tests

Group A tests consist of Subgroups
1, 2, 3, 7, 8, 9, 10, 11.

MILITARY BURN-IN

Military burn-in is in accordance with the current revision of MIL-STD-883, Test Method 1015, Conditions A through E. Test conditions are selected at AMD's option.

PIN DESCRIPTION

A₀ - A₄ Address Inputs

The 5-bit field presented at the address inputs selects one of 32 memory locations to be read from.

Q₀ - Q₇ Data Output Port

The outputs whose state represents the data read from the selected memory locations

\bar{G} Output Enable

Provides direct control of the Q output three-state buffers. Outputs disabled forces all open-collector outputs to an

OFF state and all three-state outputs to a floating or high-impedance state.

Enable = \bar{G}

Disable = G

V_{CC} Device Power Supply Pin

The most positive of the logic power supply pins.

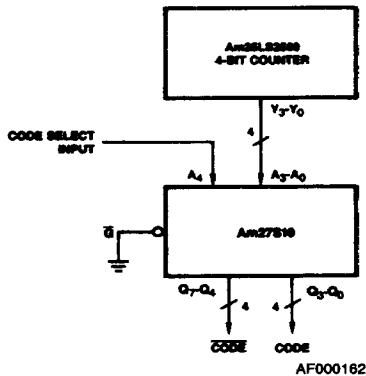
GND Device Power Supply Pin

The most negative of the logic power supply pins.

FUNCTIONAL DESCRIPTION

The Am27S19 PROM can be used as a code converter. Examples include conversion of hexadecimal, octal or BCD to seven segment display drive format. In many code conversion applications an extra PROM address input is available and may be used as a polarity control, blanking control or code

selector input. The use of a single Am27S19 to convert the outputs of a binary counter to either excess three or gray code format is illustrated below. In this case both codes are generated in true and complemented form simultaneously.



TRUTH TABLE

ADDRESS					COMPLEMENT				TRUE																		
A ₄	A ₃	A ₂	A ₁	A ₀	Q ₇	Q ₆	Q ₅	Q ₄	Q ₃	Q ₂	Q ₁	Q ₀															
0	0	0	0	0	1	1	0	0	0	0	1	1	EXCESS THREE CODE														
0	0	0	0	1	1	0	1	1	0	1	0	0		EXCESS THREE CODE													
0	0	0	1	0	1	0	1	0	0	1	0	1			EXCESS THREE CODE												
0	0	0	1	1	1	0	0	1	0	1	1	0				EXCESS THREE CODE											
0	0	1	0	0	1	0	0	0	0	1	1	1					EXCESS THREE CODE										
0	0	1	0	1	0	1	1	1	1	0	0	0						EXCESS THREE CODE									
0	0	1	1	0	0	1	1	1	0	1	0	0							EXCESS THREE CODE								
0	0	1	1	1	0	1	0	1	1	0	1	0								EXCESS THREE CODE							
0	1	0	0	0	0	1	0	0	1	0	1	1									EXCESS THREE CODE						
0	1	0	0	1	0	0	1	1	1	1	0	0										EXCESS THREE CODE					
0	1	0	1	0	X	X	X	X	X	X	X	X											EXCESS THREE CODE				
0	1	0	1	1	X	X	X	X	X	X	X	X												EXCESS THREE CODE			
0	1	1	0	0	X	X	X	X	X	X	X	X													EXCESS THREE CODE		
0	1	1	0	1	X	X	X	X	X	X	X	X														EXCESS THREE CODE	
0	1	1	1	0	X	X	X	X	X	X	X	X															EXCESS THREE CODE
0	1	1	1	1	X	X	X	X	X	X	X	X															
1	0	0	0	0	1	1	1	1	0	0	0	0	GRAY CODE														
1	0	0	0	1	1	1	1	0	0	0	0	1		GRAY CODE													
1	0	0	1	0	1	1	0	0	0	0	1	1			GRAY CODE												
1	0	0	1	1	1	0	1	0	1	0	1	0				GRAY CODE											
1	0	1	0	0	1	0	0	1	0	1	1	0					GRAY CODE										
1	0	1	0	1	1	0	0	0	0	1	1	1						GRAY CODE									
1	0	1	1	0	1	0	1	0	0	1	0	1							GRAY CODE								
1	0	1	1	1	1	0	1	0	0	1	0	1								GRAY CODE							
1	1	0	0	0	0	1	1	1	1	1	0	0									GRAY CODE						
1	1	0	0	1	0	0	1	0	1	1	0	1										GRAY CODE					
1	1	0	1	0	0	0	0	0	1	1	1	1											GRAY CODE				
1	1	0	1	1	0	0	0	0	1	1	1	0												GRAY CODE			
1	1	1	0	0	0	1	0	1	0	1	0	1													GRAY CODE		
1	1	1	0	1	0	1	0	0	0	1	0	1														GRAY CODE	
1	1	1	1	0	0	1	1	0	1	0	0	1															GRAY CODE
1	1	1	1	1	0	1	1	1	1	0	0	0															

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ABSOLUTE MAXIMUM RATINGS

Storage Temperature	-65 to +150°C
Ambient Temperature with Power Applied	-55 to +125°C
Supply Voltage	-0.5 V to +7.0 V
DC Voltage Applied to Outputs (Except During Programming)	-0.5 to +V _{CC} Max.
DC Voltage Applied to Outputs During Programming	21 V
Output Current into Outputs During Programming (Max. Duration of 1 sec.)	250 mA
DC Input Voltage	-0.5 V to 5.5 V
DC Input Current	-30 to +5 mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices	
Ambient Temperature (T _A)	0 to +75°C
Supply Voltage (V _{CC})	+4.75 V to +5.25 V
Military (M) Devices*	
Case Temperature (T _C)	-55 to +125°C
Supply Voltage (V _{CC})	+4.5 V to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

*Military products 100% tested at T_C = +25°C, +125°C, and -55°C.

DC CHARACTERISTICS over operating ranges unless otherwise specified (for APL Products, Group A, Subgroups 1, 2, 3 are tested unless otherwise noted)

Parameter Symbol	Parameter Description	Test Conditions	Min.	Typ.	Max.	Unit
V _{OH} (Note 1)	Output HIGH Voltage	V _{CC} = Min., I _{OH} = -2.0 mA V _{IN} = V _{IH} or V _{IL}	2.4			V
V _{OL}	Output LOW Voltage	V _{CC} = Min., I _{OL} = 16 mA V _{IN} = V _{IH} or V _{IL}			0.45	V
V _{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs (Note 2)	2.0			V
V _{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs (Note 2)			0.8	V
I _{IL}	Input LOW Current	V _{CC} = Max., V _{IN} = 0.45 V			-0.250	mA
I _{IH}	Input HIGH Current	V _{CC} = Max., V _{IN} = 2.7 V			25	μA
I _{SC} (Note 1)	Output Short-Circuit Current	V _{CC} = Max., V _{OUT} = 0.0 V (Note 3)	-20		-90	mA
I _{CC}	Power Supply Current	All inputs = GND, V _{CC} = Max.			115	mA
					80	
V _I	Input Clamp Voltage	V _{CC} = Min., I _{IN} = -18 mA			-1.2	V
I _{CEX}	Output Leakage Current	V _{CC} = Max. V _G = 2.4 V (Note 1)			40	μA
		V _O = 0.4 V			-40	
C _{IN}	Input Capacitance	V _{CC} = 5.00 V, T _A = 25°C		4		pF
C _{OUT}	Output Capacitance	V _{IN} /V _{OUT} = 2.0 V. @ f = 1 MHz (Note 4)		8		

Notes: 1. This applies to three-state devices only.

2. V_{IL} and V_{IH} are input conditions of output tests and are not themselves directly tested. V_{IL} and V_{IH} are absolute voltages with respect to device ground and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.

3. Not more than one output should be shorted at a time. Duration of the short circuit should not be more than one second.

4. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.

SWITCHING CHARACTERISTICS over operating ranges unless otherwise specified (for APL Products, Group A, Subgroups 9, 10, 11 are tested unless otherwise noted*)

No.	Parameter Symbol	Parameter Description	Version	COM'L		MIL		Unit
				Min.	Max.	Min.	Max.	
1	TAVQV	Address Valid to Output Valid Access Time	SA		15		20	ns
			A		25		35	
			STD		40		50	
			LS		55		70	
2	TGVQZ	Delay from Output Enable Valid to Output Hi-Z	SA		13		20	ns
			A		20		25	
			STD		25		30	
			LS		40		50	
3	TGVQV	Delay from Output Enable Valid to Output Valid	SA		13		20	ns
			A		20		25	
			STD		25		30	
			LS		40		50	

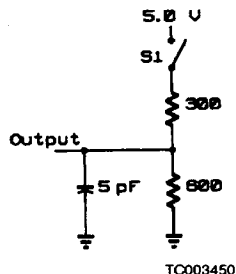
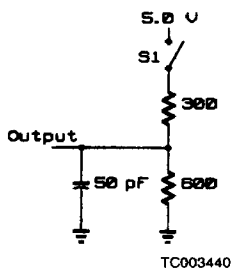
See also Switching Test Circuits.

Notes: 1. Tests are performed with input transition time of 5 ns or less, timing reference levels of 1.5 V, and input pulse levels of 0 to 3.0 V using test load in A under Switching Test Circuits.

2. TGVQZ is measured at steady state HIGH output voltage -0.5 V and steady state LOW output voltage +0.5 V output levels using the test load in B under Switching Test Circuits.

*Subgroups 7 and 8 apply to functional tests.

SWITCHING TEST CIRCUITS








A. Output Load for all tests except TGVQZ

B. Output Load for TGVQZ

- Notes: 1. All device test loads should be located within 2" of device output pin.
 2. S₁ is open for Output Data HIGH to Hi-Z and Hi-Z to Output Data HIGH tests. S₁ is closed for all other AC tests.
 3. Load capacitance includes all stray and fixture capacitance.

SWITCHING WAVEFORMS

KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	MUST BE STEADY	WILL BE STEADY
	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L
	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H
	DON'T CARE: ANY CHANGE PERMITTED	CHANGING: STATE UNKNOWN
	DOES NOT APPLY	CENTER LINE IS HIGH IMPEDANCE "OFF" STATE

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