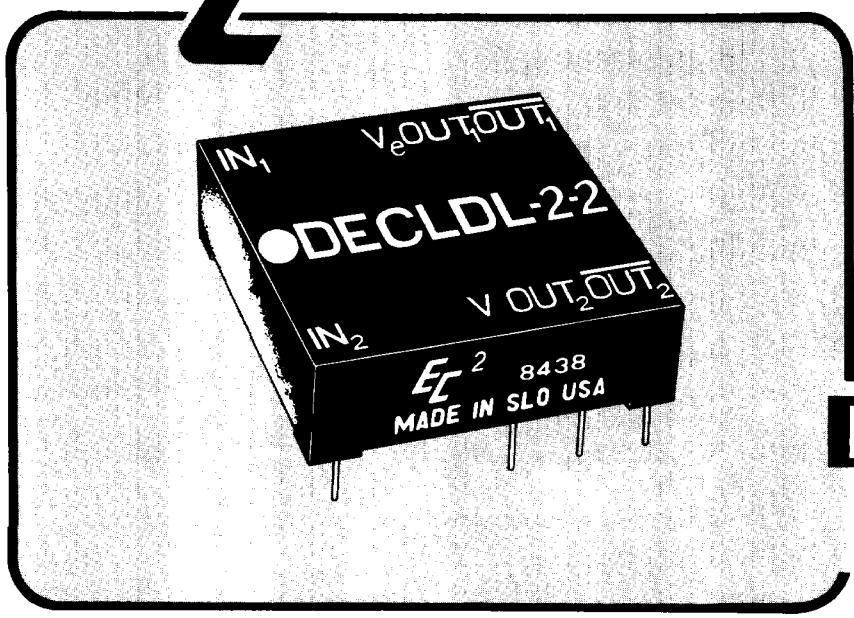


low profile

ECL 100K COMPATIBLE DUAL LOGIC DELAY LINE

- ECL 100K input and output levels
- Dual units with separate inputs and outputs
- Delays stable and precise
- 12-pin DIP package (.325 high)
- Available in delays from 2 to 20ns
- Output isolated and with 70 ECL DC fan-out capacity
- Rise time 1ns nominal

design notes

The "DIP Series" Dual Logic Delay Lines developed by Engineered Components Company have been designed to provide precise delays with required driving and pick-off circuitry contained in a 12-pin DIP package compatible with ECL "100K Series" or "10,000 Series" circuitry. The design includes compensation for propagation delays and incorporates internal termination at the output; no additional external components are needed to obtain the desired delay.

These modules accept either logic "1" or logic "0" inputs and reproduce the logic at the output without inversion. The delay lines are intended primarily for use with positive going pulses and are calibrated to the tolerances shown in the table on rising edge delay; where best accuracy is desired in applications using falling edge timing, it is recommended that a special unit be calibrated for the specific application. All modules can be driven from a standard ECL gate with an external pull-down resistor of 50 or 100 ohms to −2V or 470 ohms to −4.5V. Output is standard ECL 100K open emitter. Each module has the capability of driving up to 70 ECL DC loads.

The DECLDL is offered in 32 delays from 2 to 20ns. Each module includes two (2) separate delay lines, each isolated and fully buffered. Delay tolerances are maintained as shown in the accompanying Part Number Table, when tested under the "Test Conditions" shown.

Delay time is measured at the −1.3V level on the leading edge; rise time is 2ns maximum, when measured from 20% to 80% pulse amplitude. Temperature coefficient of delay is less than 150 ppm/°C over the operating temperature range of 0 to +85°C.

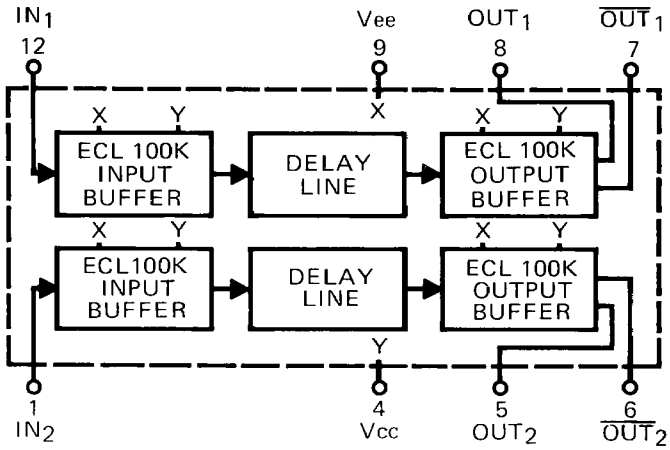
These modules are of hybrid construction utilizing the proven technologies of active integrated circuitry and of passive networks utilizing capacitive, inductive and resistive elements. The ICs utilized in these modules are burned-in to Level B of MIL-STD-883 to ensure a high MTBF. The MTBF on these modules, when calculated per MIL-HDBK-217 for a 50°C ground fixed environment, is in excess of 1 million hours.

The "DIP Series" Logic Delay Lines are packaged in a 12-pin DIP housing, molded of flame-proof Diallyl Phthalate per MIL-M-14, Type SDG-F, and are fully encapsulated in epoxy resin. Leads meet the solderability requirements of MIL-STD-202, Method 208. Corner standoffs on the housing provide positive standoff from the printed circuit board to permit solder-fillet formation and flush cleaning of solder-flux residues for improved reliability.

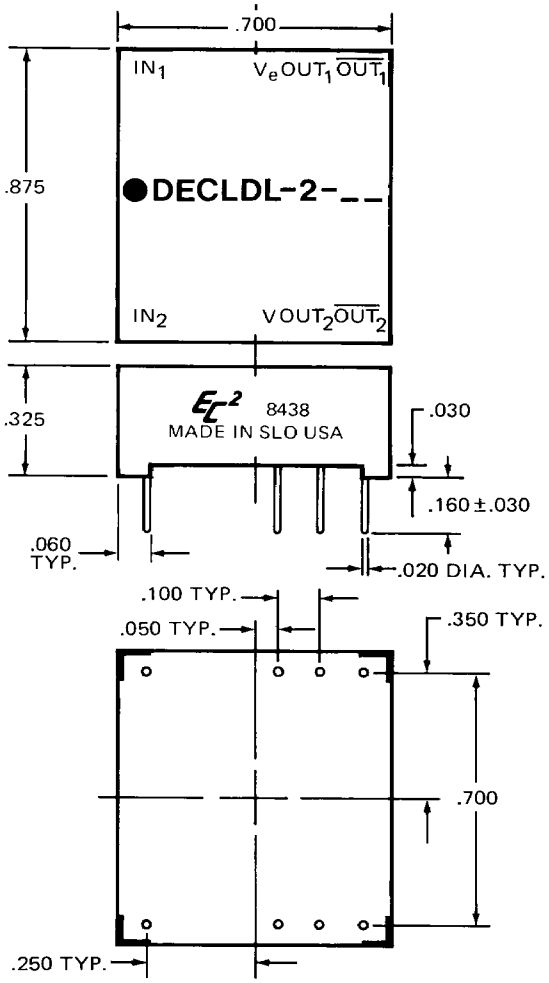
Marking consists of manufacturer's name, logo (EC2), part number, terminal identification and date code of manufacture. All marking is applied by silk screen process using white epoxy paint in accordance with MIL-STD-130 to meet the permanency of identification required by MIL-STD-202, Method 215.

EC2 engineered components company
3580 Sacramento Drive, P. O. Box 8121, San Luis Obispo, CA 93403-8121
Phone: (805) 544-3800

BLOCK DIAGRAM IS SHOWN BELOW



MECHANICAL DETAIL IS SHOWN BELOW



TEST CONDITONS

1. All measurements are made at 25°C.
2. Vee supply voltage is maintained at −4.5V DC.
3. All units are tested using a positive input pulse provided by a standard open emitter ECL 100K gate. The input and output utilizes a 50 ohm pull-down resistor to −2V; the output is also loaded with one ECL 100K gate.

ϕ4. Input pulse width used is 5 to 10ns longer than full delay of module under test; spacing between pulses (falling edge to rising edge) is three times the pulse width used.

OPERATING SPECIFICATIONS

* Supply voltage:	−4.5V ±5% to Vee
Supply current:	155ma typical
Logic 1 Input at 25°C:	
Voltage	−1.165 min.
Current	350ua max.
Logic 0 Input at 25°C:	
Voltage	−1.475V max.
Current	.5ua min.
Logic 1 Output at 25°C:	−1.025 min.
Logic 0 Output at 25°C:	−1.620 max.
Operating temperature range:	0 to +85°C
Storage temperature:	−55 to +125°C

* Delays increase or decrease less than .5% for a respective increase or decrease of 5% in supply voltage.

PART NUMBER TABLE

ϕ DELAYS AND TOLERANCES (in ns)			
PART NO.	OUTPUT	PART NO.	OUTPUT
DECLDL-2-2	2±.2	DECLDL-2-10	10±1
DECLDL-2-2.5	2.5±.2	DECLDL-2-10.5	10.5±1
DECLDL-2-3	3±.3	DECLDL-2-11	11±1
DECLDL-2-3.5	3.5±.3	DECLDL-2-11.5	11.5±1
DECLDL-2-4	4±.4	DECLDL-2-12	12±1
DECLDL-2-4.5	4.5±.4	DECLDL-2-12.5	12.5±1
DECLDL-2-5	5±.5	DECLDL-2-13	13±1
DECLDL-2-5.5	5.5±.5	DECLDL-2-13.5	13.5±1
DECLDL-2-6	6±.6	DECLDL-2-14	14±1
DECLDL-2-6.5	6.5±.6	DECLDL-2-14.5	14.5±1
DECLDL-2-7	7±.7	DECLDL-2-15	15±1
DECLDL-2-7.5	7.5±.7	DECLDL-2-16	16±1
DECLDL-2-8	8±.8	DECLDL-2-17	17±1
DECLDL-2-8.5	8.5±.8	DECLDL-2-18	18±1
DECLDL-2-9	9±.9	DECLDL-2-19	19±1
DECLDL-2-9.5	9.5±.9	DECLDL-2-20	20±1

ϕ All modules can be operated with a minimum input pulse width of 100% of full delay and pulse period approaching square wave; since delay accuracies may be somewhat degraded, it is suggested that the module be evaluated under the intended specific operating conditions. Special modules can be readily manufactured to improve accuracies and/or provide customer specified random delay times for specific applications.

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