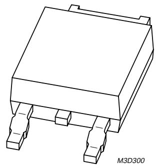


BUK9226-100B

TrenchMOS™ logic level FET

Rev. 01 — 10 December 2002 **Objective data**

1. Product profile

1.1 Description

N-channel enhancement mode field-effect power transistor in a plastic package using Philips High-Performance Automotive (HPA) TrenchMOS™ technology, featuring very low on-state resistance.

Product availability:

BUK9226-100B in SOT428 (D-PAK)

1.2 Features

- TrenchMOS^{TM} technology
- 175 °C rated
- Q101 compliant
- Logic level compatible

1.3 Applications

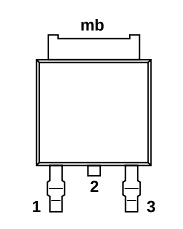
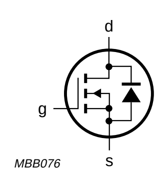
- Automotive systems
- Motors, lamps and solenoids
- 12 V, 24 V, and 42 V loads
- General purpose power switching

1.4 Quick reference data

- $E_{DS(AL)S} \leq 147$ mJ
- $I_D \leq 48$ A
- $R_{DSon} = 22$ mΩ (typ)
- $P_{tot} \leq 150$ W

2. Pinning information

Table 1: Pinning - SOT428 (D-PAK), simplified outline and symbol

Pin	Description	Simplified outline	Symbol
1	gate (g)	 **SOT428 (D-PAK)**	
2	drain (d) [1]		
3	source (s)		
mb	mounting base; connected to drain (d)		

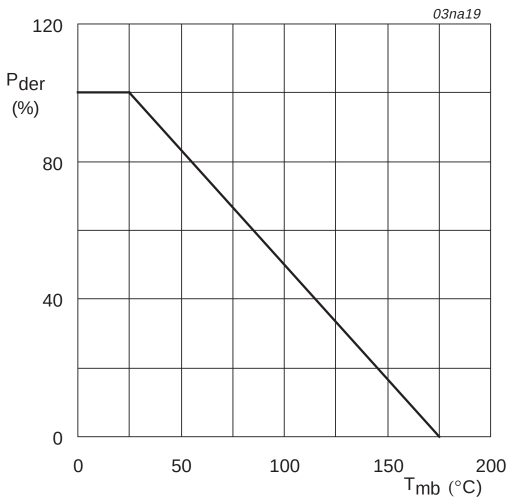
[1] It is not possible to make connection to pin 2 of the SOT428 package.

3. Limiting values

Table 2: Limiting values

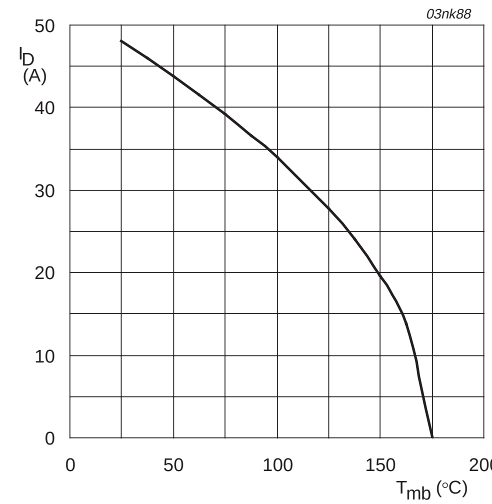
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage (DC)		-	100	V
V_{DGR}	drain-gate voltage (DC)	R_{GS} = 20 kΩ	-	100	V
V_{GS}	gate-source voltage (DC)		-	±15	V
I_D	drain current (DC)	T_{mb} = 25 °C; V_{GS} = 5 V; Figure 2 and 3	-	48	A
		T_{mb} = 100 °C; V_{GS} = 5 V; Figure 2	-	34	A
I_{DM}	peak drain current	T_{mb} = 25 °C; pulsed; $t_p \leq$ 10 µs; Figure 3	-	192	A
P_{tot}	total power dissipation	T_{mb} = 25 °C; Figure 1	-	150	W
T_{stg}	storage temperature		–55	+175	°C
T_j	junction temperature		–55	+175	°C
Source-drain diode					
I_{DR}	reverse drain current (DC)	T_{mb} = 25 °C	-	48	A
I_{DRM}	peak reverse drain current	T_{mb} = 25 °C; pulsed; $t_p \leq$ 10 µs	-	192	A
Avalanche ruggedness					
$E_{DS(AL)S}$	non-repetitive avalanche energy	unclamped inductive load; I_D = 75 A; $V_{DS} \leq$ 100 V; V_{GS} = 5 V; R_{GS} = 50 Ω; starting T_j = 25 °C	-	147	mJ



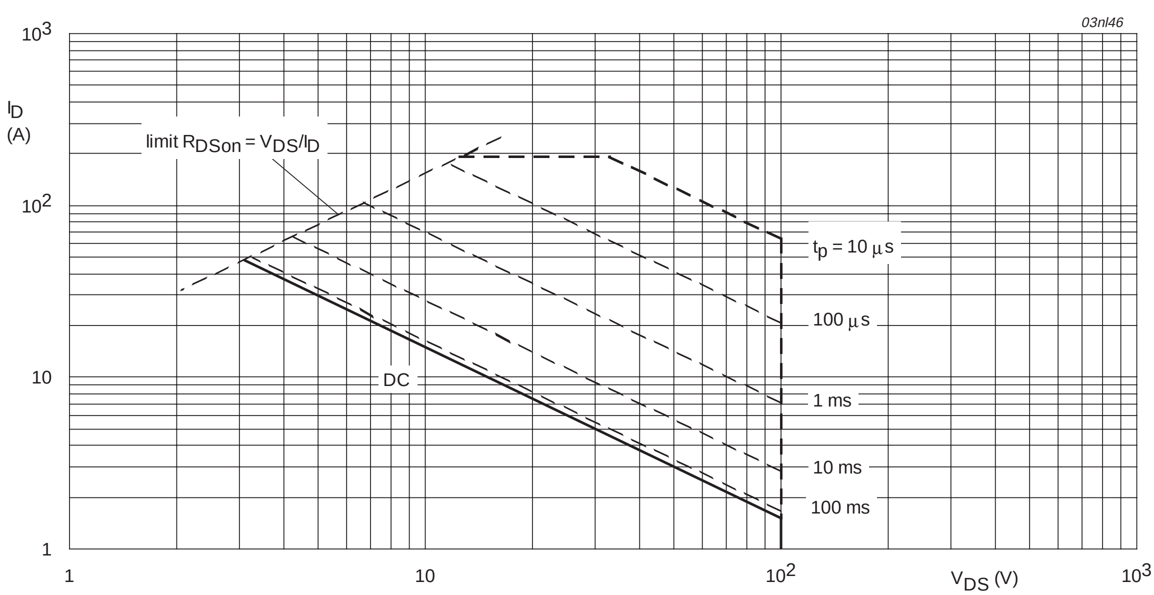
$$P_{der} = \frac{P_{tot}}{P_{tot(25^\circ C)}} \times 100\%$$

Fig 1. Normalized total power dissipation as a function of mounting base temperature.



$V_{GS} \geq 5$ V

Fig 2. Continuous drain current as a function of mounting base temperature.



$T_{mb} = 25$ °C; I_{DM} single pulse.

Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage.

4. Thermal characteristics

Table 3: Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient		-	71.4	-	K/W
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Figure 4	-	0.45	1.0	K/W

4.1 Transient thermal impedance

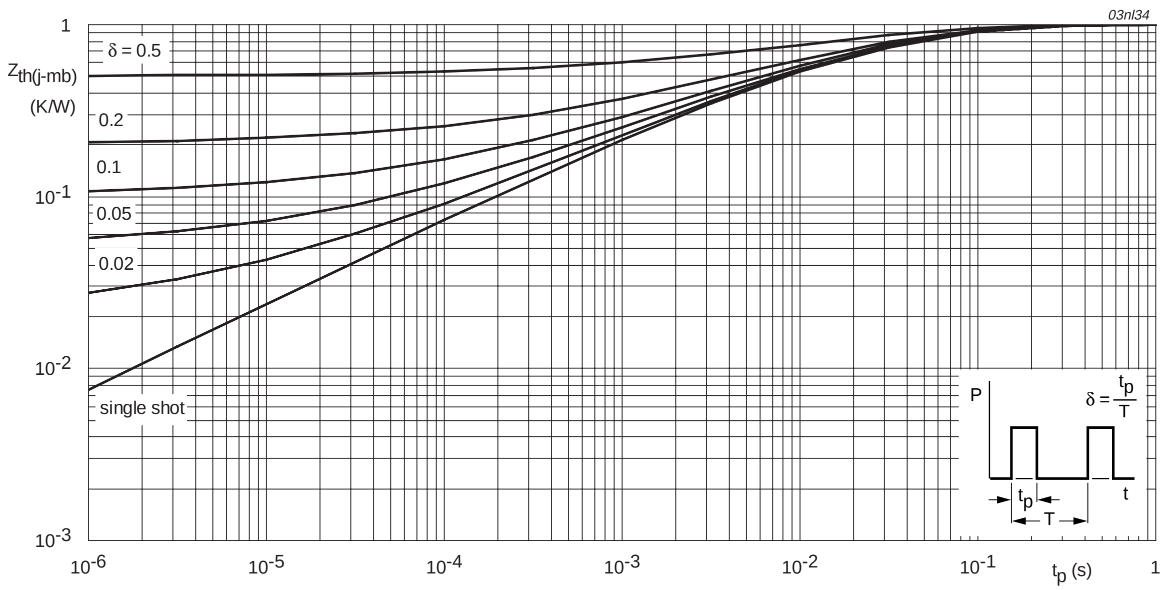


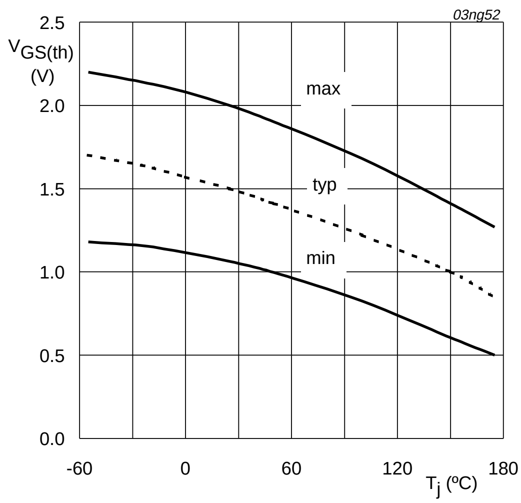
Fig 4. Transient thermal impedance from junction to mounting base as a function of pulse duration.

5. Characteristics

Table 4: Characteristics

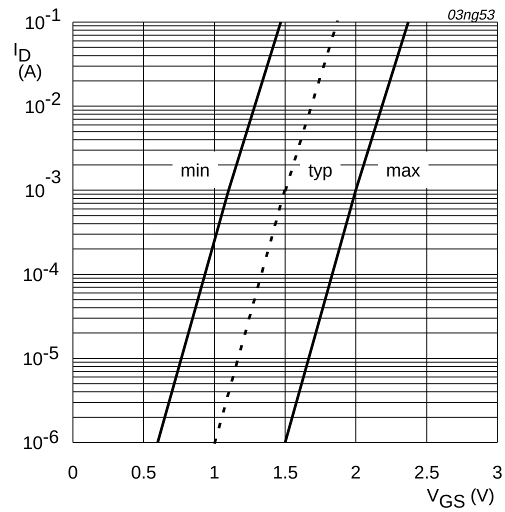
T_j = 25 °C unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 0.25 mA; V_{GS} = 0 V				
		T_j = 25 °C	100	-	-	V
		T_j = –55 °C	89	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	I_D = 1 mA; V_{DS} = V_{GS}; Figure 5				
		T_j = 25 °C	1.1	1.5	2	V
		T_j = 175 °C	0.5	-	-	V
		T_j = –55 °C	-	-	2.3	V
I_{DSS}	drain-source leakage current	V_{DS} = 100 V; V_{GS} = 0 V				
		T_j = 25 °C	-	0.02	1	µA
		T_j = 175 °C	-	-	500	µA
I_{GSS}	gate-source leakage current	V_{GS} = ±15 V; V_{DS} = 0 V	-	2	100	nA
R_{DSon}	drain-source on-state resistance	V_{GS} = 5 V; I_D = 25 A; Figure 7				
		T_j = 25 °C	-	22	26	mΩ
		T_j = 175 °C	-	-	65	mΩ
		V_{GS} = 4.5 V; I_D = 25 A	-	-	29	mΩ
		V_{GS} = 10 V; I_D = 25 A	-	20	24	mΩ
Dynamic characteristics						
$Q_{g(tot)}$	total gate charge	V_{GS} = 5 V; V_{DS} = 80 V; I_D = 25 A;	-	29	-	nC
Q_{gs}	gate-source charge		-	5	-	nC
Q_{gd}	gate-drain (Miller) charge		-	11	-	nC
C_{iss}	input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz;	-	2854	3805	pF
C_{oss}	output capacitance		-	232	278	pF
C_{rss}	reverse transfer capacitance		-	81	110	pF
$t_{d(on)}$	turn-on delay time	V_{DS} = 30 V; R_L = 1.2 Ω; V_{GS} = 5 V; R_G = 10 Ω	-	tbf	-	nS
t_r	rise time		-	tbf	-	nS
$t_{d(off)}$	turn-off delay time		-	tbf	-	nS
t_f	fall time		-	tbf	-	nS
L_d	internal drain inductance	measured from drain to centre of die	-	2.5	-	nH
L_s	internal source inductance	measured from source lead to source bond pad	-	7.5	-	nH
Source-drain diode						
V_{SD}	source-drain (diode forward) voltage	I_S = 10 A; V_{GS} = 0 V; Figure 7	-	0.85	1.2	V
t_{rr}	reverse recovery time	I_S = 20 A; dI_S/dt = –100 A/µs V_{GS} = –10 V; V_{DS} = 30 V	-	tbf	-	ns
Q_r	recovered charge		-	tbf	-	nC



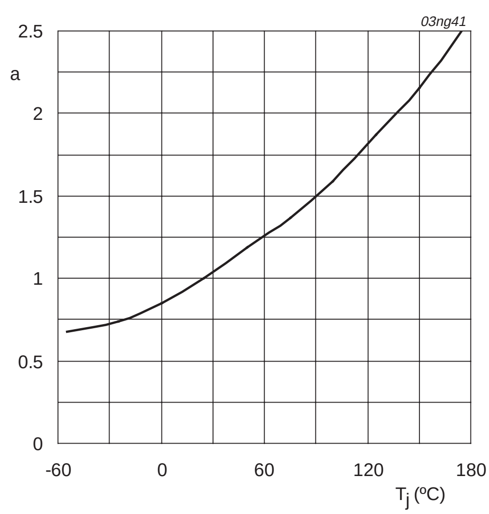
I_D = 1 mA; $V_{DS} = V_{GS}$

Fig 5. Gate-source threshold voltage as a function of junction temperature.



T_j = 25 °C; $V_{DS} = V_{GS}$

Fig 6. Sub-threshold drain current as a function of gate-source voltage.

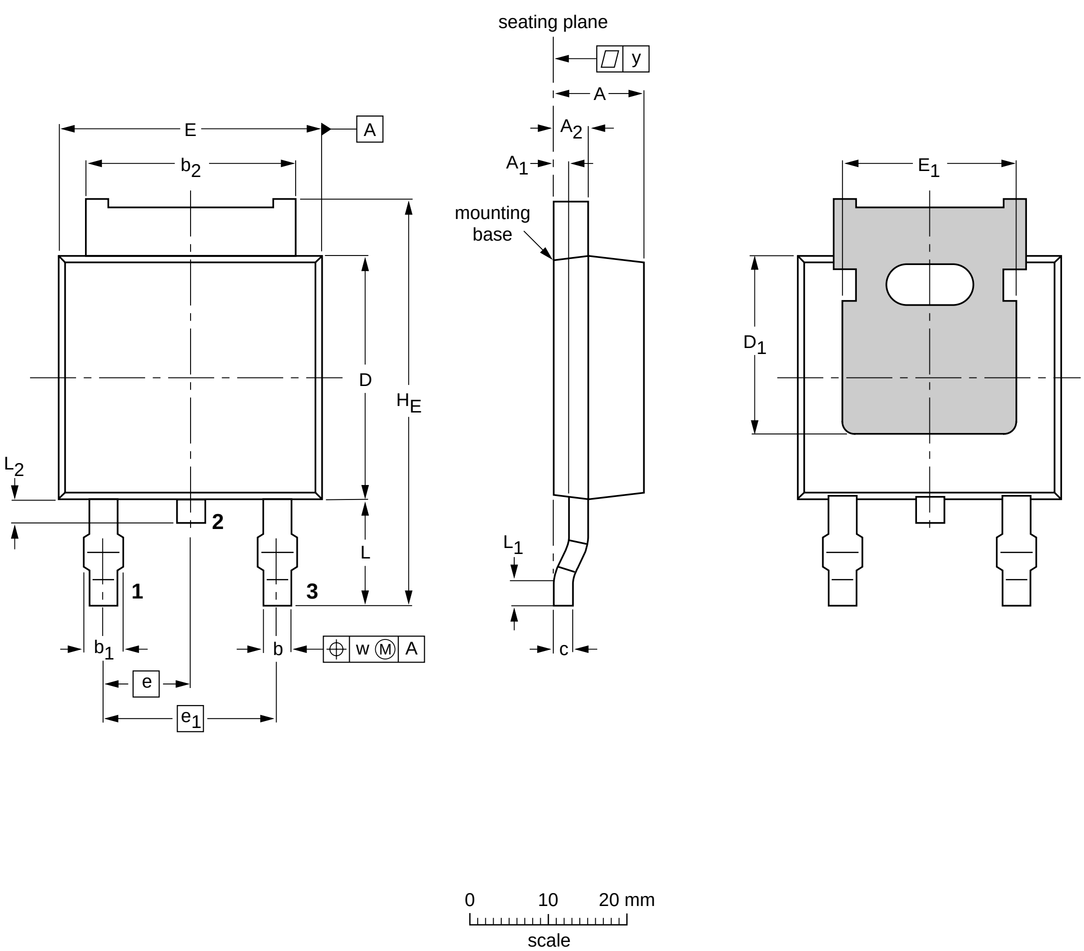


$$a = \frac{R_{DSon}}{R_{DSon(25^{\circ}C)}}$$

Fig 7. Normalized drain-source on-state resistance factor as a function of junction temperature.

6. Package outline

Plastic single-ended surface mounted package (Philips version of D-PAK); 3 leads (one lead cropped) **SOT428**



DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1(1)	A_2	b	b_1	b_2	c	D	D_1 min.	E	E_1	e	e_1	H_E	L	L_1 min.	L_2	w	y max.
mm	2.38 2.22	0.65 0.45	0.93 0.73	0.89 0.71	1.1 0.9	5.46 5.26	0.4 0.2	6.22 5.98	4.0	6.73 6.47	4.81 4.45	2.285	4.57	10.4 9.6	2.95 2.55	0.5	0.9 0.5	0.2	0.2

Note

1. Measured from heatsink back to lead.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT428		TO-252	SC-63			~~99-09-13~~ 01-12-11

Fig 8. SOT428 (D-PAK)

7. Revision history

Table 5: Revision history

Rev	Date	CPCN	Description
01	20021210	-	Objective data (9397 750 10803)

8. Data sheet status

Level	Data sheet status[1]	Product status[2][3]	Definition
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
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[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.

[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

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Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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