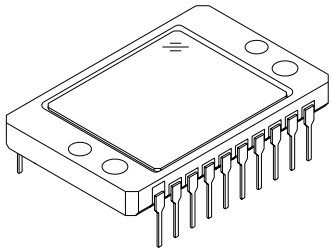
SONY

ICX285AL

Diagonal 11 mm (Type 2/3) Progressive Scan CCD Image Sensor with Square Pixel for B/W Cameras

20 pin DIP (Ceramic)



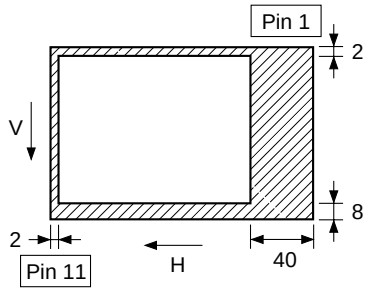
Description

The ICX285AL is a diagonal 11 mm (Type 2/3) interline CCD solid-state image sensor with a square pixel array. High sensitivity and low smear are achieved through the adoption of EXview HAD CCD technology. Progressive scan allows all pixel's signals to be output independently within approximately 1/15 second. Also, the adoption of high frame rate readout mode supports 60 frames per second. This chip features an electronic shutter with variable charge-storage time which makes it possible to realize full-frame still images without a mechanical shutter.

This chip is suitable for image input applications such as still cameras which require high resolution, etc.

Features

- Progressive scan allows individual readout of the image signals from all pixels.
- High horizontal and vertical resolution (both approximately 1024 TV-lines) still images without a mechanical shutter
- Supports high frame rate readout mode (effective 256 lines output, 60 frame/s)
- Square pixel
- Aspect ratio: 4:3
- Horizontal drive frequency: 28.64 MHz
- High sensitivity, low smear
- Low dark current, excellent anti-blooming characteristics
- Continuous variable-speed shutter
- Horizontal register: 5.0 V drive



Optical black position
(Top View)

Device Structure

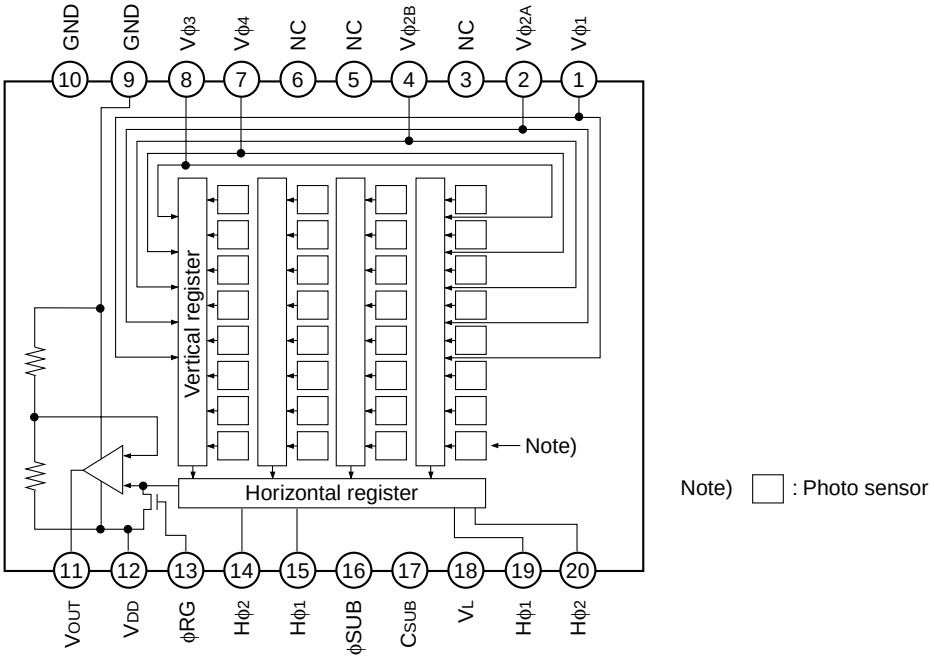
- Interline CCD image sensor
- Image size: Diagonal 11 mm (Type 2/3)
- Total number of pixels: 1434 (H) × 1050 (V) approx. 1.50M pixels
- Number of effective pixels: 1392 (H) × 1040 (V) approx. 1.45M pixels
- Number of active pixels: 1360 (H) × 1024 (V) approx. 1.40M pixels
- Chip size: 10.2 mm (H) × 8.3 mm (V)
- Unit cell size: 6.45 µm (H) × 6.45 µm (V)
- Optical black: Horizontal (H) direction: Front 2 pixels, rear 40 pixels
  Vertical (V) direction: Front 8 pixels, rear 2 pixels
- Number of dummy bits: Horizontal 20
  Vertical 3
- Substrate material: Silicon

***EXview* HAD CCD** ™

* EXview HAD CCD is a trademark of Sony Corporation.
EXview HAD CCD is a CCD that drastically improves light efficiency by including near infrared light region as a basic structure of HAD (Hole-Accumulation-Diode) sensor.

E00Y42A27

Block Diagram and Pin Configuration (Top View)



Pin Description

Pin No.	Symbol	Description	Pin No.	Symbol	Description
1	Vφ1	Vertical register transfer clock	11	V_{OUT}	Signal output
2	Vφ2A	Vertical register transfer clock	12	V_{DD}	Supply voltage
3	NC		13	φRG	Reset gate clock
4	Vφ2B	Vertical register transfer clock	14	Hφ2	Horizontal register transfer clock
5	NC		15	Hφ1	Horizontal register transfer clock
6	NC		16	φSUB	Substrate clock
7	Vφ4	Vertical register transfer clock	17	C_{SUB}	Substrate bias*1
8	Vφ3	Vertical register transfer clock	18	V_L	Protective transistor bias
9	GND	GND	19	Hφ1	Horizontal register transfer clock
10	GND	GND	20	Hφ2	Horizontal register transfer clock

*1 DC bias is generated within the CCD, so that this pin should be grounded externally through a capacitance of 0.1µF.

Absolute Maximum Ratings

Item		Ratings	Unit	Remarks
Against φSUB	V_{DD}, V_{OUT}, φRG – φSUB	–40 to +12	V	
	$V_{\phi 2A}$, $V_{\phi 2B}$ – φSUB	–50 to +15	V	
	$V_{\phi 1}$, $V_{\phi 3}$, $V_{\phi 4}$, V_L – φSUB	–50 to +0.3	V	
	$H_{\phi 1}$, $H_{\phi 2}$, GND – φSUB	–40 to +0.3	V	
	C_{SUB} – φSUB	–25 to	V	
Against GND	V_{DD}, V_{OUT}, φRG, C_{SUB} – GND	–0.3 to +22	V	
	$V_{\phi 1}$, $V_{\phi 2A}$, $V_{\phi 2B}$, $V_{\phi 3}$, $V_{\phi 4}$ – GND	–10 to +18	V	
	$H_{\phi 1}$, $H_{\phi 2}$ – GND	–10 to +6.5	V	
Against V_L	$V_{\phi 2A}$, $V_{\phi 2B}$ – V_L	–0.3 to +28	V	
	$V_{\phi 1}$, $V_{\phi 3}$, $V_{\phi 4}$, $H_{\phi 1}$, $H_{\phi 2}$, GND – V_L	–0.3 to +15	V	
Between input clock pins	Voltage difference between vertical clock input pins	to +15	V	*1
	$H_{\phi 1}$ – $H_{\phi 2}$	–6.5 to +6.5	V	
	$H_{\phi 1}$, $H_{\phi 2}$ – $V_{\phi 4}$	–10 to +16	V	
Storage temperature		–30 to +80	°C	
Performance guarantee temperature		–10 to +60	°C	
Operating temperature		–10 to +75	°C	

*1 +24 V (Max.) when clock width < 10 µs, clock duty factor < 0.1%.
+16 V (Max.) is guaranteed for power-on and power-off.

Bias Conditions

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Supply voltage	V_{DD}	14.55	15.0	15.45	V	
Protective transistor bias	V_L	*2				
Substrate clock	φSUB	*3				
Reset gate clock	φRG	*3				

DC characteristics

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Supply current	I_{DD}		9	11	mA	

*2 V_L setting is the V_{VL} voltage of the vertical clock waveform, or the same voltage as the V_L power supply for the V driver should be used.

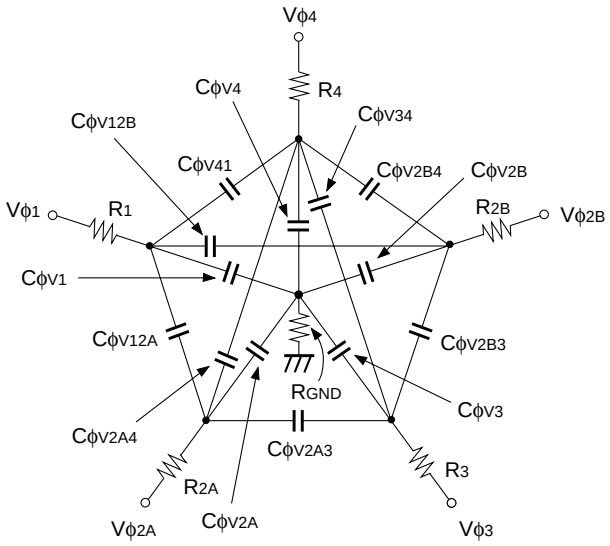
*3 Do not apply a DC bias to the substrate clock and reset gate clock pins, because a DC bias is generated within the CCD.

Clock Voltage Conditions

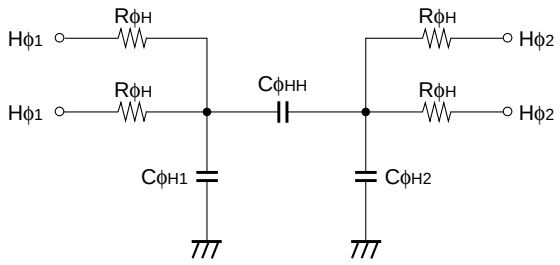
Item	Symbol	Min.	Typ.	Max.	Unit	Waveform diagram	Remarks
Readout clock voltage	V_{VT}	14.55	15.0	15.45	V	1	
Vertical transfer clock voltage	V_{VH1}, V_{VH2}	–0.05	0	0.05	V	2	$V_{VH} = (V_{VH1} + V_{VH2})/2$
	V_{VH3}, V_{VH4}	–0.2	0	0.05	V	2	
	V_{VL1}, V_{VL2}, V_{VL3}, V_{VL4}	–7.3	–7.0	–6.7	V	2	$V_{VL} = (V_{VL3} + V_{VL4})/2$
	$V\phi_V$	6.5	7.0	7.35	V	2	$V\phi_V = V_{VH}n – V_{VL}n$ (n = 1 to 4)
	$V_{VH3} – V_{VH}$	–0.25		0.1	V	2	
	$V_{VH4} – V_{VH}$	–0.25		0.1	V	2	
	V_{VHH}			1.4	V	2	High-level coupling
	V_{VHL}			1.3	V	2	High-level coupling
	V_{VLH}			1.4	V	2	Low-level coupling
	V_{VLL}			0.8	V	2	Low-level coupling
Horizontal transfer clock voltage	$V\phi_H$	4.75	5.0	5.25	V	3	
	V_{HL}	–0.05	0	0.05	V	3	
	V_{CR}	$V\phi_H/2$			V	3	Cross-point voltage
Reset gate clock voltage	$V\phi_{RG}$	3.0	3.3	5.5	V	4	
	$V_{RGLH} – V_{RGLL}$			0.4	V	4	Low-level coupling
	$V_{RGL} – V_{RGLm}$			0.5	V	4	Low-level coupling
Substrate clock voltage	$V\phi_{SUB}$	21.25	22.0	22.75	V	5	

Clock Equivalent Circuit Constants

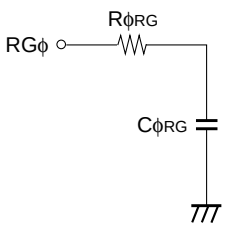
Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Capacitance between vertical transfer clock and GND	CφV1		5600		pF	
	CφV2A		6800		pF	
	CφV2B		22000		pF	
	CφV3		8200		pF	
	CφV4		22000		pF	
Capacitance between vertical transfer clocks	CφV12A		150		pF	
	CφV12B		390		pF	
	CφV2A3		270		pF	
	CφV2B3		470		pF	
	CφV14		2200		pF	
	CφV34		330		pF	
	CφV2A4		390		pF	
	CφV2B4		560		pF	
Capacitance between horizontal transfer clock and GND	CφH1		47		pF	
	CφH2		39		pF	
Capacitance between horizontal transfer clocks	CφHH		74		pF	
Capacitance between reset gate clock and GND	CφRG		4		pF	
Capacitance between substrate clock and GND	CφSUB		1300		pF	
Vertical transfer clock series resistor	R1, R3		30		Ω	
	R2A, R2B		32		Ω	
	R4		20		Ω	
Vertical transfer clock ground resistor	RGND		60		Ω	
Horizontal transfer clock series resistor	RφH		7.5		Ω	
Reset gate clock ground resistor	RφRG		24		Ω	



Vertical transfer clock equivalent circuit



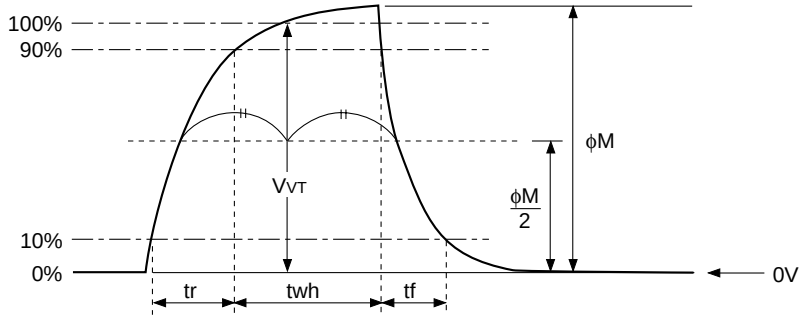
Horizontal transfer clock equivalent circuit



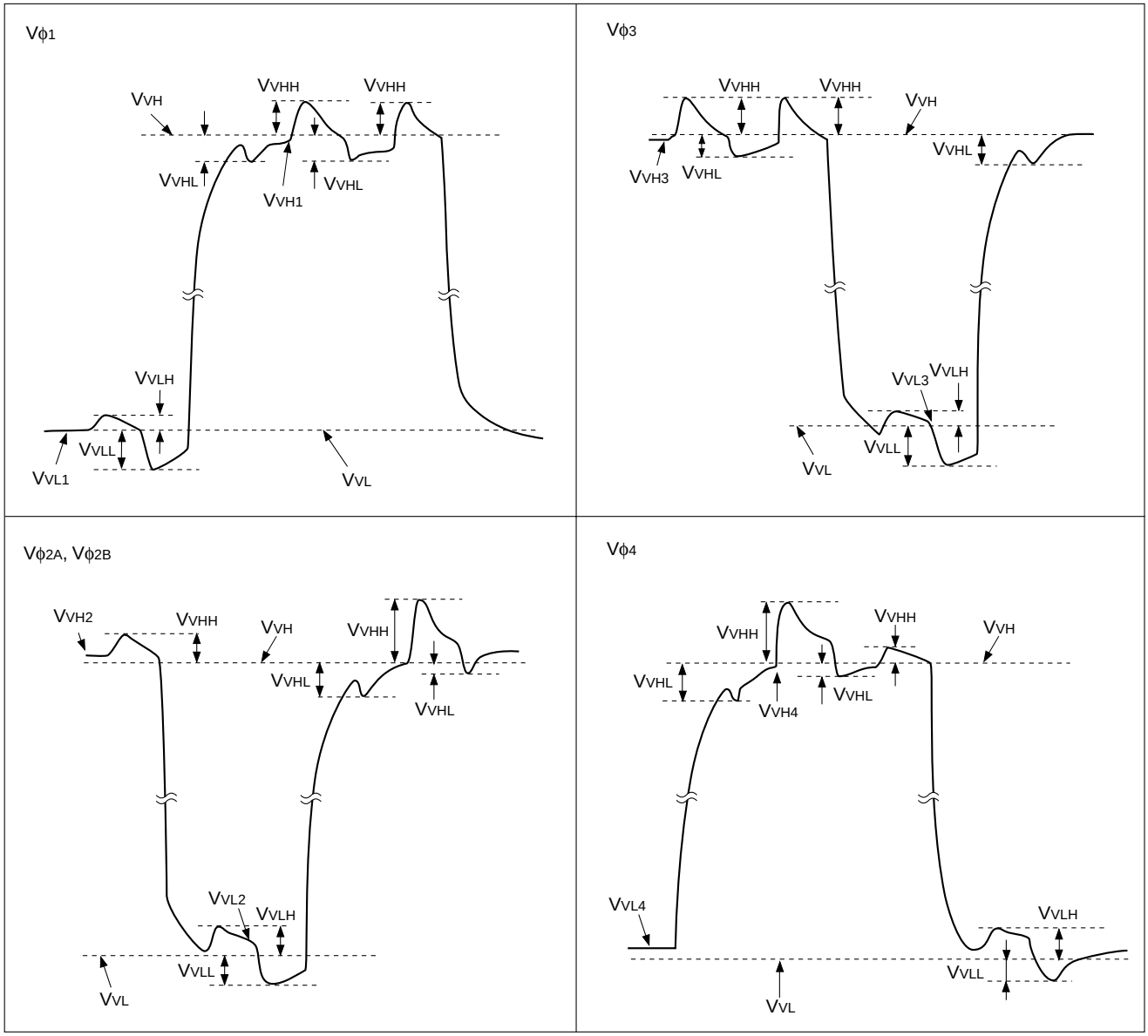
Reset gate clock equivalent circuit

Drive Clock Waveform Conditions

(1) Readout clock waveform



(2) Vertical transfer clock waveform

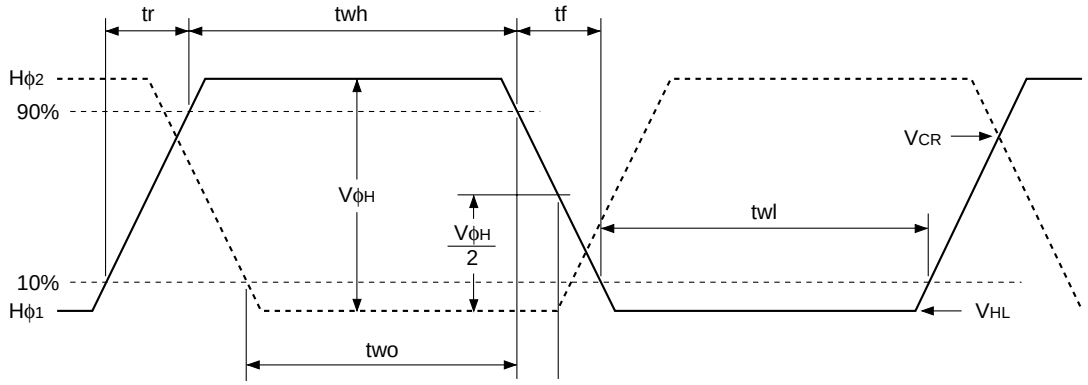


$V_{VH} = (V_{VH1} + V_{VH2})/2$

$V_{VL} = (V_{VL3} + V_{VL4})/2$

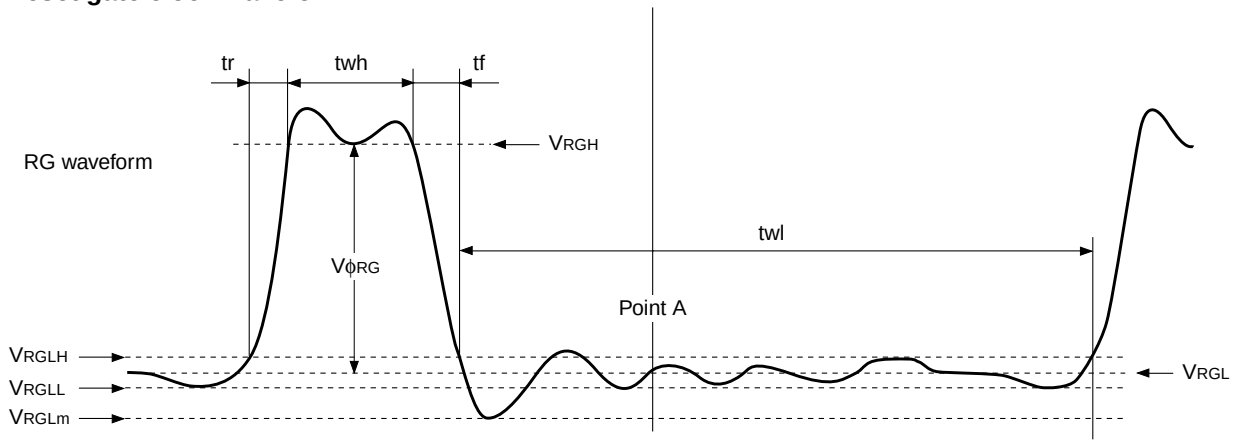
$V_{\phi V} = V_{VHn} – V_{VLn}$ (n = 1 to 4)

(3) Horizontal transfer clock waveform



Cross-point voltage for the Hϕ1 rising side of the horizontal transfer clocks Hϕ1 and Hϕ2 waveforms is V_{CR}.
The overlap period for twh and twl of horizontal transfer clocks Hϕ1 and Hϕ2 is two.

(4) Reset gate clock waveform



V_{RGLH} is the maximum value and V_{RGLL} is the minimum value of the coupling waveform during the period from Point A in the above diagram until the rising edge of RG.
In addition, V_{RGL} is the average value of V_{RGLH} and V_{RGLL}.

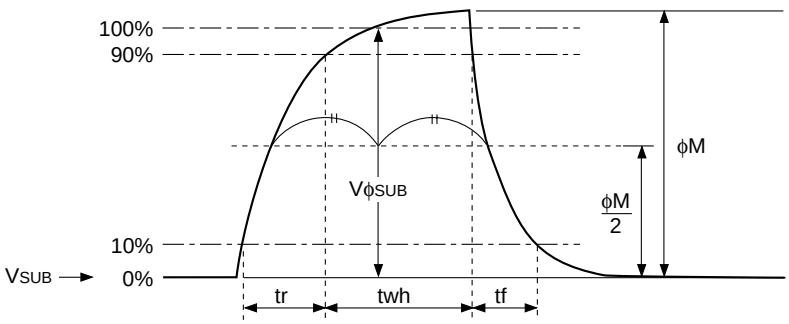
$$V_{RGL} = (V_{RGLH} + V_{RGLL})/2$$

Assuming V_{RGH} is the minimum value during the interval twh, then:

$$V\phi_{RG} = V_{RGH} - V_{RGL}$$

Negative overshoot level during the falling edge of RG is V_{RGLm}.

(5) Substrate clock waveform



(A bias generated within the CCD)

Clock Switching Characteristics (Horizontal drive frequency: 28.64 MHz)

Item		Symbol	twh			twl			tr			tf			Unit	Remarks
			Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
Readout clock		V_T	2.8	3.0						0.5			0.5		µs	During readout
Vertical transfer clock		$V\phi_1$, $V\phi_2$, $V\phi_3$, $V\phi_4$										15		250	ns	When using CXD3400N
Horizontal transfer clock	During imaging	$H\phi_1$	10	12.5		10	12.5			5	7.5		5	7.5	ns	rf ≥ rf – 2ns
		$H\phi_2$	10	12.5		10	12.5			5	7.5		5	7.5		
	During parallel-serial conversion	$H\phi_1$								0.01			0.01		µs	
		$H\phi_2$								0.01			0.01			
Reset gate clock		ϕ_{RG}	4	8			24			2			2		ns	
Substrate clock		ϕ_{SUB}	3.5	3.9							0.5			0.5	µs	During drain charge

Item	Symbol	two			Unit	Remarks
		Min.	Typ.	Max.		
Horizontal transfer clock	$H\phi_1$, $H\phi_2$	8	10		ns	

Spectral Sensitivity Characteristics (excludes lens characteristics and light source characteristics)

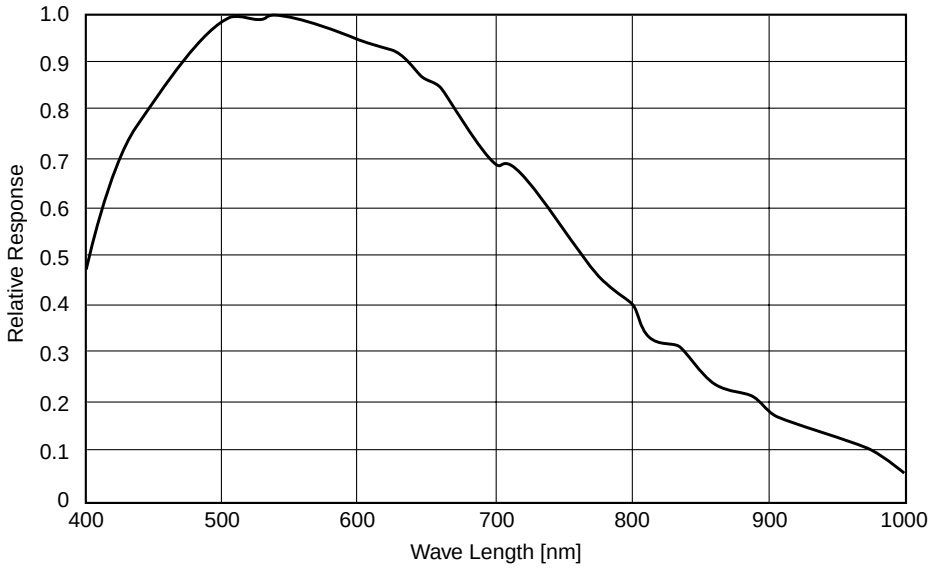


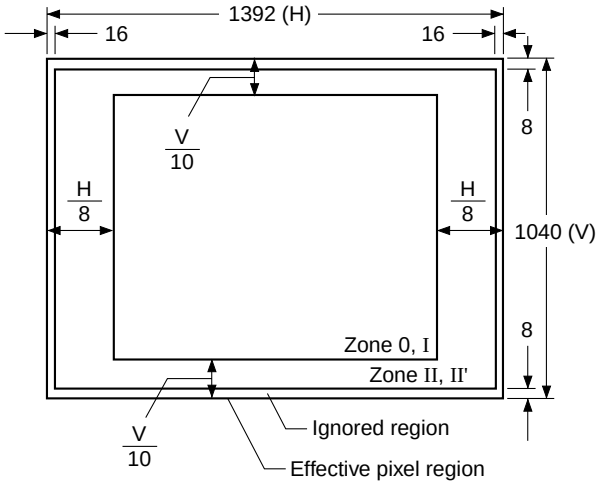
Image Sensor Characteristics

(Ta = 25°C)

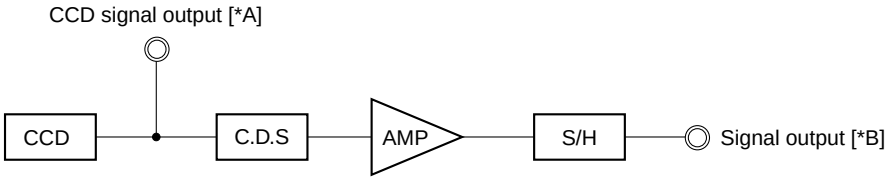
Item	Symbol	Min.	Typ.	Max.	Unit	Measurement method	Remarks
Sensitivity 1	S1	1040	1300		mV	1	1/30 s accumulation
Sensitivity 2	S2		4000		mV	2	1/30 s accumulation
Saturation signal	Vsat	850			mV	3	Ta = 60°C
Smear	Sm		–110	–100	dB	4	Progressive scan mode
			–98	–88			High frame rate readout mode
Video signal shading	SH			20	%	5	Zone 0 and I
				25			Zone 0 to II'
Dark signal	Vdt			11	mV	6	Ta = 60°C, 15 frame/s
Dark signal shading	ΔVdt			4	mV	7	Ta = 60°C, 15 frame/s, *1
Lag	Lag			0.5	%	8	

*1 Excludes vertical dark signal shading caused by vertical register high-speed transfer.

Zone Definition of Video Signal Shading



Measurement System

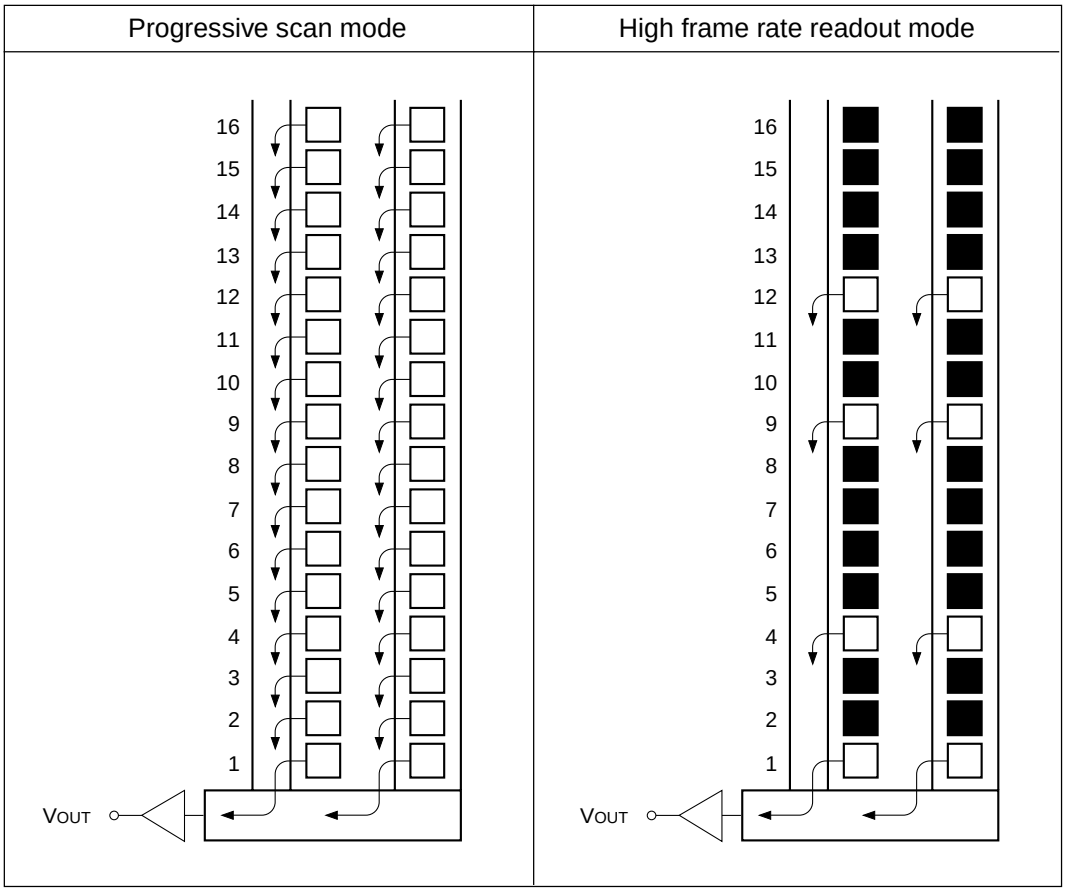


Note) Adjust the amplifier gain so that the gain between [*A] and [*B] equals 1.

Image Sensor Characteristics Measurement Method

- **Readout modes**

The diagram below shows the output methods for the following two readout modes.



Note) Blacked out portions in the diagram indicate pixels which are not read out.
Output starts from line 1 in high frame rate readout mode.

1. Progressive scan mode
   In this mode, all pixel signals are output in non-interlace format in 1/15 s.
   All pixel signals within the same exposure period are read out simultaneously, making this mode suitable for high resolution image capturing.

2. High frame rate readout mode
   All effective areas are scanned in approximately 1/60 s by reading out two out of eight lines (1st and 4th lines, 9th and 12th lines, and so on). The vertical resolution is approximately 256 TV-lines.
   This readout mode emphasizes processing speed over vertical resolution.

- **Measurement conditions**

(1) In the following measurements, the substrate voltage is set to the value indicated on the device, and the device drive conditions are at the typical values of the progressive scan mode, bias and clock voltage conditions.

(2) In the following measurements, spot blemishes are excluded and, unless otherwise specified, the optical black level (OB) is used as the reference for the signal output, which is taken as the value measured at point [*B] of the measurement system.

- **Definition of standard imaging conditions**

(1) Standard imaging condition I:
Use a pattern box (luminance: 706 cd/m^2, color temperature of 3200K halogen source) as a subject. (Pattern for evaluation is not applicable.) Use a testing standard lens with CM500S (t = 1.0 mm) as an IR cut filter and image at F8. The luminous intensity to the sensor receiving surface at this point is defined as the standard sensitivity testing luminous intensity.

(2) Standard imaging condition II:
This indicates the standard imaging condition I with the IR cut filter removed.

(3) Standard imaging condition III:
Image a light source (color temperature of 3200K) with a uniformity of brightness within 2% at all angles. Use a testing standard lens with CM500S (t = 1.0 mm) as an IR cut filter. The luminous intensity is adjusted to the value indicated in each testing item by the lens diaphragm.

1. Sensitivity 1
Set to standard imaging condition I. After selecting the electronic shutter mode with a shutter speed of 1/100 s, measure the signal output (V_{S1}) at the center of the screen, and substitute the value into the following formula.

$$S_1 = V_{S1} \times \frac{100}{30} \text{ [mV]}$$

2. Sensitivity 2
Set to standard imaging condition II. After selecting the electronic shutter mode with a shutter speed of 1/500 s, measure the signal output (V_{S2}) at the center of the screen, and substitute the value into the following formula.

$$S_2 = V_{S2} \times \frac{500}{30} \text{ [mV]}$$

3. Saturation signal
Set to standard imaging condition III. After adjusting the luminous intensity to 20 times the intensity with the average value of the signal output, 200 mV, measure the minimum value of the signal output.

4. Smear
Set to standard imaging condition III. With the lens diaphragm at F5.6 to F8, first adjust the luminous intensity to 500 times the intensity with the average value of signal output, 200 mV. Then after the readout clock is stopped and the charge drain is executed by the electronic shutter at the respective H blankings, measure the maximum value (Vsm [mV]) of the signal output and substitute the value into the following formula.

$$Sm = 20 \times \log\left(\frac{Vsm}{200} \times \frac{1}{500} \times \frac{1}{10}\right) \text{ [dB] (1/10 V method conversion value)}$$

5. Video signal shading
   Set to standard imaging condition III. With the lens diaphragm at F5.6 to F8, adjust the luminous intensity so that the average value of the signal output is 200 mV. Then measure the maximum (Vmax [mV]) and minimum (Vmin [mV]) values of the signal output and substitute the values into the following formula.

   $SH = (Vmax - Vmin)/200 \times 100$ [%]

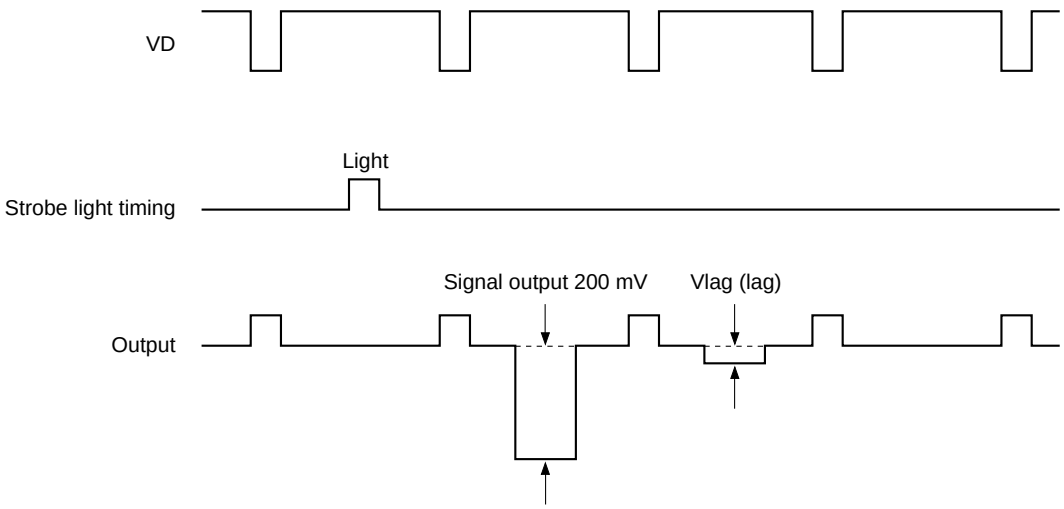
6. Dark signal
   Measure the average value of the signal output (Vdt [mV]) with the device ambient temperature 60°C and the device in the light-obstructed state, using the horizontal idle transfer level as a reference.

7. Dark signal shading
   After measuring 6, measure the maximum (Vdmax [mV]) and minimum (Vdmin [mV]) values of the dark signal output and substitute the values into the following formula.

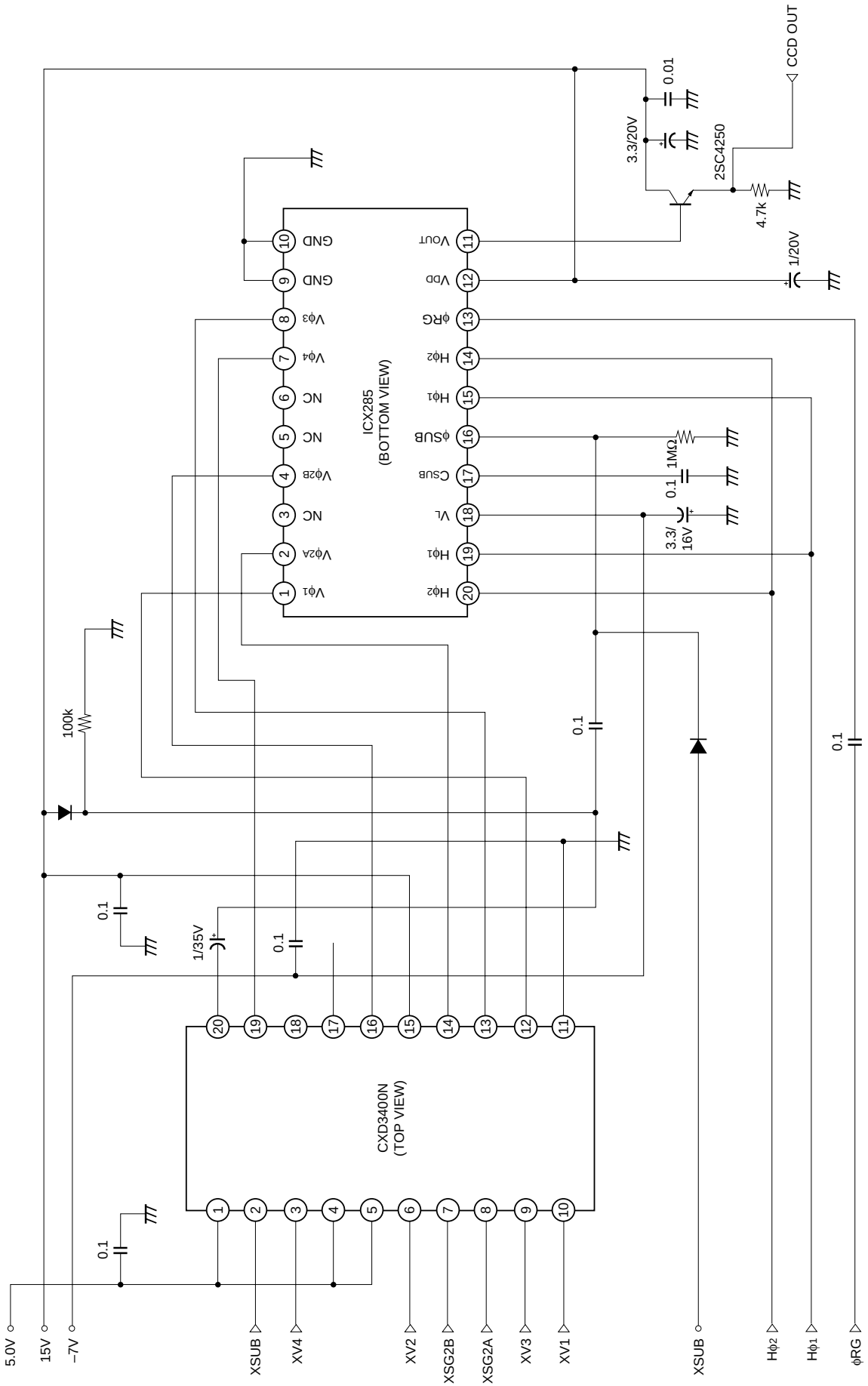
   $\Delta Vdt = Vdmax - Vdmin$ [mV]

8. Lag
   Adjust the signal output generated by strobe light to 200 mV. After setting the strobe light so that it strobes with the following timing, measure the residual signal (Vlag). Substitute the value into the following formula.

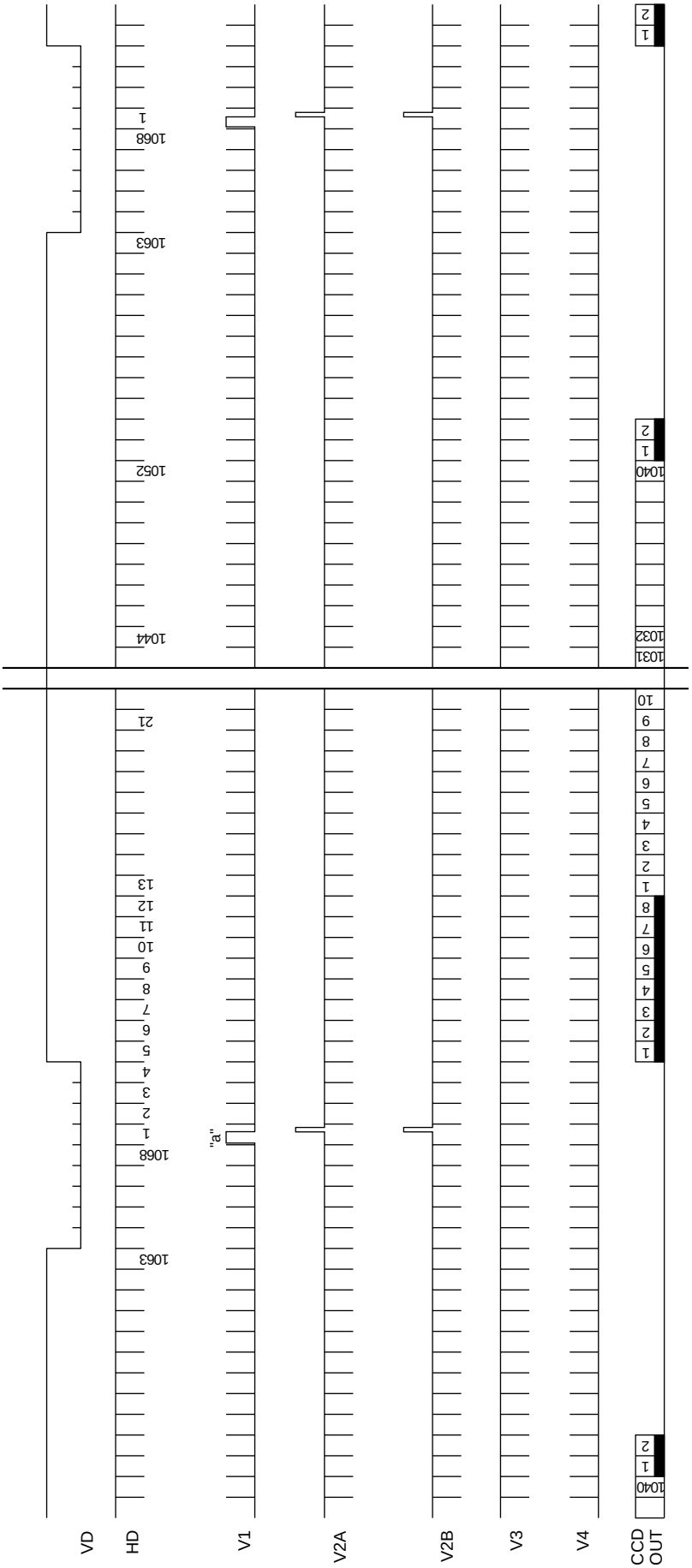
   $Lag = (Vlag/200) \times 100$ [%]



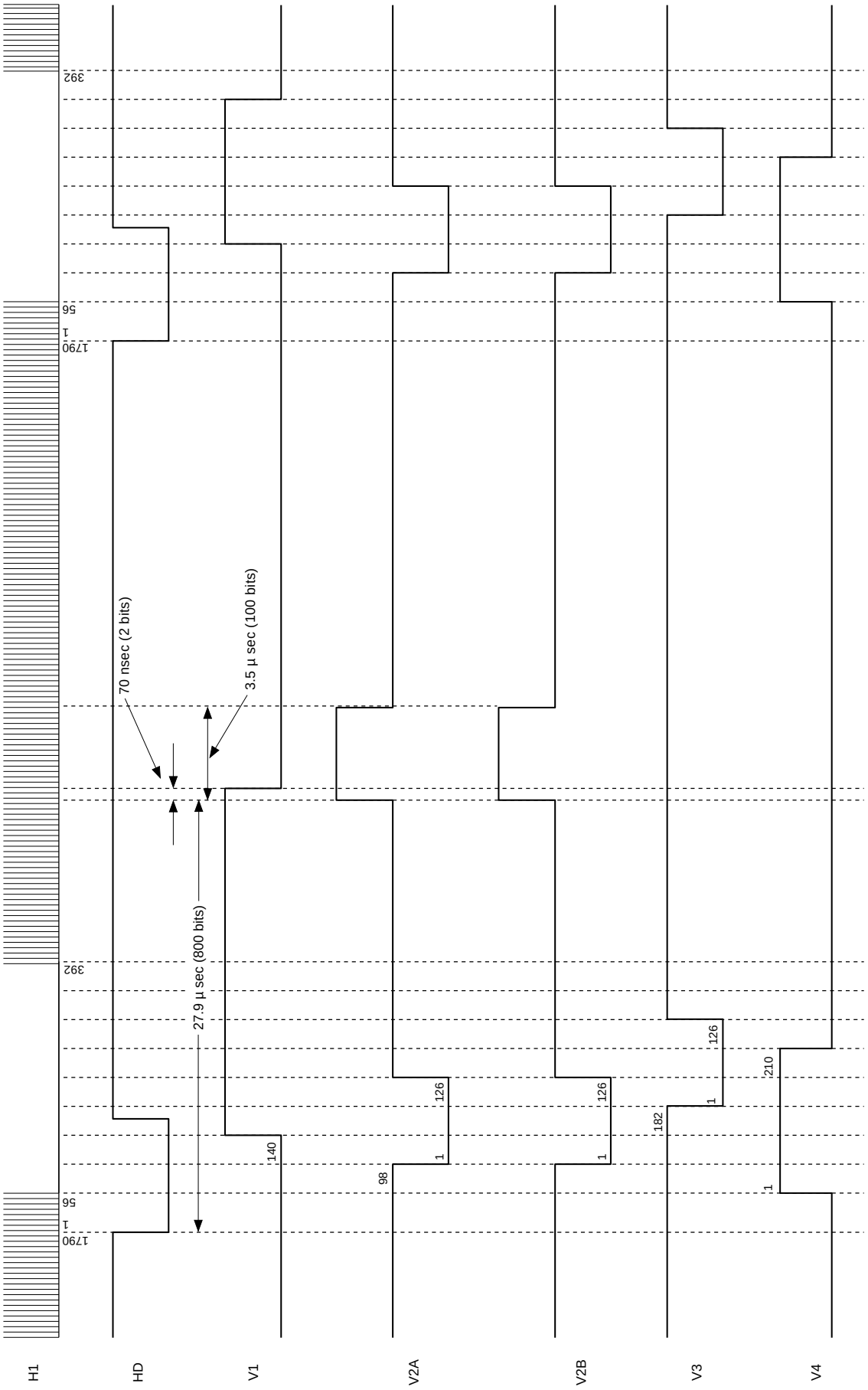
Drive Circuit



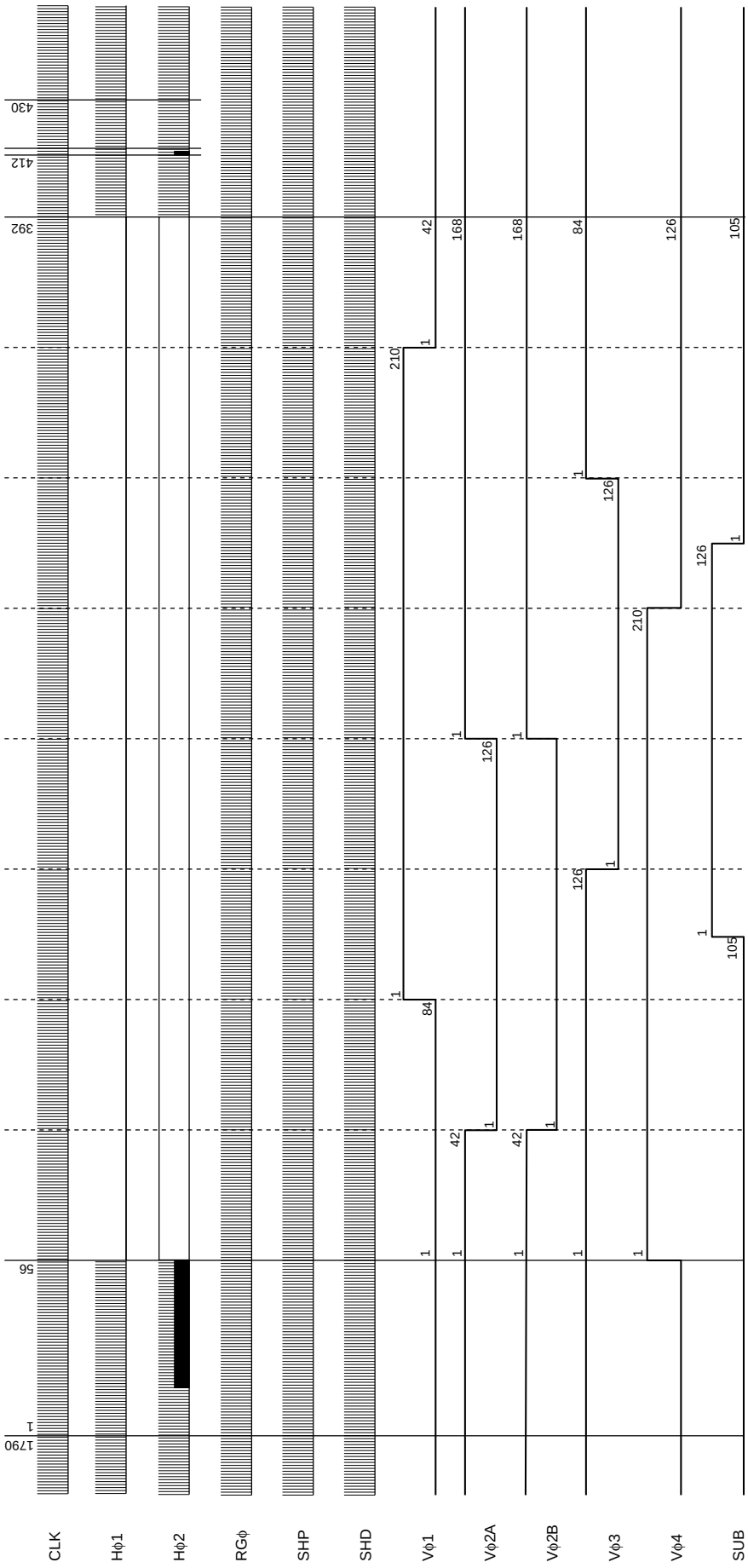
Drive Timing Chart (Vertical Sync) Progressive Scan Mode



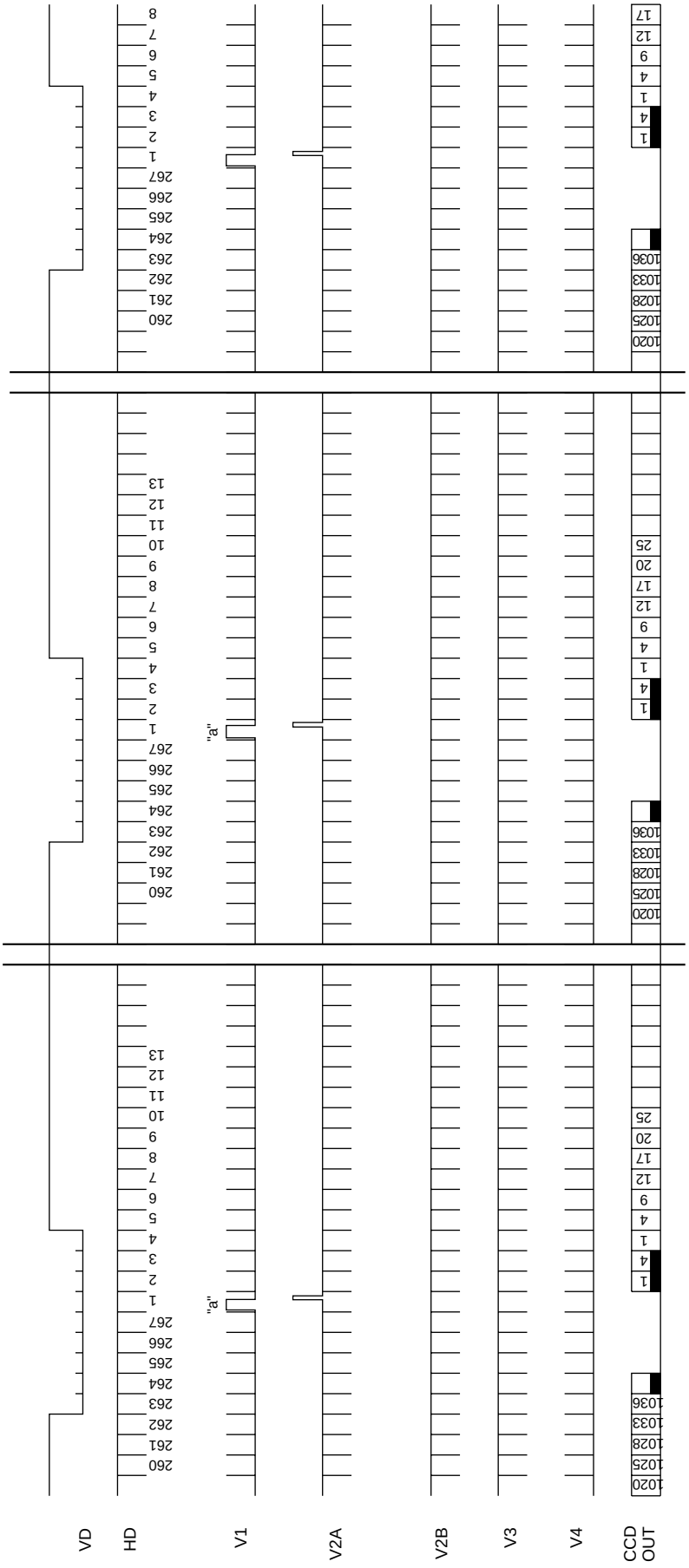
Drive Timing Chart (Vertical Sync "a" Enlarged) Progressive Scan Mode



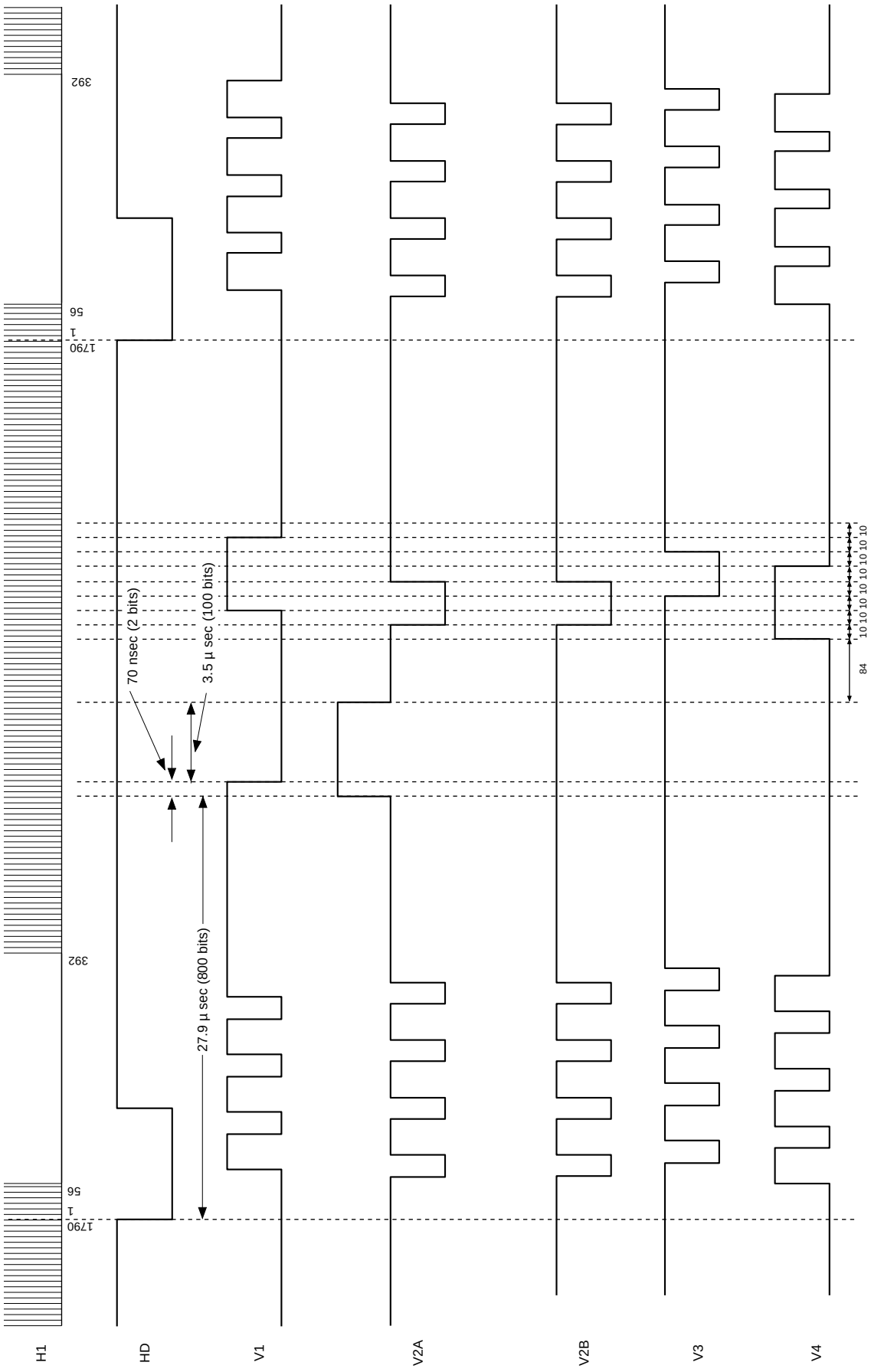
Drive Timing Chart (Horizontal Sync) Progressive Scan Mode



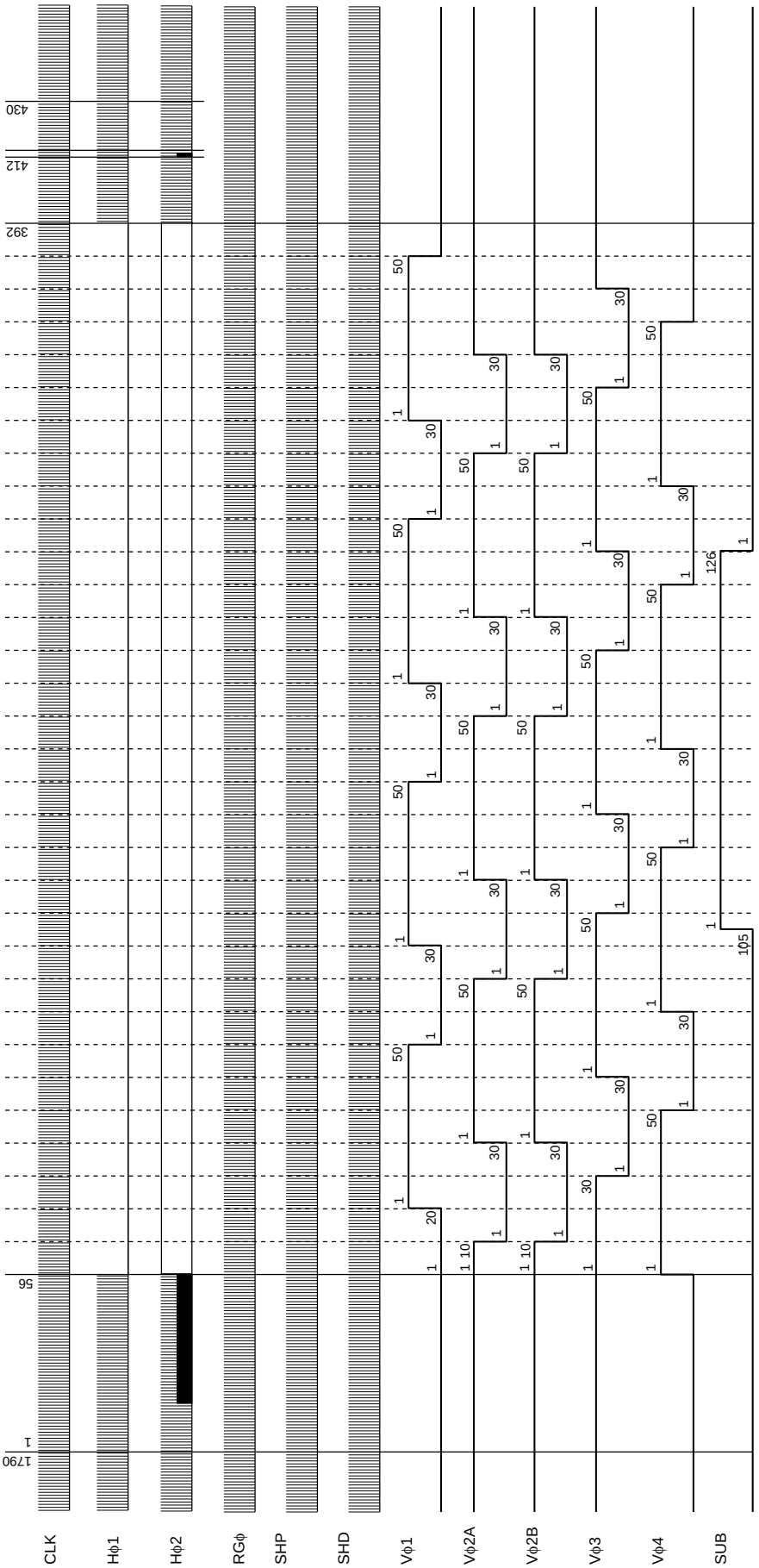
Drive Timing Chart (Vertical Sync) High Frame Rate Readout Mode



Drive Timing Chart (Vertical Sync "a" Enlarged) High Frame Rate Readout Mode



Drive Timing Chart (Horizontal Sync) High Frame Rate Readout Mode



Notes on Handling

1) Static charge prevention
   CCD image sensors are easily damaged by static discharge. Before handling be sure to take the following protective measures.
   a) Either handle bare handed or use non-chargeable gloves, clothes or material.
      Also use conductive shoes.
   b) When handling directly use an earth band.
   c) Install a conductive mat on the floor or working table to prevent the generation of static electricity.
   d) Ionized air is recommended for discharge when handling CCD image sensor.
   e) For the shipment of mounted substrates, use boxes treated for the prevention of static charges.

2) Soldering
   a) Make sure the package temperature does not exceed 80°C.
   b) Solder dipping in a mounting furnace causes damage to the glass and other defects. Use a ground 30W soldering iron and solder each pin in less than 2 seconds. For repairs and remount, cool sufficiently.
   c) To dismount an image sensor, do not use a solder suction equipment. When using an electric desoldering tool, use a thermal controller of the zero cross On/Off type and connect it to ground.

3) Dust and dirt protection
   Image sensors are packed and delivered by taking care of protecting its glass plates from harmful dust and dirt. Clean glass plates with the following operation as required, and use them.
   a) Perform all assembly operations in a clean room (class 1000 or less).
   b) Do not either touch glass plates by hand or have any object come in contact with glass surfaces. Should dirt stick to a glass surface, blow it off with an air blower. (For dirt stuck through static electricity ionized air is recommended.)
   c) Clean with a cotton bud and ethyl alcohol if the grease stained. Be careful not to scratch the glass.
   d) Keep in a case to protect from dust and dirt. To prevent dew condensation, preheat or precool when moving to a room with great temperature differences.
   e) When a protective tape is applied before shipping, just before use remove the tape applied for electrostatic protection. Do not reuse the tape.

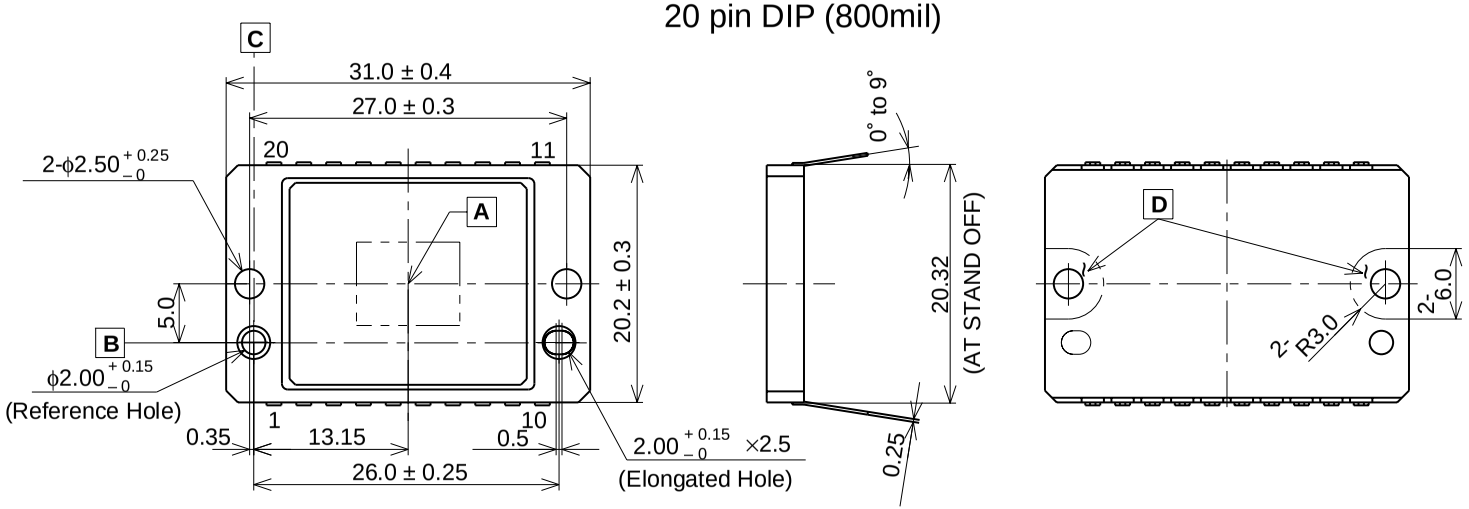
4) Do not expose to strong light (sun rays) for long periods. For continuous using under cruel condition exceeding the normal using condition, consult our company.

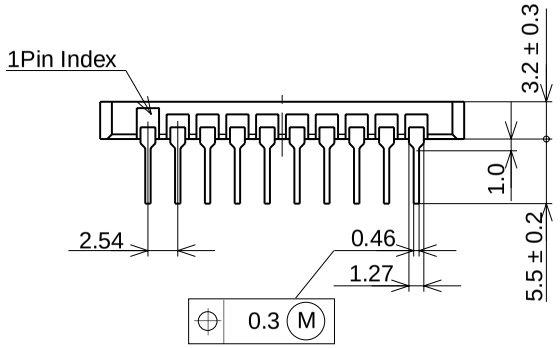
5) Exposure to high temperature or humidity will affect the characteristics. Accordingly avoid storage or usage in such conditions.

6) CCD image sensors are precise optical equipment that should not be subject to too much mechanical shocks.

Package Outline Unit: mm

20 pin DIP (800mil)





1. "**A**" is the center of the effective image area.
2. The straight line **"B"** which passes through the center of the reference hole and the elongated hole is the reference axis of vertical direction (V).
3. The straight line **"C"** which passes through the center of the reference hole at right angle to vertical reference line **"B"** is the reference axis of horizontal direction (H).
4. The bottom **"D"** is the height reference.(Two points are specified.)
5. The center of the effective image area specified relative to the reference hole is (H, V) = (13.15, 5.0) ± 0.15mm.
6. The angle of rotation relative to the reference line **"B"** is less than ± 1°
7. The height from the bottom **"D"** to the effective image area is 1.46 ± 0.15mm.
8. The tilt of the effective image area relative to the bottom **"D"** is less than 60µm.
9. The thickness of the cover glass is 0.75mm and the refractive index is 1.5.

PACKAGE STRUCTURE

PACKAGE MATERIAL	Ceramic
LEAD TREATMENT	GOLD PLATING
LEAD MATERIAL	42 ALLOY
PACKAGE MASS	5.90g
DRAWING NUMBER	AS-A11(E)