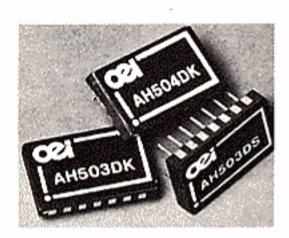


AH503/AH504

High Speed Peak Detector



Features

- Fast Acquisition: 100ns wide 1V pulse, 200ns wide 10V pulse
- High Slew Rate: 50 V/µs
- Low Droop Rate: 1 mV/μs max with C_x = 1000pF
- Wide Temperature Operation: -55°C to +125°C (AH503DS)

Applications

- Data Acquisition
- Pulse Stretcher
- Noise Measurement
- Video Peak Sense

The AH503 and AH504 peak detectors are designed for rapid acquisition of very narrow pulses. They combine high slew rates and fast settling to capture individual 1V pulses as narrow as 100ns to within ±10mV. For general applications where narrow pulses need to be acquired for analysis or processing, the lower cost AH503DK is ideal. Where the time interval for the sampling needs to be more precisely defined, the faster reset and switching times of the AH504DK may be required. When operation over the full MIL temperature range is required (~55°C to 125°C), the AH503DS, with slightly higher droop rate, will be appropriate.

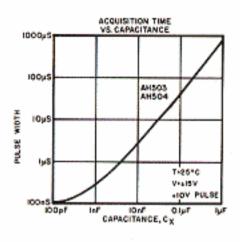
The AH503 and AH504, in standard 14 pin ceramic DIP packages, reduce board space 90% over the only previously available peak detectors in this speed range. Use of standard thin-film hybrid technology also enhances the reliability of these devices.

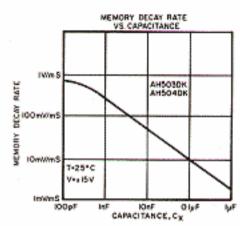
The only external component required for capturing pulses with the AH503 and AH504 is the hold capacitor, which the designer needs to optimize for the particular application, considering the trade-off between acquisition time and memory decay rate. This helps minimize design time and simplify overall circuit design.

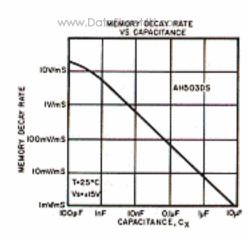
AH503/AH504 Specifications
Specifications at $T_A = +25^{\circ}C$ and $V_{oc} = \pm 15V$ DC unless otherwise specified

Parameter	Condition		ww	w.DataSheet4U.	Units
Input		AH503DI	AHE04DI	K AH503DS	
Voltage	$V_{in} = 1 MHz AC, C_X = 1000 pF$	AIIOOODI	· Allouddi	N ANSOSDS	
•	Sensing Range, $T_A = +25^{\circ}C$	+0.03/+10	٠ (*	V,min range
	Sensing Range, $T_A = Full$				
DI-I	Operating Range	+0.1/+10	*		V,min range
Resistance	Gate Lo	1.	• :		KΩmin
Basel Command	Gate Hi	500	:	:	KΩ typ
Reset Command	T _A = Full Operating Range	0.8	•		V max
Gate Open Peak Sense Command	$T_A = Full Operating Range$ $T_A = Full Operating Range$	0.8 2.4	•		V max V min
Command Load	Gate = Reset = 0V or 5V	2.4			VIIIII
Command Load	T _A = Full Operating Range	2	• 110	15.4	mA max
0.4	TA Tan operating hange				mirtinan
Output	V - 10V1: 10 1MI				
Voltage	V _{in} = 10V peak AC, 1MHz	0.0			M
	$C_X = 330 pF, R_L = 1 K\Omega$ $T_A = Full Operating Range$	9.9 9.8	.i. isa	7 · 1 · 1 · 1 / 2	V min V min
Current	V _{out} = +10V	10	11.	• 1	mA min
Resistance	Vout - 110V	1		. 🕶 141.438	Ωtyp
Overshoot	$V_{in} = +10V \text{ step, } C_{x} = 330pF$	10		 • * * * * * * * * * * * * * * * * * * *	% typ
	- III				70171
Dynamic Response Slew Rate	C - 100-E	50			Minha
Continuous Sinusoidal	C _X = 100pF	50			V/μs typ
Continuous Sinusoidai	-3 dB point, $V_{in} = 5V$ peak AC, $R_L = 1$ K Ω , $C_X = 330$ pF	10			Milania
	T. = Full Operating Range	10 9.5			MHz min
Acquisition Time	$T_A = Full Operating Range$ $V_{in} = 10V pulse, C_X = 330pF$	9.5			MHz min
(Minimum Pulse Width)	$R_L = 1K\Omega$, Settling to				
(William and alse Widay)	within ±100mV				
	T _A = Full Operating Range	200		* .	ns max
	V _{in} = 1V pulse, C _X = 100pF	200			Homax
	$R_L = 1K\Omega$, Settling to				
	within ±10mV	100		•	ns max
Reset Time	$V_{cut} = +10V$ to under $+30$ mV.				
	$C_x = 330pF$, Gate = Lo	500	300	500	ns max
Gate Turn On Time	$V_{in} = +10VDC$, Reset = Hi,				
	Observe at C _x	500	300	500	ns max.
Gate Turn Off Time	$V_{in} + 10V DC$, Reset = Hi,				
	Observe at input	500	300	300	ns max
Error Sources					
Offset Voltage	Reset = Lo				
	$T_A = Full Operating Range$	±30	•	•	mV max
Gain Error	$V_{in} = +10V DC, C_X = 330pF,$				
	$R_L = 1K\Omega$	±0.5		*	% max
	T _A = Full Operating Range	±1	•	*	% max
Memory Decay Rate					
memory beealy mate	$C_x = 1000pF$	1	1	7	mV/μs max
	TA = Full Operating Range	2	2	7	mV/μs max
Temperature Range	Д				
Operating		0/70	0/70	-55/125	°C
Derated Performance		-25/100	-25/100	-55/125	.č
Storage		-65/150	*	-55/125	č
		00.100			
Power Supply Requirements		+15			.,
Rated Voltage		±15			v v
Ope www.DataSheet4U.com Quiesees	T _A = Full Operating Range	±9/±18 +30/-10	+35/-15	+30/-10	
adiosociii odii ciii	A - Full Operating Hange	730/-10	-337-15	-30/- IU	mA max

Typical Performance Curves

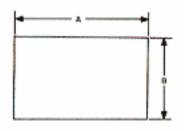


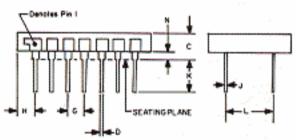




Mechanical Description

The AH503/AH504 package is a standard 14-pin bottom brazed ceramic dual-in-line package. The AH503DS is hermetically sealed.





Bottom View

Pin Numbers shown for reference only. Numbers are not marked on Package.

Q14

O(3

Oe.

OIL

010 09

08

10 20

30 40 50

60

70

- 1) Reset
- Gate
- No Connection (NC)
- 4) Digital Common
- 5) NC
- Analog Common
- 7) Offset Adjust
- 8) Analog Output
- Offset Adjust
- 10) C_x
- 11) + V_{CC}
- 12) Nwww.DataSheet4U.com
- 13) Anaiog input
- 14) V_{CC}

	Inches		Millimeters		
Dim	Min	Max	Min	Max	
A	.770	.810	19.56	20.57	
В	.480	.500	12.19	12.70	
С	.155	.215	3.94	5.46	
D	.016	.020	.41	.51	
G .	0.100 Nom.		2.54 Nom.		
Н	.080	.110	2.03	2.79	
J	.009	.012	.23	.30	
K	.150	.210	3.81	5.33	
L :	.300 Nom.		7.62 Nom.		
N	.015	.035	.38	.89	

1) Leads in true position within .010" (.255 mm)

Absolute Maximum Ratings				
Supply	±20VDC			
Input Voltage ¹	± 15V DC			
Storage Temperature Range	- 65°C to 150°C			
Operating Temperature Range	- 55°C to 125°C			
Lead Temperature (Soldering 10 second	nds) + 300°C			
Output Short Circuit Duration ²	Continuous			

- 1) For supply voltages less than ± 15V DC, the absolute maximum input is equal to the supply voltage.
- 2) Short circuit to ground only.

Application Information

Figure 1: Functional Block Diagram

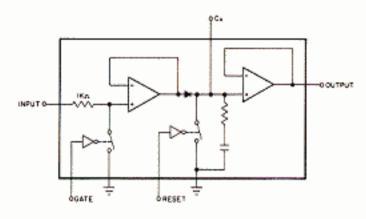
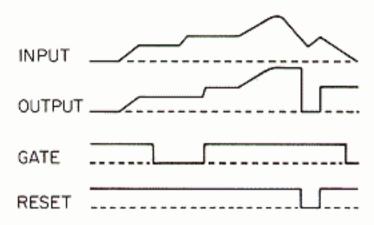


Figure 2: Timing Diagram, DataSheet4U.com



The basic difference between the AH503 and the AH504 is the speed of the internal switches used for gating and resetting the unit. The AH504 resets and gates approximately 40% faster than the AH503, allowing the user to more precisely define the specific time interval when peak detection is required.

To provide predictable, reliable performance from ~55°C to 125°C, the AH503DS had to be modified internally. The required modification also resulted in an increased memory decay rate, as specified. When actual operating temperatures do not exceed 100°C, the AH503DK is preferable.

Basic Operation

Figure 1 shows a block diagram of the basic operation of the AH503 and AH504. A diode is incorporated internally to prevent damage to the circuit from negative inputs. The two amplifier stages are each in a unity-gain follower configuration, to provide an accurate overall gain of 1. The diode shown after the input amp (actually an open-collector arrangement) allows the hold capacitor to track positive-going signals, but blocks negative-going signals. Once the peak is acquired, the FET input of the output amplifier minimizes the rate of discharge of the hold capacitor.

Acquisition time on the AH503 and AH504 relates to the width of the pulse they can capture, and not to the timing of the output. Typically, the delay between the input reaching peak value and the output settling to that value will be 500ns. This obviously varies with the value of the hold capacitor, C_x , and needs to be considered in overall circuit timing.

Figure 2 shows the basic timing of the AH503 and AH504. With the gate and reset high, the output will track the input as long as it goes positive. Changing the gate to low blocks further input rises from charging the hold capacitor. When the gate returns high, the output again tracks a positive-going input, and holds the peak level attained (disregarding the memory decay rate) until reset.

The gate and reset switches require standard TTL logic levels, and both switches are normally closed. Whenever possible, the input gate should be closed (logic level low) when resetting (also logic level low) since a positive input signal when resetting could prevent the hold capacitor from fully discharging.

For optimum operation, the end of the reset command should precede the end of the gate command by approximately 150ns. This timing is only critical when the target pulse can occur within 150ns of activating the gate to start sensing.

While all of the applications shown below are designed to capture pulses which are positive relative to ground, pin 6 (Analog Common) can actually be used to set a threshold level, above which any pulse would be captured. Pin 6 can even be tied to a negative voltage, as long as the delta between pin 6 and +V_{cc} does not exceed 20V.

Figure 3: Typical + 10V Pulse Application

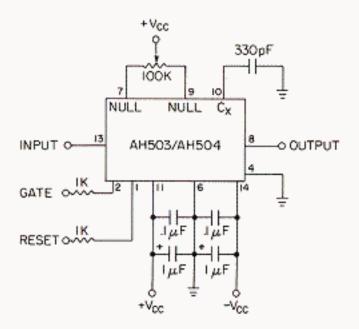


Figure 5: Peak Detector With Gain

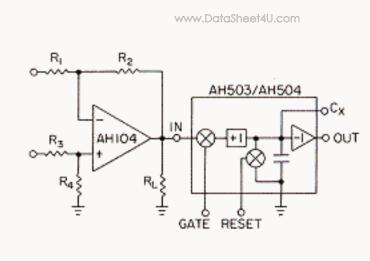
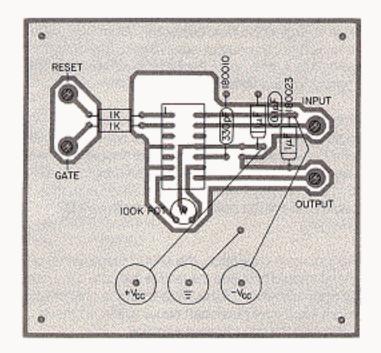


Figure 4: Suggested Board Layout



Circuit Layout

A typical circuit for the AH503 and AH504 is shown in Figure 3, with an appropriate printed circuit board layout shown in Figure 4.

A hold capacitor, C_x, of 330pF is optimal for acquiring a full +10V pulse, when slew rate, settling time, overshoot, etc., are all considered. For smaller pulses, the hold capacitor can be reduced, hence reducing acquisition time without sacrificing accuracy.

As on any high speed device, grounding is critical on the AH503 and AH504. Whenever possible, a ground plane should be used, covering as much of the circuit board as possible to provide low resistance and low impedance paths for all signal and power common returns.

If the digital supplies or common are susceptible to surges, as is common in digital systems, the digital and analog grounds need to be isolated, and power supply bypassing becomes critical.

Power supply bypassing should be used in all applications, since the AH503 and AH504 are not internally bypassed. The capacitors needed will depend on the quality of the supply, but in any case, the bypassing should be done as close as possible to the device pins.

Offset Null

If detection of peaks below +30mV is needed, the offset null circuit shown in Figure 3 can be used. Sine waves as low as +10mV peak have been captured in this method.

Adjustment should be done with the input grounded, after a reset command and with gate and reset both at +5V, so that the trimming can also adjust out any digital feed through from the logic signals.

Figure 6: Fast Acquisition/Low Droop Circuit

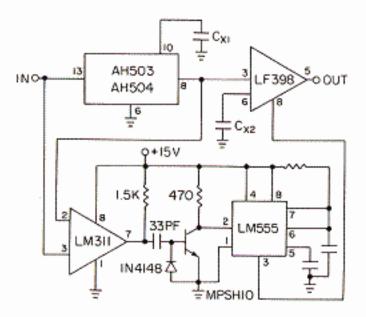
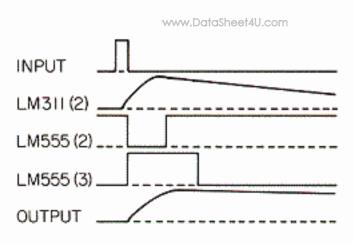


Figure 7: Timing Diagram for Figure 6



Typical Circuits

Where low level pulses need to be captured accurately, the AH503 and AH504 can be used with a wideband input amplifier, such as the AH104, to provide the required gain. The FET input of the AH104, its 80ns settling to within 1%, and its low offset voltage, when combined with the speed of the AH503 and AH504 mean that extremely low level, narrow pulses from high impedance sources can be captured very accurately.

Figure 5 shows this combination of the AH503/ AH504 and the AH104 for a peak detector with gain. With $\rm R_2$ and $\rm R_4$ at 1M Ω and $\rm R_1$ and $\rm R_3$ at 1K Ω , a gain of 1000 can be achieved. $\rm R_L$ is selected to match the output of the AH104 to the input of the AH503/AH504, and for a 10V peak output from the AH104 should typically be 1K Ω .

By using the AH104 in Figure 5 in an inverting mode, negative pulses can be captured by the AH503/AH504, with or without gain. By combining these approaches in two channels, a peak-to-peak level detector can be designed.

Similarly, an automatic gain circuitry could be designed to adjust the gain of the AH104 based on the output of the AH503/AH504. This would not be possible for capturing single pulses, but would work for a sine wave or pulse train.

Figure 6 shows a circuit designed to take maximum advantage of the fast acquisition capability of the AH503 and AH504, while overcoming the droop rate problems related to very small hold capacitors.

In this circuit, when the output of the AH503/AH504 exceeds the input, the AH503/AH504 is in the process of acquiring a pulse, although it may not have attained its full value because of internal delays. The LM311 comparator then triggers the LM555 delay. The LM555 switches the LF398 sample and hold to a sampling mode and switches back to a hold mode after the appropriate delay. Thus, C_{x2} can be made large, for low overall droop rate, while C_{x1} can be made small for minimum acquisition time.

Figure 7 shows the timing for this circuit. The width of the pulse from the LM355 needs to be calculated based on the acquisition time of the LF398, which is determined by C_{x2}.

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