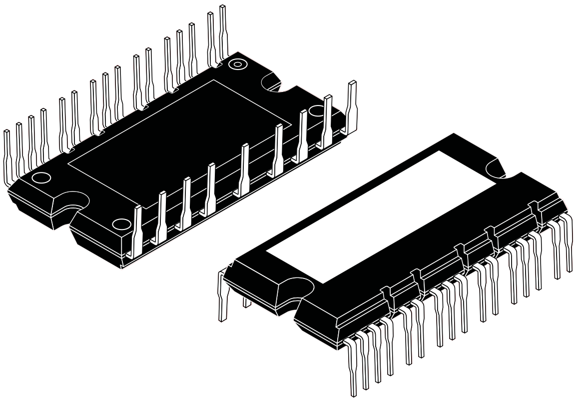
STGIPS10K60A

600 V - 10 A - SDIP-25L molded IGBT intelligent power module

Preliminary data

Features

- 600 V, 10 A 3-phase IGBT inverter bridge including control ICs for gate driving and free-wheeling diodes
- 3.3 V, 5 V, 15 V CMOS/TTL inputs comparators with hysteresis and pull down
- Internal bootstrap diode
- Dead time and interlocking function
- 5 kΩ NTC thermistor for temperature control
- $V_{CE(sat)}$ negative temperature coefficient
- Short-circuit rugged IGBT
- Under-voltage lockout
- DBC fully isolated package
- Isolation rating of 2500 Vrms/min.



SDIP-25L molded

Applications

- 3-phase inverters for low power motor drives
- Home appliances, such as washing machines, refrigerators, air conditioners

Description

The new intelligent power module developed by STMicroelectronics provides a compact, high performance AC motor drive for a simple and rugged design. It mainly targets low power inverters for applications such as home appliances and air conditioners. It combines ST proprietary control ICs with the most advanced short-circuit rugged IGBT technology.

Table 1. Device summary

Order code	Marking	Package	Packaging
STGIPS10K60A	GIPS10K60A	SDIP-25L molded	Tube

This is preliminary information on a new product now in development or undergoing evaluation. Details are subject to change without notice.

Contents

1 Internal block diagram and pin configuration

Figure 1. Internal block diagram

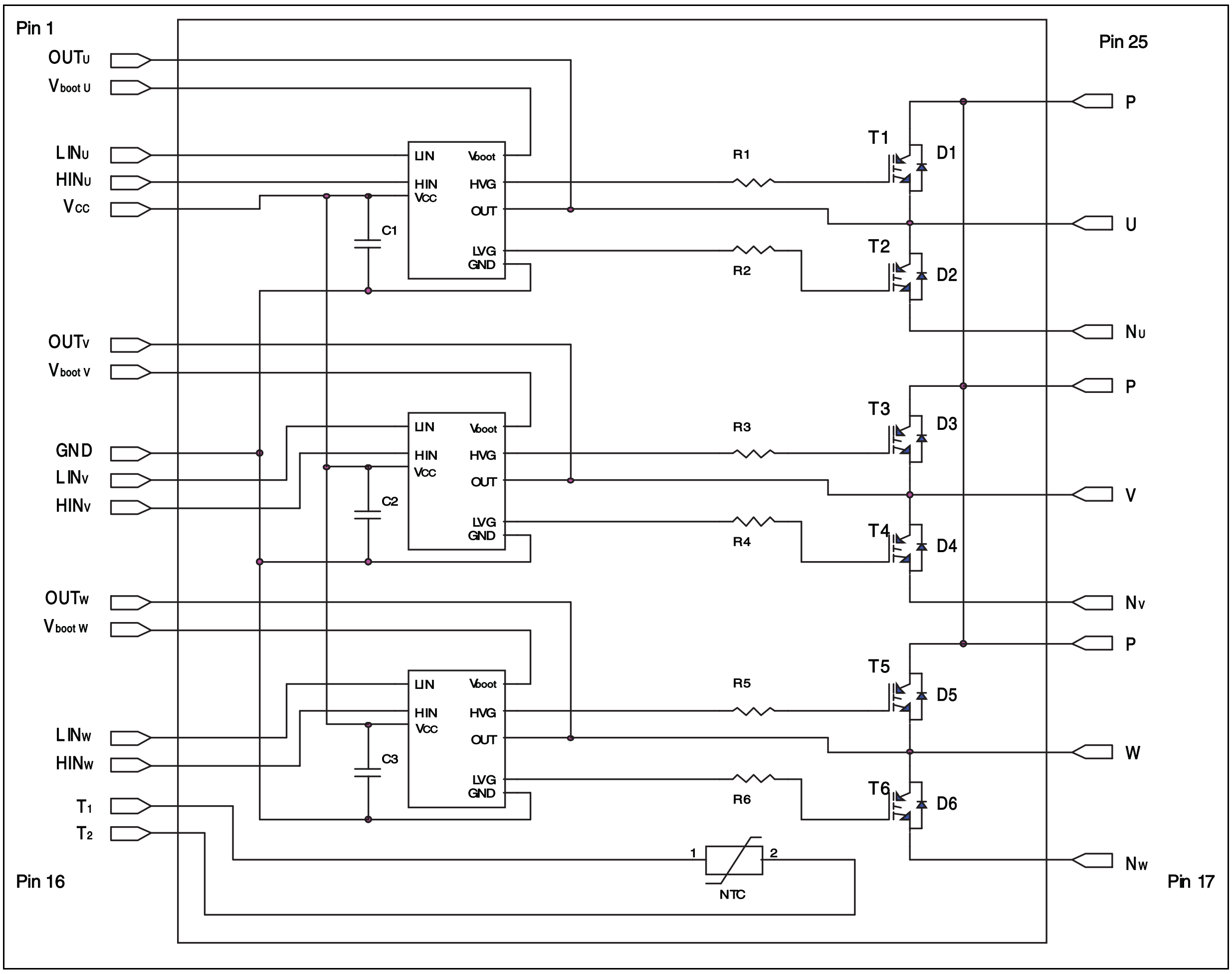
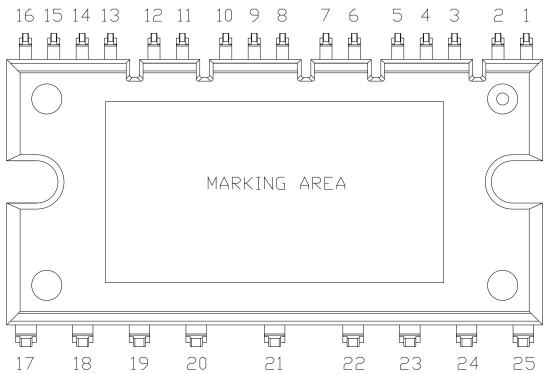


Table 2. Pin description

Pin	Symbol	Description
1	OUT_U	High side reference output for U phase
2	$V_{boot\ U}$	Bootstrap voltage for U phase
3	LIN_U	Low side logic input for U phase
4	HIN_U	High side logic input for U phase
5	V_{CC}	Low voltage power supply
6	OUT_V	High side reference output for V phase
7	$V_{boot\ V}$	Bootstrap voltage for V phase
8	GND	Ground
9	LIN_V	Low side logic input for V phase
10	HIN_V	High side logic input for V phase
11	OUT_W	High side reference output for W phase
12	$V_{boot\ W}$	Bootstrap voltage for W phase
13	LIN_W	Low side logic input for W phase
14	HIN_W	High side logic input for W phase
15	T_1	NTC thermistor terminal 1
16	T_2	NTC thermistor terminal 2
17	N_W	Negative DC input for W phase
18	W	W phase output
19	P	Positive DC input
20	N_V	Negative DC input for V phase
21	V	V phase output
22	P	Positive DC input
23	N_U	Negative DC input for U phase
24	U	U phase output
25	P	Positive DC input

Figure 2. Pin layout (bottom view)



2 Electrical ratings

Table 3. Absolute maximum ratings: inverter part

Symbol	Parameter	Value	Unit
V_{PN}	Supply voltage applied between P - N_U, N_V, N_W	450	V
$V_{PN(surge)}$	Supply voltage (surge) applied between P - N_U, N_V, N_W	500	V
V_{CES}	Collector emitter voltage (V_{IN}(1) = 0)	600	V
$\pm I_C$(2)	Each IGBT continuous collector current at T_C = 25°C	10	A
$\pm I_{CP}$(3)	Each IGBT pulsed collector current	20	A
P_{TOT}	Each IGBT total dissipation at T_C = 25°C	26	W
t_{scw}	Short-circuit withstand time, V_{CE} = 0.5 $V_{(BR)CES}$ T_j = 125 °C, V_{CC} = V_{boot}= 15 V, V_{IN}(1)= 5 V	5	µs

1. Applied between HIN_i, LIN_i and GND for i = U, V, W
2. Calculated according to the iterative formula:

$$I_C(T_C) = \frac{T_{j(max)} - T_C}{R_{thj-c} \times V_{CE(sat)(max)}(T_{j(max)}, I_C(T_C))}$$

3. Pulse width limited by max junction temperature

Table 4. Absolute maximum ratings: control part

Symbol	Parameter	Value	Unit
V_{OUT}	Output voltage applied between OUT_U, OUT_V, OUT_W - GND	-3 to V_{boot} -18	V
V_{CC}	Low voltage power supply	-0.3 to +18	V
V_{boot}	Bootstrap voltage applied between $V_{boot\ i}$ - OUT_i for i = U, V, W	-1 to 618	V
V_{IN}	Logic input voltage applied between HIN_i, LIN_i and GND for i = U, V, W	-0.3 to V_{CC}+0.3	V
dV_{out}/dt	Allowed output slew rate	50	V/ns

Table 5. Absolute maximum ratings: total system

Symbol	Parameter	Value	Unit
V_{OUT}	Output voltage applied between U, V, W - GND	450	V
V_{ISO}	Isolation withstand voltage applied between each pin and heatsink plate (AC voltage, t = 60sec.)	2500	V
T_j	Operating junction temperature	-40 to 125	°C

Table 6. Thermal data

Symbol	Parameter	Value	Unit
R_{thj-c}	Thermal resistance junction-case single IGBT	3.8	°C/W
	Thermal resistance junction-case single diode	5.5	°C/W

3 Electrical characteristics

(T_j = 25°C unless otherwise specified)

Table 7. Inverter part

Symbol	Parameter	Test conditions	Value			Unit
			Min.	Typ.	Max.	
$V_{CE(sat)}$	Collector-emitter saturation voltage	$V_{CC} = V_{boot}$ = 15 V, V_{IN}(1)= 5 V, I_C = 5 A	-	2.1	2.7	V
		$V_{CC} = V_{boot}$ = 15 V, V_{IN}(1)= 5 V, I_C = 5 A, T_j = 125 °C	-	1.8		
I_{CES}	Collector-cut off current (V_{IN}(1)=0)	V_{CE} = 600 V	-		100	µA
V_F	Diode forward voltage	V_{IN}(1) = 0, I_C = 5 A	-	1.4		V
High side inductive load						
t_{on}	Turn-on time	V_{PN} = 300 V, $V_{CC} = V_{boot}$ = 15 V, V_{IN}(1)= 0 ↔ 5 V, I_C = 5 A (see *Figure 6*)	-	320	-	ns
$t_{c(on)}$	Crossover time (on)		-	70	-	
t_{off}	Turn-off time		-	430	-	
$t_{c(off)}$	Crossover time (off)		-	135	-	
t_{rr}	Reverse recovery time		-	TBD	-	
E_{on}	Turn-on switching losses		-	TBD	-	µJ
E_{off}	Turn-off switching losses		-		-	
Low side inductive load						
t_{on}	Turn-on time	V_{PN} = 300 V, $V_{CC} = V_{boot}$ = 15 V, V_{IN}(1)= 0 ↔ 5 V, I_C = 5 A (see *Figure 6*)	-	310	-	ns
$t_{c(on)}$	Crossover time (on)		-	70	-	
t_{off}	Turn-off time		-	470	-	
$t_{c(off)}$	Crossover time (off)		-	135	-	
t_{rr}	Reverse recovery time		-	TBD	-	
E_{on}	Turn-on switching losses		-	TBD	-	µJ
E_{off}	Turn-off switching losses		-		-	

1. Applied between HIN_i, LIN_i and GND for i = U, V, W

Note: t_{ON} and t_{OFF} include the propagation delay time of the internal drive. $t_{C(ON)}$ and $t_{C(OFF)}$ are the switching time of IGBT itself under the internally given gate driving condition

3.1 Control part

Table 8. Low supply voltage

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{CCth1}	Under voltage turn on threshold		9.1	9.6	10.1	V
V_{CCth2}	Under voltage turn off threshold		7.9	8.3	8.8	V
V_{CChys}	Under voltage hystereses		0.9			V
I_{qccu}	Under voltage quiescent supply current	$V_{CC} < 9$ V		0.75	1.2	mA
I_{qcc}	Quiescent current	$V_{CC} = 15$ V		1	1.5	mA
$R_{DS(on)}$ (1)	Bootstrap driver on resistance	$V_{CC} > 12.5$ V		125		Ω

1. $R_{DS(on)}$ is tested in the following way:

$$R_{DS(on)} = \frac{(V_{CC} - V_{boot1}) - (V_{CC} - V_{boot2})}{I_{boot1}(V_{CC},\ V_{boot1}) - I_{boot2}(V_{CC},\ V_{boot2})}$$

Table 9. Bootstrap supply

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{booth1}	Under voltage turn on threshold	-	8.5	9.5	10.5	V
V_{booth2}	Under voltage turn off threshold	-	7.2	8.3	9.2	V
$V_{boothys}$	Under voltage hystereses	-	0.9			V
I_{qboot}	Quiescent current	-			250	µA

Table 10. Logic input

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{il}	Low level logic input voltage				1.1	V
V_{ih}	High level logic input voltage		1.8			V
I_{il}	Low level logic input current	V_{IN} (1) = 0	-1			µA
I_{ih}	High level logic input current	V_{IN} (1) = 15 V		20	70	µA
Dt	Dead time	see *Figure 7*		320		ns

1. Applied between HIN_i, LIN_i and GND for i = U, V, W

Table 11. NTC thermistor

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit.
R_{25}	Resistance	$T_C = 25°C$		5		kΩ
R_{125}	Resistance	$T_C = 125°C$		300		Ω
B	B-constant	$T_C = 25°C$		3435		k
T	Operating temperature		-40		125	°C

Equation 1: resistance variation vs temperature

$$R(T) = R_{25} \cdot e^{B\left(\frac{1}{T} - \frac{1}{298k}\right)}$$

Figure 3. NTC resistance vs temperature

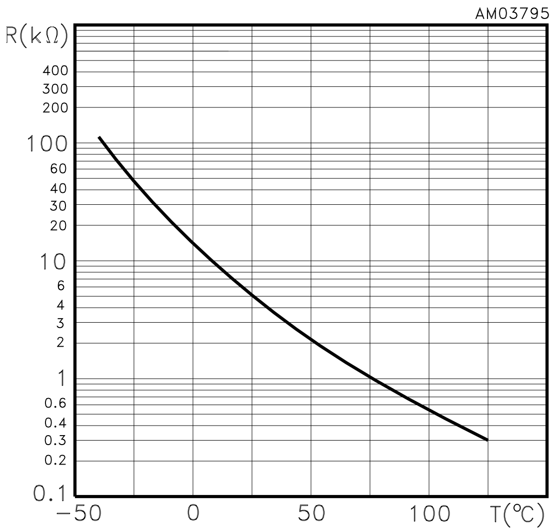


Figure 4. Maximum I_C current vs. switching frequency

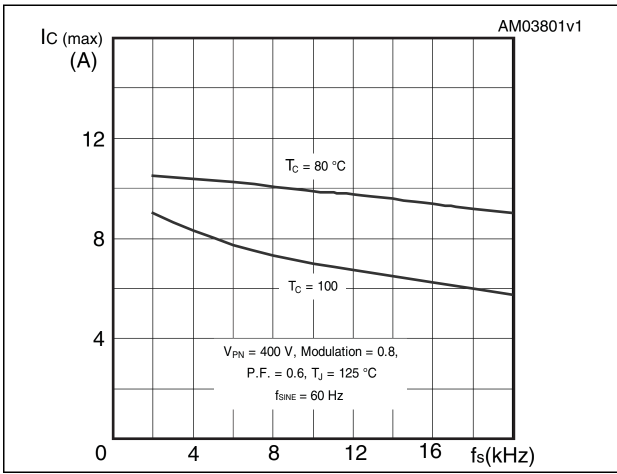


Figure 5. Maximum I_C current vs. f_{SINE}

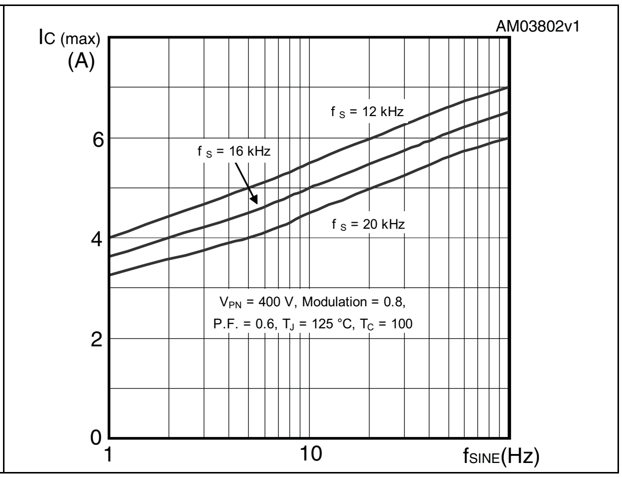


Figure 6. Switching time definition

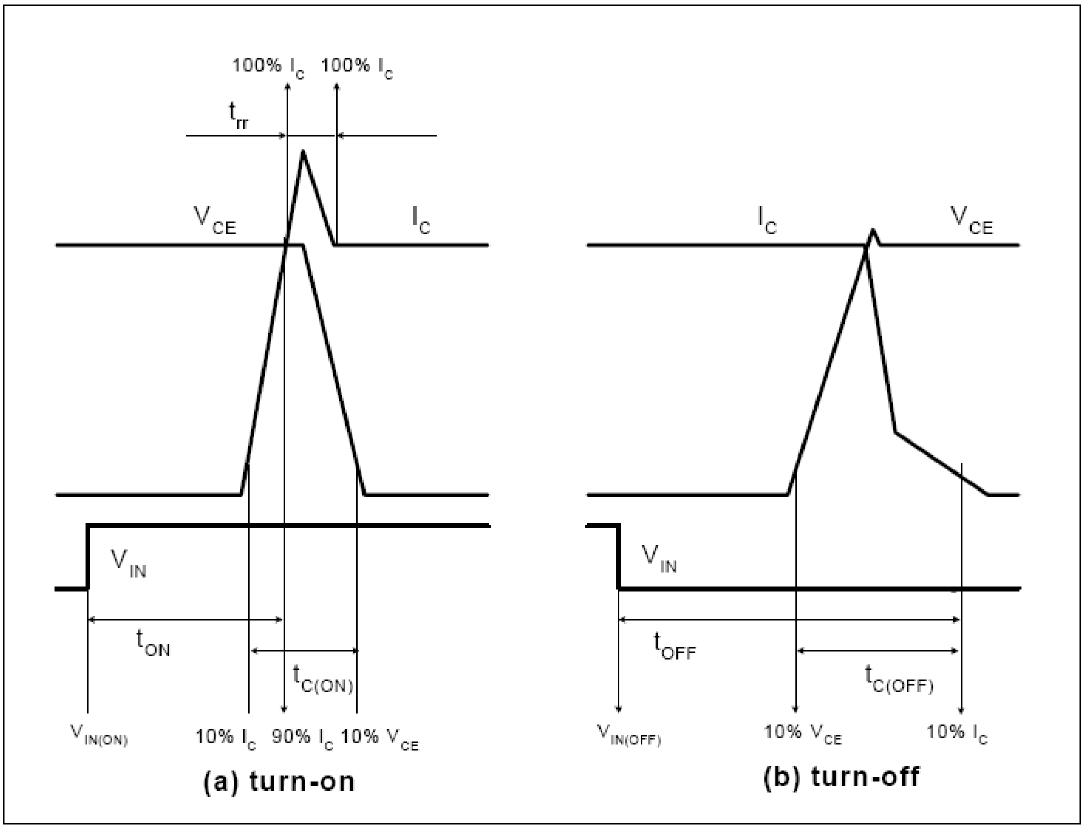
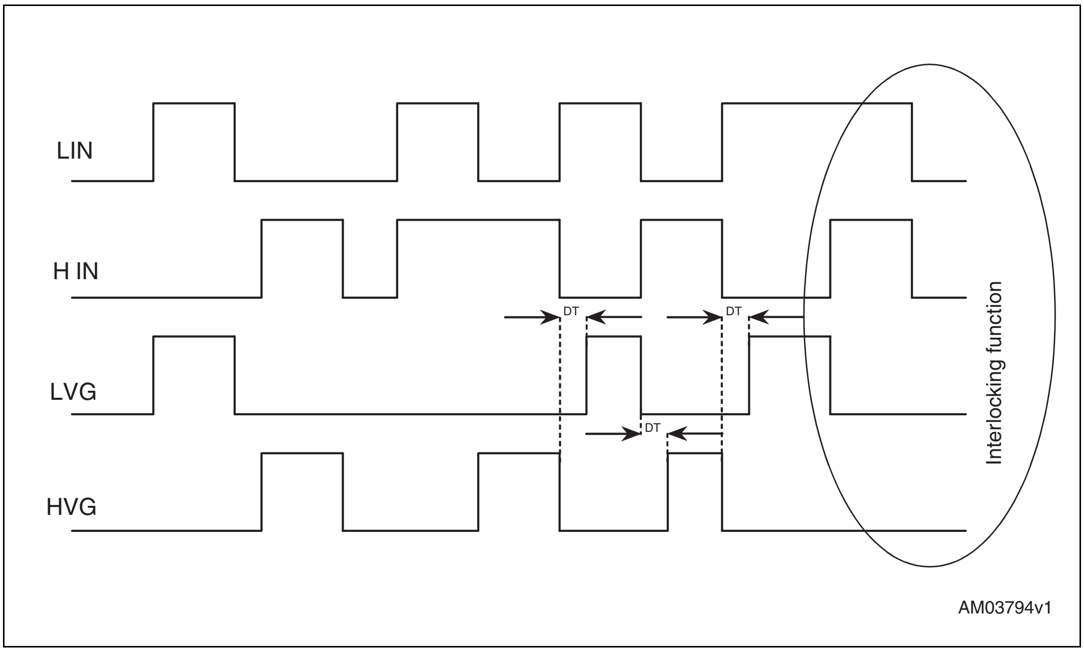
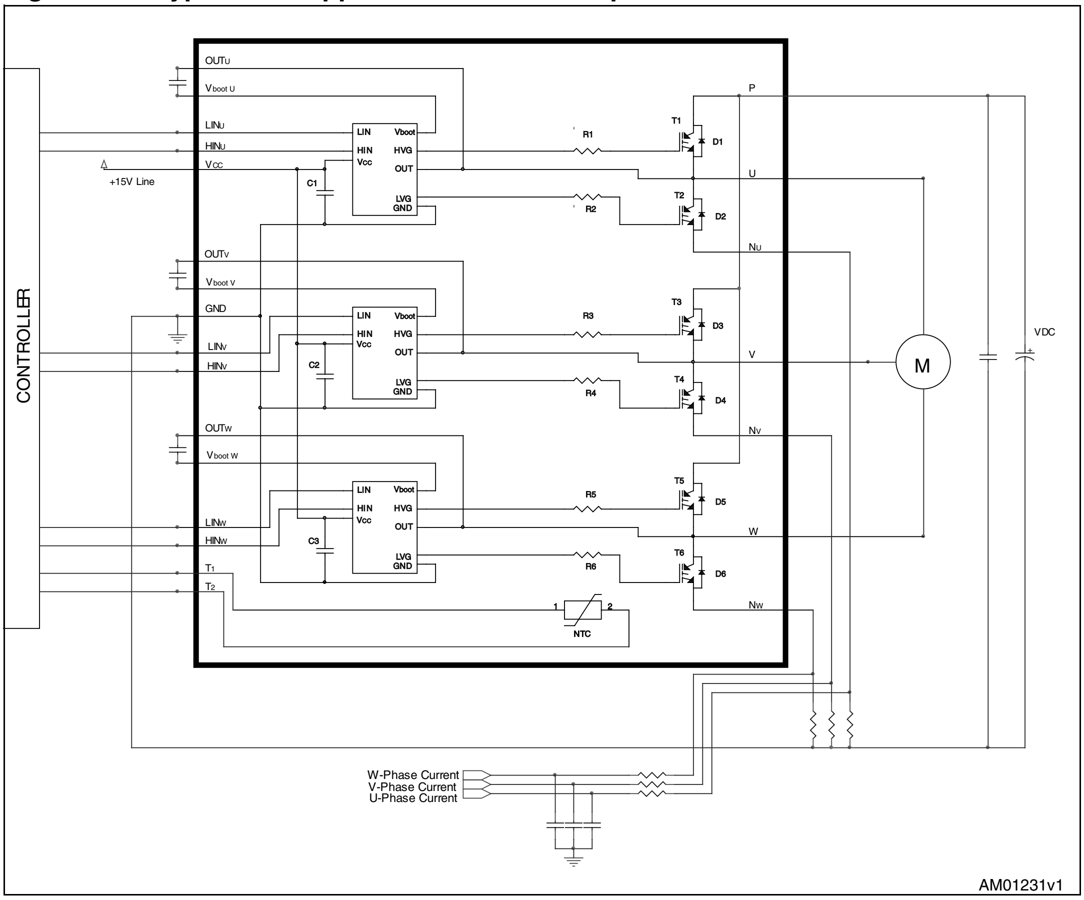


Figure 7. Dead time waveforms definition



4 Applications information

Figure 8. Typical IPM application circuit example



4.1 Recommendations

- To prevent the input signals oscillation, the wiring of each input should be as short as possible.
- By integrating an application specific type HVIC inside the module, direct coupling to MCU terminals without any opto-coupler is possible.
- Each capacitor should be located as nearby the pins of IPM as possible.
- Low inductance shunt resistors should be used for phase leg current sensing.
- Electrolytic bus capacitors should be mounted as close to the module bus terminals as possible. Additional high frequency ceramic capacitor mounted close to the module pins will further improve performance.

5 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

Table 12. SDIP-25L molded package mechanical data

Dim	(mm)		
	Min	Typ	Max
A	44	-	44.8
A1	0.95	-	1.75
A2	1.2	-	2
A3	39	-	39.8
B	21.6	-	22.4
B1	11.45	-	12.25
B2	24.83	-	25.63
C	5	-	5.8
C1	6.4	-	7.4
C2	11.1	-	12.1
e	1.95	-	2.75
e1	3.2	-	4
e2	4.3	-	5.1
e3	6.1	-	6.9
F	0.8	-	1.2
F1	0.3	-	0.7
R	3	-	4
T	0.4	-	0.7

Figure 9. SDIP-25L molded package mechanical data

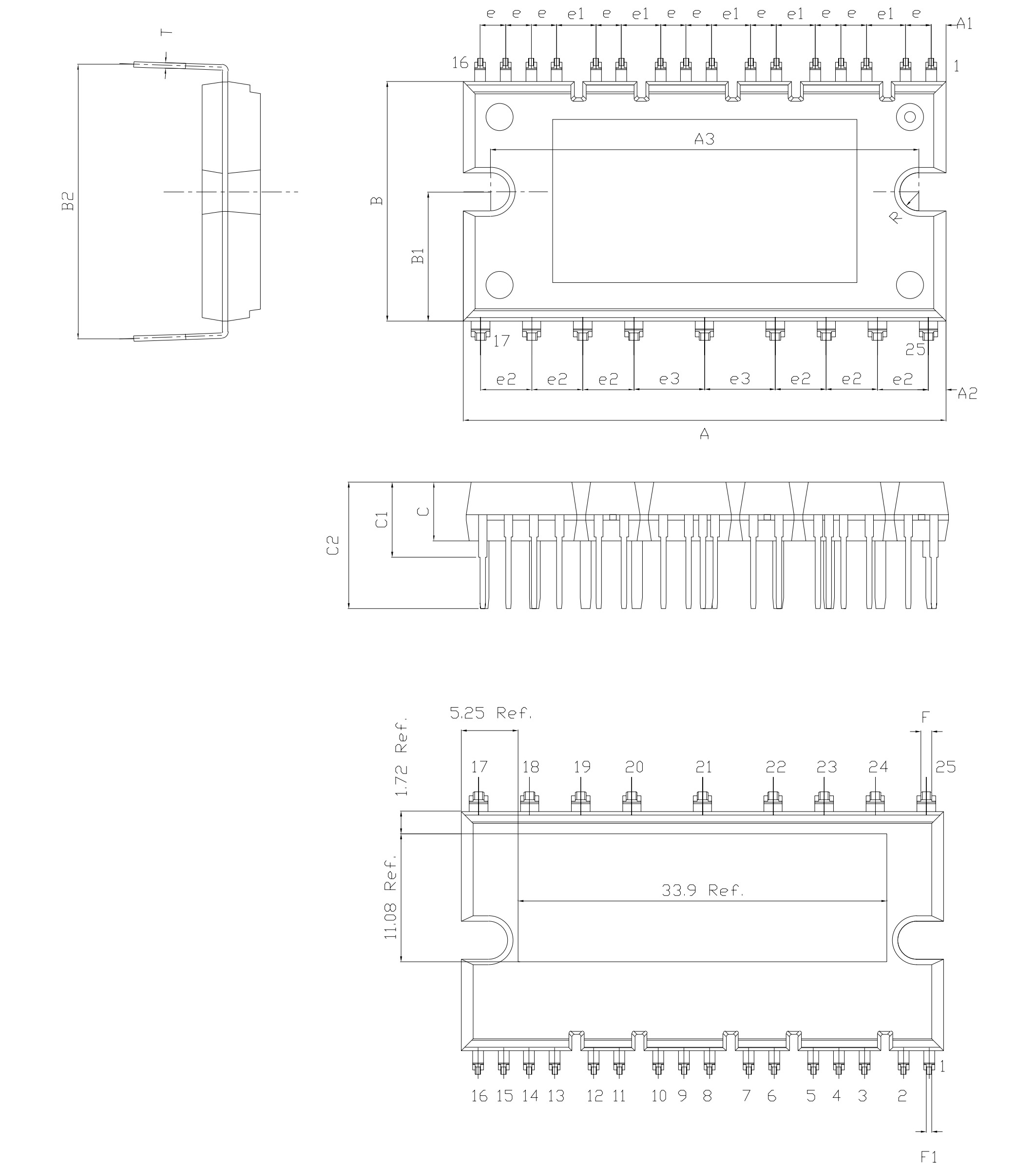


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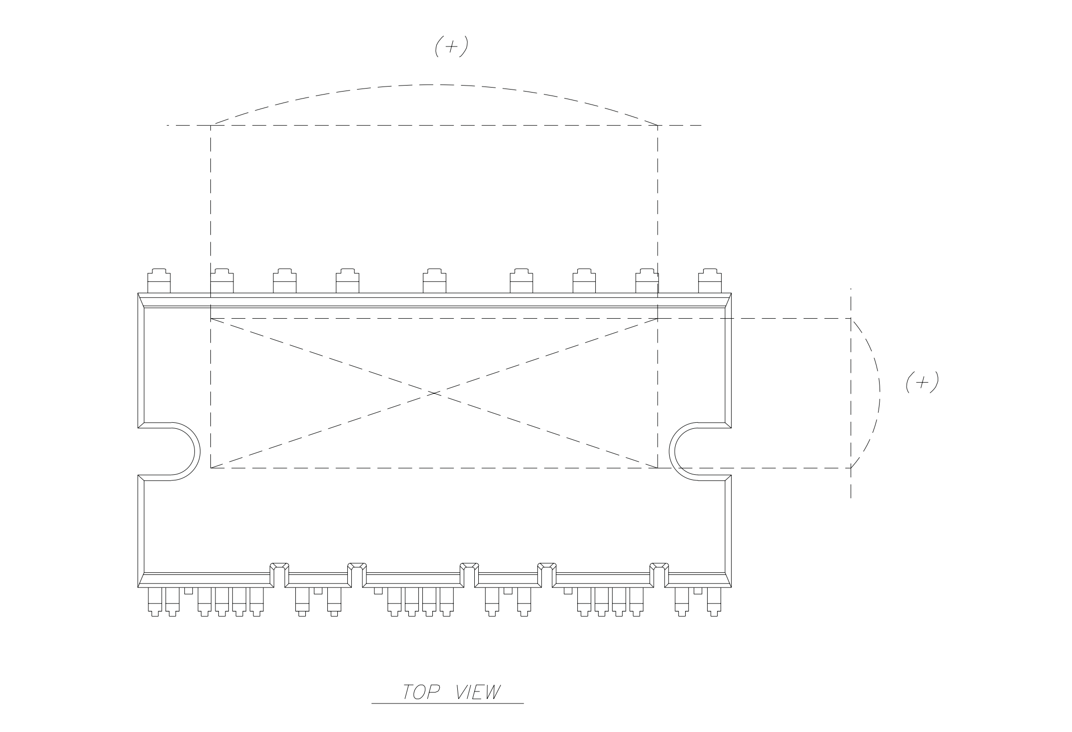
Table 13. Mechanical characteristics and ratings

Parameter	Limits			Unit
	Min.	Typ.	Max.	
Mounting torque (M3 screw)	0.59	--	0.78	N•m
Device flatness	0	--	100	µm
Weight	--	13	--	g

Figure 10. Flatness measurement position



6 Revision history

Table 14. Document revision history

Date	Revision	Changes
16-Apr-2009	1	Initial release
11-May-2009	2	Added *Figure 4: Maximum IC current vs. switching frequency* and *Figure 5: Maximum IC current vs. fSINE*