Preliminary

40-common x 128RGB-Segment, in 4096-Color 4096-Color STN LCD DRIVER

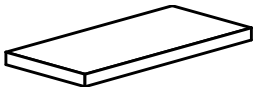
■ GENERAL DESCRIPTION

The **NJU6820** is a STN LCD driver with 40-common x 128RGB-segment in 4096-color. It consists of 384(128xRGB)-segment segment, 40-common drivers, serial and parallel MPU interface circuits, internal power supply circuits, gradation palettes and 61,440-bit for graphic display data RAM.

Each segment driver outputs 16-gradation level out of 32-gradation level of gradation palette.

Since the **NJU6820** provides a low operating voltage of 1.7V and low operating current, it is ideally suited for battery-powered handheld applications.

■ PACKAGE OUTLINE

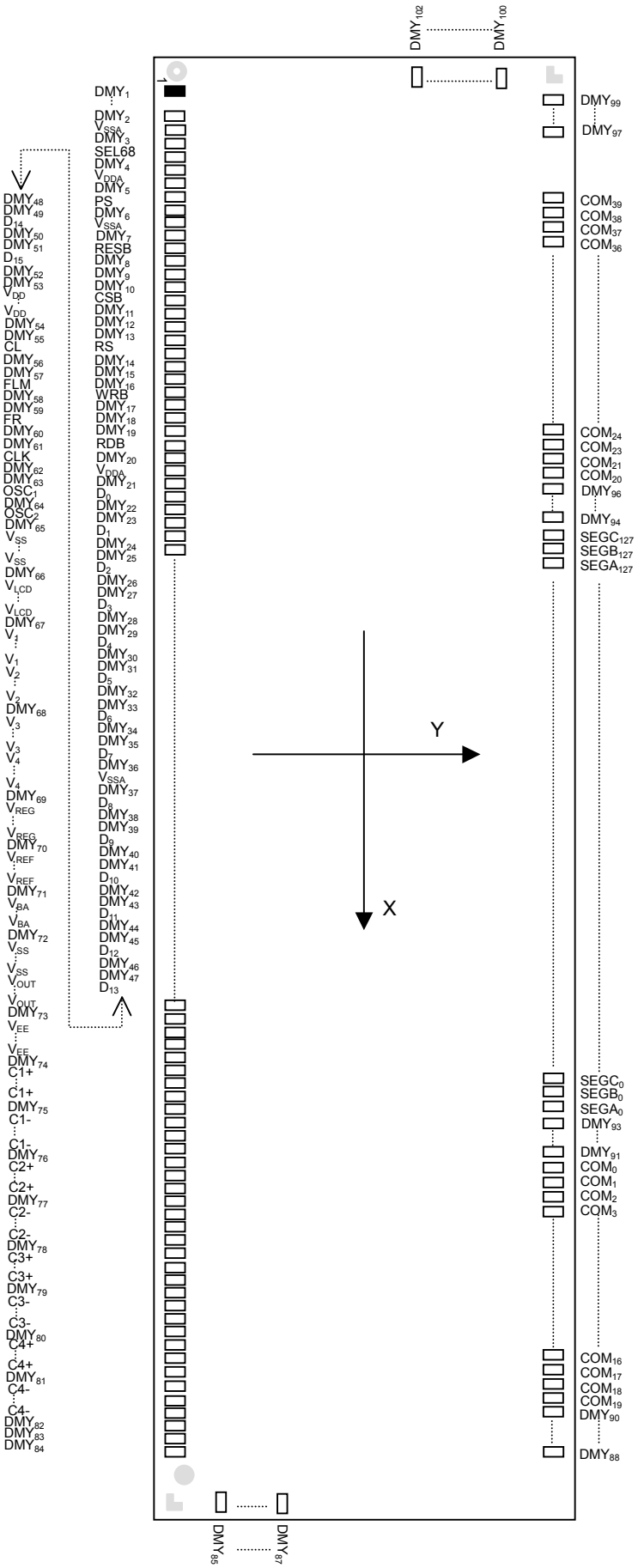


NJU6820CJ

■ FEATURES

- 4096-color STN LCD driver
- LCD drivers 40 commons, 128 RGB-segments,
- Display data RAM (DDRAM) 61,440-bit for graphic display
- Color display mode 16 gradation level out of 32 gradation level of gradation palette
- Black & white display mode 40 x 384 pixels in 16 gradation level or 40 x 384 pixels in B&W display
- 256-color driving mode
- 8/16bit Parallel interface directly-connective to 68/80 series MPU
- Programmable 8- or 16-bit data bus length for display data
- 3-/4-line Serial interface
- Programmable duty and bias ratios
- Programmable internal voltage booster (maximum 5-times)
- Programmable contrast control using 128-step EVR
- Various instructions
  Display data read/write, Display ON/OFF, Reverse display ON/OFF, All pixels ON/OFF, Column address, row address, N-line inversion, Initial display line, Initial COM line, Read-modify-write, Gradation mode control, Increment control, Data bus length, Discharge ON/OFF, Duty cycle ratio, LCD bias ratio, Boost level, EVR control, Power save ON/OFF, etc
- Internal voltage regulator
- Low operating current
- Low logic supply voltage 1.7V to 3.3V
- LCD driving supply voltage 5.0V to 18.0V
- C-MOS technology
- Rectangle out look for COG
- Package Bumped chip / TCP

■ PAD LOCATION

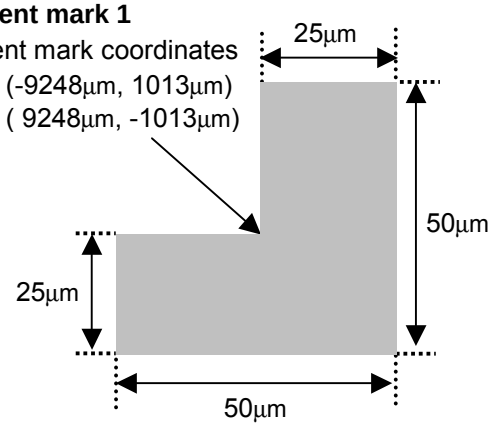


Alignment mark 1

Alignment mark coordinates

(-9248μm, 1013μm)

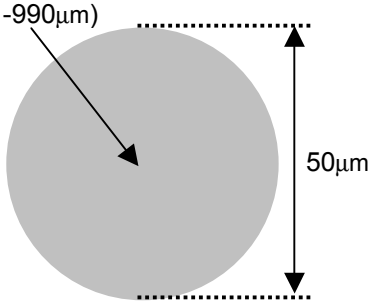
(9248μm, -1013μm)



Alignment mark 2

Alignment mark coordinates

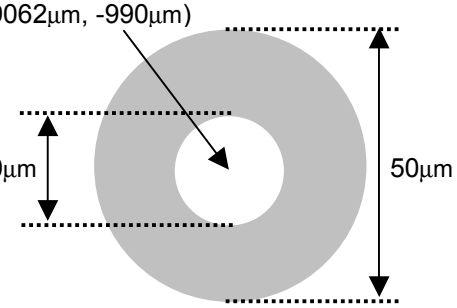
(9062μm, -990μm)



Alignment mark 3

Alignment mark coordinates

(-9062μm, -990μm)



Chip Center	:X=0um, Y=0um
Chip Size	:X=18.86mm, Y= 2.39mm
Chip Thickness	:625um ± 25um
Bump Pitch	:42um(Min)
Bump Size	:24um x 140um
Bump hight	:17.5um(Typ)
Bump Material	:Au

■ PAD COORDINATES 1

Chip Size 18860μm x 2390μm (Chip Center 0μm x 0μm)

PAD No.	Terminal	X(μm)	Y(μm)	PAD No.	Terminal	X(μm)	Y(μm)	PAD No.	Terminal	X(μm)	Y(μm)
1	DMY_0	-8967	-990	51	DMY_{24}	-6699	-990	101	DMY_{48}	-3507	-990
2	DMY_1	-8925	-990	52	DMY_{25}	-6573	-990	102	DMY_{49}	-3381	-990
3	DMY_2	-8883	-990	53	D_2	-6531	-990	103	D_{14}	-3339	-990
4	V_{SSA}	-8841	-990	54	D_2	-6489	-990	104	D_{14}	-3297	-990
5	V_{SSA}	-8799	-990	55	DMY_{26}	-6447	-990	105	DMY_{50}	-3255	-990
6	DMY_3	-8757	-990	56	DMY_{27}	-6321	-990	106	DMY_{51}	-3129	-990
7	SEL68	-8715	-990	57	D_3	-6279	-990	107	D_{15}	-3087	-990
8	SEL68	-8673	-990	58	D_3	-6237	-990	108	D_{15}	-3045	-990
9	DMY_4	-8631	-990	59	DMY_{28}	-6195	-990	109	DMY_{52}	-3003	-990
10	V_{DDA}	-8589	-990	60	DMY_{29}	-6069	-990	110	DMY_{53}	-2877	-990
11	V_{DDA}	-8547	-990	61	D_4	-6027	-990	111	V_{DD}	-2835	-990
12	DMY_5	-8505	-990	62	D_4	-5985	-990	112	V_{DD}	-2793	-990
13	PS	-8463	-990	63	DMY_{30}	-5943	-990	113	V_{DD}	-2751	-990
14	PS	-8421	-990	64	DMY_{31}	-5817	-990	114	V_{DD}	-2709	-990
15	DMY_6	-8379	-990	65	D_5	-5775	-990	115	V_{DD}	-2667	-990
16	V_{SSA}	-8337	-990	66	D_5	-5733	-990	116	V_{DD}	-2625	-990
17	V_{SSA}	-8295	-990	67	DMY_{32}	-5691	-990	117	V_{DD}	-2583	-990
18	DMY_7	-8253	-990	68	DMY_{33}	-5565	-990	118	V_{DD}	-2541	-990
19	RESB	-8211	-990	69	D_6	-5523	-990	119	V_{DD}	-2499	-990
20	RESB	-8169	-990	70	D_6	-5481	-990	120	V_{DD}	-2457	-990
21	DMY_8	-8127	-990	71	DMY_{34}	-5439	-990	121	V_{DD}	-2415	-990
22	DMY_9	-8085	-990	72	DMY_{35}	-5313	-990	122	DMY_{54}	-2289	-990
23	DMY_{10}	-8043	-990	73	D_7	-5271	-990	123	DMY_{55}	-2163	-990
24	CSb	-8001	-990	74	D_7	-5229	-990	124	CL	-2121	-990
25	CSb	-7959	-990	75	DMY_{36}	-5187	-990	125	CL	-2079	-990
26	DMY_{11}	-7917	-990	76	V_{SSA}	-5061	-990	126	DMY_{56}	-2037	-990
27	DMY_{12}	-7875	-990	77	V_{SSA}	-5019	-990	127	DMY_{57}	-1911	-990
28	DMY_{13}	-7833	-990	78	DMY_{37}	-4893	-990	128	FLM	-1869	-990
29	RS	-7791	-990	79	D_8	-4851	-990	129	FLM	-1827	-990
30	RS	-7749	-990	80	D_8	-4809	-990	130	DMY_{58}	-1785	-990
31	DMY_{14}	-7707	-990	81	DMY_{38}	-4767	-990	131	DMY_{59}	-1659	-990
32	DMY_{15}	-7665	-990	82	DMY_{39}	-4641	-990	132	FR	-1617	-990
33	DMY_{16}	-7623	-990	83	D_9	-4599	-990	133	FR	-1575	-990
34	WRb	-7581	-990	84	D_9	-4557	-990	134	DMY_{60}	-1533	-990
35	WRb	-7539	-990	85	DMY_{40}	-4515	-990	135	DMY_{61}	-1407	-990
36	DMY_{17}	-7497	-990	86	DMY_{41}	-4389	-990	136	CLK	-1365	-990
37	DMY_{18}	-7455	-990	87	D_{10}	-4347	-990	137	CLK	-1323	-990
38	DMY_{19}	-7413	-990	88	D_{10}	-4305	-990	138	DMY_{62}	-1281	-990
39	RDb	-7371	-990	89	DMY_{42}	-4263	-990	139	DMY_{63}	-1155	-990
40	RDb	-7329	-990	90	DMY_{43}	-4137	-990	140	OSC_1	-1113	-990
41	DMY_{20}	-7287	-990	91	D_{11}	-4095	-990	141	OSC_1	-1071	-990
42	V_{DDA}	-7245	-990	92	D_{11}	-4053	-990	142	DMY_{64}	-1029	-990
43	V_{DDA}	-7203	-990	93	DMY_{44}	-4011	-990	143	OSC_2	-903	-990
44	DMY_{21}	-7077	-990	94	DMY_{45}	-3885	-990	144	OSC_2	-861	-990
45	D_0	-7035	-990	95	D_{12}	-3843	-990	145	DMY_{65}	-735	-990
46	D_0	-6993	-990	96	D_{12}	-3801	-990	146	V_{SS}	-693	-990
47	DMY_{22}	-6951	-990	97	DMY_{46}	-3759	-990	147	V_{SS}	-651	-990
48	DMY_{23}	-6825	-990	98	DMY_{47}	-3633	-990	148	V_{SS}	-609	-990
49	D_1	-6783	-990	99	D_{13}	-3591	-990	149	V_{SS}	-567	-990
50	D_1	-6741	-990	100	D_{13}	-3549	-990	150	V_{SS}	-525	-990

■ PAD COORDINATES 2

Chip Size 18860μm x 2390μm (Chip Center 0μm x 0μm)

PAD No.	Terminal	X(μm)	Y(μm)	PAD No.	Terminal	X(μm)	Y(μm)	PAD No.	Terminal	X(μm)	Y(μm)
151	V_{SS}	-483	-990	201	V_4	1953	-990	251	V_{OUT}	4179	-990
152	V_{SS}	-441	-990	202	V_4	1995	-990	252	V_{OUT}	4221	-990
153	V_{SS}	-399	-990	203	V_4	2037	-990	253	V_{OUT}	4263	-990
154	V_{SS}	-357	-990	204	V_4	2079	-990	254	V_{OUT}	4305	-990
155	V_{SS}	-315	-990	205	DMY_{69}	2121	-990	255	V_{OUT}	4347	-990
156	V_{SS}	-273	-990	206	V_{REG}	2163	-990	256	V_{OUT}	4389	-990
157	DMY_{66}	-147	-990	207	V_{REG}	2205	-990	257	V_{OUT}	4431	-990
158	V_{LCD}	-21	-990	208	V_{REG}	2247	-990	258	V_{OUT}	4473	-990
159	V_{LCD}	21	-990	209	V_{REG}	2289	-990	259	DMY_{73}	4641	-990
160	V_{LCD}	63	-990	210	V_{REG}	2331	-990	260	V_{EE}	4683	-990
161	V_{LCD}	105	-990	211	V_{REG}	2373	-990	261	V_{EE}	4725	-990
162	V_{LCD}	147	-990	212	V_{REG}	2415	-990	262	V_{EE}	4767	-990
163	V_{LCD}	189	-990	213	V_{REG}	2457	-990	263	V_{EE}	4809	-990
164	V_{LCD}	231	-990	214	V_{REG}	2499	-990	264	V_{EE}	4851	-990
165	V_{LCD}	273	-990	215	V_{REG}	2541	-990	265	V_{EE}	4893	-990
166	V_{LCD}	315	-990	216	DMY_{70}	2583	-990	266	V_{EE}	4935	-990
167	DMY_{67}	357	-990	217	V_{REF}	2625	-990	267	V_{EE}	4977	-990
168	V_1	399	-990	218	V_{REF}	2667	-990	268	V_{EE}	5019	-990
169	V_1	441	-990	219	V_{REF}	2709	-990	269	V_{EE}	5061	-990
170	V_1	483	-990	220	V_{REF}	2751	-990	270	DMY_{74}	5187	-990
171	V_1	525	-990	221	V_{REF}	2793	-990	271	C1+	5229	-990
172	V_1	567	-990	222	V_{REF}	2835	-990	272	C1+	5271	-990
173	V_1	609	-990	223	V_{REF}	2877	-990	273	C1+	5313	-990
174	V_1	651	-990	224	V_{REF}	2919	-990	274	C1+	5355	-990
175	V_1	693	-990	225	V_{REF}	2961	-990	275	C1+	5397	-990
176	V_1	735	-990	226	V_{REF}	3003	-990	276	C1+	5439	-990
177	V_2	861	-990	227	DMY_{71}	3045	-990	277	C1+	5481	-990
178	V_2	903	-990	228	V_{BA}	3087	-990	278	C1+	5523	-990
179	V_2	945	-990	229	V_{BA}	3129	-990	279	C1+	5565	-990
180	V_2	987	-990	230	V_{BA}	3171	-990	280	C1+	5607	-990
181	V_2	1029	-990	231	V_{BA}	3213	-990	281	DMY_{75}	5649	-990
182	V_2	1071	-990	232	V_{BA}	3255	-990	282	C1-	5691	-990
183	V_2	1113	-990	233	V_{BA}	3297	-990	283	C1-	5733	-990
184	V_2	1155	-990	234	V_{BA}	3339	-990	284	C1-	5775	-990
185	V_2	1197	-990	235	V_{BA}	3381	-990	285	C1-	5817	-990
186	DMY_{68}	1239	-990	236	V_{BA}	3423	-990	286	C1-	5859	-990
187	V_3	1281	-990	237	V_{BA}	3465	-990	287	C1-	5901	-990
188	V_3	1323	-990	238	DMY_{72}	3507	-990	288	C1-	5943	-990
189	V_3	1365	-990	239	V_{SS}	3549	-990	289	C1-	5985	-990
190	V_3	1407	-990	240	V_{SS}	3591	-990	290	C1-	6027	-990
191	V_3	1449	-990	241	V_{SS}	3633	-990	291	C1-	6069	-990
192	V_3	1491	-990	242	V_{SS}	3675	-990	292	DMY_{76}	6111	-990
193	V_3	1533	-990	243	V_{SS}	3717	-990	293	C2+	6153	-990
194	V_3	1575	-990	244	V_{SS}	3759	-990	294	C2+	6195	-990
195	V_3	1617	-990	245	V_{SS}	3801	-990	295	C2+	6237	-990
196	V_4	1743	-990	246	V_{SS}	3843	-990	296	C2+	6279	-990
197	V_4	1785	-990	247	V_{SS}	3885	-990	297	C2+	6321	-990
198	V_4	1827	-990	248	V_{SS}	3927	-990	298	C2+	6363	-990
199	V_4	1869	-990	249	V_{OUT}	4095	-990	299	C2+	6405	-990
200	V_4	1911	-990	250	V_{OUT}	4137	-990	300	C2+	6447	-990

■ PAD COORDINATES 3

Chip Size 18860μm x 2390μm (Chip Center 0μm x 0μm)

PAD No.	Terminal	X(μm)	Y(μm)	PAD No.	Terminal	X(μm)	Y(μm)	PAD No.	Terminal	X(μm)	Y(μm)
301	C2+	6489	-990	351	C4-	8589	-990	401	$SEGA_3$	7665	990
302	C2+	6531	-990	352	C4-	8631	-990	402	$SEGB_3$	7623	990
303	DMY_{77}	6573	-990	353	C4-	8673	-990	403	$SEGC_3$	7581	990
304	C2-	6615	-990	354	C4-	8715	-990	404	$SEGA_4$	7539	990
305	C2-	6657	-990	355	C4-	8757	-990	405	$SEGB_4$	7497	990
306	C2-	6699	-990	356	C4-	8799	-990	406	$SEGC_4$	7455	990
307	C2-	6741	-990	357	C4-	8841	-990	407	$SEGA_5$	7413	990
308	C2-	6783	-990	358	DMY_{82}	8883	-990	408	$SEGB_5$	7371	990
309	C2-	6825	-990	359	DMY_{83}	8925	-990	409	$SEGC_5$	7329	990
310	C2-	6867	-990	360	DMY_{84}	8967	-990	410	$SEGA_6$	7287	990
311	C2-	6909	-990	361	DMY_{85}	9225	-910	411	$SEGB_6$	7245	990
312	C2-	6951	-990	362	DMY_{86}	9225	-868	412	$SEGC_6$	7203	990
313	C2-	6993	-990	363	DMY_{86}	9225	-826	413	$SEGA_7$	7161	990
314	DMY_{78}	7035	-990	364	DMY_{86}	9225	-784	414	$SEGB_7$	7119	990
315	C3+	7077	-990	365	DMY_{87}	9225	-742	415	$SEGC_7$	7077	990
316	C3+	7119	-990	366	DMY_{88}	9135	990	416	$SEGA_8$	7035	990
317	C3+	7161	-990	367	DMY_{89}	9093	990	417	$SEGB_8$	6993	990
318	C3+	7203	-990	368	DMY_{90}	9051	990	418	$SEGC_8$	6951	990
319	C3+	7245	-990	369	COM_{19}	9009	990	419	$SEGA_9$	6909	990
320	C3+	7287	-990	370	COM_{18}	8967	990	420	$SEGB_9$	6867	990
321	C3+	7329	-990	371	COM_{17}	8925	990	421	$SEGC_9$	6825	990
322	C3+	7371	-990	372	COM_{16}	8883	990	422	$SEGA_{10}$	6783	990
323	C3+	7413	-990	373	COM_{15}	8841	990	423	$SEGB_{10}$	6741	990
324	C3+	7455	-990	374	COM_{14}	8799	990	424	$SEGC_{10}$	6699	990
325	DMY_{79}	7497	-990	375	COM_{13}	8757	990	425	$SEGA_{11}$	6657	990
326	C3-	7539	-990	376	COM_{12}	8715	990	426	$SEGB_{11}$	6615	990
327	C3-	7581	-990	377	COM_{11}	8673	990	427	$SEGC_{11}$	6573	990
328	C3-	7623	-990	378	COM_{10}	8631	990	428	$SEGA_{12}$	6531	990
329	C3-	7665	-990	379	COM_9	8589	990	429	$SEGB_{12}$	6489	990
330	C3-	7707	-990	380	COM_8	8547	990	430	$SEGC_{12}$	6447	990
331	C3-	7749	-990	381	COM_7	8505	990	431	$SEGA_{13}$	6405	990
332	C3-	7791	-990	382	COM_6	8463	990	432	$SEGB_{13}$	6363	990
333	C3-	7833	-990	383	COM_5	8421	990	433	$SEGC_{13}$	6321	990
334	C3-	7875	-990	384	COM_4	8379	990	434	$SEGA_{14}$	6279	990
335	C3-	7917	-990	385	COM_3	8337	990	435	$SEGB_{14}$	6237	990
336	DMY_{80}	7959	-990	386	COM_2	8295	990	436	$SEGC_{14}$	6195	990
337	C4+	8001	-990	387	COM_1	8253	990	437	$SEGA_{15}$	6153	990
338	C4+	8043	-990	388	COM_0	8211	990	438	$SEGB_{15}$	6111	990
339	C4+	8085	-990	389	DMY_{91}	8169	990	439	$SEGC_{15}$	6069	990
340	C4+	8127	-990	390	DMY_{92}	8127	990	440	$SEGA_{16}$	6027	990
341	C4+	8169	-990	391	DMY_{93}	8085	990	441	$SEGB_{16}$	5985	990
342	C4+	8211	-990	392	$SEGA_0$	8043	990	442	$SEGC_{16}$	5943	990
343	C4+	8253	-990	393	$SEGB_0$	8001	990	443	$SEGA_{17}$	5901	990
344	C4+	8295	-990	394	$SEGC_0$	7959	990	444	$SEGB_{17}$	5859	990
345	C4+	8337	-990	395	$SEGA_1$	7917	990	445	$SEGC_{17}$	5817	990
346	C4+	8379	-990	396	$SEGB_1$	7875	990	446	$SEGA_{18}$	5775	990
347	DMY_{81}	8421	-990	397	$SEGC_1$	7833	990	447	$SEGB_{18}$	5733	990
348	C4-	8463	-990	398	$SEGA_2$	7791	990	448	$SEGC_{18}$	5691	990
349	C4-	8505	-990	399	$SEGB_2$	7749	990	449	$SEGA_{19}$	5649	990
350	C4-	8547	-990	400	$SEGC_2$	7707	990	450	$SEGB_{19}$	5607	990

■ PAD COORDINATES 4

Chip Size 18860μm x 2390μm (Chip Center 0μm x 0μm)

PAD No.	Terminal	X(μm)	Y(μm)	PAD No.	Terminal	X(μm)	Y(μm)	PAD No.	Terminal	X(μm)	Y(μm)
451	$SEGC_{19}$	5565	990	501	$SEGB_{36}$	3465	990	551	$SEGA_{53}$	1365	990
452	$SEGA_{20}$	5523	990	502	$SEGC_{36}$	3423	990	552	$SEGB_{53}$	1323	990
453	$SEGB_{20}$	5481	990	503	$SEGA_{37}$	3381	990	553	$SEGC_{53}$	1281	990
454	$SEGC_{20}$	5439	990	504	$SEGB_{37}$	3339	990	554	$SEGA_{54}$	1239	990
455	$SEGA_{21}$	5397	990	505	$SEGC_{37}$	3297	990	555	$SEGB_{54}$	1197	990
456	$SEGB_{21}$	5355	990	506	$SEGA_{38}$	3255	990	556	$SEGC_{54}$	1155	990
457	$SEGC_{21}$	5313	990	507	$SEGB_{38}$	3213	990	557	$SEGA_{55}$	1113	990
458	$SEGA_{22}$	5271	990	508	$SEGC_{38}$	3171	990	558	$SEGB_{55}$	1071	990
459	$SEGB_{22}$	5229	990	509	$SEGA_{39}$	3129	990	559	$SEGC_{55}$	1029	990
460	$SEGC_{22}$	5187	990	510	$SEGB_{39}$	3087	990	560	$SEGA_{56}$	987	990
461	$SEGA_{23}$	5145	990	511	$SEGC_{39}$	3045	990	561	$SEGB_{56}$	945	990
462	$SEGB_{23}$	5103	990	512	$SEGA_{40}$	3003	990	562	$SEGC_{56}$	903	990
463	$SEGC_{23}$	5061	990	513	$SEGB_{40}$	2961	990	563	$SEGA_{57}$	861	990
464	$SEGA_{24}$	5019	990	514	$SEGC_{40}$	2919	990	564	$SEGB_{57}$	819	990
465	$SEGB_{24}$	4977	990	515	$SEGA_{41}$	2877	990	565	$SEGC_{57}$	777	990
466	$SEGC_{24}$	4935	990	516	$SEGB_{41}$	2835	990	566	$SEGA_{58}$	735	990
467	$SEGA_{25}$	4893	990	517	$SEGC_{41}$	2793	990	567	$SEGB_{58}$	693	990
468	$SEGB_{25}$	4851	990	518	$SEGA_{42}$	2751	990	568	$SEGC_{58}$	651	990
469	$SEGC_{25}$	4809	990	519	$SEGB_{42}$	2709	990	569	$SEGA_{59}$	609	990
470	$SEGA_{26}$	4767	990	520	$SEGC_{42}$	2667	990	570	$SEGB_{59}$	567	990
471	$SEGB_{26}$	4725	990	521	$SEGA_{43}$	2625	990	571	$SEGC_{59}$	525	990
472	$SEGC_{26}$	4683	990	522	$SEGB_{43}$	2583	990	572	$SEGA_{60}$	483	990
473	$SEGA_{27}$	4641	990	523	$SEGC_{43}$	2541	990	573	$SEGB_{60}$	441	990
474	$SEGB_{27}$	4599	990	524	$SEGA_{44}$	2499	990	574	$SEGC_{60}$	399	990
475	$SEGC_{27}$	4557	990	525	$SEGB_{44}$	2457	990	575	$SEGA_{61}$	357	990
476	$SEGA_{28}$	4515	990	526	$SEGC_{44}$	2415	990	576	$SEGB_{61}$	315	990
477	$SEGB_{28}$	4473	990	527	$SEGA_{45}$	2373	990	577	$SEGC_{61}$	273	990
478	$SEGC_{28}$	4431	990	528	$SEGB_{45}$	2331	990	578	$SEGA_{62}$	231	990
479	$SEGA_{29}$	4389	990	529	$SEGC_{45}$	2289	990	579	$SEGB_{62}$	189	990
480	$SEGB_{29}$	4347	990	530	$SEGA_{46}$	2247	990	580	$SEGC_{62}$	147	990
481	$SEGC_{29}$	4305	990	531	$SEGB_{46}$	2205	990	581	$SEGA_{63}$	105	990
482	$SEGA_{30}$	4263	990	532	$SEGC_{46}$	2163	990	582	$SEGB_{63}$	63	990
483	$SEGB_{30}$	4221	990	533	$SEGA_{47}$	2121	990	583	$SEGC_{63}$	21	990
484	$SEGC_{30}$	4179	990	534	$SEGB_{47}$	2079	990	584	$SEGA_{64}$	-21	990
485	$SEGA_{31}$	4137	990	535	$SEGC_{47}$	2037	990	585	$SEGB_{64}$	-63	990
486	$SEGB_{31}$	4095	990	536	$SEGA_{48}$	1995	990	586	$SEGC_{64}$	-105	990
487	$SEGC_{31}$	4053	990	537	$SEGB_{48}$	1953	990	587	$SEGA_{65}$	-147	990
488	$SEGA_{32}$	4011	990	538	$SEGC_{48}$	1911	990	588	$SEGB_{65}$	-189	990
489	$SEGB_{32}$	3969	990	539	$SEGA_{49}$	1869	990	589	$SEGC_{65}$	-231	990
490	$SEGC_{32}$	3927	990	540	$SEGB_{49}$	1827	990	590	$SEGA_{66}$	-273	990
491	$SEGA_{33}$	3885	990	541	$SEGC_{49}$	1785	990	591	$SEGB_{66}$	-315	990
492	$SEGB_{33}$	3843	990	542	$SEGA_{50}$	1743	990	592	$SEGC_{66}$	-357	990
493	$SEGC_{33}$	3801	990	543	$SEGB_{50}$	1701	990	593	$SEGA_{67}$	-399	990
494	$SEGA_{34}$	3759	990	544	$SEGC_{50}$	1659	990	594	$SEGB_{67}$	-441	990
495	$SEGB_{34}$	3717	990	545	$SEGA_{51}$	1617	990	595	$SEGC_{67}$	-483	990
496	$SEGC_{34}$	3675	990	546	$SEGB_{51}$	1575	990	596	$SEGA_{68}$	-525	990
497	$SEGA_{35}$	3633	990	547	$SEGC_{51}$	1533	990	597	$SEGB_{68}$	-567	990
498	$SEGB_{35}$	3591	990	548	$SEGA_{52}$	1491	990	598	$SEGC_{68}$	-609	990
499	$SEGC_{35}$	3549	990	549	$SEGB_{52}$	1449	990	599	$SEGA_{69}$	-651	990
500	$SEGA_{36}$	3507	990	550	$SEGC_{52}$	1407	990	600	$SEGB_{69}$	-693	990

■ PAD COORDINATES 5

Chip Size 18860μm x 2390μm (Chip Center 0μm x 0μm)

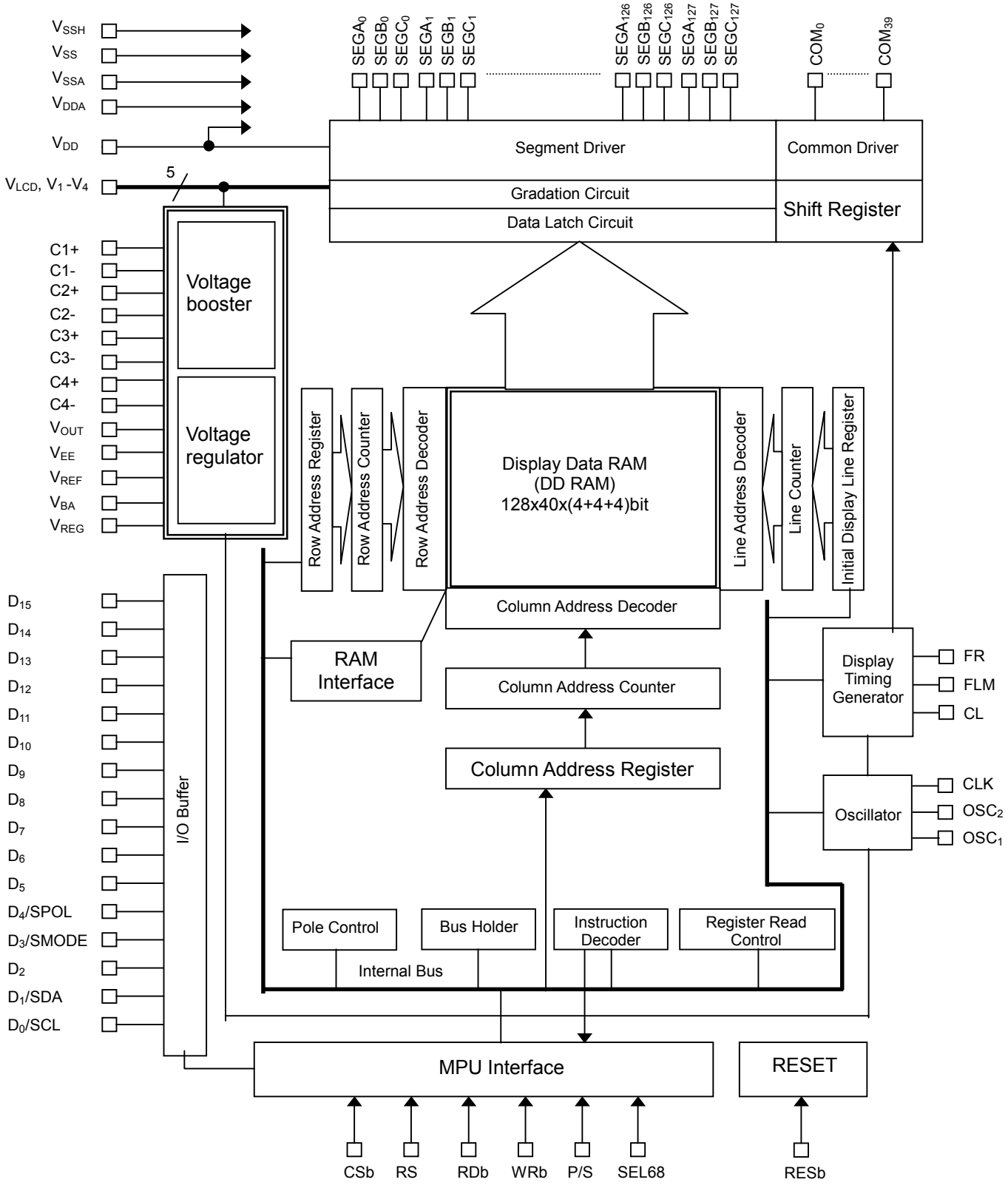
PAD No.	Terminal	X(μm)	Y(μm)	PAD No.	Terminal	X(μm)	Y(μm)	PAD No.	Terminal	X(μm)	Y(μm)
601	$SEGC_{69}$	-735	990	651	$SEGB_{86}$	-2835	990	701	$SEGA_{103}$	-4935	990
602	$SEGA_{70}$	-777	990	652	$SEGC_{86}$	-2877	990	702	$SEGB_{103}$	-4977	990
603	$SEGB_{70}$	-819	990	653	$SEGA_{87}$	-2919	990	703	$SEGC_{103}$	-5019	990
604	$SEGC_{70}$	-861	990	654	$SEGB_{87}$	-2961	990	704	$SEGA_{104}$	-5061	990
605	$SEGA_{71}$	-903	990	655	$SEGC_{87}$	-3003	990	705	$SEGB_{104}$	-5103	990
606	$SEGB_{71}$	-945	990	656	$SEGA_{88}$	-3045	990	706	$SEGC_{104}$	-5145	990
607	$SEGC_{71}$	-987	990	657	$SEGB_{88}$	-3087	990	707	$SEGA_{105}$	-5187	990
608	$SEGA_{72}$	-1029	990	658	$SEGC_{88}$	-3129	990	708	$SEGB_{105}$	-5229	990
609	$SEGB_{72}$	-1071	990	659	$SEGA_{89}$	-3171	990	709	$SEGC_{105}$	-5271	990
610	$SEGC_{72}$	-1113	990	660	$SEGB_{89}$	-3213	990	710	$SEGA_{106}$	-5313	990
611	$SEGA_{73}$	-1155	990	661	$SEGC_{89}$	-3255	990	711	$SEGB_{106}$	-5355	990
612	$SEGB_{73}$	-1197	990	662	$SEGA_{90}$	-3297	990	712	$SEGC_{106}$	-5397	990
613	$SEGC_{73}$	-1239	990	663	$SEGB_{90}$	-3339	990	713	$SEGA_{107}$	-5439	990
614	$SEGA_{74}$	-1281	990	664	$SEGC_{90}$	-3381	990	714	$SEGB_{107}$	-5481	990
615	$SEGB_{74}$	-1323	990	665	$SEGA_{91}$	-3423	990	715	$SEGC_{107}$	-5523	990
616	$SEGC_{74}$	-1365	990	666	$SEGB_{91}$	-3465	990	716	$SEGA_{108}$	-5565	990
617	$SEGA_{75}$	-1407	990	667	$SEGC_{91}$	-3507	990	717	$SEGB_{108}$	-5607	990
618	$SEGB_{75}$	-1449	990	668	$SEGA_{92}$	-3549	990	718	$SEGC_{108}$	-5649	990
619	$SEGC_{75}$	-1491	990	669	$SEGB_{92}$	-3591	990	719	$SEGA_{109}$	-5691	990
620	$SEGA_{76}$	-1533	990	670	$SEGC_{92}$	-3633	990	720	$SEGB_{109}$	-5733	990
621	$SEGB_{76}$	-1575	990	671	$SEGA_{93}$	-3675	990	721	$SEGC_{109}$	-5775	990
622	$SEGC_{76}$	-1617	990	672	$SEGB_{93}$	-3717	990	722	$SEGA_{110}$	-5817	990
623	$SEGA_{77}$	-1659	990	673	$SEGC_{93}$	-3759	990	723	$SEGB_{110}$	-5859	990
624	$SEGB_{77}$	-1701	990	674	$SEGA_{94}$	-3801	990	724	$SEGC_{110}$	-5901	990
625	$SEGC_{77}$	-1743	990	675	$SEGB_{94}$	-3843	990	725	$SEGA_{111}$	-5943	990
626	$SEGA_{78}$	-1785	990	676	$SEGC_{94}$	-3885	990	726	$SEGB_{111}$	-5985	990
627	$SEGB_{78}$	-1827	990	677	$SEGA_{95}$	-3927	990	727	$SEGC_{111}$	-6027	990
628	$SEGC_{78}$	-1869	990	678	$SEGB_{95}$	-3969	990	728	$SEGA_{112}$	-6069	990
629	$SEGA_{79}$	-1911	990	679	$SEGC_{95}$	-4011	990	729	$SEGB_{112}$	-6111	990
630	$SEGB_{79}$	-1953	990	680	$SEGA_{96}$	-4053	990	730	$SEGC_{112}$	-6153	990
631	$SEGC_{79}$	-1995	990	681	$SEGB_{96}$	-4095	990	731	$SEGA_{113}$	-6195	990
632	$SEGA_{80}$	-2037	990	682	$SEGC_{96}$	-4137	990	732	$SEGB_{113}$	-6237	990
633	$SEGB_{80}$	-2079	990	683	$SEGA_{97}$	-4179	990	733	$SEGC_{113}$	-6279	990
634	$SEGC_{80}$	-2121	990	684	$SEGB_{97}$	-4221	990	734	$SEGA_{114}$	-6321	990
635	$SEGA_{81}$	-2163	990	685	$SEGC_{97}$	-4263	990	735	$SEGB_{114}$	-6363	990
636	$SEGB_{81}$	-2205	990	686	$SEGA_{98}$	-4305	990	736	$SEGC_{114}$	-6405	990
637	$SEGC_{81}$	-2247	990	687	$SEGB_{98}$	-4347	990	737	$SEGA_{115}$	-6447	990
638	$SEGA_{82}$	-2289	990	688	$SEGC_{98}$	-4389	990	738	$SEGB_{115}$	-6489	990
639	$SEGB_{82}$	-2331	990	689	$SEGA_{99}$	-4431	990	739	$SEGC_{115}$	-6531	990
640	$SEGC_{82}$	-2373	990	690	$SEGB_{99}$	-4473	990	740	$SEGA_{116}$	-6573	990
641	$SEGA_{83}$	-2415	990	691	$SEGC_{99}$	-4515	990	741	$SEGB_{116}$	-6615	990
642	$SEGB_{83}$	-2457	990	692	$SEGA_{100}$	-4557	990	742	$SEGC_{116}$	-6657	990
643	$SEGC_{83}$	-2499	990	693	$SEGB_{100}$	-4599	990	743	$SEGA_{117}$	-6699	990
644	$SEGA_{84}$	-2541	990	694	$SEGC_{100}$	-4641	990	744	$SEGB_{117}$	-6741	990
645	$SEGB_{84}$	-2583	990	695	$SEGA_{101}$	-4683	990	745	$SEGC_{117}$	-6783	990
646	$SEGC_{84}$	-2625	990	696	$SEGB_{101}$	-4725	990	746	$SEGA_{118}$	-6825	990
647	$SEGA_{85}$	-2667	990	697	$SEGC_{101}$	-4767	990	747	$SEGB_{118}$	-6867	990
648	$SEGB_{85}$	-2709	990	698	$SEGA_{102}$	-4809	990	748	$SEGC_{118}$	-6909	990
649	$SEGC_{85}$	-2751	990	699	$SEGB_{102}$	-4851	990	749	$SEGA_{119}$	-6951	990
650	$SEGA_{86}$	-2793	990	700	$SEGC_{102}$	-4893	990	750	$SEGB_{119}$	-6993	990

■ PAD COORDINATES 6

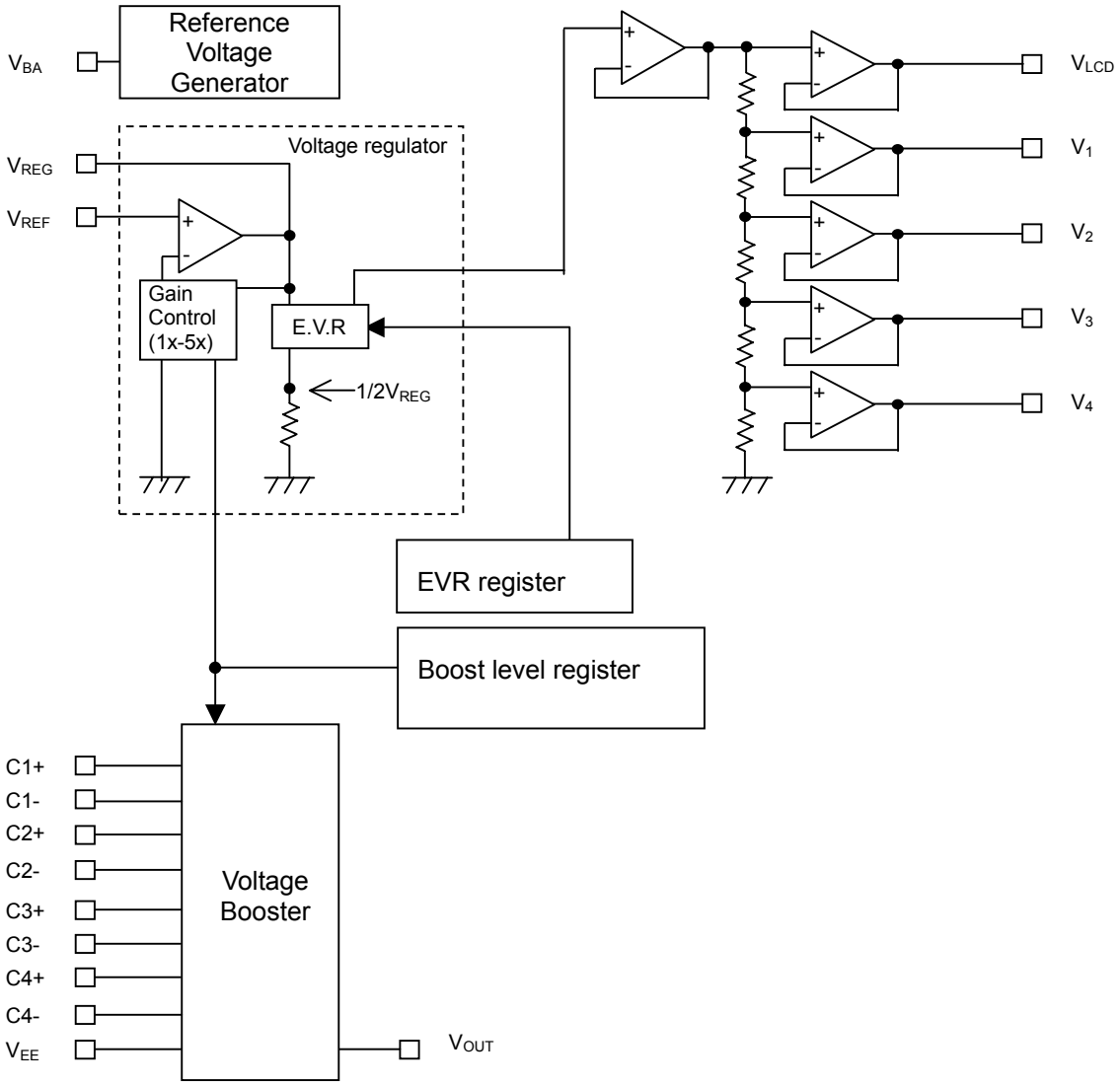
Chip Size 18860μm x 2390μm (Chip Center 0μm x 0μm)

PAD No.	Terminal	X(μm)	Y(μm)	PAD No.	Terminal	X(μm)	Y(μm)	PAD No.	Terminal	X(μm)	Y(μm)
751	$SEGC_{119}$	-7035	990	801	DMY_{99}	-9135	990				
752	$SEGA_{120}$	-7077	990	802	DMY_{100}	-9225	-742				
753	$SEGB_{120}$	-7119	990	803	DMY_{101}	-9225	-784				
754	$SEGC_{120}$	-7161	990	804	DMY_{101}	-9225	-826				
755	$SEGA_{121}$	-7203	990	805	DMY_{101}	-9225	-868				
756	$SEGB_{121}$	-7245	990	806	DMY_{102}	-9225	-910				
757	$SEGC_{121}$	-7287	990	801	DMY_{99}	-9135	990				
758	$SEGA_{122}$	-7329	990	802	DMY_{100}	-9225	-742				
759	$SEGB_{122}$	-7371	990	803	DMY_{101}	-9225	-784				
760	$SEGC_{122}$	-7413	990	804	DMY_{101}	-9225	-826				
761	$SEGA_{123}$	-7455	990	805	DMY_{101}	-9225	-868				
762	$SEGB_{123}$	-7497	990	806	DMY_{102}	-9225	-910				
763	$SEGC_{123}$	-7539	990	801	DMY_{99}	-9135	990				
764	$SEGA_{124}$	-7581	990	802	DMY_{100}	-9225	-742				
765	$SEGB_{124}$	-7623	990								
766	$SEGC_{124}$	-7665	990								
767	$SEGA_{125}$	-7707	990								
768	$SEGB_{125}$	-7749	990								
769	$SEGC_{125}$	-7791	990								
770	$SEGA_{126}$	-7833	990								
771	$SEGB_{126}$	-7875	990								
772	$SEGC_{126}$	-7917	990								
773	$SEGA_{127}$	-7959	990								
774	$SEGB_{127}$	-8001	990								
775	$SEGC_{127}$	-8043	990								
776	DMY_{94}	-8085	990								
777	DMY_{95}	-8127	990								
778	DMY_{96}	-8169	990								
779	COM_{20}	-8211	990								
780	COM_{21}	-8253	990								
781	COM_{22}	-8295	990								
782	COM_{23}	-8337	990								
783	COM_{24}	-8379	990								
784	COM_{25}	-8421	990								
785	COM_{26}	-8463	990								
786	COM_{27}	-8505	990								
787	COM_{28}	-8547	990								
788	COM_{29}	-8589	990								
789	COM_{30}	-8631	990								
790	COM_{31}	-8673	990								
791	COM_{32}	-8715	990								
792	COM_{33}	-8757	990								
793	COM_{34}	-8799	990								
794	COM_{35}	-8841	990								
795	COM_{36}	-8883	990								
796	COM_{37}	-8925	990								
797	COM_{38}	-8967	990								
798	COM_{39}	-9009	990								
799	DMY_{97}	-9051	990								
800	DMY_{98}	-9093	990								

■ BLOCK DIAGRAM



■ POWER SUPPLY CIRCUITS BLOCK DIAGRAM



■ TERMINAL DESCRIPTION 1

No.	Symbol	I/O	Function
111-121	V_{DD}	Power	Power supply for logic circuits
146-156	V_{SS}	Power	GND for logic circuits
239-248	V_{SSH}	Power	GND for high voltage circuits
10,11, 42,43,	V_{DDA}	Power	This terminal is internally connected to the V_{DD} level. •This terminal is used to fix the selection terminals to the V_{DD} level. Note) Do not use this terminal for a main power supply.
4,5, 16,17, 76,77,	V_{SSA}	Power	This terminal is internally connected to the V_{SS} level. •This terminal is used to fix the selection terminals to the V_{SS} level. Note) Do not use this terminal for a main GND.
158-166 168-176 177-185 187-195 196-204	V_{LCD} V_1 V_2 V_3 V_4	Power/O	LCD driving voltages •When the internal voltage booster is not used, external LCD driving voltages (V_1 to V_4 and V_{LCD}) must be supplied on these terminals. The external voltages must be maintained with the following relation. $V_{SS}<V_4<V_3<V_2<_{V1}<V_{LCD}$ • When the internal voltage booster is used, the LCD driving voltages (V_1 to V_4 and V_{LCD}) are enabled by the "Power control" instruction. The capacitors between the V_{SS} and these terminals are necessary.
271-280 282-291	C1+ C1-	O	Capacitor connection terminals for the voltage booster
293-302 304-313	C2+ C2-	O	Capacitor connection terminals for the voltage booster
315-324 326-335	C3+ C3-	O	Capacitor connection terminals for the voltage booster
337-346 348-357	C4+ C4-	O	Capacitor connection terminals for the voltage booster
228-237	V_{BA}	O	Output of the reference-voltage generator
217-226	V_{REF}	I	Input of the voltage regulator
260-269	V_{EE}	Power	Input of the voltage booster •This terminal is normally connected to the V_{DD} level.
249-258	V_{OUT}	Power/O	Output of the voltage booster Input for high voltage circuits in using external power supply
206-215	V_{REG}	O	Output of the voltage regulator
19,20	RESb	I	Reset Active "0"
7,8	SEL68	I	MPU interface type select SEL68 | H | L Status | 68 series | 80 series

■ TERMINAL DESCRIPTION 2

<table>
<tr><th>No.</th><th>Symbol</th><th>I/O</th><th>Function</th></tr>
<tr><td>45,46</td><td>D_0/SCL</td><td>I/O</td><td rowspan="5">Parallel interface:
D_7 to D_0 : 8-bit bi-directional bus
•In the parallel interface mode (P/S="1"), these terminals connect to 8-bit bi-directional MPU bus.

Serial interface:
SDA : serial data
SCL : serial clock
SMODE : 3-/4-line serial interface mode selection
SPOL : RS polarity selection (in the 3-line serial interface mode)
•In the 3-/4-line serial interface mode (P/S="0"), the D0 terminal is assigned to the SCL and the D_1 terminal to the SDA.
•In the 3-line serial interface mode, the D_4 terminal is assigned to the SPOL.
•Serial data on the SDA is fetched at the rising edge of the SCL signal in the order of the D_7, D_6…D_0, and the fetched data is converted into 8-bit parallel data at the falling edge of the 8th SCL signal.
•The SCL signal must be set to "0" after data transmissions or during non-access.</td></tr>
<tr><td>49,50</td><td>D_1/SDA</td><td>I/O</td></tr>
<tr><td>57,58</td><td>D_3/SMODE</td><td>I/O</td></tr>
<tr><td>61,62</td><td>D_4/SPOL</td><td>I/O</td></tr>
<tr><td>53,54
65,66
69,70
73,74</td><td>D_2
D_5
D_6
D_7</td><td>I/O</td></tr>
<tr><td>79,80
83,84
87,88
91,92
95,96
99,100
103,104
107,108</td><td>D_8
D_9
D_{10}
D_{11}
D_{12}
D_{13}
D_{14}
D_{15}</td><td>I/O</td><td>8-bit bi-directional bus
•In the 16-bit data bus mode, these terminals are assigned to the upper 8-bit data bus.
•In the serial interface mode or 8-bit data bus mode of the parallel interface, these terminals must be fixed to "1" or "0".</td></tr>
<tr><td>24,25</td><td>CSb</td><td>I</td><td>Chip select
Active "0"</td></tr>
<tr><td>29,30</td><td>RS</td><td>I</td><td>Resister select
•This signal distinguishes transferred data as an instruction or display data as follows.
<table><tr><td>RS</td><td>H</td><td>L</td></tr><tr><td>Distinct.</td><td>Instruction</td><td>Display data</td></tr></table></td></tr>
<tr><td>39,40</td><td>RDb (E)</td><td>I</td><td>80 series MPU interface (P/S="1", SEL68="0")
RDb signal. Active "L".

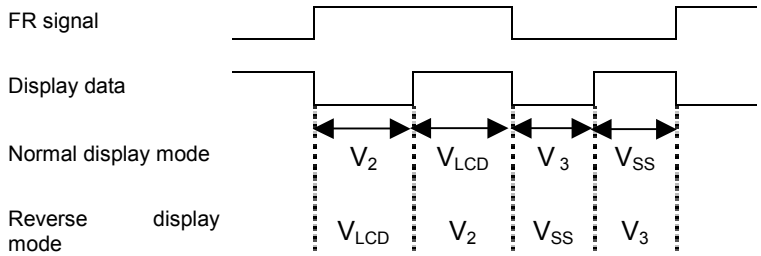
68 series MPU interface (P/S="1", SEL68="1")
Enable signal. Active "H".</td></tr>
<tr><td>34,35</td><td>WRb (R/W)</td><td>I</td><td>80 series MPU interface (P/S="1", SEL68="0")
WRb signal. Active "L".

68 series MPU interface (P/S="1", SEL68="1")
R/W signal.
<table><tr><td>R/W</td><td>H</td><td>L</td></tr><tr><td>Status</td><td>Read</td><td>Write</td></tr></table></td></tr>
</table>

■ TERMINAL DESCRIPTION 3

<table>
<tr><th>No.</th><th>Symbol</th><th>I/O</th><th>Function</th></tr>
<tr><td>13,14</td><td>P/S</td><td>I</td><td>Parallel / serial interface mode selection
<table>
<tr><th>P/S</th><th>Chip Select</th><th>Data/ Instruction</th><th>Data</th><th>Read/Write</th><th>Serial clock</th></tr>
<tr><td>H</td><td>CSb</td><td>RS</td><td>D_0 ~ D_7</td><td>RDb, WRb</td><td>-</td></tr>
<tr><td>L</td><td>CSb</td><td>RS</td><td>SDA (D_1)</td><td>Write only</td><td>SCL (D_0)</td></tr>
</table>
•Since the D_{15} to D_5 and D_2 terminals are in the high impedance in the serial inter face mode (P/S=”0”), they must be fixed to “1” or “0”. The RDb and WRb terminals also must be “1” or “0”.</td></tr>
<tr><td>124,125</td><td>CL</td><td>O</td><td>This terminal must be opened.</td></tr>
<tr><td>128,129</td><td>FLM</td><td>O</td><td>This terminal must be opened.</td></tr>
<tr><td>132,133</td><td>FR</td><td>O</td><td>This terminal must be opened.</td></tr>
<tr><td>136,137</td><td>CLK</td><td>O</td><td>This terminal must be opened.</td></tr>
<tr><td>140,141
143,144</td><td>OSC_1
OSC_2</td><td>I
O</td><td>OSC
•When the internal oscillator clock is used, OSC_1 terminal must be fixed to “1” or “0”, and the OSC_2 terminal must be opened. When the oscillation frequency from the internal oscillator is adjusted by an external resistor between OSC_1 terminal and OSC_2.
•When an external oscillator is used, external clock is input to the OSC_1 terminal or an external resistor is connected between the OSC_1 and OSC_2 terminals.</td></tr>
</table>

■ TERMINAL DESCRIPTION 4

<table>
<tr><th>No.</th><th>Symbol</th><th>I/O</th><th>Function</th></tr>
<tr><td>392-775</td><td>$SEGA_0$ - $SEGA_{127}$,
$SEGB_0$ - $SEGB_{127}$,
$SEGC_0$ - $SEGC_{127}$</td><td>O</td><td>Segment output
<table><tr><th>REV Mode</th><th>Turn-off</th><th>Turn-on</th></tr><tr><td>Normal</td><td>0</td><td>1</td></tr><tr><td>Reverse</td><td>1</td><td>0</td></tr></table>•These terminals output LCD driving waveforms in accordance with the combination of the FR signal and display data.
<u>In the B/W mode</u>
  </td></tr>
<tr><td>369-388,
779-798,</td><td>COM_0 -COM_{39}</td><td>O</td><td>Common output
● These terminals output LCD driving waveforms in accordance with the combination of the FR signal and scanning data.
<table><tr><th>Data</th><th>FR</th><th>Output level</th></tr><tr><td>H</td><td>H</td><td>V_{SS}</td></tr><tr><td>L</td><td>H</td><td>V_1</td></tr><tr><td>H</td><td>L</td><td>V_{LCD}</td></tr><tr><td>L</td><td>L</td><td>V_4</td></tr></table></td></tr>
</table>

Terminal No.

1-3, 12, 18, 21-23, 26-28, 31-33, 36-38, 41, 47, 48, 51, 52, 55, 56, 59, 60, 63, 64, 67, 68, 71, 72, 75, 81, 82, 85, 86, 89, 90, 93, 94, 97, 98, 101, 102, 105, 106, 109, 110, 122, 123, 126, 127, 130, 131, 134, 135, 138, 139, 142, 145, 157, 167, 186, 205, 216, 227, 238, 259, 270, 281, 292, 314, 325, 336, 347, 358-368, 389-391, 776-778, 799-806 are dummy.)

■ Functional Description

(1) MPU Interface

(1-1) Selection of Parallel / serial interface mode select

The P/S terminal is used to select parallel or serial interface mode as shown in the following table. In the serial interface mode, it is possible to read out display data from the DDRAM and status from the internal registers.

Table1

P/S	P/S mode	CSb	RS	RDb	WRb	SEL68	SDA	SCL	Data
H	Parallel I/F	CSb	RS	RDb	WRb	SEL68			D_7-D_0 (D_{15}-D_0)
L	Serial I/F	CSb	RS	-	-	-	SDA	SCL	-

Note 1) " -" : Fix to "1" or "0".

(1-2) Selection of MPU interface type

In the parallel interface mode, the SEL68 terminal is used to select 68- or 80-series MPU interface type as shown in the following table.

Table2

SEL68	MPU type	CSb	RS	RDb	WRb	Data
H	68 series MPU	CSb	RS	E	R/W	D_7-D_0 (D_{15}-D_0)
L	80 series MPU	CSb	RS	RDb	WRb	D_7-D_0 (D_{15}-D_0)

(1-3) Data distinction

In the parallel interface mode, the combination of RS, RDb, and WRb (R/W) signals distinguishes transferred data between the LSI and MPU as instruction or display data, as shown in the following table.

Table3

RS	68 series	80 series		Function
	R/W	RDb	WRb	
H	H	L	H	Read out instruction data
H	L	H	L	Write instruction data
L	H	L	H	Read out display data
L	L	H	L	Write display data

(1-4) Selection of serial interface mode

In the serial interface mode, the SMODE terminal is used to select the 3- or 4-line serial interface mode as shown in the following table.

Table4

SMODE	Serial interface mode
H	3-line
L	4-line

(1-5) 4-line serial interface mode

In the 4-line serial interface mode, when during the chip select is active (CSb="0"), the SDA and the SCL are enabled. When During the chip select is not active (CSb="1"), the SDA and the SCL are disabled and the internal shift register and the counter are being initialized. The 8-bit serial data on the SDA is fetched at the rising edge of the SCL signal (serial clock) in order of the D_7, D_6…D_0, and the fetched data is converted into the 8-bit parallel data at the rising edge of the 8th SCL signal.

In the 4-line serial interface mode, the transferred data on the SDA is distinguished as display data or instruction data in accordance with the condition of the RS signal.

Table5

RS	Data distinction
H	Instruction data
L	Display data

Since the serial interface operation is sensitive to external noises, the SCL should be set to "0" after data transmissions or during non-access. To release a mal-function caused by the external noises, the chip-selected status should be released (CSb="1") after each of the 8-bit data transmissions. The following figure illustrates the interface timing for the 4-line serial interface operation.

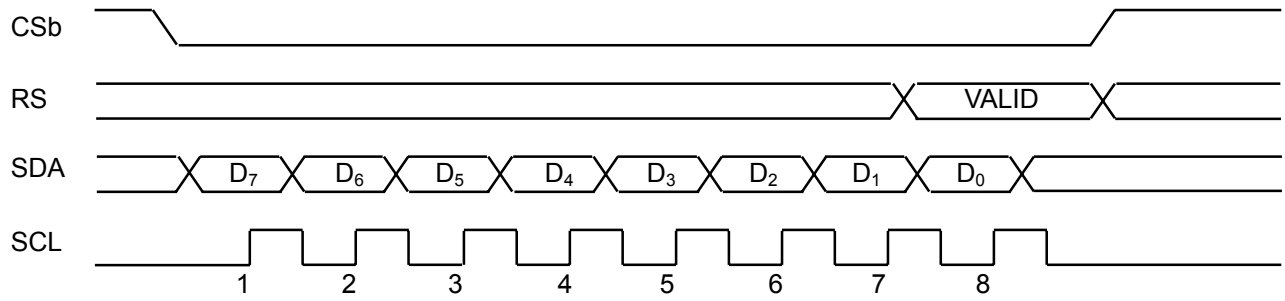


Fig1 4-line serial interface timing

(1-6) 3-line serial interface mode

In the 3-line serial interface mode, when the chip select is active (CSb="0"), the SDA and SCL are enabled. When the chip select is not active (CSb="1"), the SDA and SCL are disabled and the internal shift register and counter are being initialized. 9-bit serial data on the SDA is fetched at the rising edge of the SCL signal in order of the RS, D_7, D_6…D_0, and the fetched data is converted into the 9-bit parallel data at the rising edge of the 9th SCL signal.

In the 3-line serial interface mode, data on the SDA is distinguished as display data or instruction data in accordance with the condition of the RS bit of SDA data and the status of the SPOL, as follows.

Table6

SPOL=L		SPOL=H	
RS	Data distinction	RS	Data distinction
L	Display data	L	Instruction data
H	Instruction data	H	Display data

Since the serial interface operation is sensitive to external noises, the SCL must be set to "0" after data transmissions or during non-access. To release a mal-function caused by the external noises, the chip-selected status should be released (CSb="1") after each of 9-bit data transmissions. The following figure illustrates the interface timing of the 3-line serial interface operation.

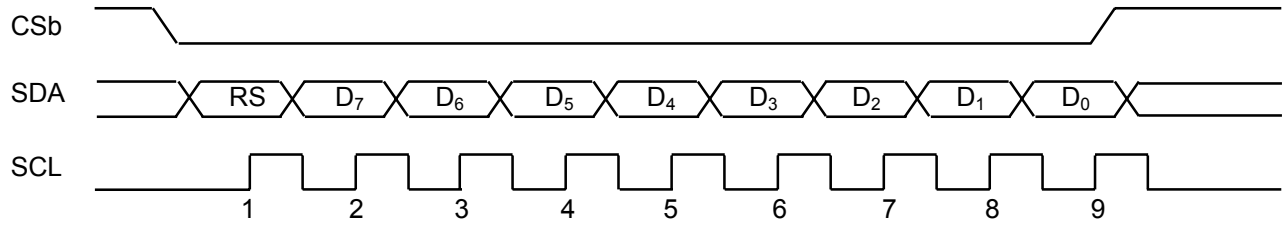


Fig2 3-line serial interface timing

(2) Access to the DDRAM

When the CSb signal is ”0”, the transferred data from MPU is written into the DDRAM or instruction register in accordance with the condition of the RS signal.

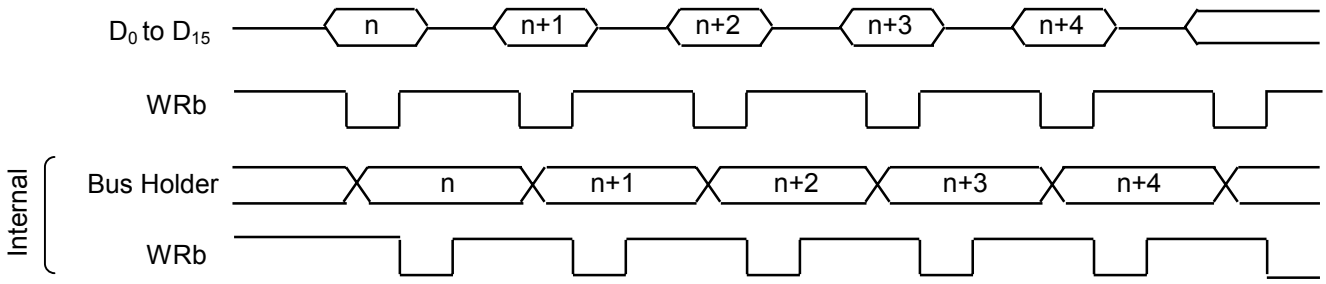
When the RS signal is “1”, the transferred data is distinguished as display data. After the “column address” and “row address” instructions are executed, the display data can be written into the DDRAM by the “display data write” instruction. The display data is written at the rising edge of the WRb signal in the 80 series MPU mode, or at the falling edge of the E signal in the 68 series MPU mode.

Table6

RS	Data
L	Display RAM Data
H	Internal Command Register

In the sequence of the “display data read” operation, the transferred data from MPU is temporarily held in the internal bus-holder and then transferred to the internal data-bus. When the “display data read” operation is executed just after the “column address” and “row address” instructions or “display data write” instruction, unexpected data on the bus-holder is read out at the 1st execution, then the data of designated DDRAM address is read out from the 2nd execution. For this reason, a dummy read cycle must be executed to avoid the unexpected 1st data read.

Display data write operation



Display data read operation

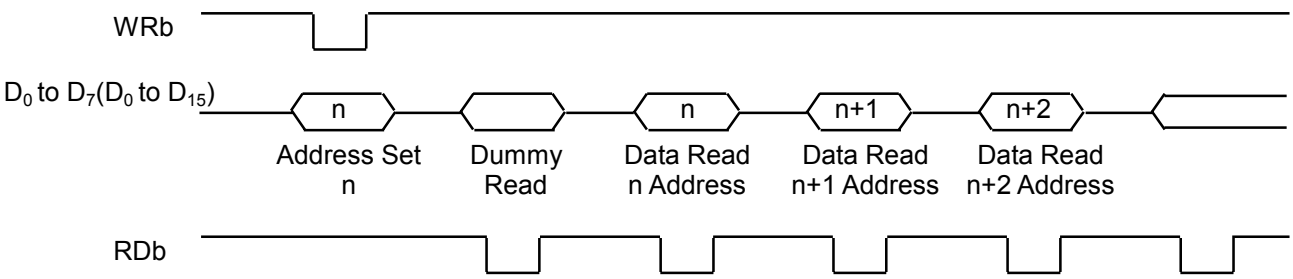


Fig3

Note) In the16-bit data bus mode, instruction data must be 16-bit as well as the display data.

(3) Access to the instruction register

Each instruction resisters is assigned to each address between 0_H and F_H, and the content of the instruction register can be read out by the combination of the “Instruction resister address” and ”Instruction resister read”.

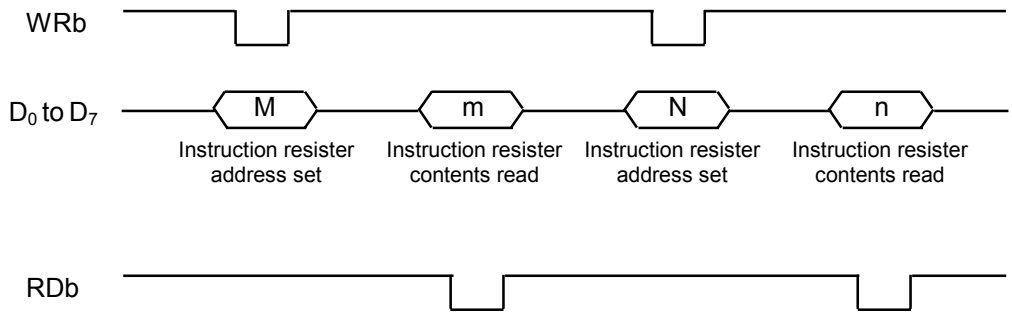


Fig4

(4) 8-/16-bit data bus length for display data (in the parallel interface mode)

The 8- or 16-bit data bus length for display data is determined by the “WLS” of the “Data bus length” instruction.

In the 16-bit data bus mode, not only the display data but also the instruction data is required to be transferred by 16-bit data (D_{15} to D_0). However, for the access to the instruction register, the only lower 8-bit data (D_7 to D_0) of the 16-bit data is valid. For the access to the DDRAM, all of the 16-bit data (D_{15} to D_0) is valid.

Table8

WLS	Data bus length mode
0	8-bit
1	16-bit

(5) Initial display line register

The initial display line resister specifies the line address, corresponding to the initial COM line, by the “Initial display line” instruction. The initial COM line signifies the common driver, starting scanning the display data in the DDRAM, and specified by the “Initial COM line” instruction.

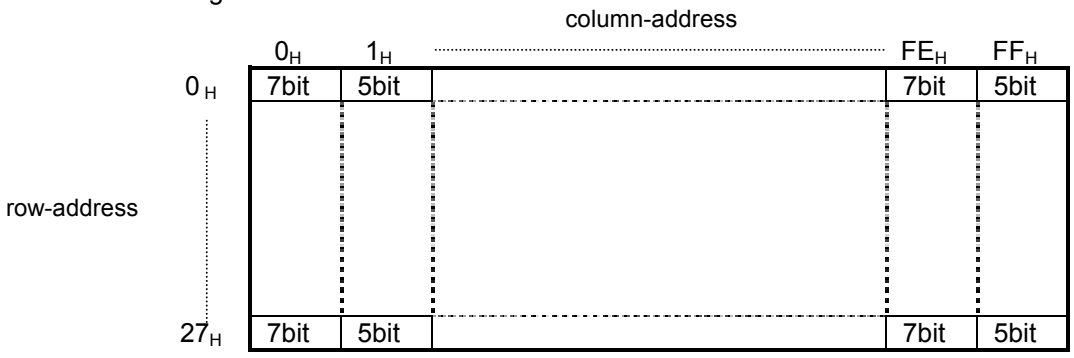
The line address, established in the initial display line resister, is preset into the line counter whenever the FLM signal becomes “1”. At the rising edge of the CL signal, the line counter is counted-up and addressed 384-bit display data corresponding to the counted-up line address, is latched into the data latch circuit. At the falling edge of the CL signal, the latched data outputs to the segment drivers.

(6) DDRAM mapping

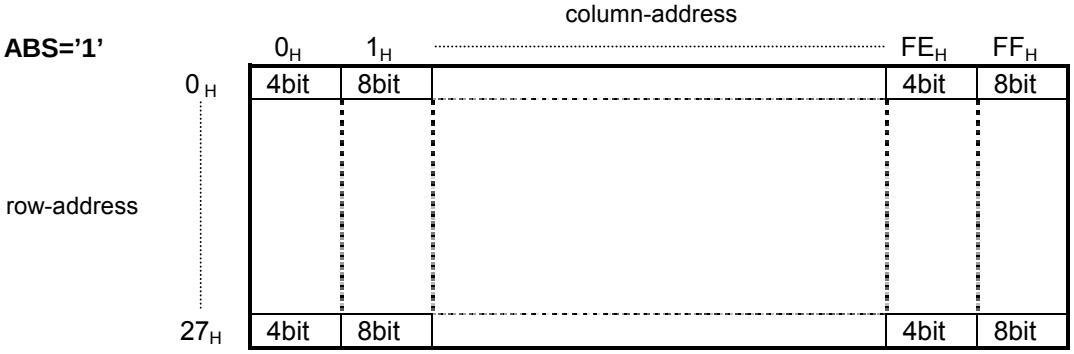
The DDRAM is capable of 1,536-bit (12-bit x 128-segment) for the column address and 40-bit for the row address.

In the gradation mode, each pixel for RGB corresponds to successive 3-segment drivers, and each segment driver has 16-gradation. Therefore, the LSI can drive up to 128x40 pixels in 4096-color display (16-gradation x 16-gradation x 16-gradation).

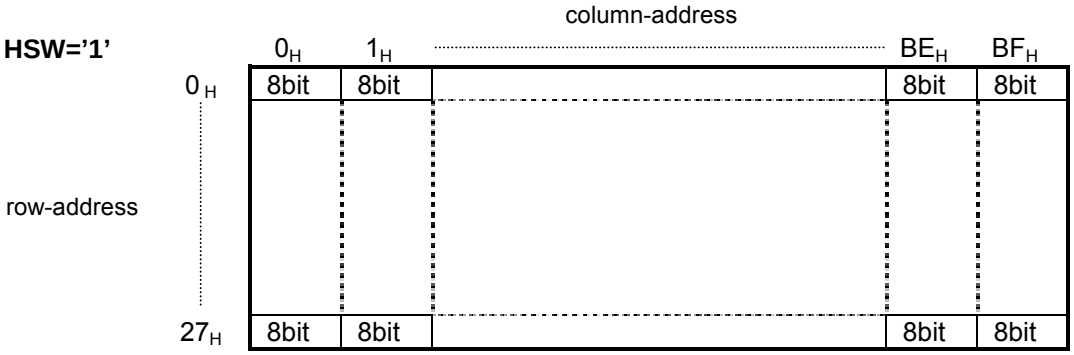
- In the 8-bit data bus length mode



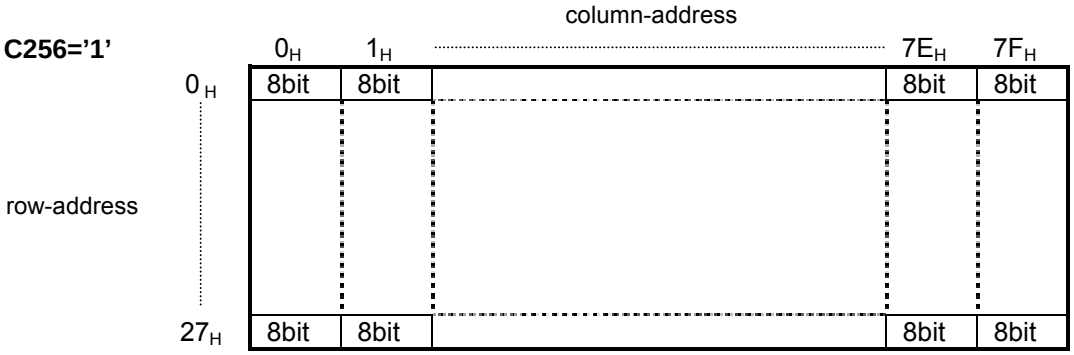
ABS='1'



HSW='1'



C256='1'



- In the 16-bit data bus length mode

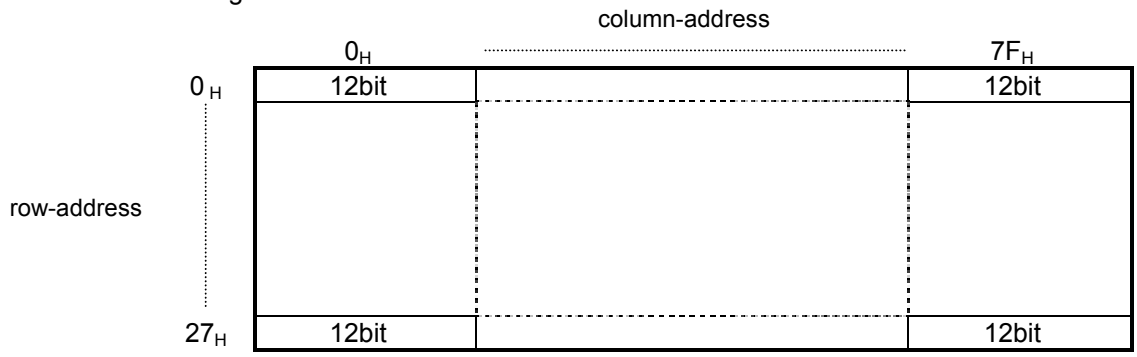


Fig6

In the B&W mode, only MSB data from each 4-bit display data group in the DDRAM is used. Therefore, 384 x 40 pixels in the B&W and 128 x 40 pixels in the 8-gradation are available.

The range of the column address varies depending on data bus length. The range between 00_H and FF_H is used in the 8-bit data bus length and the range between 00_H and $7F_H$ is in the 16-bit data bus length.

The increments for the column address and row address are set to the auto-increment mode by programming the “AXI” and “AYI” registers of the “Increment control” instruction. In this mode, the contents of the column address and row address counters automatically increment whenever the DDRAM is accessed.

The column address and row address counters, independent of the line counter. They are used to designate the column and row addresses for the display data transferred from MPU. On the other hand, the line counter is used to generate the line address, and output display data to the segment drivers, being synchronized with the display control timing of the FLM and CL signals.

RAM Map 1

Mode	WLS	ABS	HSW	REF	256	SEG0												SEG1													SEG126												SEG127											
						Palette A				Palette B				Palette C				Palette A				Palette B				Palette C					Palette A				Palette B				Palette C				Palette A				Palette B				Palette C			
						A3	A2	A1	A0	B3	B2	B1	B0	C3	C2	C1	C0	A3	A2	A1	A0	B3	B2	B1	B0	C3	C2	C1	C0		A3	A2	A1	A0	B3	B2	B1	B0	C3	C2	C1	C0	A3	A2	A1	A0	B3	B2	B1	B0	C3	C2	C1	C0
16bit	1	0	X	0	0	X=00H												X=01H													X=7EH												X=7FH											
						D15	D14	D13	D12	D10	D9	D8	D7	D4	D3	D2	D1	D15	D14	D13	D12	D10	D9	D8	D7	D4	D3	D2	D1		D15	D14	D13	D12	D10	D9	D8	D7	D4	D3	D2	D1	D15	D14	D13	D12	D10	D9	D8	D7	D4	D3	D2	D1
	1	0	X	1	0	X=7FH												X=7EH													X=01H												X=00H											
						D15	D14	D13	D12	D10	D9	D8	D7	D4	D3	D2	D1	D15	D14	D13	D12	D10	D9	D8	D7	D4	D3	D2	D1		D15	D14	D13	D12	D10	D9	D8	D7	D4	D3	D2	D1	D15	D14	D13	D12	D10	D9	D8	D7	D4	D3	D2	D1
	1	1	X	0	0	X=00H												X=01H													X=7EH												X=7FH											
						D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0		D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
	1	1	X	1	0	X=7FH												X=7EH													X=01H												X=00H											
						D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0		D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
8bit	0	0	0	0	0	X=00H							X=01H					X=02H							X=03H					X=FCH							X=FDH				X=FEH							X=FFH			
						D7	D6	D5	D4	D2	D1	D0	D7	D4	D3	D2	D1	D7	D6	D5	D4	D2	D1	D0	D7	D4	D3	D2	D1		D7	D6	D5	D4	D2	D1	D0	D7	D4	D3	D2	D1	D7	D6	D5	D4	D2	D1	D0	D7	D4	D3	D2	D1
	0	0	0	1	0	X=FEH							X=FFH					X=FCH							X=FDH					X=02H							X=03H				X=00H							X=01H			
						D7	D6	D5	D4	D2	D1	D0	D7	D4	D3	D2	D1	D7	D6	D5	D4	D2	D1	D0	D7	D4	D3	D2	D1		D7	D6	D5	D4	D2	D1	D0	D7	D4	D3	D2	D1	D7	D6	D5	D4	D2	D1	D0	D7	D4	D3	D2	D1
	0	1	0	0	0	X=00H							X=01H					X=02H							X=03H					X=FCH							X=FDH				X=FEH							X=FFH			
						D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0		D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
	0	1	0	1	0	X=FEH							X=FFH					X=FCH							X=FDH					X=02H							X=03H				X=00H							X=01H			
						D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0		D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
	0	X	1	0	0	X=00H								X=01H					X=02H								X=BDH					X=BEH								X=BFH											
						D7	D6	D5	D4	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0		D7	D6	D5	D4	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
	0	X	1	1	0	X=BEH(L)				X=BFH								X=BDH								X=BEH(H)					X=01H(L)				X=02H								X=00H								X=01H(H)			
						D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0	D7	D6	D5	D4		D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0	D7	D6	D5	D4

RAM Map 2 (256 Color Mode)

Mode	WLS	ABS	HSW	REF	256	SEG0												SEG1													SEG126												SEG127											
						Palette A				Palette B				Palette C				Palette A				Palette B				Palette C					Palette A				Palette B				Palette C				Palette A				Palette B				Palette C			
						A3	A2	A1	A0	B3	B2	B1	B0	C3	C2	C1	C0	A3	A2	A1	A0	B3	B2	B1	B0	C3	C2	C1	C0		A3	A2	A1	A0	B3	B2	B1	B0	C3	C2	C1	C0	A3	A2	A1	A0	B3	B2	B1	B0	C3	C2	C1	C0
						↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑		↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑
8bit	0	X	X	0	1	X=00H												X=01H													X=7EH												X=7FH											
						-	-	-	-	D7	D6	D5	D4	D3	D2	D1	D0	-	-	-	-	D7	D6	D5	D4	D3	D2	D1	D0		-	-	-	-	D7	D6	D5	D4	D3	D2	D1	D0	-	-	-	-	D7	D6	D5	D4	D3	D2	D1	D0
	0	X	X	1	1	X=7FH												X=7EH													X=01H												X=00H											
						-	-	-	-	D7	D6	D5	D4	D3	D2	D1	D0	-	-	-	-	D7	D6	D5	D4	D3	D2	D1	D0		-	-	-	-	D7	D6	D5	D4	D3	D2	D1	D0	-	-	-	-	D7	D6	D5	D4	D3	D2	D1	D0

SWAP

REF	SWAP	Palette A				Palette B				Palette C			
		A3	A2	A1	A0	B3	B2	B1	B0	C3	C2	C1	C0
0	0	SEGAx				SEGBx				SEGCx			
1	1												
0	1	SEGCx				SEGBx				SEGAx			
1	0												

Note1) In the 256-color mode, the vacant LSB bit is filled with "1".
Note2) The function of 256-color mode is different from that of fixed 8-gradation mode (fixed 256-color mode).
Note3) The written data in the DD RAM in "C256"=0 in not compatible with the data in "C256"=1.
Note4) In the 256-color mode, only 8-bit length mode is available, but 16-bit is not.

(7) Window addressing mode

In addition to the above usual DDRAM addressing, it is possible to access some part of DDRAM in using the window addressing mode, in which the start and end points are designated. The start point is determined by the “column address” and “row address” instructions, and the end point is determined by the “Window end column address” and “Window end row address” instructions, The setting example of the window addressing is listed, as follows.

1. Set WIN=1, AXI=1 and AYI=1 by the “Increment control” instruction
2. Set the start point by the “column address” and “row address” instructions
3. Set the end point by the “Window end column address” and “Window end row address” instructions
4. Enable to access to the DDRAM in the window addressing mode

In the window addressing mode (WIN=1, AXI=1, AYI=1), the read-modify-write operation is available by setting “0” to the “AIM” register of the ”Increment control” instruction.

And in the window addressing mode, the following start and end point must be maintained to abide a malfunction.

AX (column address of start point)≤ EX (column address of end point)≤ Maximum of column address
AY (row address of start point)≤ EY (row address of end point)≤ Maximum of row address

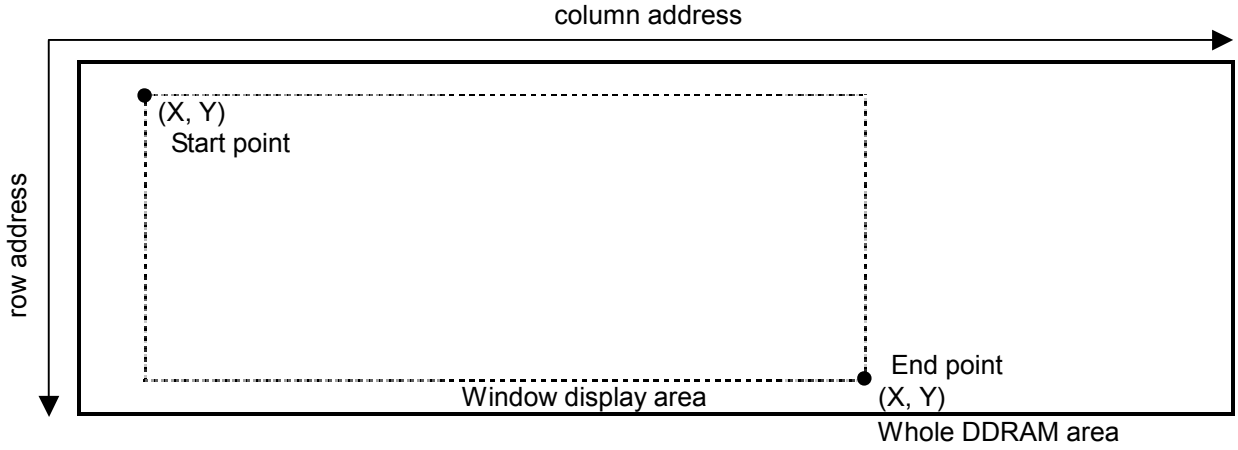


Fig7

(8) Reverse display ON/OFF

The “Reverse display ON/OFF” function is used to reverse the display data without changing the contents of the DDRAM.

Table9

REV	Display	DDRAM data → Display data	
0	Normal	0	0
		1	1
1	Reverse	0	1
		1	0

(9) Segment direction

The “Segment direction” function is used to reverse the assignment for the segment drivers and column address, and it is possible to reduce the restrictions for the placement of the LSI on the LCD modules.

(10) The relationship among the DDRAM column address, display data and segment drivers

In the color mode, and 16-bit data bus mode

HSW	ABS	REF	SWAP	Column address / bit / segment assign		
*	0	0	0	$X=00_H$	←→	$X=7F_H$
*	0	1	1	$X=7F_H$	←→	$X=00_H$

D_{15}	D_{14}	D_{13}	D_{12}	D_{10}	D_9	D_8	D_7	D_4	D_3	D_2	D_1	←→	D_{15}	D_{14}	D_{13}	D_{12}	D_{10}	D_9	D_8	D_7	D_4	D_3	D_2	D_1
palette A				palette B				palette C				←→	palette A				palette B				palette C			
$SEGA_0$				$SEGB_0$				$SEGC_0$				←→	$SEGA_{127}$				$SEGB_{127}$				$SEGC_{127}$			

HSW	ABS	REF	SWAP	Column address / bit / segment assign		
*	0	0	1	$X=00_H$	←→	$X=7F_H$
*	0	1	0	$X=7F_H$	←→	$X=00_H$

D_{15}	D_{14}	D_{13}	D_{12}	D_{10}	D_9	D_8	D_7	D_4	D_3	D_2	D_1	←→	D_{15}	D_{14}	D_{13}	D_{12}	D_{10}	D_9	D_8	D_7	D_4	D_3	D_2	D_1
palette A				palette B				palette C				←→	palette A				palette B				palette C			
$SEGC_0$				$SEGB_0$				$SEGA_0$				←→	$SEGC_{127}$				$SEGB_{127}$				$SEGA_{127}$			

HSW	ABS	REF	SWAP	Column address / bit / segment assign		
*	1	0	0	$X=00_H$	←→	$X=7F_H$
*	1	1	1	$X=7F_H$	←→	$X=00_H$

D_{11}	D_{10}	D_9	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	←→	D_{11}	D_{10}	D_9	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
palette A				palette B				palette C				←→	palette A				palette B				palette C			
$SEGA_0$				$SEGB_0$				$SEGC_0$				←→	$SEGA_{127}$				$SEGB_{127}$				$SEGC_{127}$			

HSW	ABS	REF	SWAP	Column address / bit / segment assign		
*	1	0	1	$X=00_H$	←→	$X=7F_H$
*	1	1	0	$X=7F_H$	←→	$X=00_H$

D_{11}	D_{10}	D_9	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	←→	D_{11}	D_{10}	D_9	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
palette A				palette B				palette C				←→	palette A				palette B				palette C			
$SEGC_0$				$SEGB_0$				$SEGA_0$				←→	$SEGC_{127}$				$SEGB_{127}$				$SEGA_{127}$			

In the color mode, and 8-bit data bus mode

HSW	ABS	REF	SWAP	Column address / bit / segment assign						
0	0	0	0	$X=00_H$	$X=01_H$	←→	$X=FE_H$		$X=FF_H$	
0	0	1	1	$X=FE_H$	$X=FF_H$	←→	$X=00_H$		$X=01_H$	
				D_7 D_6 D_5 D_4 D_2 D_1 D_0	D_7 D_4 D_3 D_2 D_1	←→	D_7 D_6 D_5 D_4 D_2 D_1 D_0		D_7 D_4 D_3 D_2 D_1	
				palette A	palette B	palette C	←→	palette A	palette B	palette C
				$SEGA_0$	$SEGB_0$	$SEGC_0$	←→	$SEGA_{127}$	$SEGB_{127}$	$SEGC_{127}$

HSW	ABS	REF	SWAP	Column address / bit / segment assign						
0	0	0	1	$X=00_H$	$X=01_H$	←→	$X=FE_H$		$X=FF_H$	
0	0	1	0	$X=FE_H$	$X=FF_H$	←→	$X=00_H$		$X=01_H$	
				D_7 D_6 D_5 D_4 D_2 D_1 D_0	D_7 D_4 D_3 D_2 D_1	←→	D_7 D_6 D_5 D_4 D_2 D_1 D_0		D_7 D_4 D_3 D_2 D_1	
				palette A	palette B	palette C	←→	palette A	palette B	palette C
				$SEGC_0$	$SEGB_0$	$SEGA_0$	←→	$SEGC_{127}$	$SEGB_{127}$	$SEGA_{127}$

HSW	ABS	REF	SWAP	Column address / bit / segment assign						
0	1	0	0	$X=00_H$	$X=01_H$	←→	$X=FE_H$		$X=FF_H$	
0	1	1	1	$X=FE_H$	$X=FF_H$	←→	$X=00_H$		$X=01_H$	
				D_3 D_2 D_1 D_0	D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0	←→	D_3 D_2 D_1 D_0		D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0	
				palette A	palette B	palette C	←→	palette A	palette B	palette C
				$SEGA_0$	$SEGB_0$	$SEGC_0$	←→	$SEGA_{127}$	$SEGB_{127}$	$SEGC_{127}$

HSW	ABS	REF	SWAP	Column address / bit / segment assign						
0	1	0	1	$X=00_H$	$X=01_H$	←→	$X=FE_H$		$X=FF_H$	
0	1	1	0	$X=FE_H$	$X=FF_H$	←→	$X=00_H$		$X=01_H$	
				D_3 D_2 D_1 D_0	D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0	←→	D_3 D_2 D_1 D_0		D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0	
				palette A	palette B	palette C	←→	palette A	palette B	palette C
				$SEGC_0$	$SEGB_0$	$SEGA_0$	←→	$SEGC_{127}$	$SEGB_{127}$	$SEGA_{127}$

			HSW	ABS	REF	SWAP
			1	*	1	1
SEGA 0	Palette A	D3	X=BEH	Column-address / bit / segment assign		
		D2				
		D1				
		D0				
SEGB 0	Palette B	D7	X=BFH			
		D6				
		D5				
		D4				
SEGC 0	Palette C	D3				
		D2				
		D1				
		D0				
SEGA 1	Palette A	D7	X=BDH			
		D6				
		D5				
		D4				
SEGB 1	Palette B	D3				
		D2				
		D1				
		D0				
SEGC 1	Palette C	D7	X=BEH			
		D6				
		D5				
		D4				
SEGA 126	Palette A	D3	X=01H			
		D2				
		D1				
		D0				
SEGB 126	Palette B	D7	X=02H			
		D6				
		D5				
		D4				
SEGC 126	Palette C	D3				
		D2				
		D1				
		D0				
SEGA 127	Palette A	D7	X=00H			
		D6				
		D5				
		D4				
SEGB 127	Palette B	D3				
		D2				
		D1				
		D0				
SEGC 127	Palette C	D7	X=01H			
		D6				
		D5				
		D4				

			HSW	ABS	REF	SWAP
			1	*	1	0
SEGC 0	Palette A	D3	X=BEH	Column-address / bit / segment assign		
		D2				
		D1				
		D0				
SEGB 0	Palette B	D7	X=BFH			
		D6				
		D5				
		D4				
SEGA 0	Palette C	D3				
		D2				
		D1				
		D0				
SEGC 1	Palette A	D7	X=BDH			
		D6				
		D5				
		D4				
SEGB 1	Palette B	D3				
		D2				
		D1				
		D0				
SEGA 1	Palette C	D7	X=BEH			
		D6				
		D5				
		D4				
SEGC 126	Palette A	D3	X=01H			
		D2				
		D1				
		D0				
SEGB 126	Palette B	D7	X=02H			
		D6				
		D5				
		D4				
SEGA 126	Palette C	D3				
		D2				
		D1				
		D0				
SEGC 127	Palette A	D7	X=00H			
		D6				
		D5				
		D4				
SEGB 127	Palette B	D3				
		D2				
		D1				
		D0				
SEGA 127	Palette C	D7	X=01H			
		D6				
		D5				
		D4				

			HSW	ABS	REF	SWAP
			1	*	0	1
SEGC 0	Palette A	D7	X=00H	Column-address / bit / segment assign		
		D6				
		D5				
		D4				
SEGB 0	Palette B	D3				
		D2				
		D1				
		D0				
SEGA 0	Palette C	D7	X=01H			
		D6				
		D5				
		D4				
SEGC 1	Palette A	D3				
		D2				
		D1				
		D0				
SEGB 1	Palette B	D7	X=02H			
		D6				
		D5				
		D4				
SEGA 1	Palette C	D3				
		D2				
		D1				
		D0				
SEGC 126	Palette A	D7	X=BDH			
		D6				
		D5				
		D4				
SEGB 126	Palette B	D3				
		D2				
		D1				
		D0				
SEGA 126	Palette C	D7	X=BEH			
		D6				
		D5				
		D4				
SEGC 127	Palette A	D3				
		D2				
		D1				
		D0				
SEGB 127	Palette B	D7	X=BFH			
		D6				
		D5				
		D4				
SEGA 127	Palette C	D3				
		D2				
		D1				
		D0				

			HSW	ABS	REF	SWAP
			1	*	0	0
SEGA 0	Palette A	D7	X=00H	Column-address / bit / segment assign		
		D6				
		D5				
		D4				
SEGB 0	Palette B	D3				
		D2				
		D1				
		D0				
SEGC 0	Palette C	D7	X=01H			
		D6				
		D5				
		D4				
SEGA 1	Palette A	D3				
		D2				
		D1				
		D0				
SEGB 1	Palette B	D7	X=02H			
		D6				
		D5				
		D4				
SEGC 1	Palette C	D3				
		D2				
		D1				
		D0				
SEGA 126	Palette A	D7	X=BDH			
		D6				
		D5				
		D4				
SEGB 126	Palette B	D3				
		D2				
		D1				
		D0				
SEGC 126	Palette C	D7	X=BEH			
		D6				
		D5				
		D4				
SEGA 127	Palette A	D3				
		D2				
		D1				
		D0				
SEGB 127	Palette B	D7	X=BFH			
		D6				
		D5				
		D4				
SEGC 127	Palette C	D3				
		D2				
		D1				
		D0				

In the color mode, 8-bit data bus mode, and C256 mode (C256=1)

HSW	ABS	REF	SWAP	Column address / bit / segment assign															
*	*	0	0	$X=00_H$								←→	$X=7F_H$						
*	*	1	1	$X=7F_H$								←→	$X=00_H$						
				D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	←→	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
				palette A			palette B			palette C		←→	palette A			palette B			palette C	
				$SEGA_0$			$SEGB_0$			$SEGC_0$		←→	$SEGA_{127}$			$SEGB_{127}$			$SEGC_{127}$	

HSW	ABS	REF	SWAP	Column address / bit / segment assign															
*	*	0	1	$X=00_H$								←→	$X=7F_H$						
*	*	1	0	$X=7F_H$								←→	$X=00_H$						
				D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	←→	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
				palette A			palette B			palette C		←→	palette A			palette B			palette C	
				$SEGC_0$			$SEGB_0$			$SEGA_0$		←→	$SEGC_{127}$			$SEGB_{127}$			$SEGA_{127}$	

In the B&W mode, and 16-bit data bus mode

HSW	ABS	REF	SWAP	Column address / bit / segment assign
*	0	0	0	$X=00_H$ ←→ $X=7F_H$
*	0	1	1	$X=7F_H$ ←→ $X=00_H$

	D_{15}	D_{14}	D_{13}	D_{12}	D_{11}	D_{10}	D_9	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	←→	D_{15}	D_{14}	D_{13}	D_{12}	D_{11}	D_{10}	D_9	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
	$SEGA_0$					$SEGB_0$						$SEGC_0$					←→	$SEGA_{127}$					$SEGB_{127}$						$SEGC_{127}$				

HSW	ABS	REF	SWAP	Column address / bit / segment assign
*	0	0	1	$X=00_H$ ←→ $X=7F_H$
*	0	1	0	$X=7F_H$ ←→ $X=00_H$

	D_{15}	D_{14}	D_{13}	D_{12}	D_{11}	D_{10}	D_9	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	←→	D_{15}	D_{14}	D_{13}	D_{12}	D_{11}	D_{10}	D_9	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
	$SEGC_0$					$SEGB_0$						$SEGA_0$					←→	$SEGC_{127}$					$SEGB_{127}$						$SEGA_{127}$				

HSW	ABS	REF	SWAP	Column address / bit / segment assign
*	1	0	0	$X=00_H$ ←→ $X=7F_H$
*	1	1	1	$X=7F_H$ ←→ $X=00_H$

	D_{15}	D_{14}	D_{13}	D_{12}	D_{11}	D_{10}	D_9	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	←→	D_{15}	D_{14}	D_{13}	D_{12}	D_{11}	D_{10}	D_9	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
					$SEGA_0$				$SEGB_0$				$SEGC_0$				←→					$SEGA_{127}$				$SEGB_{127}$				$SEGC_{127}$			

HSW	ABS	REF	SWAP	Column address / bit / segment assign
*	1	0	1	$X=00_H$ ←→ $X=7F_H$
*	1	1	0	$X=7F_H$ ←→ $X=00_H$

	D_{15}	D_{14}	D_{13}	D_{12}	D_{11}	D_{10}	D_9	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	←→	D_{15}	D_{14}	D_{13}	D_{12}	D_{11}	D_{10}	D_9	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
					$SEGC_0$				$SEGB_0$				$SEGA_0$				←→					$SEGC_{127}$				$SEGB_{127}$				$SEGA_{127}$			

In the B&W mode, and 8-bit data bus mode

HSW	ABS	REF	SWAP	Column address / bit / segment assign																							
0	0	0	0	$X=00_H$							$X=01_H$					←→	$X=FE_H$							$X=FF_H$				
0	0	1	1	$X=FE_H$							$X=FF_H$					←→	$X=00_H$							$X=01_H$				
				D_7	D_6	D_5	D_4	D_2	D_1	D_0	D_7	D_4	D_3	D_2	D_1	←→	D_7	D_6	D_5	D_4	D_2	D_1	D_0	D_7	D_4	D_3	D_2	D_1
				$SEGA_0$				$SEGB_0$			$SEGC_0$					←→	$SEGA_{127}$				$SEGB_{127}$			$SEGC_{127}$				

HSW	ABS	REF	SWAP	Column address / bit / segment assign																							
0	0	0	1	$X=00_H$							$X=01_H$					←→	$X=FE_H$							$X=FF_H$				
0	0	1	0	$X=FE_H$							$X=FF_H$					←→	$X=00_H$							$X=01_H$				
				D_7	D_6	D_5	D_4	D_2	D_1	D_0	D_7	D_4	D_3	D_2	D_1	←→	D_7	D_6	D_5	D_4	D_2	D_1	D_0	D_7	D_4	D_3	D_2	D_1
				$SEGC_0$				$SEGB_0$			$SEGA_0$					←→	$SEGC_{127}$				$SEGB_{127}$			$SEGA_{127}$				

HSW	ABS	REF	SWAP	Column address / bit / segment assign																							
0	1	0	0	$X=00_H$							$X=01_H$					←→	$X=FE_H$							$X=FF_H$				
0	1	1	1	$X=FE_H$							$X=FF_H$					←→	$X=00_H$							$X=01_H$				
				D_3	D_2	D_1	D_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	←→	D_3	D_2	D_1	D_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
				$SEGA_0$				$SEGB_0$				$SEGC_0$				←→	$SEGA_{127}$				$SEGB_{127}$				$SEGC_{127}$			

HSW	ABS	REF	SWAP	Column address / bit / segment assign																							
0	1	0	1	$X=00_H$							$X=01_H$					←→	$X=FE_H$							$X=FF_H$				
0	1	1	0	$X=FE_H$							$X=FF_H$					←→	$X=00_H$							$X=01_H$				
				D_3	D_2	D_1	D_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	←→	D_3	D_2	D_1	D_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
				$SEGC_0$				$SEGB_0$				$SEGA_0$				←→	$SEGC_{127}$				$SEGB_{127}$				$SEGA_{127}$			

HSW	ABS	REF	SWAP			
1	*	0	0			
SEGA 0	D7	X=00H	Column-address / bit / segment assign			
	D6					
	D5					
	D4					
SEGB 0	D3					
	D2					
	D1					
	D0					
SEGC 0	D7	X=01H				
	D6					
	D5					
	D4					
SEGA 1	D3					
	D2					
	D1					
	D0					
SEGB 1	D7	X=02H				
	D6					
	D5					
	D4					
SEGC 1	D3					
	D2					
	D1					
	D0					
SEGA 126	D7	X=BDH				
	D6					
	D5					
	D4					
SEGB 126	D3					
	D2					
	D1					
	D0					
SEGC 126	D7	X=BEH				
	D6					
	D5					
	D4					
SEGA 127	D3					
	D2					
	D1					
	D0					
SEGB 127	D7	X=BFH				
	D6					
	D5					
	D4					
SEGC 127	D3					
	D2					
	D1					
	D0					

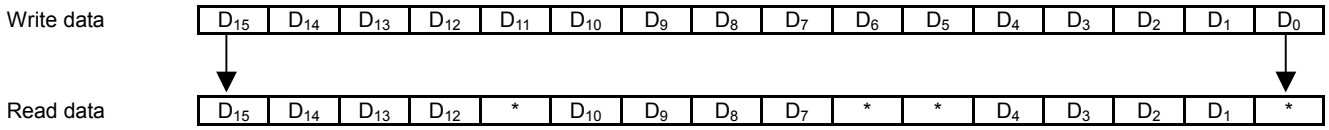
HSW	ABS	REF	SWAP			
1	*	1	1			
SEGC 0	D7	X=00H	Column-address / bit / segment assign			
	D6					
	D5					
	D4					
SEGB 0	D3					
	D2					
	D1					
	D0					
SEGA 0	D7	X=01H				
	D6					
	D5					
	D4					
SEGC 1	D3					
	D2					
	D1					
	D0					
SEGB 1	D7	X=02H				
	D6					
	D5					
	D4					
SEGA 1	D3					
	D2					
	D1					
	D0					
SEGC 126	D7	X=BDH				
	D6					
	D5					
	D4					
SEGB 126	D3					
	D2					
	D1					
	D0					
SEGA 126	D7	X=BEH				
	D6					
	D5					
	D4					
SEGC 127	D3					
	D2					
	D1					
	D0					
SEGB 127	D7	X=BFH				
	D6					
	D5					
	D4					
SEGA 127	D3					
	D2					
	D1					
	D0					

HSW	ABS	REF	SWAP			
1	*	1	0			
SEGC 0	D3	X=BEH	Column-address / bit / segment assign			
	D2					
	D1					
	D0					
SEGB 0	D7	X=BFH				
	D6					
	D5					
	D4					
SEGA 0	D3					
	D2					
	D1					
	D0					
SEGC 1	D7	X=BDH				
	D6					
	D5					
	D4					
SEGB 1	D3					
	D2					
	D1					
	D0					
SEGA 1	D7	X=BEH				
	D6					
	D5					
	D4					
SEGC 126	D3	X=01H				
	D2					
	D1					
	D0					
SEGB 126	D7	X=02H				
	D6					
	D5					
	D4					
SEGA 126	D3					
	D2					
	D1					
	D0					
SEGC 127	D7	X=00H				
	D6					
	D5					
	D4					
SEGB 127	D3					
	D2					
	D1					
	D0					
SEGA 127	D7	X=01H				
	D6					
	D5					
	D4					

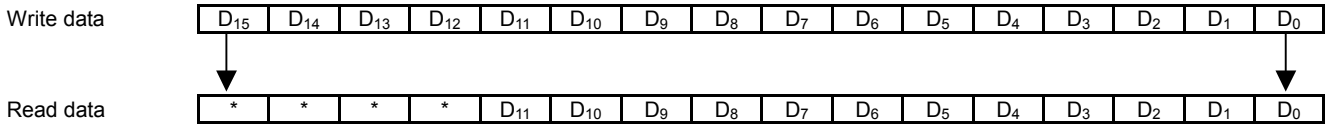
HSW	ABS	REF	SWAP			
1	*	1	1			
SEGA 0	D3	X=BEH	Column-address / bit / segment assign			
	D2					
	D1					
	D0					
SEGB 0	D7	X=BFH				
	D6					
	D5					
	D4					
SEGC 0	D3					
	D2					
	D1					
	D0					
SEGA 1	D7	X=BDH				
	D6					
	D5					
	D4					
SEGB 1	D3					
	D2					
	D1					
	D0					
SEGC 1	D7	X=BEH				
	D6					
	D5					
	D4					
SEGA 126	D3	X=01H				
	D2					
	D1					
	D0					
SEGB 126	D7	X=02H				
	D6					
	D5					
	D4					
SEGC 126	D3					
	D2					
	D1					
	D0					
SEGA 127	D7	X=00H				
	D6					
	D5					
	D4					
SEGB 127	D3					
	D2					
	D1					
	D0					
SEGC 127	D7	X=01H				
	D6					
	D5					
	D4					

Bit assignments between write and read data (in the 16-bit data bus mode)

ABS=0

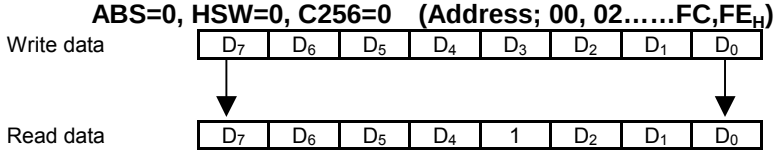


ABS=1

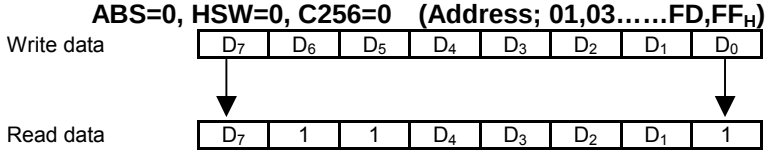


Examples of write and read data (In the 8 bit bus mode)

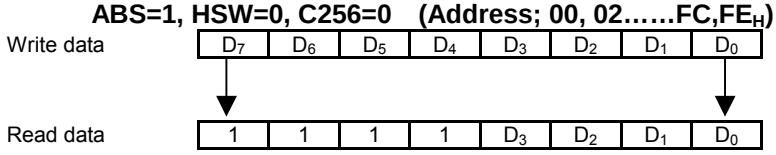
ABS=0, HSW=0, C256=0 (Address; 00, 02……FC,FE_H)



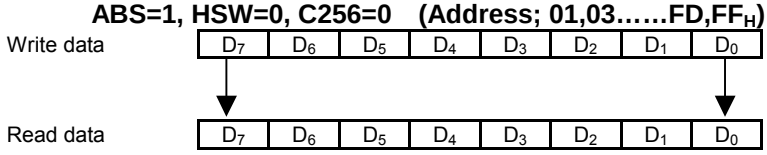
ABS=0, HSW=0, C256=0 (Address; 01,03……FD,FF_H)



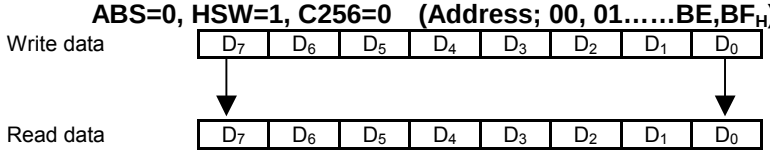
ABS=1, HSW=0, C256=0 (Address; 00, 02……FC,FE_H)



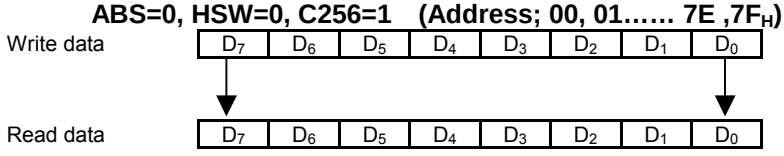
ABS=1, HSW=0, C256=0 (Address; 01,03……FD,FF_H)



ABS=0, HSW=1, C256=0 (Address; 00, 01……BE,BF_H)



ABS=0, HSW=0, C256=1 (Address; 00, 01…… 7E ,$7F_H$)



* : Invalid data

(11) Gradation palette

In the gradation mode, either variable or fixed gradation mode is selected by programming the “PWM” register of the “Gradation control” instruction.

PWM=0: Variable gradation mode
(Select 16 gradation levels out of 32-gradation level of the gradation palette)

PWM=1: Fixed gradation mode
(Fixed 8-gradation levels)

In these mode, each of the gradation palettes Aj, Bj and Cj can select 16-gradation level out of 32-gradation level by setting 5-bit data to the “PA” registers in the “Gradation palette j” instructions (j=0 to Fh).

For instance, the gradation palettes Aj correspond to the SEGAi, the Bj to SEGBi and the Cj to SEGCi (j=0 to 15, i=0 to 127).

Correspondence between display data and gradation palettes

Table 10 (Palette Aj, Palette Bj, Palette Cj (j=0 to 15))

(MSB) Display data (LSB)				Gradation palette	Default palette value
0	0	0	0	Palette 0	0 0 0 0 0
0	0	0	1	Palette 1	0 0 0 1 1
0	0	1	0	Palette 2	0 0 1 0 1
0	0	1	1	Palette 3	0 0 1 1 1
0	1	0	0	Palette 4	0 1 0 0 1
0	1	0	1	Palette 5	0 1 0 1 1
0	1	1	0	Palette 6	0 1 1 0 1
0	1	1	1	Palette 7	0 1 1 1 1
1	0	0	0	Palette 8	1 0 0 0 1
1	0	0	1	Palette 9	1 0 0 1 1
1	0	1	0	Palette10	1 0 1 0 1
1	0	1	1	Palette11	1 0 1 1 1
1	1	0	0	Palette12	1 1 0 0 1
1	1	0	1	Palette13	1 1 0 1 1
1	1	1	0	Palette14	1 1 1 0 1
1	1	1	1	Palette15	1 1 1 1 1

Gradation palette table (Variable gradation mode, PWM=”0”, MON=”0”)

Table 11 (Palette Aj, Palette Bj, Palette Cj (j=0 to 15))

Palette value	Gradation level	Gradation palette	Palette value	Gradation level	Gradation palette
0 0 0 0 0	0	Palette 0(default)	1 0 0 0 0	16/31	
0 0 0 0 1	1/31		1 0 0 0 1	17/31	Palette 0(default)8
0 0 0 1 0	2/31		1 0 0 1 0	18/31	
0 0 0 1 1	3/31	Palette 1(default)	1 0 0 1 1	19/31	Palette 9(default)
0 0 1 0 0	4/31		1 0 1 0 0	20/31	
0 0 1 0 1	5/31	Palette 2(default)	1 0 1 0 1	21/31	Palette 10(default)
0 0 1 1 0	6/31		1 0 1 1 0	22/31	
0 0 1 1 1	7/31	Palette 3(default)	1 0 1 1 1	23/31	Palette 11(default)
0 1 0 0 0	8/31		1 1 0 0 0	24/31	
0 1 0 0 1	9/31	Palette 4(default)	1 1 0 0 1	25/31	Palette 12(default)
0 1 0 1 0	10/31		1 1 0 1 0	26/31	
0 1 0 1 1	11/31	Palette 5(default)	1 1 0 1 1	27/31	Palette 13(default)
0 1 1 0 0	12/31		1 1 1 0 0	28/31	
0 1 1 0 1	13/31	Palette 6(default)	1 1 1 0 1	29/31	Palette 14(default)
0 1 1 1 0	14/31		1 1 1 1 0	30/31	
0 1 1 1 1	15/31	Palette 7(default)	1 1 1 1 1	31/31	Palette 15(default)

Gradation palette table (Fixed gradation mode, PWM="1", MON="0")

Table 12 8-gradation segment drivers

(MSB) Display data (LSB)				Gradation level
0	0	0	*	0/7
0	0	1	*	1/7
0	1	0	*	2/7
0	1	1	*	3/7
1	0	0	*	4/7
1	0	1	*	5/7
1	1	0	*	6/7
1	1	1	*	7/7

(MSB) Display data (LSB)				Gradation level
0	0	*	*	0/7
0	0	*	*	
0	1	*	*	3/7
0	1	*	*	
1	0	*	*	5/7
1	0	*	*	
1	1	*	*	7/7
1	1	*	*	

Correspondence between display data and gradation level (B&W mode, MON="1")

Table 13

(MSB) Display data (LSB)				Gradation level
0	*	*	*	0
1	*	*	*	1

*:Don't care

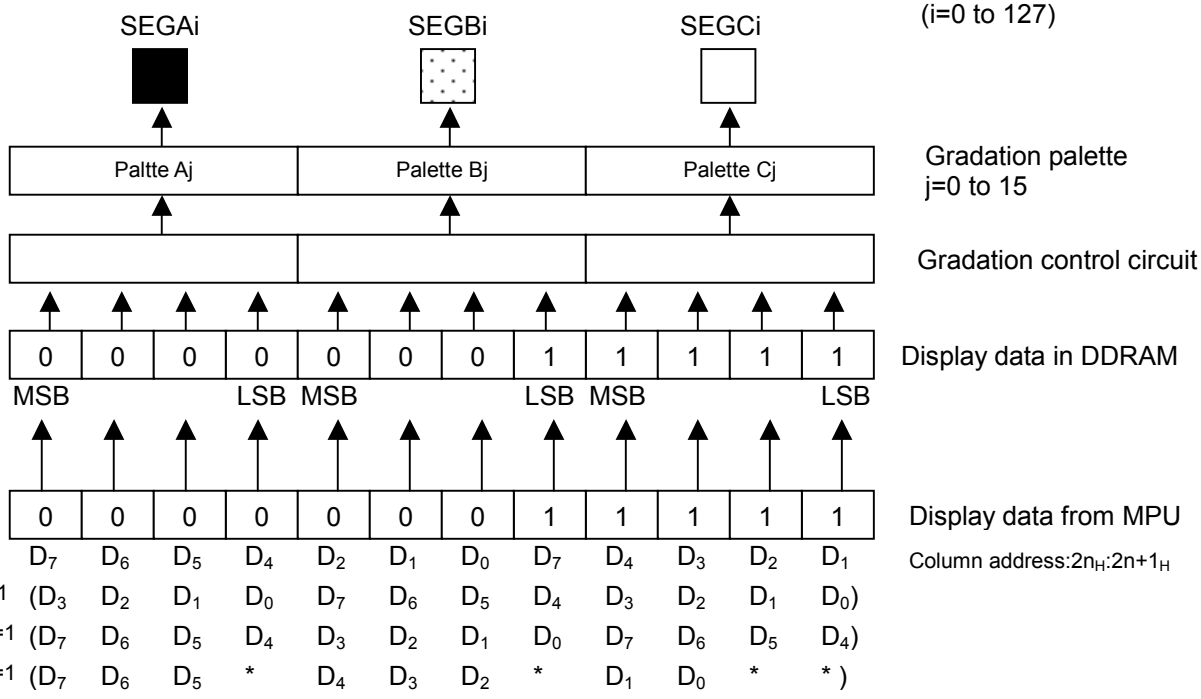
(12) Gradation control and display data

(12-1) Gradation mode

In the graduation mode, each pixel for RGB corresponds to successive 3 segment drivers, and each segment driver provides 16-gradation PWM output by controlling 4 bit display data of the DDRAM. Accordingly, the LSI can drive up to 128x40 pixels in 4096-color (16-gradation x 16-gradation x 16-gradation = 4-bit x 4-bit x 4-bit).

In addition, the LSI can transfer the display data for the RGB by 16-bit at once or 8-bit two-times. The data assignment between gradation palettes and segment drivers varies in accordance with setting for the "SWAP" and "REF" registers of the "Display control (2)" instruction.

(REF, SWAP)=(0, 0) or (1, 1)

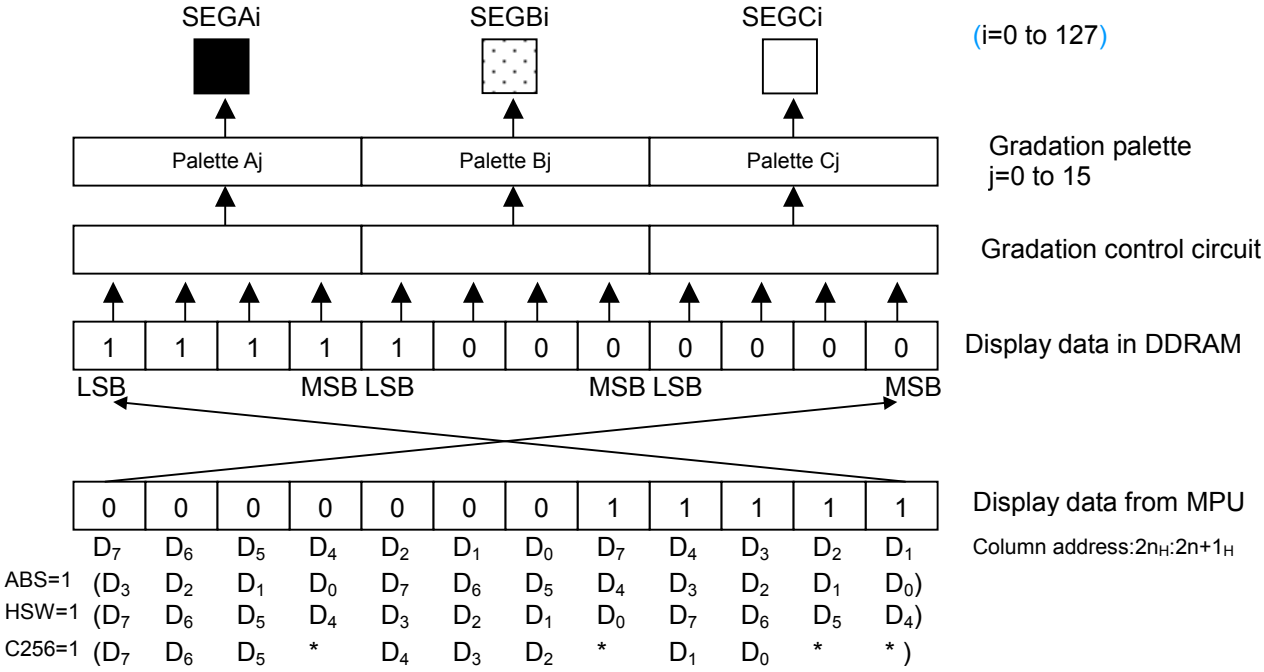


Note) DDRAM column address :$2n_H$,$2n_H+1_H$ (REF="0")

:FE_H-2n_H , $FF_H-(2n_H+1_H)$ (REF="1")

HSW=1; 00_H to BF_H, C256=1; 00_H to $7F_H$

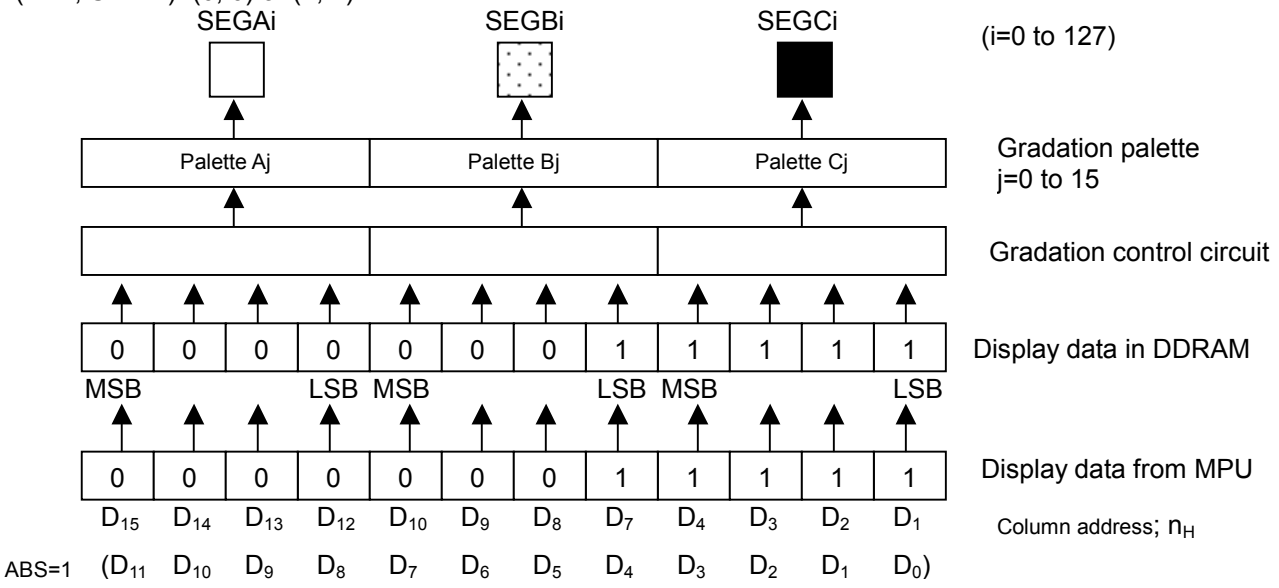
(REF, SWAP)=(0, 1) or (1, 0)



Note) DDRAM column address : $2n_H$,$2n_H+1_H$ (REF="0")
: FE_H -$2n_H$, FF_H-($2n_H+1_H$) (REF="1")
HSW=1; 00_H to BF_H, C256=; 00_H to $7F_H$

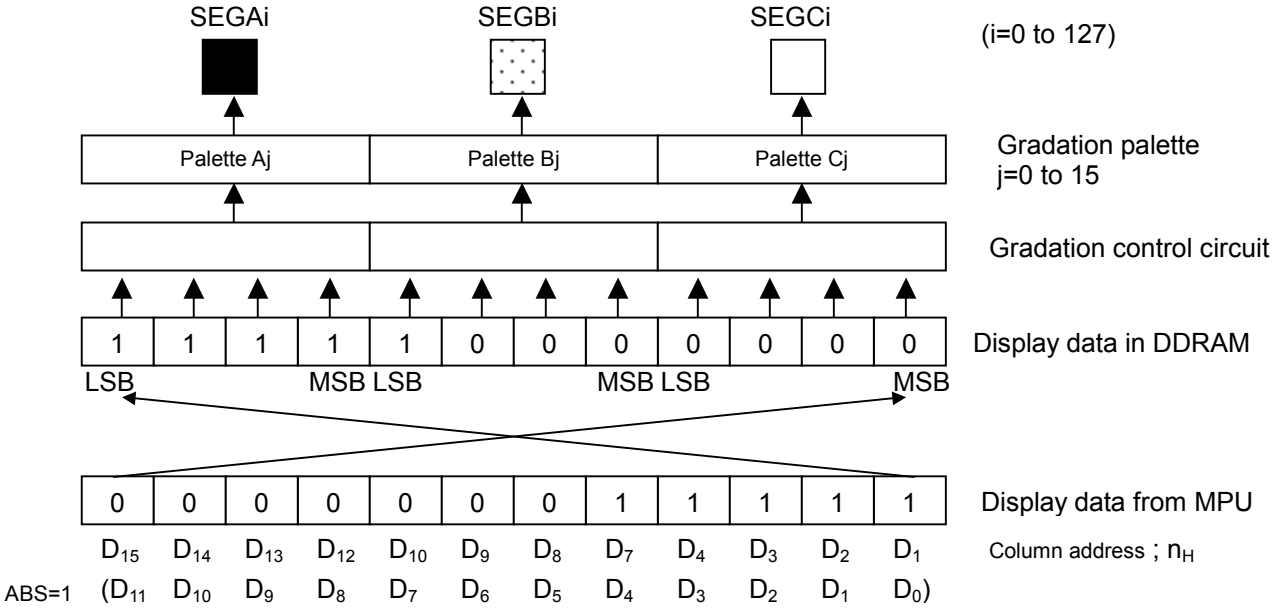
In the 16-bit data bus mode, the data assignments between the gradation palettes and the segment drivers vary in accordance with setting for the "SWAP" and "REF" bit of the "Display control (2)" instruction as well as the assignment in the 8-bit data bus mode.

(REF, SWAP)=(0, 0) or (1, 1)



Note) DDRAM column address :n_H (REF="0")
:$7F_H$ - n_H(REF="1")

(REF, SWAP)=(0, 1) or (1, 0)



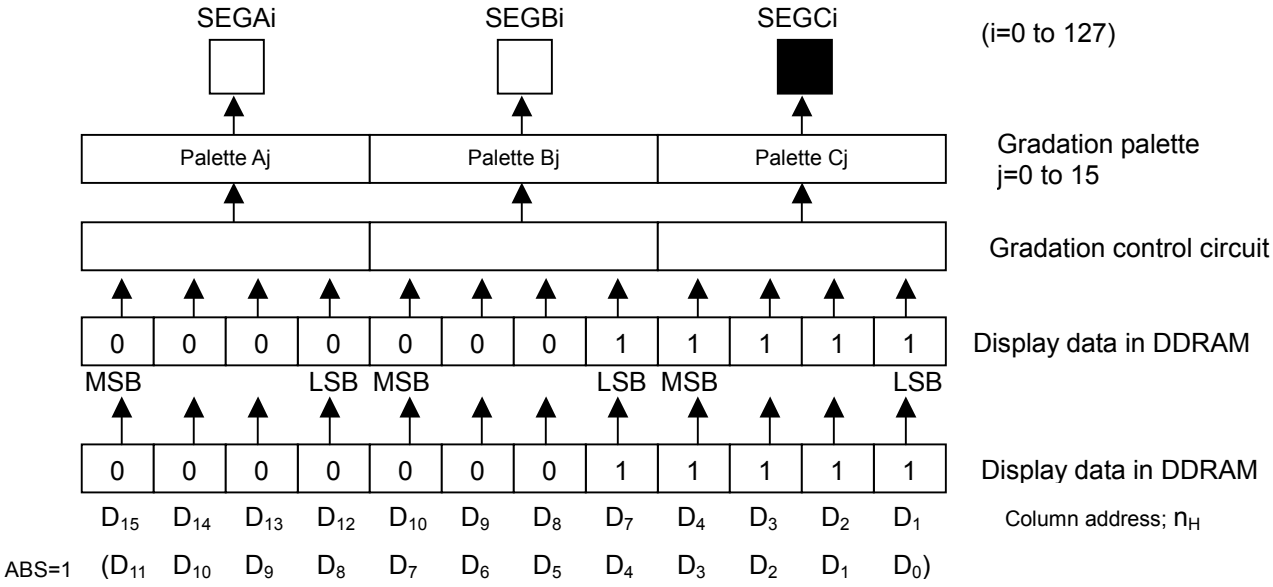
Note) DDRAM column address :n_H (REF="0")
:$7F_H - n_H$ (REF="1")

(12-2) B&W mode (MON="1")

In the B&W mode, 3 bits of the MSB data are used in both of the 16-bit and 8-bit data bus modes.

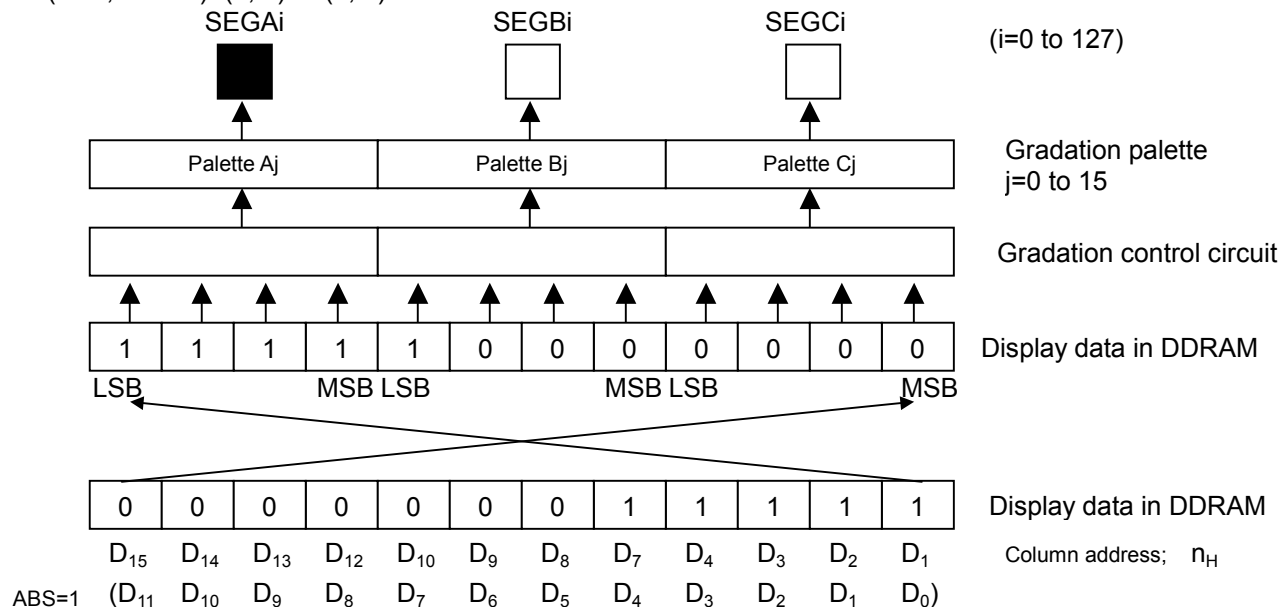
In the 16-bit data bus mode (Similarly 8-bit data bus access)

(REF, SWAP)=(0, 0) or (1, 1)



Note) DDRAM column address : n_H (REF="0")
: $7F_H$-n_H (REF="1")

(REF, SWAP)=(0, 1) or (1, 0)



Note) DDRAM column address : n_H (REF="0")
: $7F_H$-n_H (REF="1")

(13) Display timing generator

The display-timing generator creates the timing pulses such as the CL, the FLM, the FR and the CLK by dividing the oscillation frequency oscillate an external or internal resister mode. The each of timing pulses is outputted through the each output terminals by “SON” = 1.

(14) LCD line clock (CL)

The LCD line clock (CL) is used as a count-up signal for the line counter and a latch signal for the data latch circuit. At the rising edge of the CL signal, the line counter is counted-up and the 384-bit display data, corresponding to this line address, is latched into the data latch circuit. And at the falling edge of the CL signal, this latched data output on the segment drivers. Read out timing of the display data, from DDRAM to the latch circuits is completely independent of the access timing to the MPU. For this reason, the MPU can access to the LSI regardless of an internal operation.

(15) LCD alternate signal (FR) and LCD synchronous signal (FLM)

The FR and FLM signals are created from the CL signal. The FR signal is used to alternate the crystal polarization on a LCD panel. It is programmed that the FR signal is toggle on every frame in the default setting or once every N lines in the N-line inversion mode. The FLM signal is used to indicate a start line of a new display frame. It presets an initial display line address of the line counter when the FLM signal becomes ”1”.

(16) Data latch circuit

The data latch circuit is used temporarily store the display data that will output to the segment drivers. The display data in this circuit is updated in synchronization of the CL signal.

The “All pixels ON/OFF”, “Display ON/OFF” and “Reverse display ON/OFF” instructions change the display data in this circuit but do not change the display data of the DDRAM.

(17) Common and segment drivers

The LSI includes 384-segment drivers and 40-common drivers. The common drivers generate the LCD driving waveforms composed of the V_{LCD}, V_1, V_4 and V_{SS} in accordance with the FR signal and scanning data. The segment drivers generate waveforms composed of the V_{LCD}, V_2, V_3 and V_{SS} in accordance with the FR signal and display data.

LCD Driving waveforms (In the B&W mode, Reverse display OFF, 1/41 duty)

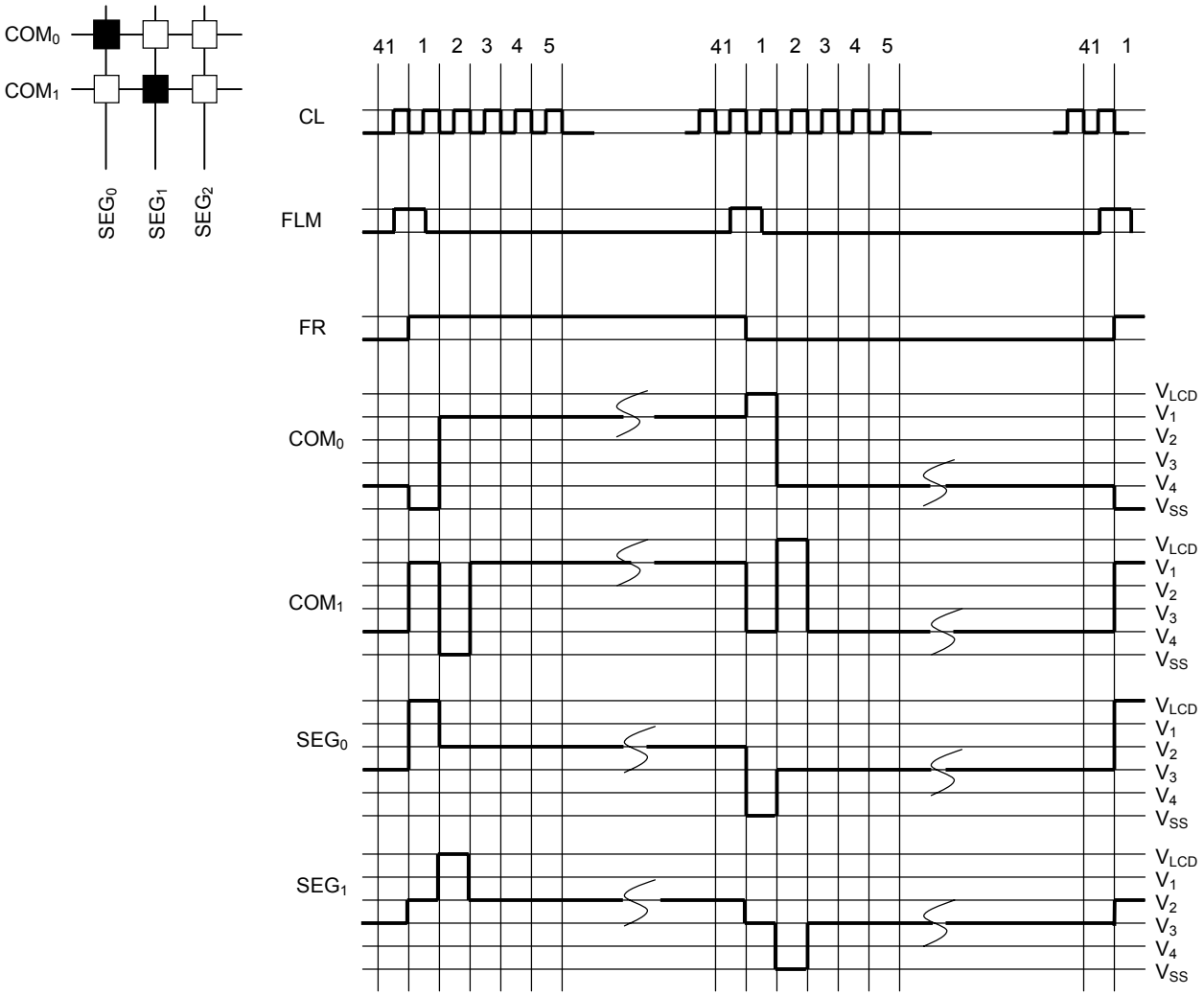


Fig 8

(18) Oscillator

The oscillator generates internal clocks for the display timing and the voltage booster. Since the LSI has internal capacitor (C) and resistor (R) for the oscillation, external capacitor and resistor are not usually required. However, in case that an external resistor is used, the resister is connected between the OSC1 and OSC2 terminals. The external resistor becomes enabled by setting "1" to the "CKS" register of "Data bus length" instruction. When the internal oscillator is not used, the external clocks with 50% duty cycle ratio must be input to the OSC1 terminal.

In addition, the feed back resister for the oscillation is varied by programming the "Rf" register of the "Frequency control" instruction, so that it is possible to optimize the frame frequency for a LCD panel. Setting examples of the MON (B&W /Gradation) and the PWM (Variable gradation /Fixed gradation) are described, as follows.

(18-1) Internal oscillation mode (CKS=0)

Symbol	MON	PWM	Display mode
f_1	0	0	Variable gradation mode
f_2	0	1	Fixed gradation mode
f_3	1	*	B&W mode

*: Don't care

(18-2) External resistor oscillation mode(CKS=1)

The internal clocks must be adjusted to the same frequency as the one in using the internal oscillation mode, and the "MON" and "PWM" registers must be set as well.

(18-3) External clock input mode (CKS=1)

The external clocks must be adjusted to the same frequency as the one in using the internal oscillation mode, and the "MON" and "PWM" registers must be set as well.

(19) Power supply circuits

The internal power supply circuits are composed of the voltage booster, the electrical variable resister (EVR), the voltage regulator, reference voltage generator and the voltage followers.

The condition of the power supply circuits is arranged by programming the "DCON" and "AMPON" registers on the "Power control" instruction. For this arrangement, same parts of the internal power supply circuits are activated in using an external power supply, as shown in the following table.

Table 14

DCON	AMPON	Voltage booster	Voltage followers Voltage regulator EVR	External voltage	Note
0	0	Disable	Disable	V_{OUT}, V_{LCD}, V_1, V_2, V_3, V_4	1, 3
0	1	Disable	Enable	V_{OUT}	2, 3
1	1	Enable	Enable	–	–

Note1) The internal power circuits are not used. The external V_{OUT} is required and the C1+, C1-, C2+, C2-, C3+, C3-, C4+, C4-, V_{OUT}, V_{REF}, V_{REG} and V_{EE} terminals must be open.

Note2) The internal power circuits except the voltage booster are used. The external V_{OUT} is required and the C1+, C1-, C2+, C2-, C3+, C3-, C4+, C4- and V_{EE} terminals must be open. The reference voltage is required to V_{REF} terminal.

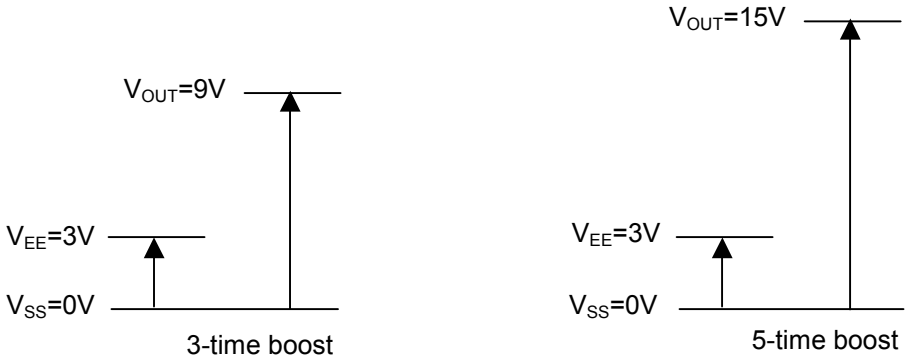
Note3) The relation among the voltages should be maintained as follows.

$V_{OUT} \geq V_{LCD} \geq V_1 \geq V_2 \geq V_3 \geq V_4 \geq V_{SS}$

(20) Voltage booster

The voltage booster generates maximum 5x voltage of the V_{EE} level. It is programmed so that the boost level is selected out of 1x, 2x, 3x, 4x, and 5x by the “Boost level select” instruction. The boosted voltage V_{OUT} must not exceed beyond the value of 18.0V, otherwise the voltage stress may cause a permanent damage to the LSI.

Boosted voltages



Capacitor connections for the voltage Booster

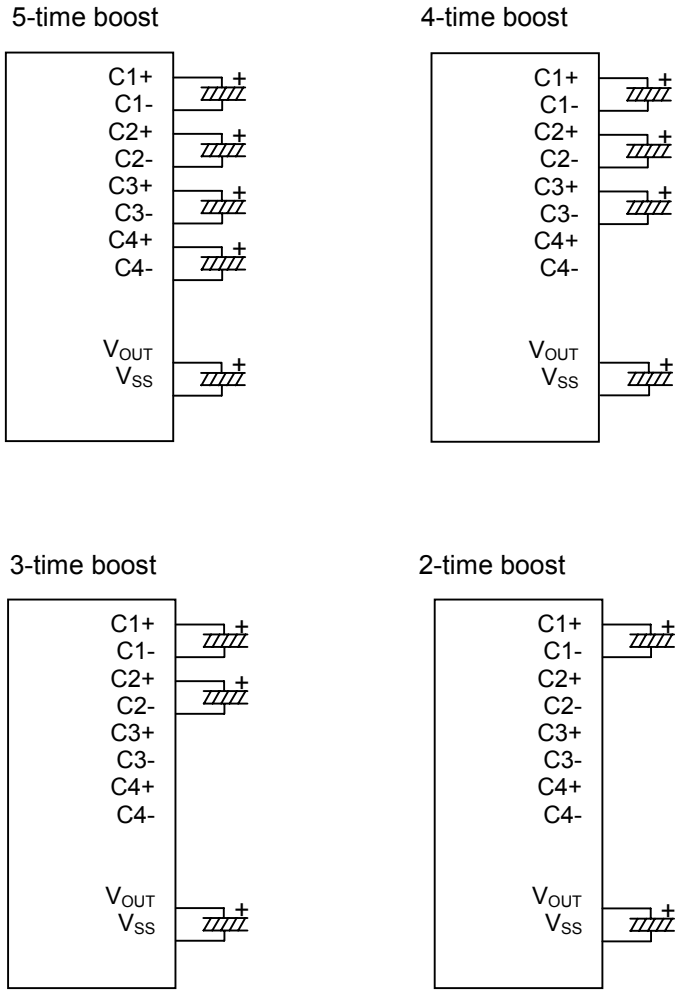


Fig 9

(21) Reference voltage generator

The reference voltage generator is used to produce the reference voltage (V_{BA}), which is output from the V_{BA} terminal and should be input to the V_{REF} terminal.

$$V_{BA} = V_{EE} \times 0.9$$

(22) Voltage regulator

The voltage regulator, composed of the gain control circuit and an operational amplifier, and is used to gain the reference voltage (V_{REF}) and to create the regulated voltage (V_{REG}). The V_{REG} is used as an input voltage to the EVR circuits, which is programmed by the “VU” register of the “Boost level” instruction.

$$V_{REG} = V_{REF} \times N \qquad \text{(N: register value for the boost level)}$$

(23) Electrical variable resister (EVR)

The EVR, variable within 128-step, and is used to fine-tune the LCD driving voltage (V_{LCD}) by programming the “DV” register in the “EVR control” instruction, so that it is possible to optimize the contrast level for a LCD panels.

$$V_{LCD} = 0.5 \times V_{REG} + M (V_{REG} - 0.5 \times V_{REG}) / 127 \quad \text{(M: register value for the EVR)}$$

(24) LCD driving voltage generation circuit

LCD driving voltage generation circuit generates the V_{LCD} voltage levels as V_{LCD}, V_1, V_2, V_3 and V_4 with internal E.V.R and the Bleeder resistors. The bias ratio of LCD driving voltage can be selected out of 1/4, 1/5, 1/6, 1/7 and 1/8.

In using the internal power supply, the capacitors CA_2 must be connected to the V_{LCD}, V_1, V_2, V_3 and V_4 terminals, and the CA_2 value must be determined by the evaluation with actual LCD modules.

In using the external power supply, the external LCD driving voltages such as the V_{LCD}, V_1, V_2, V_3 and V_4 are supplied and the internal power supply circuits must be set to “OFF” by DCON = AMPON = "0". In this mode, voltage booster terminals such as C1+, C1-, C2+, C2-, C3+, C3-, C4+, C4-, V_{EE}, V_{REF} and V_{REG} must be opened.

In case that the voltage booster is not used but only some parts of internal power supply circuits (Voltage followers, Voltage regulator and EVR) are used, the C1+, C1-, C2+, C2-, C3+, C3-, C4+ and C4- terminals must be opened. And, the external power supply is input to the V_{OUT} terminal, and the reference voltage to the V_{REF} terminal. The capacitor CA_3 must connect to the V_{REG} terminal for voltage stabilization.

Connections of the capacitor for the voltage booster

Using all of the internal power supply circuits
(5-time boost)

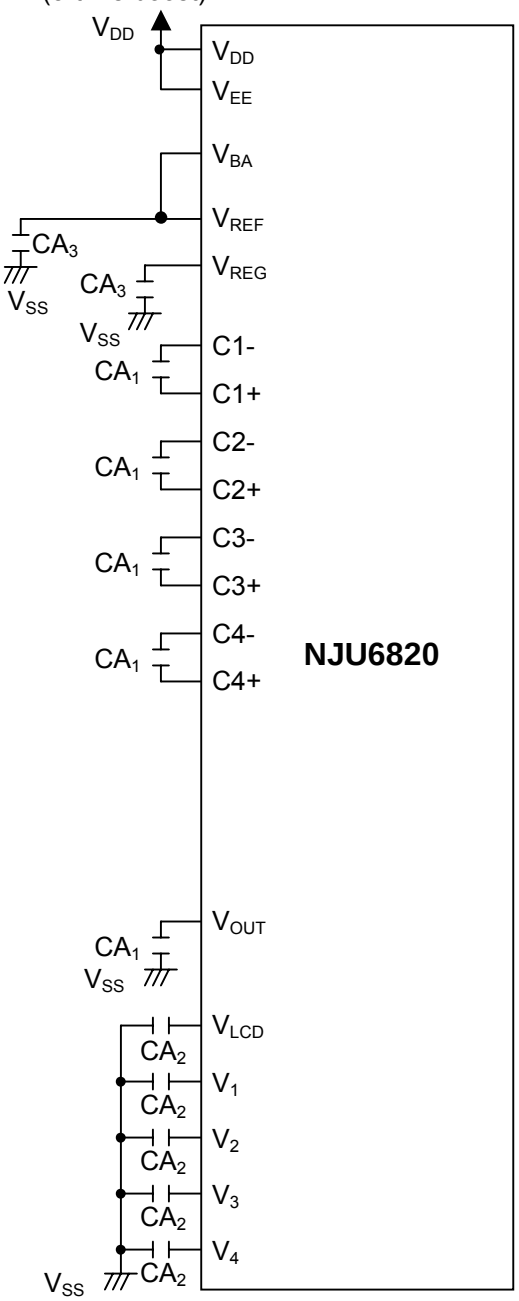


Fig 10

Using only external power supply circuits

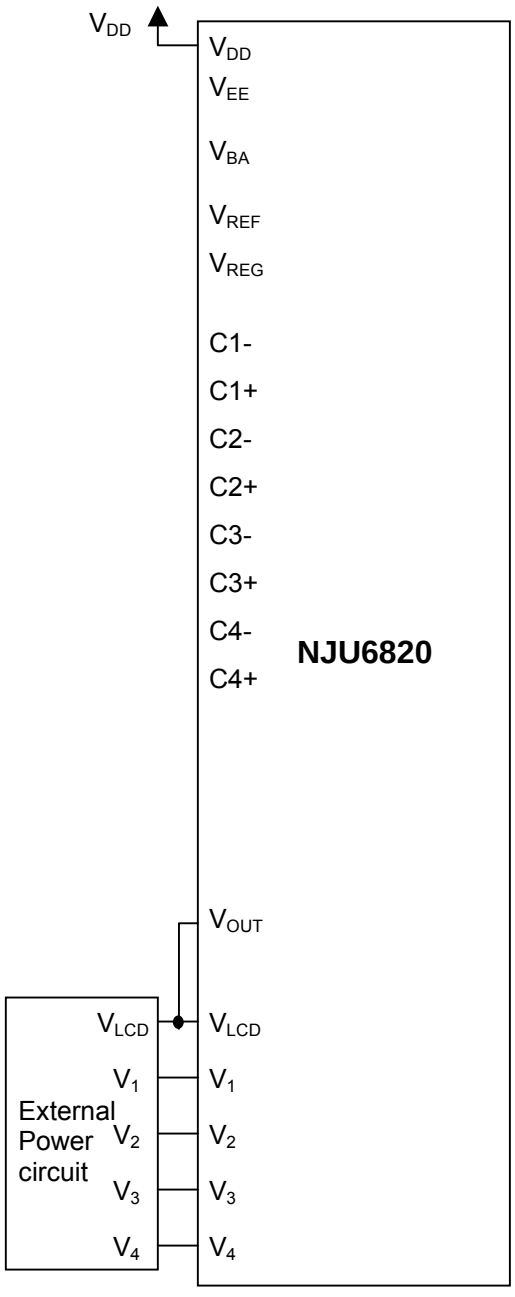


Fig11

Reference values

CA_1	1.0 to 4.7uF
CA_2	1.0 to 2.2uF
CA_3	0.1uF

Note) B grade capacitors are required.

Using internal power supply circuits
Without the reference voltage generator(1)
(5-time boost)

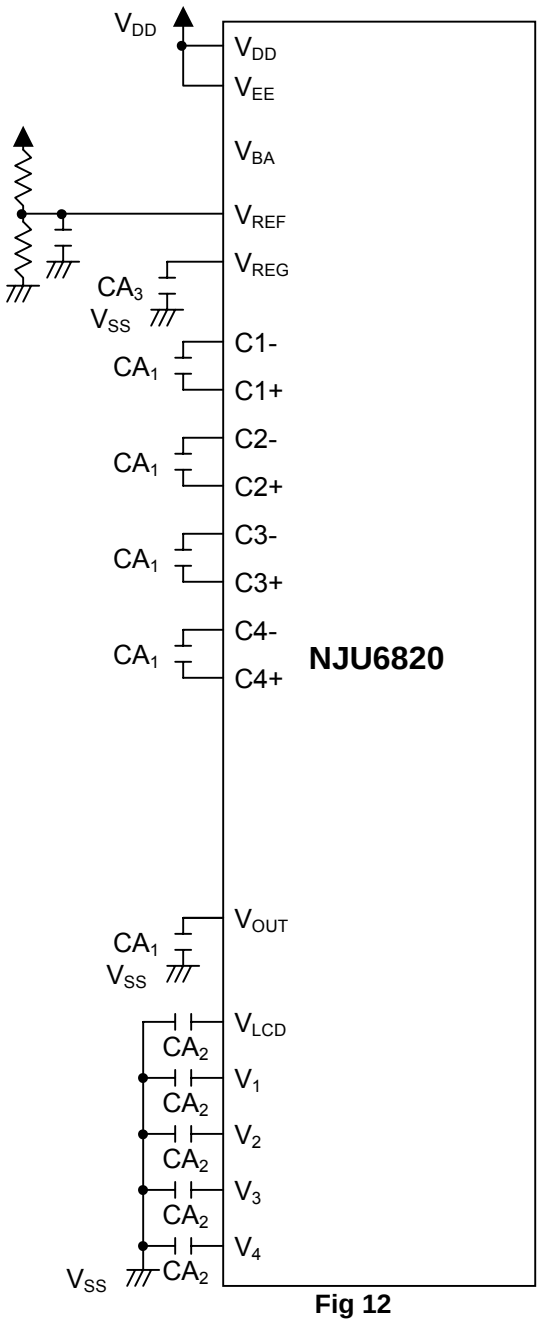


Fig 12

Using internal power supply circuit
Without the reference voltage generator(2)
(5-time boost)

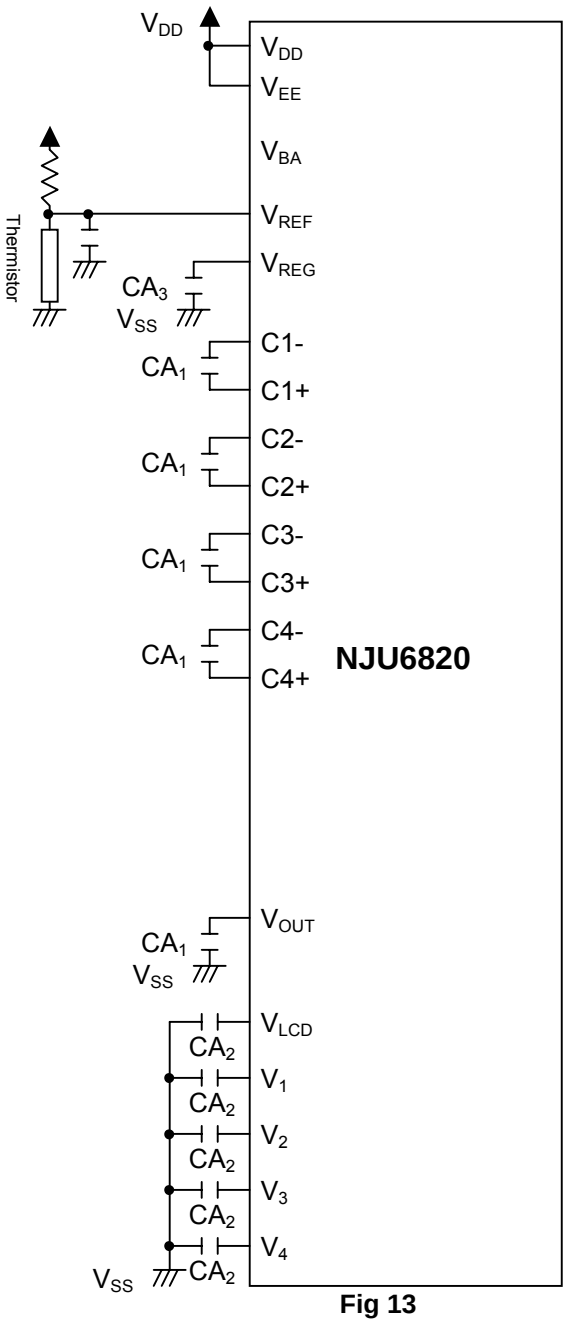


Fig 13

Reference value

CA_1	1.0 to 4.7µF
CA_2	1.0 to 2.2µF
CA_3	0.1µF

Note) B grade capacitors are required.

Using internal power supply circuits
Without the voltage booster

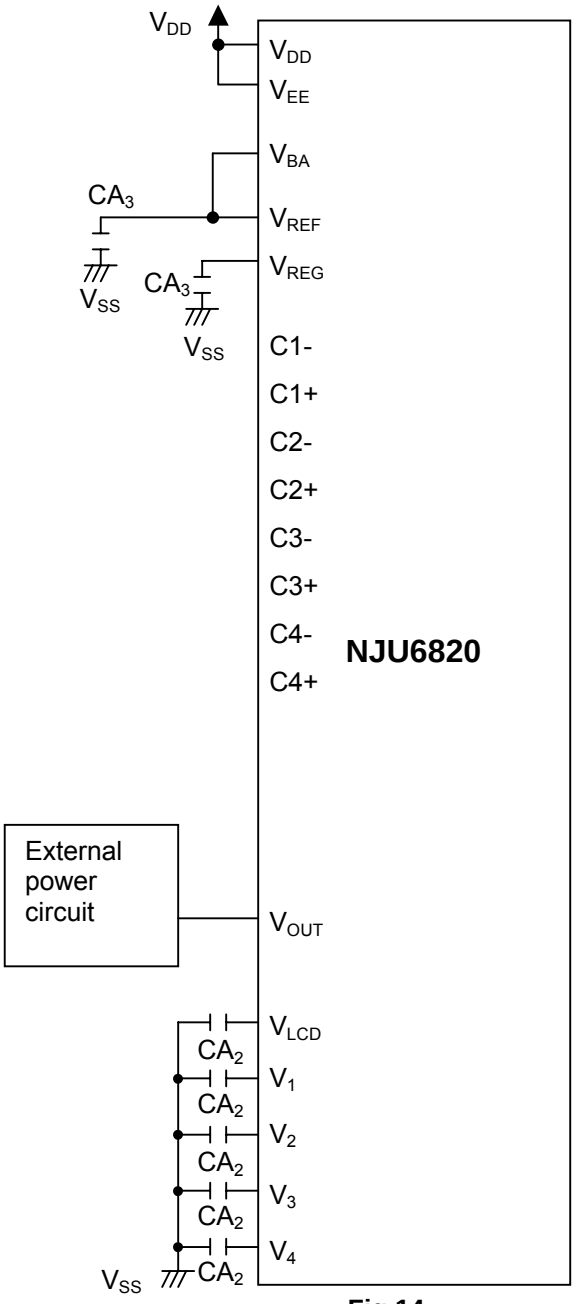


Fig 14

Reference value

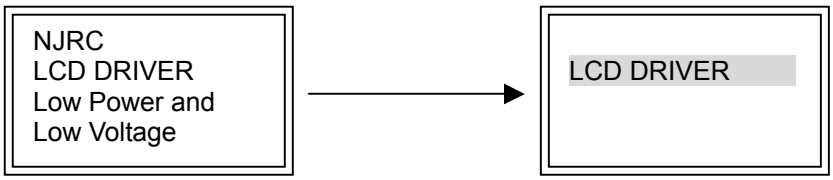
CA_1	1.0 to 4.7µF
CA_2	1.0 to 2.2µF
CA_3	0.1µF

Note) B grade capacitors are required.

(25) Partial display function

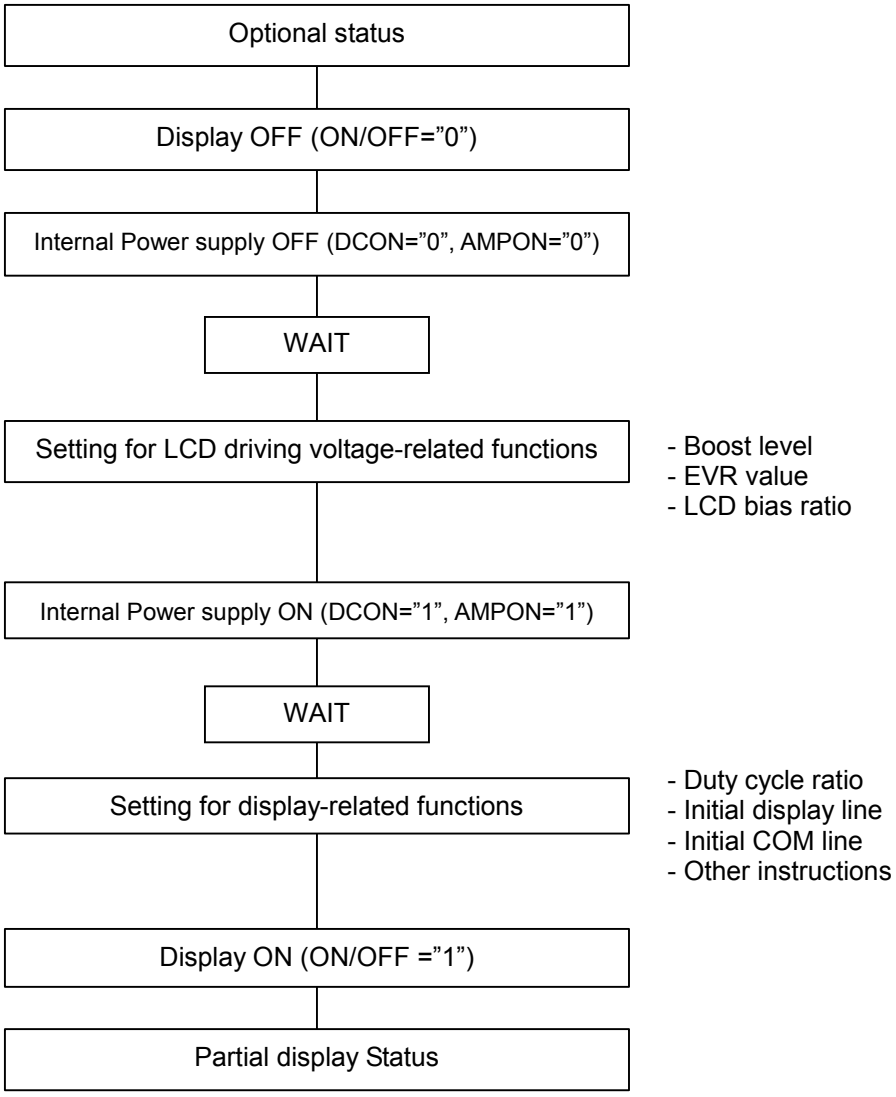
The partial display function is used to partially specify some parts of display area on LCD panels. By using this function, LCD modules can work in lower duty cycle ratio, lower LCD bias ratio, lower boost level and lower LCD driving voltage. It is usually used to display a time and calendar, and is also used to optimize the LSI condition in accordance with the display size. It can be programmed to select the duty cycle ratio (1/5, 1/9, 1/13, 1/17, 1/21, 1/25, 1/29, 1/33, 1/37, 1/41 in case "DSE" is "0"), the LCD bias ratio, the boost level and the EVR value by the instructions.

Partial display image



Normal display　　Partial display

Partial display sequence



(26) Discharge circuit

Discharge circuit is used to discharge the electric charge of the capacitors on the V_1 to V_4 and V_{LCD} terminals. This circuit is activated by setting “0” to the “DIS” register of the “Discharge” instruction or by setting “RESb” terminal to ”0” level. The “Discharge ON/OFF” instruction is usually required just after the internal power supply is turned off by setting “0” into the “DCON” and “AMPON” registers, or just after the external power supply is turned off. During the discharge operation, the internal or external power supply must not be turned on.

(27) Reset circuit

The reset circuit initializes the LSI into the following default status. It is activated by setting the RESb terminal to “0”. The RESB terminal is usually required to connect to MPU reset terminal in order that the LSI can be initialized at the same timing of the MPU.

- Default status

1. DDRAM display data :Undefined
2. column address :$(00)_H$
3. row address :$(00)_H$
4. Initial display line :$(0)_H$ (1st line)
5. Display ON/OFF :OFF
6. Reverse display ON/OFF :OFF (normal)
7. Duty cycle ratio :1/41 duty(DSE=0)
8. N-line Inversion ON/OFF :OFF
9. COM scan direction :$COM_0 \rightarrow COM_{39}$
10. Increment mode :OFF
11. Reverse SEG direction :OFF (normal)
12. SWAP mode :OFF (normal)
13. EVR value :(0, 0, 0, 0, 0, 0, 0)
14. Internal power supply :OFF
15. Display mode :Gradation display mode
16. LCD bias ratio :1/8 bias
17. Gradation Palette 0 :(0, 0, 0, 0, 0)
18. Gradation Palette 1 :(0, 0, 0, 1, 1)
19. Gradation Palette 2 :(0, 0, 1, 0, 1)
20. Gradation Palette 3 :(0, 0, 1, 1, 1)
21. Gradation Palette 4 :(0, 1, 0, 0, 1)
22. Gradation Palette 5 :(0, 1, 0, 1, 1)
23. Gradation Palette 6 :(0, 1, 1, 0, 1)
24. Gradation Palette 7 :(0, 1, 1, 1, 1)
25. Gradation Palette 8 :(1, 0, 0, 0, 1)
26. Gradation Palette 9 :(1, 0, 0, 1, 1)
27. Gradation Palette 10 :(1, 0, 1, 0, 1)
28. Gradation Palette 11 :(1, 0, 1, 1, 1)
29. Gradation Palette 12 :(1, 1, 0, 0, 1)
30. Gradation Palette 13 :(1, 1, 0, 1, 1)
31. Gradation Palette 14 :(1, 1, 1, 0, 1)
32. Gradation Palette 15 :(1, 1, 1, 1, 1)
33. Gradation mode control :Variable gradation mode
34. Data bus length :8-bit data bus length
35. Discharge circuit :(DIS/DIS2) : ”0”

(28) Power supply ON/OFF sequences

The following paragraphs describe power supply ON/OFF sequences, which are to protect the LSI from over current.

(28-1) Using an external power supply

- Power supply ON sequence

  Logic voltage (V_{DD}) must be always input first, and next the LCD driving voltages (V_1 to V_4 and V_{LCD}) are turned on. In using the external V_{OUT}, the V_{DD} must be input first, next the reset operation must be performed, and finally the V_{OUT} can be input.

- Power supply OFF sequence

  Either the reset operation, cutting off the V_1 to V_4 and V_{LCD} from the LSI by the RESb terminal or the "Power control" instruction must be performed first, and next the V_{DD} is turned off. It is recommended that a series-resister between 50 Ω and 100 Ω is added on the V_{LCD} line (or V_{OUT} line in using only the external V_{OUT} voltage) in order to protect the LSI from the over current.

(28-2) Using the internal power supply circuits

- Power supply ON sequence

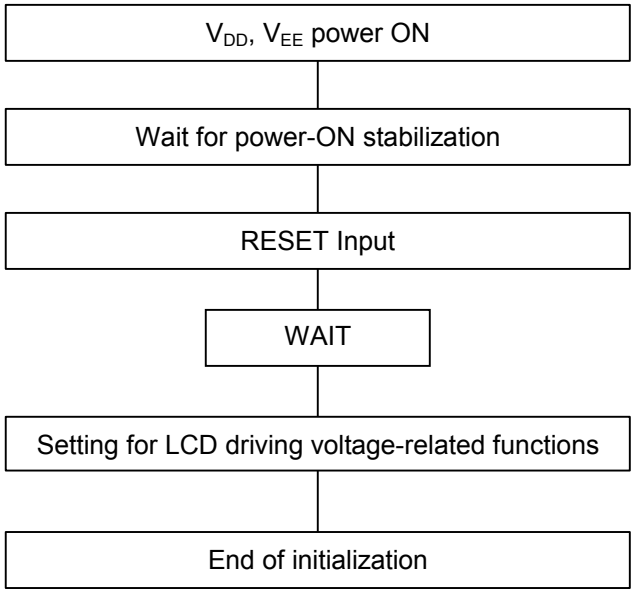
  The V_{DD} must be input first, next the reset operation must be performed, and finally the V_1 to V_4 and V_{LCD} can be turned on by setting "1" to the "DCON" and "AMPON" registers of the "Power control" instruction.

- Power supply OFF sequence

  Either the reset operation by the RESb terminal or the "Power control" instruction must be performed first, and next the input voltage for the voltage booster (V_{EE}) and the V_{DD} can be turned off. If the V_{EE} is supplied from different power sources for V_{DD}, the V_{EE} is turned off first, and next the V_{DD} is turned off.

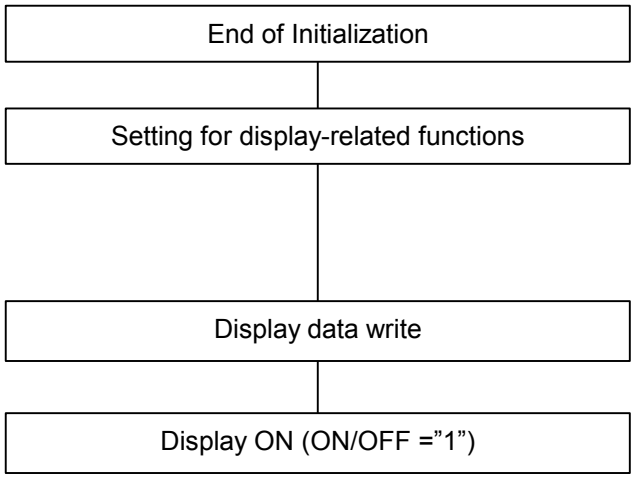
(29) Referential instruction sequences

(29-1) Initialization in using the internal power supply circuits



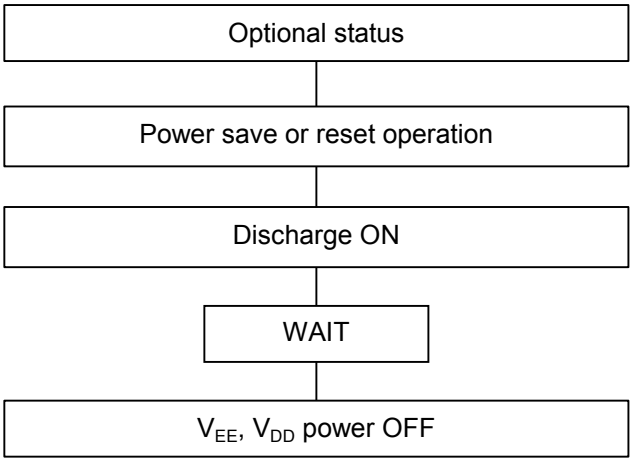
- EVR value
- LCD bias ratio
- Power control (DCON="1", AMPON="1")

(29-2) Display data writing



- Initial display line
- Increment mode
- column address
- row address

(29-3) Power OFF



- All COM/SEG output V_{SS} level.

(30) Instruction table

Instruction Table (1)

Instructions	Code (80 series MPU I/F)							Code								Functions
	CSB	RS	RDB	WRB	RE_2	RE_1	RE_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
Display data write	0	0	1	0	0/1	0/1	0/1	Write Data								Write display data to DDRAM
Display data read	0	0	0	1	0/1	0/1	0/1	Read Data								Read display data from DDRAM
column address (Lower) [0_H]	0	1	1	0	0	0	0	0	0	0	0	AX3	AX2	AX1	AX0	DDRAM column address
column address (Upper) [1_H]	0	1	1	0	0	0	0	0	0	0	1	AX7	AX6	AX5	AX4	DDRAM column address
row address (Lower) [2_H]	0	1	1	0	0	0	0	0	0	1	0	AY3	AY2	AY1	AY0	DDRAM row address
row address (Upper) [3_H]	0	1	1	0	0	0	0	0	0	1	1	*	*	AY5	AY4	DDRAM row address
Initial display line (Lower) [4_H]	0	1	1	0	0	0	0	0	1	0	0	LA3	LA2	LA1	LA0	Row address for an initial COM line (Scan start line)
Initial display line (Upper) [5_H]	0	1	1	0	0	0	0	0	1	0	1	*	*	LA5	LA4	Row address for an initial COM line (Scan start line)
N-line inversion (Lower) [6_H]	0	1	1	0	0	0	0	0	1	1	0	N3	N2	N1	N0	The number of N-line inversion
N-line inversion (Upper) [7_H]	0	1	1	0	0	0	0	0	1	1	1	*	*	N5	N4	The number of N-line inversion
Display control (1) [8_H]	0	1	1	0	0	0	0	1	0	0	0	SHIFT	MON	ALL ON	ON/ OFF	SHIFT: Common direction MON: Gradation or B/W display mode ALLON: All pixels ON/OFF ON/OFF: Display ON/OFF
Display control (2) [9_H]	0	1	1	0	0	0	0	1	0	0	1	REV	NLIN	SWAP	REF	REV: Reverse display ON/OFF NLIN: N-line inversion ON/OFF, SWAP: SWAP mode ON/OFF REF: Segment direction
Increment control [A_H]	0	1	1	0	0	0	0	1	0	1	0	WIN	AIM	AYI	AXI	WIN: Window addressing mode ON/OFF AIM: Read-modify-write ON/OFF AYI: Row auto-increment mode ON/OFF AXI: column auto-increment mode ON/OFF
Power control [B_H]	0	1	1	0	0	0	0	1	0	1	1	AMP ON	HALT	DC ON	ACL	AMPON: Voltage followers ON/OFF HALT: Power save ON/OFF DCON: Voltage booster ON/OFF ACL: Reset
Duty cycle ratio [C_H]	0	1	1	0	0	0	0	1	1	0	0	DS3	DS2	DS1	DS0	Sets LCD duty cycle ratio
Boost level [D_H]	0	1	1	0	0	0	0	1	1	0	1	*	VU2	VU1	VU0	Sets boost level
LCD bias ratio [E_H]	0	1	1	0	0	0	0	1	1	1	0	*	B2	B1	B0	Sets LCD bias ratio
RE register [F_H]	0	1	1	0	0/1	0/1	0/1	1	1	1	1	TST_0	RE_2	RE_1	RE_0	RE flag set

Note 1) * : Don't care.

Note 2) [N_H] : Address of instruction register

Note 3) The dual instructions including upper and lower bytes is enabled after either upper or lower bytes are set into the register. The only "EVR control" instruction is enabled after both of the upper and lower bytes are set.

Instruction Table (2)

Instructions	Code (80 series MPU I/F)							Code								Functions
	CSB	RS	RDB	WRB	RE_2	RE_1	RE_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
Gradation palette A0/A8 (Lower) [0_H]	0	1	1	0	0	0	1	0	0	0	0	PA03/ PA83	PA02/ PA82	PA01/ PA81	PA00/ PA80	Sets palette values to gradation palette A0(PS=0)/A8(PS=1)
Gradation palette A0/A8 (Upper) [1_H]	0	1	1	0	0	0	1	0	0	0	1	*	*	*	PA04/ PA84	Sets palette values to gradation palette A0(PS=0)/A8(PS=1)
Gradation palette A1/A9 (Lower) [2_H]	0	1	1	0	0	0	1	0	0	1	0	PA13/ PA93	PA12/ PA92	PA11/ PA91	PA10/ PA90	Sets palette values to gradation palette A1(PS=0)/A9(PS=1)
Gradation palette A1/A9 (Upper) [3_H]	0	1	1	0	0	0	1	0	0	1	1	*	*	*	PA14/ PA94	Sets palette values to gradation palette A1(PS=0)/A9(PS=1)
Gradation palette A2/A10 (Lower) [4_H]	0	1	1	0	0	0	1	0	1	0	0	PA23/ PA103	PA22/ PA102	PA21/ PA101	PA20/ PA100	Sets palette values to gradation palette A2(PS=0)/A10(PS=1)
Gradation palette A2/A10 (Upper) [5_H]	0	1	1	0	0	0	1	0	1	0	1	*	*	*	PA24/ PA104	Sets palette values to gradation palette A2(PS=0)/A10(PS=1)
Gradation palette A3/A11 (Lower) [6_H]	0	1	1	0	0	0	1	0	1	1	0	PA33/ PA113	PA32/ PA112	PA31/ PA111	PA30/ PA110	Sets palette values to gradation palette A3(PS=0)/A11(PS=1)
Gradation palette A3/A11 (Upper) [7_H]	0	1	1	0	0	0	1	0	1	1	1	*	*	*	PA34/ PA114	Sets palette values to gradation palette A3(PS=0)/A11(PS=1)
Gradation palette A4/A12 (Lower) [8_H]	0	1	1	0	0	0	1	1	0	0	0	PA43/ PA123	PA42/ PA122	PA41/ PA121	PA40/ PA120	Sets palette values to gradation palette A4(PS=0)/A12(PS=1)
Gradation palette A4/A12 (Upper) [9_H]	0	1	1	0	0	0	1	1	0	0	1	*	*	*	PA44/ PA124	Sets palette values to gradation palette A4(PS=0)/A12(PS=1)
Gradation palette A5/A13 (Lower) [A_H]	0	1	1	0	0	0	1	1	0	1	0	PA53/ PA133	PA52/ PA132	PA51/ PA131	PA50/ PA130	Sets palette values to gradation palette A5(PS=0)/A13(PS=1)
Gradation palette A5/A13 (Upper) [B_H]	0	1	1	0	0	0	1	1	0	1	1	*	*	*	PA54/ PA134	Sets palette values to gradation palette A5(PS=0)/A13(PS=1)
Gradation palette A6/A14 (Lower) [C_H]	0	1	1	0	0	0	1	1	1	0	0	PA63/ PA143	PA62/ PA142	PA61/ PA141	PA60/ PA140	Sets palette values to gradation palette A6(PS=0)/A14(PS=1)
Gradation palette A6/A14 (Upper) [D_H]	0	1	1	0	0	0	1	1	1	0	1	*	*	*	PA64/ PA144	Sets palette values to gradation palette A6(PS=0)/A14(PS=1)
RE register [F_H]	0	1	1	0	0/1	0/1	0/1	1	1	1	1	TST_0	RE_2	RE_1	RE_0	RE flag set

Note 1) * : Don't care.
Note 2) [N_H] : Address of Instruction register
Note 3) The dual instructions including upper and lower bytes is enabled after either upper or lower bytes are set into the register. The only "EVR control" instruction is enabled after both of the upper and lower bytes are set.

Instruction Table (3)

Instructions	Code (80 series MPU I/F)							Code								Functions
	CSB	RS	RDB	WRB	RE_2	RE_1	RE_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
Gradation palette A7/A15 (Lower) [0_H]	0	1	1	0	0	1	0	0	0	0	0	PA73/ PA153	PA72/ PA152	PA71/ PA151	PA70/ PA150	Sets palette values to gradation palette A7(PS=0)/A15(PS=1)
Gradation palette A7/A15 (Upper) [1_H]	0	1	1	0	0	1	0	0	0	0	1	*	*	*	PA74/ PA154	Sets palette values to gradation palette A7(PS=0)/A15(PS=1)
Gradation palette B0/B8 (Lower) [2_H]	0	1	1	0	0	1	0	0	0	1	0	PB03/ PB83	PB02/ PB82	PB01/ PB81	PB00/ PB80	Sets palette values to gradation palette B0(PS=0)/B8(PS=1)
Gradation palette B0/B8 (Upper) [3_H]	0	1	1	0	0	1	0	0	0	1	1	*	*	*	PB04/ PB84	Sets palette values to gradation palette B0(PS=0)/B8(PS=1)
Gradation palette B1/B9 (Lower) [4_H]	0	1	1	0	0	1	0	0	1	0	0	PB13/ PB93	PB12/ PB92	PB11/ PB91	PB10/ PB90	Sets palette values to gradation palette B1(PS=0)/B9(PS=1)
Gradation palette B1/B9 (Upper) [5_H]	0	1	1	0	0	1	0	0	1	0	1	*	*	*	PB14/ PB94	Sets palette values to gradation palette B1(PS=0)/B9(PS=1)
Gradation palette B2/B10 (Lower) [6_H]	0	1	1	0	0	1	0	0	1	1	0	PB23/ PB103	PB22/ PB102	PB21/ PB101	PB20/ PB100	Sets palette values to gradation palette B2(PS=0)/B10(PS=1)
Gradation palette B2/B10 (Upper) [7_H]	0	1	1	0	0	1	0	0	1	1	1	*	*	*	PB24/ PB104	Sets palette values to gradation palette B2(PS=0)/B10(PS=1)
Gradation palette B3/B11 (Lower) [8_H]	0	1	1	0	0	1	0	1	0	0	0	PB33/ PB113	PB32/ PB112	PB31/ PB111	PB30/ PB110	Sets palette values to gradation palette B3(PS=0)/B11(PS=1)
Gradation palette B3/B11 (Upper) [9_H]	0	1	1	0	0	1	0	1	0	0	1	*	*	*	PB34/ PB114	Sets palette values to gradation palette B3(PS=0)/B11(PS=1)
Gradation palette B4/B12 (Lower) [A_H]	0	1	1	0	0	1	0	1	0	1	0	PB43/ PB123	PB42/ PB122	PB41/ PB121	PB40/ PB120	Sets palette values to gradation palette B4(PS=0)/B12(PS=1)
Gradation palette B4/B12 (Upper) [B_H]	0	1	1	0	0	1	0	1	0	1	1	*	*	*	PB44/ PB124	Sets palette values to gradation palette B4(PS=0)/B12(PS=1)
Gradation palette B5/B13 (Lower) [C_H]	0	1	1	0	0	1	0	1	1	0	0	PB53/ PB133	PB52/ PB132	PB51/ PB131	PB50/ PB130	Sets palette values to gradation palette B5(PS=0)/B13(PS=1)
Gradation palette B5/B13 (Upper) [D_H]	0	1	1	0	0	1	0	1	1	0	1	*	*	*	PB54/ PB134	Sets palette values to gradation palette B5(PS=0)/B13(PS=1)
RE register [F_H]	0	1	1	0	0/1	0/1	0/1	1	1	1	1	TST_0	RE_2	RE_1	RE_0	RE flag set

Note 1) * : Don't care.
Note 2) [N_H] : Address of Instruction register
Note 3) The dual instructions including upper and lower bytes is enabled after either upper or lower bytes are set into the register. The only "EVR control" instruction is enabled after both of the upper and lower bytes are set.

Instruction Table (4)

Instructions	Code (80 series MPU I/F)							Code								Functions
	CSB	RS	RDB	WRB	RE_2	RE_1	RE_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
Gradation palette B6/B14 (Lower) [0_H]	0	1	1	0	0	1	1	0	0	0	0	PB63/ PB143	PB62/ PB142	PB61/ PB141	PB60/ PB140	Sets palette values to gradation palette B6(PS=0)/B14(PS=1)
Gradation palette B6/B14 (Upper) [1_H]	0	1	1	0	0	1	1	0	0	0	1	*	*	*	PB64/ PB144	Sets palette values to gradation palette B6(PS=0)/B14(PS=1)
Gradation palette B7/B15 (Lower) [2_H]	0	1	1	0	0	1	1	0	0	1	0	PB73/ PB153	PB72/ PB152	PB71/ PB151	PB70/ PB150	Sets palette values to gradation palette B7(PS=0)/B15(PS=1)
Gradation palette B7/B15 (Upper) [3_H]	0	1	1	0	0	1	1	0	0	1	1	*	*	*	PB74/ PB154	Sets palette values to gradation palette B7(PS=0)/B15(PS=1)
Gradation palette C0/C8 (Lower) [4_H]	0	1	1	0	0	1	1	0	1	0	0	PC03/ PC83	PC02/ PC82	PC01/ PC81	PC00/ PC80	Sets palette values to gradation palette C0(PS=0)/C8(PS=1)
Gradation palette C0/C8 (Upper) [5_H]	0	1	1	0	0	1	1	0	1	0	1	*	*	*	PC04/ PC84	Sets palette values to gradation palette C0(PS=0)/C8(PS=1)
Gradation palette C1/C9 (Lower) [6_H]	0	1	1	0	0	1	1	0	1	1	0	PC13/ PC93	PC12/ PC92	PC11/ PC91	PC10/ PC90	Sets palette values to gradation palette C1(PS=0)/C9(PS=1)
Gradation palette C1/C9 (Upper) [7_H]	0	1	1	0	0	1	1	0	1	1	1	*	*	*	PC14/ PC94	Sets palette values to gradation palette C1(PS=0)/C9(PS=1)
Gradation palette C2/C10 (Lower) [8_H]	0	1	1	0	0	1	1	1	0	0	0	PC23/ PC103	PC22/ PC102	PC21/ PC101	PC20/ PC100	Sets palette values to gradation palette C2(PS=0)/C10(PS=1)
Gradation palette C2/C10 (Upper) [9_H]	0	1	1	0	0	1	1	1	0	0	1	*	*	*	PC24/ PC104	Sets palette values to gradation palette C2(PS=0)/C10(PS=1)
Gradation palette C3/C11 (Lower) [A_H]	0	1	1	0	0	1	1	1	0	1	0	PC33/ PC113	PC32/ PC112	PC31/ PC111	PC30/ PC110	Sets palette values to gradation palette C3(PS=0)/C11(PS=1)
Gradation palette C3/C11 (Upper) [B_H]	0	1	1	0	0	1	1	1	0	1	1	*	*	*	PC34/ PC114	Sets palette values to gradation palette C3(PS=0)/C11(PS=1)
Gradation palette C4/C12 (Lower) [C_H]	0	1	1	0	0	1	1	1	1	0	0	PC43/ PC123	PC42/ PC122	PC41/ PC121	PC40/ PC120	Sets palette values to gradation palette C4(PS=0)/C12(PS=1)
Gradation palette C4/C12 (Upper) [D_H]	0	1	1	0	0	1	1	1	1	0	1	*	*	*	PC44/ PC124	Sets palette values to gradation palette C4(PS=0)/C12(PS=1)
RE register [F_H]	0	1	1	0	0/1	0/1	0/1	1	1	1	1	TST_0	RE_2	RE_1	RE_0	RE flag set

Note 1) * : Don't care.

Note 2) [N_H] : Address of Instruction register

Note 3) The dual instructions including upper and lower bytes is enabled after either upper or lower bytes are set into the register. The only "EVR control" instruction is enabled after both of the upper and lower bytes are set.

Instruction Table (5)

Instructions	Code (80 series MPU I/F)							Code								Functions
	CSB	RS	RDB	WRB	RE_2	RE_1	RE_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
Gradation palette C5/C13 (Lower) [0_H]	0	1	1	0	1	0	0	0	0	0	0	PC53/ PC133	PC52/ PC132	PC51/ PC131	PC50/ PC130	Sets palette values to gradation palette C5(PS=0)/C13(PS=1)
Gradation palette C5/C13 (Upper) [1_H]	0	1	1	0	1	0	0	0	0	0	1	*	*	*	PC54/ PC134	Sets palette values to gradation palette C5(PS=0)/C13(PS=1)
Gradation palette C6/C14 (Lower) [2_H]	0	1	1	0	1	0	0	0	0	1	0	PC63/PC143	PC62/ PC142	PC61/ PC141	PC60/ PC140	Sets palette values to gradation palette C6(PS=0)/C14(PS=1)
Gradation palette C6/C14 (Upper) [3_H]	0	1	1	0	1	0	0	0	0	1	1	*	*	*	PC64/ PC144	Sets palette values to gradation palette C6(PS=0)/C14(PS=1)
Gradation palette C7/C15 (Lower) [4_H]	0	1	1	0	1	0	0	0	1	0	0	PC73/ PC153	PC72/ PC152	PC71/ PC151	PC70/ PC150	Sets palette values to gradation palette C7(PS=0)/C15(PS=1)
Gradation palette C7/C15 (Upper) [5_H]	0	1	1	0	1	0	0	0	1	0	1	*	*	*	PC74/ PC154	Sets palette values to gradation palette C7(PS=0)/C15(PS=1)
Initial COM line [6_H]	0	1	1	0	1	0	0	0	1	1	0	SC3	SC2	SC1	SC0	Sets scan-starting common driver
Display control Signal/ Duty Select [7_H]	0	1	1	0	1	0	0	0	1	1	1	*	*	DSE	SON	SON : Display clock ON/OFF DSE : Duty-1 ON/OFF
Gradation mode control [8_H]	0	1	1	0	1	0	0	1	0	0	0	PWM	C256	*	*	PWM : Variable/Fixed gradation mode C256 : 256-Color Mode ON/OFF
Data bus length [9_H]	0	1	1	0	1	0	0	1	0	0	1	HSW	ABS	CKS	WLS	HSW : High speed access ON/OFF ABS : ABS mode ON/OFF CKS : Internal/external oscilation WLS : Display data Length
EVR control (Lower) [A_H]	0	1	1	0	1	0	0	1	0	1	0	DV3	DV2	DV1	DV0	Sets EVR level (Lower bit)
EVR control (Upper) [B_H]	0	1	1	0	1	0	0	1	0	1	1	*	DV6	DV5	DV4	Sets EVR level (Upper bit)
Frequency control [D_H]	0	1	1	0	1	0	0	1	1	0	1	*	RF2	RF1	RF0	Oscillation frequency
Discharge ON/OFF [E_H]	0	1	1	0	1	0	0	1	1	1	0	*	*	DIS2	DIS	Discharge the electric charge in capacitors on V_1 to V_4 and V_{LCD}
RE register [F_H]	0	1	1	0	0/1	0/1	0/1	1	1	1	1	TST_0	RE_2	RE_1	RE_0	RE flag
Instruction register address [C_H]	0	1	1	0	1	0	0	1	1	0	0	Reading address				Sets instruction register address
Instruction register read	0	1	0	1	0/1	0/1	0/1	*	*	*	*	Read Data				Read out instruction register data

Note 1) * : Don't care.

Note 2) [N_H] : Address of Instruction register

Note 3) The dual instructions including upper and lower bytes is enabled after either upper or lower bytes are set into the register. The only "EVR control" instruction is enabled after both of the upper and lower bytes are set.

Note 4) CKS=0: Internal oscillation mode (default)
CKS=1: External oscillation mode

Instruction Table (6)

Instructions	Code (80 series MPU I/F)							Code								Functions
	CSB	RS	RDB	WRB	RE_2	RE_1	RE_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
Window end column address (Lower) [0_H]	0	1	1	0	1	0	1	0	0	0	0	EX3	EX2	EX1	EX0	Sets column address for end point
Window end column address (Upper) [1_H]	0	1	1	0	1	0	1	0	0	0	1	EX7	EX6	EX5	EX4	Sets column address for end point
Window end row address (Lower) [2_H]	0	1	1	0	1	0	1	0	0	1	0	EY3	EY2	EY1	EY0	Sets row address for end point
Window end row address (Upper) [3_H]	0	1	1	0	1	0	1	0	0	1	1	*	*	EY5	EY4	Sets row address for end point
Initial reverse line (Lower) [4_H]	0	1	1	0	1	0	1	0	1	0	0	LS3	LS2	LS1	LS0	Sets address for reverse line
Initial reverse line (Upper) [5_H]	0	1	1	0	1	0	1	0	1	0	1	*	*	LS5	LS4	Sets address for reverse line
Last reverse line (Lower) [6_H]	0	1	1	0	1	0	1	0	1	1	0	LE3	LE2	LE1	LE0	Sets address for reverse line
Last reverse line (Upper) [7_H]	0	1	1	0	1	0	1	0	1	1	1	*	*	LE5	LE4	Sets address for reverse line
Reverse line display ON/OFF [8_H]	0	1	1	0	1	0	1	1	0	0	0	*	*	BT	LREV	BT : Blink type setting LREV : Reverse line display ON/OFF
Gradation palette setting control / Icon SEG address set [9_H]	0	1	1	0	1	0	1	1	0	0	1	*	*	*	PS	PS : gradation setting
PWM control [A_H]	0	1	1	0	1	0	1	1	0	1	0	PWMS	PWMA	PWMB	PWMC	Sets PWM mode
RE register [F_H]	0	1	1	0	0/1	0/1	0/1	1	1	1	1	TST_0	RE_2	RE_1	RE_0	RE flag

Note 1) * : Don't care.

Note 2) [N_H] : Address of Instruction register

Note 3) The dual instructions including upper and lower bytes is enabled after either upper or lower bytes are set into the register. The only "EVR control" instruction is enabled after both of the upper and lower bytes are set.

(31) Instruction descriptions

This chapter provides detail descriptions and instruction registers. Nonexistent instruction codes must not be set into the LSI.

(31-1) Display data write

The “Display data write” instruction is used to write 8-bit display data into the DDRAM.

CSB	RS	RDb	WRb	RE_2	RE_1	RE_0
0	0	1	0	0/1	0/1	0/1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Display data							

(31-2) Display data read

The “Display data read” instruction is used to read out 8-bit display data from the DDRAM, where the column address and row address must be specified beforehand by the “column address” and “row address” instructions. The dummy read is required just after the “column address” and “row address” instructions.

CSB	RS	RDb	WRb	RE_2	RE_1	RE_0
0	0	0	1	0/1	0/1	0/1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Display data							

(31-3) Column address

The “column address” instruction is used to specify the column address for the display data’s reading and writing operations. It requires dual bytes for lower 4-bit and upper 4-bit data. The instruction for the lower 4-bit data must be executed first, next the instruction for the upper 4-bit.

CSB	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	0	0	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	0	0	0	AX_3	AX_2	AX_1	AX_0

CSB	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	0	0	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	0	0	1	AX_7	AX_6	AX_5	AX_4

(31-4) Row address

The “row address” instruction is used to specify the row address for the display data read and write operations. It requires dual bytes for lower 4-bit and upper 2-bit data. The instruction for the lower 4-bit data must be executed first, next the instruction for upper 2-bit. The row address is specified in between 00_H and 27_H. The setting for nonexistent row address between 28_H and $3F_H$ is prohibited.

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	0	0	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	0	1	0	AY_3	AY_2	AY_1	AY_0

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	0	0	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	0	1	1	*	*	AY_5	AY_4

(31-5) Initial display line

The “Initial display line” instruction is used to specify the line address corresponding to the initial COM line. The initial COM line specified by the “Initial COM line” instruction and indicates the common driver that starts scanning data.

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	0	0	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	0	0	LA_3	LA_2	LA_1	LA_0

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	0	0	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	0	1	*	*	LA_5	LA_4

LA_5	LA_4	LA_3	LA_2	LA_1	LA_0	Line Address
0	0	0	0	0	0	0
0	0	0	0	0	1	1
			:			:
1	0	0	1	1	1	39

(31-6) N-line inversion

The “N-line inversion” instruction is used to control the alternate rates of the liquid crystal direction. It is programmed to select the N value between 2 and 39, and the FR signal toggles once every N lines by setting “1” into the “NLIN” register of the “Display control (2)” instruction. When the N-line inversion is disabled by setting “0” into the “NLIN” register, the FR signal toggles by the frame.

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	0	0	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	1	0	N3	N2	N1	N0

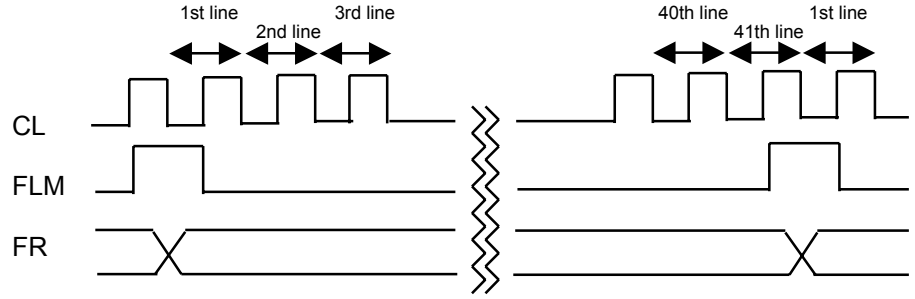
CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	0	0	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	1	1	*	*	N5	N4

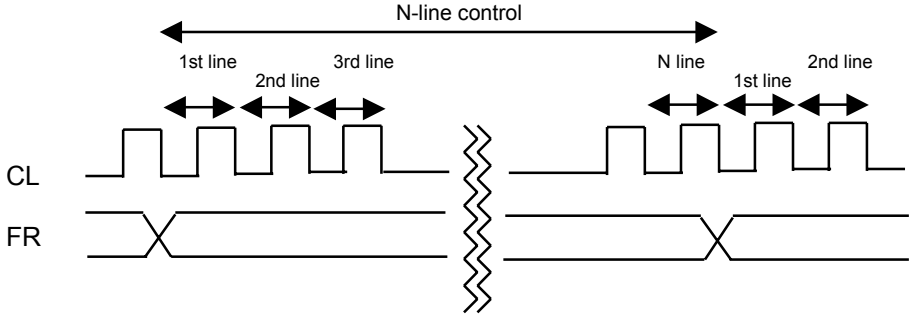
LA_5	LA_4	LA_3	LA_2	LA_1	LA_0	N value
0	0	0	0	0	0	Inhibited*
0	0	0	0	0	1	2
			:			:
1	0	0	1	1	0	39

● N-line Inversion Timing (1/41 duty cycle ratio)

N-line inversion OFF



N-line inversion ON



(31-7) Display control (1)

The “Display control (1)” instruction is used to control display conditions by setting the “Display ON/OFF”, “All pixels ON/OFF”, Display mode” and “Common direction” registers.

CSB	RS	RDB	WRB	RE_2	RE_1	RE_0
0	1	1	0	0	0	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	0	SHIFT	MON	ALLON	ON/OFF

● ON/OFF register

ON/OFF=0 : Display OFF (All COM/SEG output Vss level.)
ON/OFF=1 : Display ON

● All ON register

The “All pixels ON/OFF” register is used to turn on all pixels without changing display data of the DDRAM. The setting for the “All pixels ON/OFF” register has a priority over the “Reverse display ON/OFF” register.

ALLON=0 : Normal
ALLON=1 : All pixels turn on.

● MON register

MON=0 : Gradation mode
MON=1 : B&W mode

● SHIFT register

SHIFT=0 : $COM_0 \rightarrow COM_{39}$
SHIFT=1 : $COM_{39} \rightarrow COM_0$

(31-8) Display control (2)

The “Display control (2)” instruction is used to control display conditions by setting “Segment direction”, “SWAP mode ON/OFF”, “N-line inversion ON/OFF” and “Reverse display ON/OFF” registers.

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	0	0	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	1	REV	NLIN	SWAP	REF

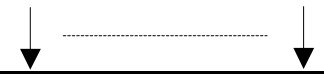
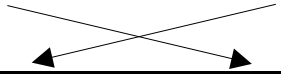
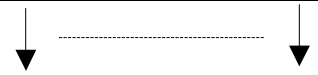
● REF register

The “REF” register is used to reverse the assignment between segment drivers and column address, and it is possible to reduce restrictions for placement of the LSI on the LCD modules. For more information, see (10) “The relation among the DDRAM column address, display data and segment drivers”.

● SWAP register

The “SWAP” register is used to reverse the arrangement of the display data in the DDRAM.

SWAP=0 : SWAP mode OFF (Normal)
SWAP=1 : SWAP mode ON

	SWAP=”0”	SWAP=”1”
Write data	D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0	D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0
		
RAM data	D7 d6 d5 d4 d3 d2 d1 d0	d0 d1 d2 d3 d4 d5 d6 d7
		
Read data	D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0	D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0

● NLIN register

The “NLIN” is used to enable or disable the N-line inversion.

NLIN=0 : N-line inversion OFF (The FR signal toggles by the flame.)
NLIN=1 : N-line inversion ON (The FR signal toggles once every N frames.)

● REV register

The “REV” register is used to enable or disable the reverse display mode that reverses the polarity of the display data without changing the display data of the DDRAM.

REV=0 : Reverse display mode OFF
REV=1 : Reverse display mode ON

REV	Display	DDRAM data → Display data	
0	Normal	0	0
		1	1
1	Reverse	0	1
		1	0

(31-9) Increment control

The “Increment control” instruction is used for the increment mode. In using the auto-increment mode, DDRAM address automatically increments (+1) whenever the DDRAM is accessed by the “Display data write” or “Display data read” instruction. Therefore, once “Display data write” or “Display data read” instruction is established, it is possible to continuously access to the DDRAM without the “column address” and “row address” instructions. The settings for the “AIM”, “AXI” and “AYI” registers are listed in the following tables.

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	0	0	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	1	0	WIN	AIM	AYI	AXI

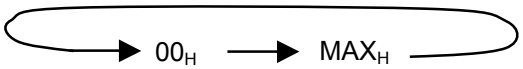
● AIM, AYI and AXI registers

AIM	Increment mode	Note
0	Auto-increment for both of the display data read and write operations	1
1	Auto-increment for the display write operation (Read modify write)	2

Note 1) It is effective for usual operations accessing successive addresses.
Note 2) It is effective for the read-modify-write operation.

AYI	AXI	Increment mode	Note
0	0	No auto-increment	1
0	1	Auto-increment for the column address	2
1	0	Auto-increment for the row address	3
1	1	Auto-increment for the column address and row address	4

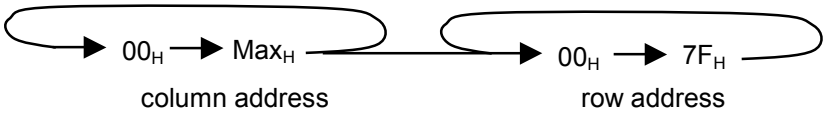
Note 1) Auto-increment is disabled regardless of the “AIM” register.
Note 2) Auto-increment is of the column address is enabled in accordance with the “AIM” register.



MAX_H in the 8-bit data bus mode : FF_H
MAX_H in the 16-bit data bus mode : $7F_H$

Note 3) Auto-increment of the row address is enabled in accordance with the “AIM” register.

Note 4) Auto-increment of the column address and the row address are enabled. The row address increments whenever the column address reaches to the MAX_H.



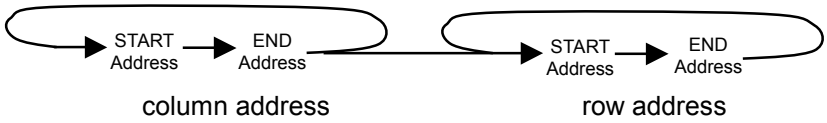
MAX_H in the 8-bit data bus mode : FF_H
MAX_H in the 16-bit data bus mode : $7F_H$

● WIN register

The “WIN” register is used to access to the DDRAM for the window display area, where the start point is determined by the “column address” and “row address” instructions, and the end point by the “Window end column address “and ”Window end row address” instructions. The setting sequence for the window display area is listed as follows. For more detail, see (7) “Window addressing mode”.

WIN=0 :Window addressing mode OFF
WIN=1 :Window addressing mode ON

1. Set WIN=1, AXI=1, and AYI=1 by “Increment control” instruction.
2. Set the start point by the “column address” and “row address” instructions
3. Set the end point by the “Window end column address” and “Window end row address” instructions
4. Enable to access to the DDRAM in the window addressing mode



(31-10) Power control

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	0	0	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	1	1	AMPON	HALT	DCON	ACL

● ACL register

The “ACL” register is used to initialize the internal power supply circuits.

ACL=0 : Initialization OFF (Normal)
ACL=1 : Initialization ON

When the data of the “ACL register” is read out by the “Instruction register read” instruction, the read-out data is “1” during the initialization and “0” after the initialization. This initialization is performed by using the signal produced by 2 clocks on the OSC_1. For this reason, the wait time for 2 clocks of the OSC_1 necessary until next instruction.

● DCON register

The “DCON” register is used to enable or disable the voltage booster.

DCON=0 : Voltage booster OFF
DCON=1 : Voltage booster ON

● HALT register

The “HALT” register is used to enable or disable the power save mode. It is possible reduce operating current down to stand-by level. The internal status in the power save mode is listed below.

HALT=0 : Power save OFF (Normal)
HALT=1 : Power save ON

Internal status in the power save mode

- The oscillation circuits and internal power supply circuits are halted.
- All segment and common drivers output V_{SS} level.
- The clock input into the OSC_1 is inhibited.
- The display data in the DDRAM is maintained.
- The operational modes before the power save mode are maintained.
- The V_1 to V_4 and V_{LCD} are in the high impedance.

As a power save ON sequence, the “Display OFF” must be executed first, next the “Power save ON” instruction, and then all common and segment drivers output the V_{SS} level. And as power save OFF sequence, the “Power save OFF” instruction is executed first, next the “Display ON” instruction. If the “Power save OFF” instruction is executed in the display ON status, unexpected pixels may instantly turn on.

● AMPON register

The “AMPON” register is used to enable or disable the voltage followers, voltage regulator and EVR.

AMPON=0 : The voltage followers, voltage regulator the EVR OFF
AMPON=1 : The voltage followers, voltage regulator the EVR ON

(31-11) Duty cycle ratio

The "Duty cycle ratio" instruction is used to select LCD duty cycle ratio for the partial display function. The partial display function specifies some parts of display area on a LCD panel in the condition of lower duty cycle ratio, lower LCD bias ratio, lower boost level and lower LCD driving voltage. Therefore, it is possible to optimize the LSI's conditions with extremely low power consumption.

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	0	0	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	1	0	0	DS_3	DS_2	DS_1	DS_0

DS_3	DS_2	DS_1	DS_0	Duty cycle ratio		Row way displays
				DSE=0	DSE=1	
0	0	0	0	1/41	1/40	40 commons
0	0	0	1	1/37	1/36	37 commons
0	0	1	0	1/33	1/32	33 commons
0	0	1	1	1/29	1/28	29 commons
0	1	0	0	1/25	1/24	25 commons
0	1	0	1	1/21	1/20	21 commons
0	1	1	0	1/17	1/16	17 commons
0	1	1	1	1/13	1/12	13 commons
1	0	0	0	1/9	1/8	9 commons
1	0	0	1	1/5	1/4	5 commons
1	0	1	0	Inhibited		
1	0	1	1	Inhibited		
1	1	0	0	Inhibited		
1	1	0	1	Inhibited		
1	1	1	0	Inhibited		
1	1	1	1	Inhibited		

The duty cycle ratio is controlled by the "DS_3 to DS_0" registers of the "Duty cycle ratio" instruction and the "DSE" register of the "Display Clock / Duty-1" instruction.

DSE="0" : The number of commons + 1 (Duty cycle ratio in the default setting)
DSE="1" : The number of commons (Duty-1)

When the "DSE" is "0", all common drivers output non-selective levels in period of last common. And the segment drivers output the same data for the last line as the data for previous line: For instance they output the same data for the 40^{th} and 41^{th} lines when the duty cycle ratio is set to 1/41. For the setting of the "DSE" register, see (31-17) "Display clock / Duty-1".

(31-12) Boost level

The "Boost level" is used to select the multiple of the voltage booster for the partial display function.

CSB	RS	RDB	WRB	RE_2	RE_1	RE_0
0	1	1	0	0	0	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	1	0	1	*	VU_2	VU_1	VU_0

VU_2	VU_1	VU_0	Boost level
0	0	0	1-time (No boost)
0	0	1	2-time
0	1	0	3-time
0	1	1	4-time
1	0	0	5-time
1	0	1	Inhibited
1	1	0	Inhibited
1	1	1	Inhibited

(31-13) LCD bias ratio

The “LCD bias ratio” is used to select the LCD bias ratio for the partial display function.

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	0	0	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	1	1	0	*	B_2	B_1	B_0

B_2	B_1	B_0	LCD bias ratio
0	0	0	1/8
0	0	1	1/7
0	1	0	1/6
0	1	1	1/5
1	0	0	1/4
1	0	1	Inhibited
1	1	0	Inhibited
1	1	1	Inhibited

(31-14) RE flag

The “RE flag” registers are used to determine the contents for the RE registers (RE_2, RE_1 and RE_0) and it is possible to access to the instruction registers.

The data in the “TST_0” register must be “0”, and it is used maker tests only.

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	0/1	0/1	0/1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	1	1	1	TST_0	RE_2	RE_1	RE_0

(31-15) Gradation palette A, B and C

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	0	0	1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	0	0	0	PA_{03}/ PA_{83}	PA_{02}/ PA_{82}	PA_{01}/ PA_{81}	PA_{00}/ PA_{80}

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	0	0	1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	0	0	1	*	*	*	PA_{04}/ PA_{84}

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	0	0	1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	0	1	0	PA_{13}/ PA_{93}	PA_{12}/ PA_{92}	PA_{11}/ PA_{91}	PA_{10}/ PA_{90}

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	0	0	1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	0	1	1	*	*	*	PA_{14}/ PA_{94}

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	0	0	1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	0	0	PA_{23}/ PA_{103}	PA_{22}/ PA_{102}	PA_{21}/ PA_{101}	PA_{20}/ PA_{100}

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	0	0	1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	0	1	*	*	*	PA_{24}/ PA_{104}

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	0	0	1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	1	0	PA_{33}/ PA_{113}	PA_{32}/ PA_{112}	PA_{31}/ PA_{111}	PA_{30}/ PA_{110}

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	0	0	1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	1	1	*	*	*	PA_{34}/ PA_{114}

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	0	0	1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	0	PA_{43}/ PA_{123}	PA_{42}/ PA_{122}	PA_{41}/ PA_{121}	PA_{40}/ PA_{120}

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	0	0	1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	1	*	*	*	PA_{44}/ PA_{124}

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	0	0	1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	1	0	PA_{53}/ PA_{133}	PA_{52}/ PA_{132}	PA_{51}/ PA_{131}	PA_{50}/ PA_{130}

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	0	0	1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	1	1	*	*	*	PA_{54}/ PA_{134}

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	0	0	1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	1	0	0	PA_{63}/ PA_{143}	PA_{62}/ PA_{142}	PA_{61}/ PA_{141}	PA_{60}/ PA_{140}

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	0	0	1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	1	0	1	*	*	*	PA_{64}/ PA_{144}

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	0	1	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	0	0	0	PA_{73}/ PA_{153}	PA_{72}/ PA_{152}	PA_{71}/ PA_{151}	PA_{70}/ PA_{150}

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	0	1	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	0	0	1	*	*	*	PA_{74}/ PA_{154}

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	0	1	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	0	1	0	PB_{03}/ PB_{83}	PB_{02}/ PB_{82}	PB_{01}/ PB_{81}	PB_{00}/ PB_{80}

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	0	1	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	0	1	1	*	*	*	PB_{04}/ PB_{84}

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	0	1	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	0	0	PB_{13}/ PB_{93}	PB_{12}/ PB_{92}	PB_{11}/ PB_{91}	PB_{10}/ PB_{90}

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	0	1	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	0	1	*	*	*	PB_{14}/ PB_{94}

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	0	1	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	1	0	PB_{23}/ PB_{103}	PB_{22}/ PB_{102}	PB_{21}/ PB_{101}	PB_{20}/ PB_{100}

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	0	1	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	1	1	*	*	*	PB_{24}/ PB_{104}

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	0	1	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	0	PB_{33}/ PB_{113}	PB_{32}/ PB_{112}	PB_{31}/ PB_{111}	PB_{30}/ PB_{110}

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	0	1	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	1	*	*	*	PB_{34}/ PB_{114}

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	0	1	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	1	0	PB_{43}/ PB_{123}	PB_{42}/ PB_{122}	PB_{41}/ PB_{121}	PB_{40}/ PB_{120}

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	0	1	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	1	1	*	*	*	PB_{44}/ PB_{124}

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	0	1	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	1	0	0	PB_{53}/ PB_{133}	PB_{52}/ PB_{132}	PB_{51}/ PB_{131}	PB_{50}/ PB_{130}

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	0	1	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	1	0	1	*	*	*	PB_{54}/ PB_{134}

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	0	1	1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	0	0	0	PB_{63}/ PB_{143}	PB_{62}/ PB_{142}	PB_{61}/ PB_{141}	PB_{60}/ PB_{140}

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	0	1	1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	0	0	1	*	*	*	PB_{64}/ PB_{144}

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	0	1	1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	0	1	0	PB_{73}/ PB_{153}	PB_{72}/ PB_{152}	PB_{71}/ PB_{151}	PB_{70}/ PB_{150}

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	0	1	1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	0	1	1	*	*	*	PB_{74}/ PB_{154}

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	0	1	1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	0	0	PC_{03}/ PC_{83}	PC_{02}/ PC_{82}	PC_{01}/ PC_{81}	PC_{00}/ PC_{80}

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	0	1	1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	0	1	*	*	*	PC_{04}/ PC_{84}

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	0	1	1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	1	0	PC_{13}/ PC_{93}	PC_{12}/ PC_{92}	PC_{11}/ PC_{91}	PC_{10}/ PC_{90}

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	0	1	1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	1	1	*	*	*	PC_{14}/ PC_{94}

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	0	1	1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	0	PC_{23}/ PC_{103}	PC_{22}/ PC_{102}	PC_{21}/ PC_{101}	PC_{20}/ PC_{100}

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	0	1	1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	1	*	*	*	PC_{24}/ PC_{104}

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	0	1	1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	1	0	PC_{33}/ PC_{113}	PC_{32}/ PC_{112}	PC_{31}/ PC_{111}	PC_{30}/ PC_{110}

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	0	1	1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	1	1	*	*	*	PC_{34}/ PC_{114}

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	0	1	1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	1	0	0	PC_{43}/ PC_{123}	PC_{42}/ PC_{122}	PC_{41}/ PC_{121}	PC_{40}/ PC_{120}

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	0	1	1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	1	0	1	*	*	*	PC_{44}/ PC_{124}

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	1	0	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	0	0	0	PC_{53}/ PC_{133}	PC_{52}/ PC_{132}	PC_{51}/ PC_{131}	PC_{50}/ PC_{130}

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	1	0	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	0	0	1	*	*	*	PC_{54}/ PC_{134}

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	1	0	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	0	1	0	PC_{63}/ PC_{143}	PC_{62}/ PC_{142}	PC_{61}/ PC_{141}	PC_{60}/ PC_{140}

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	1	0	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	0	1	1	*	*	*	PC_{64}/ PC_{144}

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	1	0	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	0	0	PC_{73}/ PC_{153}	PC_{72}/ PC_{152}	PC_{71}/ PC_{151}	PC_{70}/ PC_{150}

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	1	0	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	0	1	*	*	*	PC_{74}/ PC_{154}

Gradation Palette Table (Variable gradation mode, PWM="0" and MON="0")

(Palette Aj, Palette Bj, Palette Cj, (j=0 to 15))

Palette Value	Gradation Level	Note	Palette Value	Gradation Level	Note
0 0 0 0 0	0/31	Gradation Palette 0 Initial Value	1 0 0 0 0	16/31	
0 0 0 0 1	1/31		1 0 0 0 1	17/31	Gradation Palette 8 Initial Value
0 0 0 1 0	2/31		1 0 0 1 0	18/31	
0 0 0 1 1	3/31	Gradation Palette 1 Initial Value	1 0 0 1 1	19/31	Gradation Palette 9 Initial Value
0 0 1 0 0	4/31		1 0 1 0 0	20/31	
0 0 1 0 1	5/31	Gradation Palette2 Initial Value	1 0 1 0 1	21/31	Gradation Palette 10 Initial Value
0 0 1 1 0	6/31		1 0 1 1 0	22/31	
0 0 1 1 1	7/31	Gradation Palette 3 Initial Value	1 0 1 1 1	23/31	Gradation Palette 11 Initial Value
0 1 0 0 0	8/31		1 1 0 0 0	24/31	
0 1 0 0 1	9/31	Gradation Palette 4 Initial Value	1 1 0 0 1	25/31	Gradation Palette 12 Initial Value
0 1 0 1 0	10/31		1 1 0 1 0	26/31	
0 1 0 1 1	11/31	Gradation Palette 5 Initial Value	1 1 0 1 1	27/31	Gradation Palette 13 Initial Value
0 1 1 0 0	12/31		1 1 1 0 0	28/31	
0 1 1 0 1	13/31	Gradation Palette 6 Initial Value	1 1 1 0 1	29/31	Gradation Palette 14 Initial Value
0 1 1 1 0	14/31		1 1 1 1 0	30/31	
0 1 1 1 1	15/31	Gradation Palette 7 Initial Value	1 1 1 1 1	31/31	Gradation Palette 15 Initial Value

(31-16) Initial COM line

The “Initial COM line” instruction is used to specify the common driver that starts scanning the display data. The line address, corresponding to the initial COM line, is specified by the “Initial display line” instruction.

CSB	RS	RDB	WRB	RE_2	RE_1	RE_0
0	1	1	0	1	0	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	1	0	SC_3	SC_2	SC_1	SC_0

SC3	SC2	SC1	SC0	Initial COM line (SHIFT=0)	Initial COM line (SHIFT=1)
0	0	0	0	COM_0	COM_{39}
0	0	0	1	COM_4	COM_{31}
0	0	1	0	COM_8	COM_{27}
0	0	1	1	COM_{16}	COM_{23}
0	1	0	0	COM_{20}	COM_{19}
0	1	0	1	COM_{24}	COM_{15}
0	1	1	0	COM_{28}	COM_{11}
0	1	1	1	COM_{32}	COM_7
1	0	0	0	COM_{36}	COM_3
1	0	0	1	Inhibited	Inhibited
1	0	1	0	Inhibited	Inhibited
1	0	1	1	Inhibited	Inhibited
1	1	0	0	Inhibited	Inhibited
1	1	0	1	Inhibited	Inhibited
1	1	1	0	Inhibited	Inhibited
1	1	1	1	Inhibited	Inhibited

SHIFT=0: Positive scan direction (for instance, $COM_0 \rightarrow COM_{39}$)
SHIFT=1: Negative scan direction (for instance, $COM_{39} \rightarrow COM_0$)

(31-17) Display clock / Duty-1

The “Display clock / Duty-1” instruction is used to enable or disable the display clocks (CL, FLM, FR, and CLK), and to control ON/OFF of the “Duty-1”. For more detail about the “Duty-1”, see (31-11) “Duty cycle ratio”.

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	1	0	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	1	1	*	*	DSE	SON

SON=0: CL, FLM, FR, and CLK outputs level “0”.
SON=1: CL, FLM, FR, and CLK outputs are active.

DSE=0: Duty -1 OFF
DSE=1: Duty -1 ON

(31-18) Gradation mode control

The “Gradation mode control” is used select display mode as follows.

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	1	0	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	0	PWM	C256	*	*

- PWM register
  PWM=0: Variable gradation mode
  (Variable 16-gradation levels out of 32-gradation level of the gradation palette)
  PWM=1: Fixed gradation mode
  (Fixed 8-gradation levels)

- C256 register
  C256=0 256-color mode OFF (4,096-color in the default setting)
  C256=1 256-color mode ON

(31-19) Data bus length

The “Data bus length” instruction is used to select the 8- or 16- bit data bus length and determine the internal or external oscillation. In the 16-bit data bus mode, instruction data must be 16-bit (D_{15} to D_0) as well as display data. However, for the access to the instruction registers, the lower 8-bit data (D_7 to D_0) of the 16-bit data is valid. For the access to the DDRAM, all of the 16-bit data (D_{15} to D_0) is valid.

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	1	0	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	1	HSW	ABS	CKS	WLS

- HSW register
  HSW =0: High Speed access mode OFF
  HSW=1: High Speed access mode ON (only in the 8-bit data bus length)

- ABS register
  ABS=0: ABS mode OFF (normal)
  ABS=1: ABS mode ON

- WLS register
  WLS=0: 8-bit data bus length
  WLS =1: 16-bit data bus length

- CKS register
  CKS =0: Internal oscillation
  (The OSC_1 terminal must be fixd “1” or “0”.)
  CKS =1: External oscillation
  (By the external clock into the OSC_1 or external resister between the OSC_1 and OSC_2. OSC_2 should be open when clock is inputted from OSC_1.)

(31-20) EVR control

The “EVR control” instruction is used to fine-tune the LCD driving voltage (V_{LCD}) so that it is possible to optimize the contrast level for a LCD panel.

This instruction must be programmed by upper 3-bit data first, next lower 4-bit data. And it becomes enabled when the lower 4-bit data is programmed, so that it can prevent unexpected high voltage for the VLCD from being generated.

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	1	0	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	1	0	DV_3	DV_2	DV_1	DV_0

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	1	0	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	1	1	*	DV_6	DV_5	DV_4

DV_6	DV_5	DV_4	DV_3	DV_2	DV_1	DV_0	V_{LCD}
0	0	0	0	0	0	0	Low
0	0	0	0	0	0	1	:
			:				:
1	1	1	1	1	1	1	High

The formula of the V_{LCD} is shown below.

V_{LCD} [V] = 0.5 x V_{REG} + M (V_{REG} − 0.5 x V_{REG}) / 127

$V_{BA} = V_{EE} \times 0.9$
$V_{REG} = V_{REF} \times N$

V_{BA} : Output voltage of the reference voltage generator
V_{REF} : Input voltage of the voltage regulator
V_{REG} : Output voltage of the voltage regulator
N : Register value for the voltage booster
M : Register value for the EVR

(31-21) Frequency control

The “Frequency control” instruction is used to control the frame frequency for a LCD panel.

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	1	0	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	1	0	1	*	Rf_2	Rf_1	Rf_0

● Rfx register (x=0, 1, 2)

The “Rfx” register is used to determine the feed back resister value for the internal oscillator and it is possible to adjust the frame frequency for the LCD modules.

Rf 2	Rf 1	Rf 0	Feedback resistor value
0	0	0	Reference value
0	0	1	0.8 x reference value
0	1	0	0.9 x reference value
0	1	1	1.1 x reference value
1	0	0	1.2 x reference value
1	0	1	0.7 x reference value
1	1	0	1.3 x reference value
1	1	1	Inhibited

(31-22) Discharge ON/OFF

Discharge circuit is used to discharge the electric charge of the capacitors on the V_1 to V_4 and the V_{LCD} terminals. The “Discharge ON/OFF” instruction is usually required just after the internal power supply is turned off by setting “0” into the “DCON” and “AMPON” registers, or just after the external power supply is turned off. During the discharge operation, the internal or external power supply must not be turned on.

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	1	0	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	1	1	0	*	*	DIS2	DIS

DIS=0: Discharge OFF (Capacitors on the V_{LCD}, V_1, V_2, V_3 and V_4)
DIS=1: Discharge ON (Capacitors on the V_{LCD}, V_1, V_2, V_3 and V_4)

DIS2=0: Discharge OFF (Resistance between V_{OUT} and V_{EE})
DIS2=1: Discharge ON (Resistance between V_{OUT} and V_{EE})

Note) V_{OUT} and V_{EE} are internally connected with the resistor (100kΩ typical) in the power-ON.

(31-23) Instruction register address

The “Instruction register address” is used to specify the instruction register address, so that it is possible to read out the contents of the instruction registers in combination with the “Instruction register read” instruction.

CSB	RS	RDB	WRB	RE_2	RE_1	RE_0
0	1	1	0	1	0	0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	1	0	0	RA_3	RA_2	RA_1	RA_0

(31-24) Instruction register read

The “Instruction register read” instruction is used to read out the contents of the instruction register in combination with the “Instruction register address” instruction.

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	0	1	0/1	0/1	0/1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
*	*	*	*	Internal register data read			

(31-25) Window end column address

The “Window end column address” is used to specify the column address for the window end point. The lower 4-bit data is required to be programmed first and then the upper 4-bit data can be programmed.

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	1	0	1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	0	0	0	EX_3	EX_2	EX_1	EX_0

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	1	0	1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	0	0	1	EX_7	EX_6	EX_5	EX_4

(31-26) Window end row address set

The “Window end row address” is used to specify the row address for the window end point. The lower 4-bit data is required to be programmed first and then the upper 2-bit data can be programmed.

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	1	0	1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	0	1	0	EY_3	EY_2	EY_1	EY_0

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	1	0	1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	0	1	1	*	*	EY_5	EY_4

(31-27) Initial reverse line

The “Initial reverse line” instruction is used to specify the initial reverse line address for the reverse line display. Lower 4-bit data must be programmed first, next upper 2-bit data. It is programmed in between 00_H and 27_H and the line address beyond 27_H is inhibited. The address relation: LSi < LEi (i=7 to 0) must be maintained in the reverse line display.

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	1	0	1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	0	0	LS_3	LS_2	LS_1	LS_0

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	1	0	1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	0	1	*	*	LS_5	LS_4

(31-28) Last reverse line

The “Last reverse line” instruction is used to specify the last reverse line address for the reverse line display. Lower 4-bit must be programmed first, next upper 2-bit data. It is programmed in between 00_H and 27_H and the line address beyond 27_H is inhibited. The address relation: LSi < LEi (i=7 to 0) must be maintained in the reverse line display.

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	1	0	1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	1	0	LE_3	LE_2	LE_1	LE_0

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	1	0	1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	1	1	*	*	LE_5	LE_4

(31-29) Reverse line display ON/OFF

The “Reverse line display ON/OFF” is used to enable or disable the reverse line display for the blink operation and determine the reverse line display mode.

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	1	0	1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	0	*	*	BT	LREV

- LREV register

The “LREV” register is used to enable or disable the reverse line display.

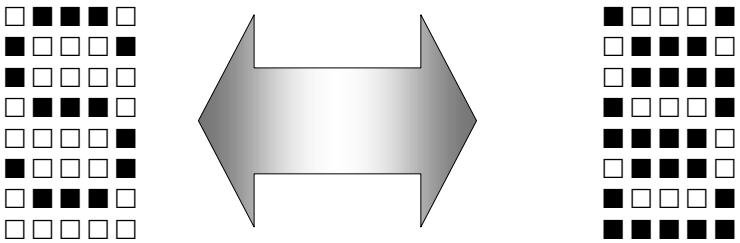
LREV =0: Reverse line display OFF (Normal)
LREV =1: Reverse line display ON

● BT register

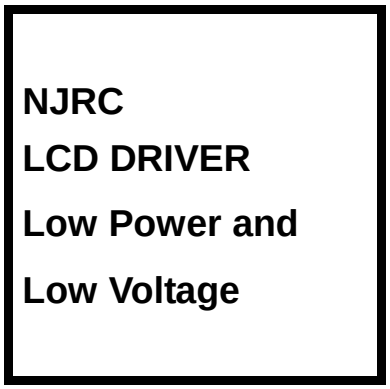
The “BT” register is used to determine the reverse line display mode in the reverse line display ON (LREV=1) status.

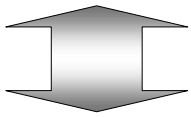
BT =0: Normal reverse line display
BT =1: Blink once every 32 frames

Display examples in the LREV=”1” and BT=”1”

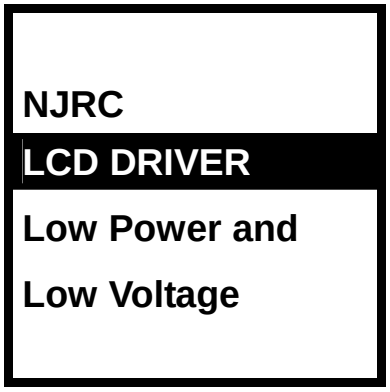


Blink once every 32 frames





Blink once every 32 frames



←Initial reverse line address

←Last reverse line address

(31-30) Gradation Palette setting control

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	1	0	1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	1	*	*	*	PS

● PS register

PS=0: Lower 8 Gradation setting
PS=1: Upper 8 Gradation setting

(31-31) PWM control

The “PWM control” is used to determine the PWM type for the segment waveforms, where the type can be specified for each of the SEGAi, SEGBi and SEGCi (i=0-127) drivers.

CSb	RS	RDb	WRb	RE_2	RE_1	RE_0
0	1	1	0	1	0	1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	1	0	PWMS	PWMA	PWMB	PWMC

● PWMS register

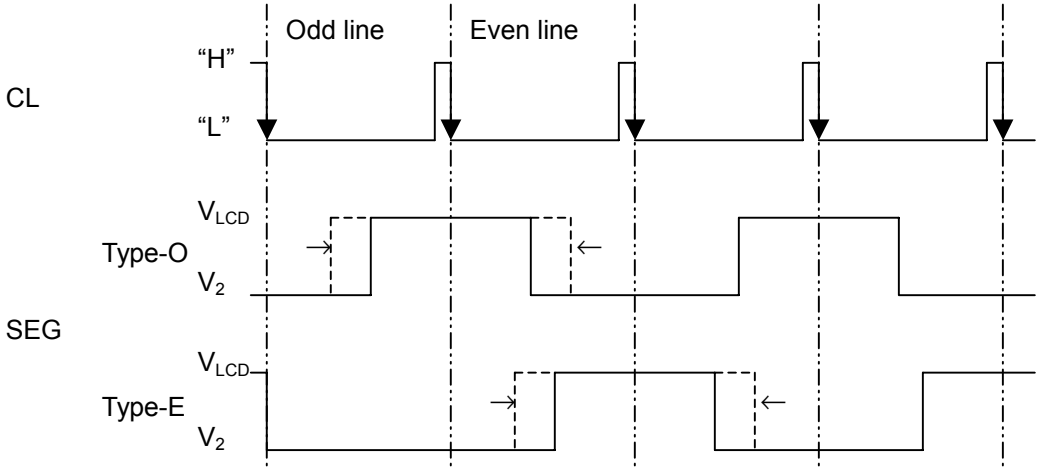
PWMS=0: Type 1
PWMS=1: Type 2

● PWMA, B and C registers

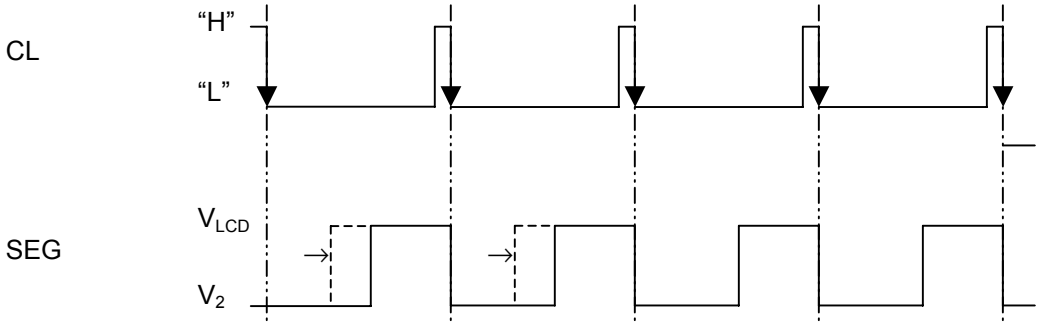
The “PWMA, PWMB and PWMC” registers are used to select the type 1-O or type 1-E.

PWMZ=0 (Z=A, B and C): Type 1-O
PWMZ=1 (Z=A, B and C): Type 1-E

PWM type1 (PWMS=”0”)



PWM type2 (PWMS=”1”)



(32) The relationship between Common drivers and row addresses
Row address assignment of common drivers is programmed by the " SHIFT " register of the " Display control (1) " , " Duty cycle ratio ", " Internal display line " and " Initial COM line " instructions.

When initial display line is "0"

If the " SHIFT " is " 0 ", the scan direction is normal. When the " LA_0 to LA_6 " registers of the " Initial display line "instruction is " 0 ", the " MY " corresponding to the initial COM line is " 0 " and is increasing during display.

When initial display line is not "0"

If the " SHIFT " is " 1 ", the scan direction is inversed. When the " LA_0 to LA_6 " registers of the " Initial display line "instruction is not " 0 ", the " MY " corresponding to the initial COM line is this setting value and is increasing during display.

The following are examples of setting the start-line 0 or 5 at 1/41, 1/17, or 1/17 duty.

(32-1) Initial display line “0”, 1/41 duty cycle (Common forward scan)

SHIFT="0"(Common forward scan), $DS_{3,2,1,0}$="0000", LA_7…LA_0="00000000"(Initial display line 0)																			
SC_3	SC_2	SC_1	SC_0	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	Inhibited	Inhibited	Inhibited	Inhibited	Inhibited	Inhibited
COM_0				0	36	32	28	24	20	16	12	8	4						
COM_1																			
COM_2																			
COM_3					39														
COM_4					0														
COM_5																			
COM_6						39													
COM_7																			
COM_8						0													
COM_9																			
COM_{10}																			
COM_{11}							39												
COM_{12}							0												
COM_{13}																			
COM_{14}																			
COM_{15}								39											
COM_{16}								0											
COM_{17}																			
COM_{18}																			
COM_{19}									39										
COM_{20}									0										
COM_{21}																			
COM_{22}																			
COM_{23}										39									
COM_{24}										0									
COM_{25}																			
COM_{26}																			
COM_{27}											39								
COM_{28}											0								
COM_{29}																			
COM_{30}																			
COM_{31}												39							
COM_{32}												0							
COM_{33}																			
COM_{34}																			
COM_{35}													39						
COM_{36}													0						
COM_{37}																			
COM_{38}																			
COM_{39}				39	35	31	27	23	19	15	11	7	3						
(40^{rd} COM period) *1				39	39	39	39	39	39	39	39	39	39						

DS: Duty cycle ratio, SC: Initial COM line, LA: Initial display line

*1 : 40^{th} COM period is not selected.

(32-2) Initial display line “0”, 1/41 duty cycle (Common backward scan)

SHIFT="1"(Common forward scan), $DS_{3,2,1,0}$="0000", LA_7…LA_0="00000000"(Initial display line 0)																			
SC_3	SC_2	SC_1	SC_0	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	Inhibited	Inhibited	Inhibited	Inhibited	Inhibited	Inhibited
COM_0				39	3	7	11	15	19	23	27	31	35						
COM_1																			
COM_2																			
COM_3					0														
COM_4					39														
COM_5																			
COM_6																			
COM_7						0													
COM_8						39													
COM_9																			
COM_{10}																			
COM_{11}							0												
COM_{12}							39												
COM_{13}																			
COM_{14}																			
COM_{15}								0											
COM_{16}								39											
COM_{17}																			
COM_{18}																			
COM_{19}									0										
COM_{20}									39										
COM_{21}																			
COM_{22}																			
COM_{23}										0									
COM_{24}										39									
COM_{25}																			
COM_{26}																			
COM_{27}											39								
COM_{28}											0								
COM_{29}																			
COM_{30}																			
COM_{31}												39							
COM_{32}												0							
COM_{33}																			
COM_{34}																			
COM_{35}													39						
COM_{36}													0						
COM_{37}																			
COM_{38}																			
COM_{39}				0	4	8	12	16	20	24	28	32	36						
(40^{rd} COM period) *1				39	39	39	39	39	39	39	39	39	39						

DS: Duty cycle ratio, SC: Initial COM line, LA: Initial display line

*1 : 40^{th} COM period is not selected.

(32-3) Initial display line “0”, 1/17 duty cycle (Common forward scan)

SHIFT=”0”(Common forward scan), $DS_{3,2,1,0}$=”0110”, LA_7….LA_0=”00000000”(Initial display line 0)

SC_3	SC_2	SC_1	SC_0	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	Inhibited	Inhibited	Inhibited	Inhibited	Inhibited	Inhibited
COM_0				0							12	8	4						
COM_1																			
COM_2																			
COM_3											15								
COM_4					0														
COM_5																			
COM_6																			
COM_7												15							
COM_8						0													
COM_9																			
COM_{10}																			
COM_{11}													15						
COM_{12}							0												
COM_{13}																			
COM_{14}																			
COM_{15}				15															
COM_{16}								0											
COM_{17}																			
COM_{18}																			
COM_{19}					15														
COM_{20}									0										
COM_{21}																			
COM_{22}																			
COM_{23}						15													
COM_{24}										0									
COM_{25}																			
COM_{26}																			
COM_{27}							15												
COM_{28}											0								
COM_{29}																			
COM_{30}																			
COM_{31}								15											
COM_{32}												0							
COM_{33}																			
COM_{34}																			
COM_{35}									15										
COM_{36}													0						
COM_{37}																			
COM_{38}																			
COM_{39}										15	11	7	3						
(17rd COM period) *1				16	16	16	16	16	16	16	16	16	16						

DS: Duty cycle ratio, SC: Initial COM line, LA: Initial display line

*1 : 17th COM period is not selected.

(32-4) Initial display line “0”, 1/17 duty cycle (Common backward scan)

SHIFT=”1”(Common forward scan), $DS_{3,2,1,0}$=”0110”, LA_7….LA_0=”00000000”(Initial display line 0)

SC_3	SC_2	SC_1	SC_0	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	Inhibited	Inhibited	Inhibited	Inhibited	Inhibited	Inhibited
COM_0										15	11	7	3						
COM_1																			
COM_2																			
COM_3													0						
COM_4									15										
COM_5																			
COM_6																			
COM_7												0							
COM_8								15											
COM_9																			
COM_{10}																			
COM_{11}											0								
COM_{12}							15												
COM_{13}																			
COM_{14}																			
COM_{15}										0									
COM_{16}						15													
COM_{17}																			
COM_{18}																			
COM_{19}									0										
COM_{20}					15														
COM_{21}																			
COM_{22}																			
COM_{23}								0											
COM_{24}				15															
COM_{25}																			
COM_{26}																			
COM_{27}							0												
COM_{28}													0						
COM_{29}																			
COM_{30}																			
COM_{31}						0													
COM_{32}												0							
COM_{33}																			
COM_{34}																			
COM_{35}					0														
COM_{36}											0								
COM_{37}																			
COM_{38}																			
COM_{39}				0							12	8	4						
(17rd COM period) *1				16	16	16	16	16	16	16	16	16	16						

DS: Duty cycle ratio, SC: Initial COM line, LA: Initial display line

*1 : 17th COM period is not selected.

(32-5) Initial display line “0”, 1/5 duty cycle (Common forward scan)

SHIFT=“0”(Common forward scan), $DS_{3,2,1,0}$=“1001”, LA_7…LA_0=“00000000”(Initial display line 0)

SC_3	SC_2	SC_1	SC_0	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	Inhibited	Inhibited	Inhibited	Inhibited	Inhibited	Inhibited
COM_0				0															
COM_1				↓															
COM_2																			
COM_3				3															
COM_4					0														
COM_5					↓														
COM_6																			
COM_7					3														
COM_8						0													
COM_9						↓													
COM_{10}																			
COM_{11}						3													
COM_{12}							0												
COM_{13}							↓												
COM_{14}																			
COM_{15}							3												
COM_{16}								0											
COM_{17}								↓											
COM_{18}																			
COM_{19}								3											
COM_{20}									0										
COM_{21}									↓										
COM_{22}																			
COM_{23}									3										
COM_{24}										0									
COM_{25}										↓									
COM_{26}																			
COM_{27}										3									
COM_{28}											0								
COM_{29}											↓								
COM_{30}																			
COM_{31}											3								
COM_{32}												0							
COM_{33}												↓							
COM_{34}																			
COM_{35}												3							
COM_{36}													0						
COM_{37}													↓						
COM_{38}																			
COM_{39}													3						
(5rd COM period) *1				4	4	4	4	4	4	4	4	4	4						

DS: Duty cycle ratio, SC: Initial COM line, LA: Initial display line
*1 : 5th COM period is not selected.

(32-6) Initial display line “0”, 1/5 duty cycle (Common forward scan)

SHIFT=“1”(Common forward scan), $DS_{3,2,1,0}$=“1001”, LA_7…LA_0=“00000000”(Initial display line 0)

SC_3	SC_2	SC_1	SC_0	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	Inhibited	Inhibited	Inhibited	Inhibited	Inhibited	Inhibited
COM_0													3						
COM_1													↑						
COM_2																			
COM_3													0						
COM_4												3							
COM_5												↑							
COM_6																			
COM_7												0							
COM_8											3								
COM_9											↑								
COM_{10}																			
COM_{11}											0								
COM_{12}										3									
COM_{13}										↑									
COM_{14}																			
COM_{15}										0									
COM_{16}									3										
COM_{17}									↑										
COM_{18}																			
COM_{19}									0										
COM_{20}								3											
COM_{21}								↑											
COM_{22}																			
COM_{23}								0											
COM_{24}							3												
COM_{25}							↑												
COM_{26}																			
COM_{27}							0												
COM_{28}						3													
COM_{29}						↑													
COM_{30}																			
COM_{31}						0													
COM_{32}					3														
COM_{33}					↑														
COM_{34}																			
COM_{35}					0														
COM_{36}				3															
COM_{37}				↑															
COM_{38}																			
COM_{39}				0															
(5rd COM period) *1				4	4	4	4	4	4	4	4	4	4						

DS: Duty cycle ratio, SC: Initial COM line, LA: Initial display line
*1 : 5rd COM period is not selected.

(33) Initial display line “5”, 1/41 duty cycle (Common forward scan)

SHIFT=”0”(Common forward scan), $DS_{3,2,1,0}$=”0000”, LA_7….LA_0=”00000101”(Initial display line 0)

SC_3	SC_2	SC_1	SC_0	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	Inhibited	Inhibited	Inhibited	Inhibited	Inhibited	Inhibited
COM_0				5	1	37	33	29	25	21	17	13	9						
COM_1																			
COM_2						39													
COM_3						0													
COM_4					5														
COM_5																			
COM_6							39												
COM_7							0												
COM_8						5													
COM_9																			
COM_{10}								39											
COM_{11}								0											
COM_{12}							5												
COM_{13}																			
COM_{14}									39										
COM_{15}									0										
COM_{16}								5											
COM_{17}																			
COM_{18}										39									
COM_{19}										0									
COM_{20}									5										
COM_{21}																			
COM_{22}											39								
COM_{23}											0								
COM_{24}										5									
COM_{25}																			
COM_{26}												39							
COM_{27}												0							
COM_{28}											5								
COM_{29}																			
COM_{30}													39						
COM_{31}												5	0						
COM_{32}																			
COM_{33}																			
COM_{34}				39															
COM_{35}				0									5						
COM_{36}																			
COM_{37}																			
COM_{38}					39														
COM_{39}				4	0	36	32	28	24	20	16	12	8						
(40^{rd} COM period) *1				39	39	39	39	39	39	39	39	39	39						

DS: Duty cycle ratio, SC: Initial COM line, LA: Initial display line

*1 : 40^{th} COM period is not selected.

(33-1) Initial display line “5”, 1/41 duty cycle (Common backward scan)

SHIFT=”1”(Common forward scan), $DS_{3,2,1,0}$=”0000”, LA_7….LA_0=”00000101”(Initial display line 0)

SC_3	SC_2	SC_1	SC_0	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	Inhibited	Inhibited	Inhibited	Inhibited	Inhibited	Inhibited
COM_0				4	0	36	32	28	24	20	16	12	8						
COM_1					39														
COM_2																			
COM_3																			
COM_4				0															
COM_5				39															
COM_6																			
COM_7																			
COM_8													0						
COM_9													39						
COM_{10}																			
COM_{11}																			
COM_{12}												0							
COM_{13}												39							
COM_{14}																			
COM_{15}																			
COM_{16}											0								
COM_{17}											39								
COM_{18}																			
COM_{19}																			
COM_{20}										0									
COM_{21}										39									
COM_{22}																			
COM_{23}																			
COM_{24}									0										
COM_{25}									39										
COM_{26}																			
COM_{27}																			
COM_{28}								0											
COM_{29}								39											
COM_{30}																			
COM_{31}																			
COM_{32}							0												
COM_{33}							39												
COM_{34}																			
COM_{35}																			
COM_{36}						0													
COM_{37}						39													
COM_{38}																			
COM_{39}				5	1	37	33	29	25	21	17	13	9						
(40^{rd} COM period) *1				39	39	39	39	39	39	39	39	39	39						

DS: Duty cycle ratio, SC: Initial COM line, LA: Initial display line

*1 : 40^{th} COM period is not selected.

(33-2) Initial display line “5”, 1/17 duty cycle (Common forward scan)

SHIFT=”0”(Common forward scan), $DS_{3,2,1,0}$=”0110”, LA_7….LA_0=”00000101”(Initial display line 0)

SC_3	SC_2	SC_1	SC_0	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	Inhibited	Inhibited	Inhibited	Inhibited	Inhibited	Inhibited
COM_0				5							17	13	9						
COM_1				↓							↓	↓	↓						
COM_2											20								
COM_3																			
COM_4					5														
COM_5					↓														
COM_6												20							
COM_7																			
COM_8						5													
COM_9						↓													
COM_{10}													20						
COM_{11}																			
COM_{12}							5												
COM_{13}							↓												
COM_{14}				↓															
COM_{15}				20															
COM_{16}								5											
COM_{17}					↓			↓											
COM_{18}																			
COM_{19}					20														
COM_{20}									5										
COM_{21}									↓										
COM_{22}																			
COM_{23}						20													
COM_{24}										5									
COM_{25}										↓									
COM_{26}																			
COM_{27}							20												
COM_{28}											5								
COM_{29}											↓								
COM_{30}								↓											
COM_{31}								20											
COM_{32}												5							
COM_{33}												↓							
COM_{34}									↓										
COM_{35}									20										
COM_{36}													5						
COM_{37}										↓	↓	↓	↓						
COM_{38}																			
COM_{39}										20	16	12	8						
(17rd COM period) *1				16	16	16	16	16	16	16	16	16	16						

DS: Duty cycle ratio, SC: Initial COM line, LA: Initial display line

*1 : 17th COM period is not selected.

(33-3) Initial display line “5”, 1/17 duty cycle (Common backward scan)

SHIFT=”1”(Common forward scan), $DS_{3,2,1,0}$=”0110”, LA_7….LA_0=”00000101”(Initial display line 0)

SC_3	SC_2	SC_1	SC_0	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	Inhibited	Inhibited	Inhibited	Inhibited	Inhibited	Inhibited
COM_0										20	16	12	8						
COM_1										↑	↑	↑	↑						
COM_2																			
COM_3													5						
COM_4									20										
COM_5									↑										
COM_6																			
COM_7												5							
COM_8								20											
COM_9								↑											
COM_{10}																			
COM_{11}											5								
COM_{12}							20												
COM_{13}							↑												
COM_{14}																			
COM_{15}										5									
COM_{16}						20				↑									
COM_{17}						↑													
COM_{18}																			
COM_{19}									5										
COM_{20}					20				↑										
COM_{21}					↑				↑										
COM_{22}																			
COM_{23}								5											
COM_{24}				20				↑											
COM_{25}				↑				↑											
COM_{26}																			
COM_{27}							5												
COM_{28}													20						
COM_{29}													↑						
COM_{30}																			
COM_{31}						5													
COM_{32}						↑						20							
COM_{33}						↑						↑							
COM_{34}																			
COM_{35}					5														
COM_{36}					↑						20								
COM_{37}					↑						↑								
COM_{38}																			
COM_{39}				5							17	13	9						
(17rd COM period) *1				16	16	16	16	16	16	16	16	16	16						

DS: Duty cycle ratio, SC: Initial COM line, LA: Initial display line

*1 : 17th COM period is not selected.

(33-4) Initial display line “5”, 1/5 duty cycle (Common forward scan)

SHIFT="0"(Common forward scan), $DS_{3,2,1,0}$="1001", LA_7…LA_0="00000101"(Initial display line 0)																	
SC_3	SC_2	SC_1	SC_0	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	Inhibited	Inhibited	Inhibited	Inhibited	Inhibited	Inhibited
COM_0				5															
COM_1				↓															
COM_2																			
COM_3				8															
COM_4					5														
COM_5					↓														
COM_6																			
COM_7					8														
COM_8						5													
COM_9						↓													
COM_{10}																			
COM_{11}						8													
COM_{12}							5												
COM_{13}							↓												
COM_{14}																			
COM_{15}							8												
COM_{16}								5											
COM_{17}								↓											
COM_{18}																			
COM_{19}								8											
COM_{20}									5										
COM_{21}									↓										
COM_{22}																			
COM_{23}									8										
COM_{24}										5									
COM_{25}										↓									
COM_{26}																			
COM_{27}										8									
COM_{28}											5								
COM_{29}											↓								
COM_{30}																			
COM_{31}											8								
COM_{32}												5							
COM_{33}												↓							
COM_{34}																			
COM_{35}												8							
COM_{36}													5						
COM_{37}													↓						
COM_{38}																			
COM_{39}													8						
(5rd COM period) *1				4	4	4	4	4	4	4	4	4	4						

DS: Duty cycle ratio, SC: Initial COM line, LA: Initial display line
*1 : 5th COM period is not selected.

(33-5) Initial display line “5”, 1/5 duty cycle (Common forward scan)

SHIFT="1"(Common forward scan), $DS_{3,2,1,0}$="1001", LA_7…LA_0="00000101"(Initial display line 0)																	
SC_3	SC_2	SC_1	SC_0	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	Inhibited	Inhibited	Inhibited	Inhibited	Inhibited	Inhibited
COM_0													8						
COM_1													↑						
COM_2																			
COM_3													5						
COM_4												8							
COM_5												↑							
COM_6																			
COM_7												5							
COM_8											8								
COM_9											↑								
COM_{10}																			
COM_{11}											5								
COM_{12}										8									
COM_{13}										↑									
COM_{14}																			
COM_{15}										5									
COM_{16}									8										
COM_{17}									↑										
COM_{18}																			
COM_{19}									5										
COM_{20}								8											
COM_{21}								↑											
COM_{22}																			
COM_{23}								5											
COM_{24}							8												
COM_{25}							↑												
COM_{26}																			
COM_{27}							5												
COM_{28}						8													
COM_{29}						↑													
COM_{30}																			
COM_{31}						5													
COM_{32}					8														
COM_{33}					↑														
COM_{34}																			
COM_{35}					5								3						
COM_{36}				8															
COM_{37}				↑															
COM_{38}																			
COM_{39}				5															
(5rd COM period) *1				4	4	4	4	4	4	4	4	4	4						

DS: Duty cycle ratio, SC: Initial COM line, LA: Initial display line
*1 : 5th COM period is not selected.

(33-6) Initial display line “0”, 1/40 duty cycle (Common forward scan, DSE=”1”)

SHIFT=”0”(Common forward scan), $DS_{3,2,1,0}$=”0000”, LA_7….LA_0=”00000000”(Initial display line 0) DSE=”1”																		
SC_3	SC_2	SC_1	SC_0	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	Inhibited	Inhibited	Inhibited	Inhibited	Inhibited	Inhibited
COM_0				0	36	32	28	24	20	16	12	8	4						
COM_1																			
COM_2																			
COM_3					39														
COM_4					0														
COM_5																			
COM_6																			
COM_7						39													
COM_8						0													
COM_9																			
COM_{10}																			
COM_{11}							39												
COM_{12}							0												
COM_{13}																			
COM_{14}																			
COM_{15}								39											
COM_{16}								0											
COM_{17}																			
COM_{18}																			
COM_{19}									39										
COM_{20}									0										
COM_{21}																			
COM_{22}																			
COM_{23}										39									
COM_{24}										0									
COM_{25}																			
COM_{26}																			
COM_{27}											39								
COM_{28}											0								
COM_{29}																			
COM_{30}																			
COM_{31}												39							
COM_{32}												0							
COM_{33}																			
COM_{34}																			
COM_{35}													39						
COM_{36}													0						
COM_{37}																			
COM_{38}																			
COM_{39}				39	35	31	27	23	19	15	11	7	3						

DS: Duty cycle ratio, SC: Initial COM line, LA: Initial display line

■ ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	CONDITION	TERMINAL	RATING	UNIT
Supply Voltage (1)	V_{DD}	V_{SS}=0V Ta = +25°C	V_{DD}	-0.3 to +4.0	V
Supply Voltage (2)	V_{EE}		V_{EE}	-0.3 to +4.0	V
Supply Voltage (3)	V_{OUT}		V_{OUT}	-0.3 to +19.0	V
Supply Voltage (4)	V_{REG}		V_{REG}	-0.3 to +19.0	V
Supply Voltage (5)	V_{LCD}		V_{LCD}	-0.3 to +19.0	V
Supply Voltage (6)	V_1, V_2, V_3, V_4		V_1, V_2, V_3, V_4	-0.3 to V_{LCD} + 0.3	V
Input Voltage	V_I		*1	-0.3 to V_{DD} + 0.3	V
Storage Temperature	T_{stg}			-45 to +125	°C

Note 1) D_0 to D_{15}, CSb, RS, RDb, WRb, OSC_1, RESb, $TEST_1$, $TEST_2$, terminals.

■ RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	TERMINAL	MIN	TYP	MAX	UNIT	NOTE
Supply Voltage	V_{DD1}	V_{DD}	1.7		3.3	V	*1
	V_{DD2}		2.4		3.3	V	*2
	V_{EE}	V_{EE}	2.4		3.3	V	*3
Operating Voltage	V_{LCD}	V_{LCD}	5		18.0	V	*4
	V_{OUT}	V_{OUT}			18.0	V	
	V_{REG}	V_{REG}			$V_{OUT} \times 0.9$	V	
	V_{REF}	V_{REF}	2.1		3.3	V	*5
Operating Temperature	T_{opr}		-30		85	°C	

Note1) Applies to the condition when the reference voltage generator is not used.
Note2) Applies to the condition when the reference voltage generator is used.
Note3) Applies to the condition when the voltage booster is used.
Note4) The following relationship among the supply voltages must be maintained.
$V_{SS}<V_4<V_3<V_2<V_1<V_{LCD}\leq V_{OUT}$
Note5) The relationship: $V_{REF}<V_{EE}$ must be maintained.

■ DC CHARACTERISTICS 1

V_{SS} = 0V, V_{DD} = +1.7 to +3.3V, Ta = -30 to +85°C

PARAMETER	SYMBOL	CONDITION		MIN	TYP	MAX	UNIT	NOTE
High level input voltage	V_{IH}			0.8 V_{DD}		V_{DD}	V	*1
Low level input voltage	V_{IL}			0		0.2V_{DD}	V	*1
High level output voltage	V_{OH1}	I_{OH} = -0.4mA		V_{DD} - 0.4			V	*2
Low level output voltage	V_{OL1}	I_{OL} = 0.4mA				0.4	V	*2
High level output voltage	V_{OH2}	I_{OH} = -0.1mA		V_{DD} - 0.4			V	*3
Low level output voltage	V_{OL2}	I_{OL} = 0.1mA				0.4	V	*3
Input leakage current	I_{LI}	V_I = V_{SS} or V_{DD}		-10		10	µA	*4
Output leakage current	I_{LO}	V_I = V_{SS} or V_{DD}		-10		10	µA	*5
Driver ON-resistance	R_{ON1}	$\|\Delta V_{ON}\|$ = 0.5V	V_{LCD} = 10V		1	2	kΩ	*6
			V_{LCD} = 6V		2	4		
Stand-by current	I_{STB}	CSb=H, Ta=25°C	V_{DD} = 3V			15	µA	*7
Internal oscillation Frequency	f_{OSC1}	V_{DD} = 3V Ta = 25°C		152	186	220	kHz	*8
	f_{OSC2}			34	42	50		*9
	f_{OSC3}			4.9	6.0	7.1		*10
External oscillation Frequency	f_{r1}	Rf=51kΩ			172		kHz	*11
	f_{r2}	Rf=240kΩ			40			
	f_{r3}	Rf=1800kΩ			5.5			
Voltage converter output voltage	V_{OUT}	N-time booster (N=2 to 5) RL = 500kΩ (V_{OUT} - V_{SS})		(N x V_{EE}) x 0.95			V	*12
Supply current (1)	I_{DD1}	V_{DD} = 3V, 5-time booster Whole ON pattern			520	780	µA	*13
Supply current (2)	I_{DD2}	V_{DD} = 3V, 5-time booster Checker pattern			650	980		
Supply current (3)	I_{DD3}	V_{DD} = 3V,4-time booster Whole ON pattern			360	540		
Supply current (4)	I_{DD4}	V_{DD} = 3V, 4-time booster Checker pattern			450	680		
V_{BA} Operating voltage	V_{BA}	V_{EE} = 2.4 to 3.3V		(0.9 V_{EE}) x 0.98	0.9 V_{EE}	(0.9 V_{EE}) x 1.02	V	*14
V_{REG} Operating voltage	V_{REG}	V_{EE} = 2.4 to 3.3V V_{REF} = 0.9 x V_{EE} N-time booster (N=2 to 5)		(V_{REF} x N) x 0.97	(V_{REF} x N)	(V_{REF} x N) x 1.03	V	*15
Output Voltage	V_2			-100	0	+100	mV	*16
	V_3			-100	0	+100		
	V_{D12}			-30	0	+30		
	V_{D34}			-30	0	+30		
	V_{D24}			-30	0	+30		

■ CLOCK and FRAME FREQUENCY

PARAMETER	SYMBOL	Display mode	Display duty cycle ratio (1/D) <DSE=0>				NOTE
			1/41 to 1/25	1/21 to 1/13	1/9	1/5	
Internal clock	f_{OSC}	16 Gradation mode	f_{OSC} / (62xD)	f_{OSC} / (62xDx2)	f_{OSC} / (62xDx4)	f_{OSC} / (62xDx8)	FLM
		Simplified 8 gradation mode	f_{OSC} / (14xD)	f_{OSC} / (14xDx2)	f_{OSC} / (14xDx4)	f_{OSC} / (14xDx8)	
		B&W mode	f_{OSC} / (2xD)	f_{OSC} / (2xDx2)	f_{OSC} / (2xDx4)	f_{OSC} / (2xDx8)	
External clock	f_{CK}	16 Gradation mode	f_{CK} / (62xD)	f_{CK} / (62xDx2)	f_{CK} / (62xDx4)	f_{CK} / (62xDx8)	
		Simplified 8 gradation mode	f_{CK} / (14xD)	f_{CK} / (14xDx2)	f_{CK} / (14xDx4)	f_{CK} / (14xDx8)	
		B&W mode	f_{CK} / (2xD)	f_{CK} / (2xDx2)	f_{CK} / (2xDx4)	f_{CK} / (2xDx8)	

APPLIED TERMINALS and CONDITIONS

Note 1) D_0-D_{15}, CSb, RS, RDb, WRb, P/S, SEL68, RESb

Note 2) D_0-D_{15}

Note 3) CL, FLM, FR, CLK

Note 4) CSb, RS, SEL68, RDb, WRb, P/S, RESb, OSC_1

Note 5) D_0-D_{15} in the high impedance

Note 6) $SEGA_0$-$SEGA_{127}$, $SEGB_0$-$SEGB_{127}$, $SEGC_0$-$SEGC_{127}$, COM_0-COM_{39}
- Defines the resistance between the COM/SEG terminals and each of the power supply terminals (V_{LCD}, V_1, V_2, V_3 and V_4) at the condition of 0.5V deference and 1/8 LCD bias ratio.

Note 7) V_{DD}
- The oscillator is halted, CSb="1" (disabled), No-load on the COM/SEG drivers

Note 8) OSC
- Defines the internal oscillation frequency at (Rf_2, Rf_1, Rf_0)=(0,0,0) in the variable gradation mode.

Note 9) OSC
- Defines the internal oscillation frequency at (Rf_2, Rf_1, Rf_0)=(0,0,0) in the fixed gradation mode.

Note 10) OSC
- Defines the internal oscillation frequency at (Rf_2, Rf_1, Rf_0)=(0,0,0) in the Black & White mode.

Note 11) V_{DD}=3V, Ta=25°C

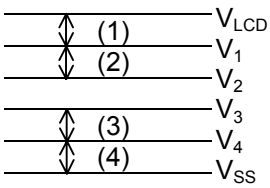
Note 12) V_{OUT}
- Applies to the condition when the internal voltage booster, the internal oscillator and internal power circuits are used.
- V_{EE}=2.4V to 3.3V, EVR= (1,1,1,1,1,1,1), 1/4 to 1/8 LCD bias, 1/41 duty cycle, No-load on COM/SEG drivers
- RL=500KΩ between the V_{OUT} and the V_{SS}, CA_1=CA_2=1.0uF, CA_3=0.1uF, DCON="1", AMPON="1"

Note 13) V_{DD}
- Applies to the condition using the internal oscillator and internal power circuits, no access between the LSI and MPU.
- EVR= (1,1,1,1,1,1,1), All pixels turned-on or checkerboard display in gradation mode.
No-load on the COM/SEG drivers.
- V_{DD}=V_{EE}, V_{REF}=0.9V_{EE}, CA_1=CA_2=1.0uF, CA_3=0.1uF, DCON="1", AMPON="1", NLIN="0"
1/41 Duty cycle, Ta=25°C

Note 14) V_{BA}
- Applies to the condition that V_{BA}=V_{REF} and voltage booster N= 1. DCON="0", V_{OUT}=13.5V input.

Note 15) V_{REG}
- V_{EE}=2.4V to 3.3V, V_{REF}=0.9V_{EE}, V_{OUT}=18V, 1/4 to 1/8 LCD bias ratio, 1/41 duty cycle, EVR=(1,1,1,1,1,1,1)
- Checkerboard display, No-load on the COM/SEG drivers, the voltage booster N=2 to 5 CA_1=CA_2=1.0uF, CA_3=0.1uF, DCON="0", AMPON="1", NLIN="0"

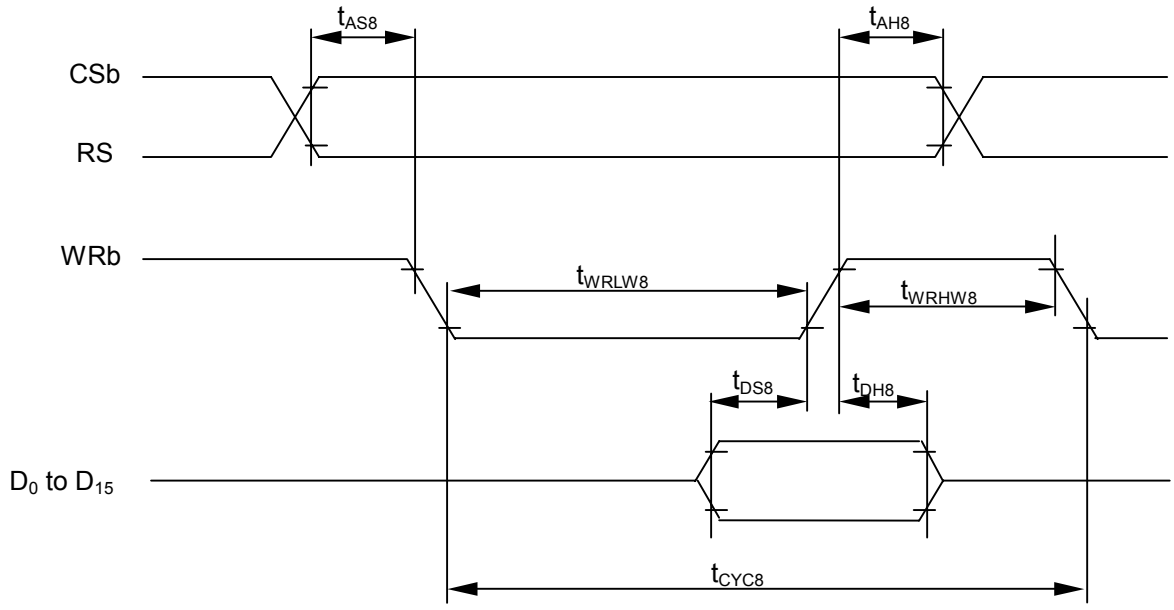
Note 16) V_{LCD}, V_1, V_2, V_3, V_4
- V_{EE}=3.0V, V_{REF}=0.9V_{EE}, V_{OUT}=15V, 1/4 to 1/8 LCD Bias, EVR= (1,1,1,1,1,1,1), Display OFF, No-load on the COM/SEG drivers, voltage booster N=5, CA_1=CA_2=1.0uF, CA_3=0.1uF, DCON="0", AMPON="1"



V_{D12}: (1)-(2)
V_{D34}: (3)-(4)
V_{D24}: (2)-(4)

■ AC CHARACTERISTICS

- Write operation (80-type MPU)



(V_{DD}=2.5 to 3.3V, Ta=-30 to +85°C)

PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
Address hold time Address setup time	t_{AH8} t_{AS8}		0 0		ns ns	CSb RS
System cycle time Enable "L" level pulse width Enable "H" level pulse width	t_{CYC8} t_{WRLW8} t_{WRHW8}		90 35 35		ns ns ns	WRb
Data setup time Data hold time	t_{DS8} t_{DH8}		30 5		ns ns	D_0 to D_{15}

(V_{DD}=2.2 to 2.5V, Ta=-30 to +85°C)

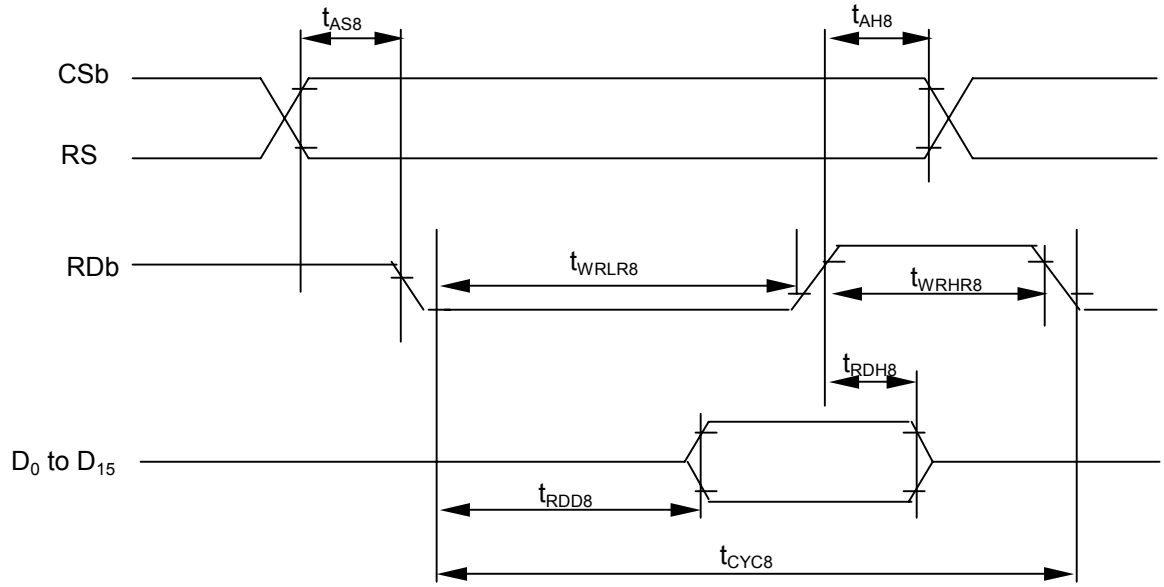
PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
Address hold time Address setup time	t_{AH8} t_{AS8}		0 0		ns ns	CSb RS
System cycle time Enable "L" level pulse width Enable "H" level pulse width	t_{CYC8} t_{WRLW8} t_{WRHW8}		160 70 70		ns ns ns	WRb
Data setup time Data hold time	t_{DS8} t_{DH8}		40 5		ns ns	D_0 to D_{15}

(V_{DD}=1.7 to 2.2V, Ta=-30 to +85°C)

PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
Address hold time Address setup time	t_{AH8} t_{AS8}		0 0		ns ns	CSb RS
System cycle time Enable "L" level pulse width Enable "H" level pulse width	t_{CYC8} t_{WRLW8} t_{WRHW8}		180 80 80		ns ns ns	WRb
Data setup time Data hold time	t_{DS8} t_{DH8}		70 10		ns ns	D_0 to D_{15}

Note) Each timing is specified based on 20% and 80% of V_{DD}.

- **Read operation (80-type MPU)**



(V_{DD}=2.5 to 3.3V, Ta=-30 to +85°C)

PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
Address hold time Address setup time	t_{AH8} t_{AS8}		0 0		ns ns	CSb RS
System cycle time Enable "L" level pulse width Enable "H" level pulse width	t_{CYC8} t_{WRLR8} t_{WRHR8}		180 80 80		ns ns ns	RDB
Read Data delay time Read Data hold time	t_{RDD8} t_{RDH8}	CL=15pF	 0	60	ns ns	D_0 to D_{15}

(V_{DD}=2.2 to 2.5V, Ta=-30 to +85°C)

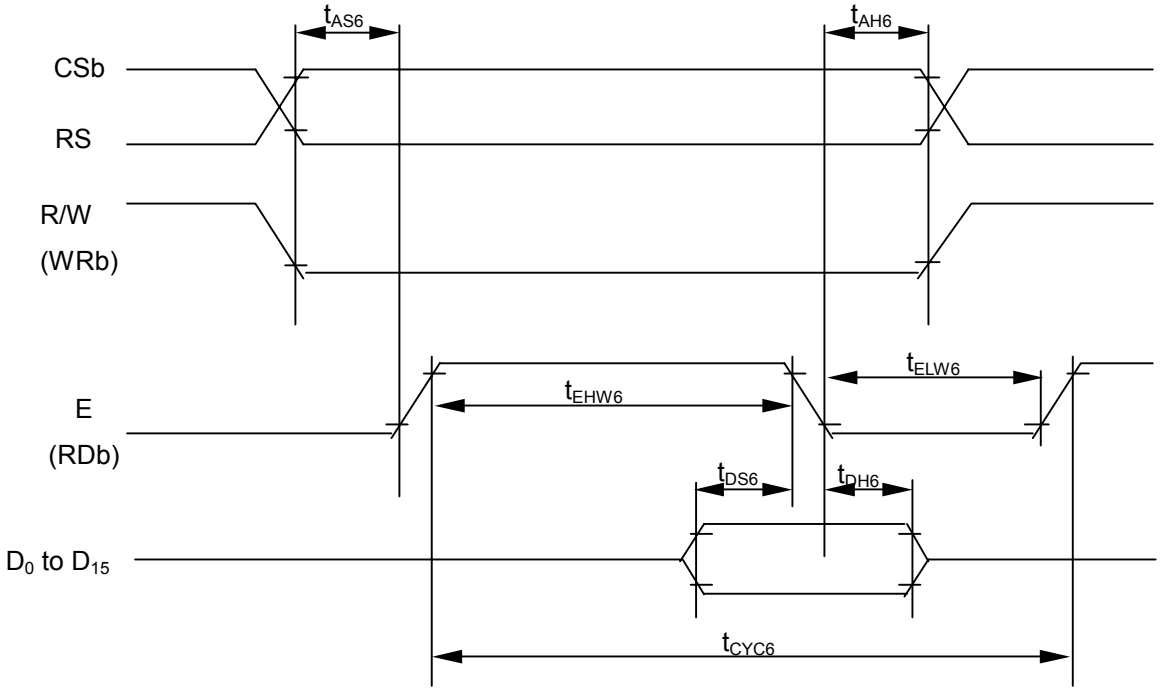
PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
Address hold time Address setup time	t_{AH8} t_{AS8}		0 0		ns ns	CSb RS
System cycle time Enable "L" level pulse width Enable "H" level pulse width	t_{CYC8} t_{WRLR8} t_{WRHR8}		180 80 80		ns ns ns	RDb
Read Data delay time Read Data hold time	t_{RDD8} t_{RDH8}	CL=15pF	 0	60	ns ns	D_0 to D_{15}

(V_{DD}=1.7 to 2.2V, Ta=-30 to +85°C)

PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
Address hold time Address setup time	t_{AH8} t_{AS8}		0 0		ns ns	CSb RS
System cycle time Enable "L" level pulse width Enable "H" level pulse width	t_{CYC8} t_{WRLR8} t_{WRHR8}		250 120 120		ns ns ns	RDb
Read Data delay time Read Data hold time	t_{RDD8} t_{RDH8}	CL=15pF	 0	110	ns ns	D_0 to D_{15}

Note) Each timing is specified based on 20% and 80% of V_{DD}.

- **Write operation (68-type MPU)**



(V_{DD}=2.5 to 3.3V, Ta=-30 to +85°C)

PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
Address hold time Address setup time	t_{AH6} t_{AS6}		0 0		ns ns	CSb RS
System cycle time Enable "L" level pulse width Enable "H" level pulse width	t_{CYC6} t_{ELW6} t_{EHW6}		90 35 35		ns ns ns	E
Data setup time Data hold time	t_{DS6} t_{DH6}		40 5		ns ns	D_0 to D_{15}

(V_{DD}=2.2 to 2.5V, Ta=-30 to +85°C)

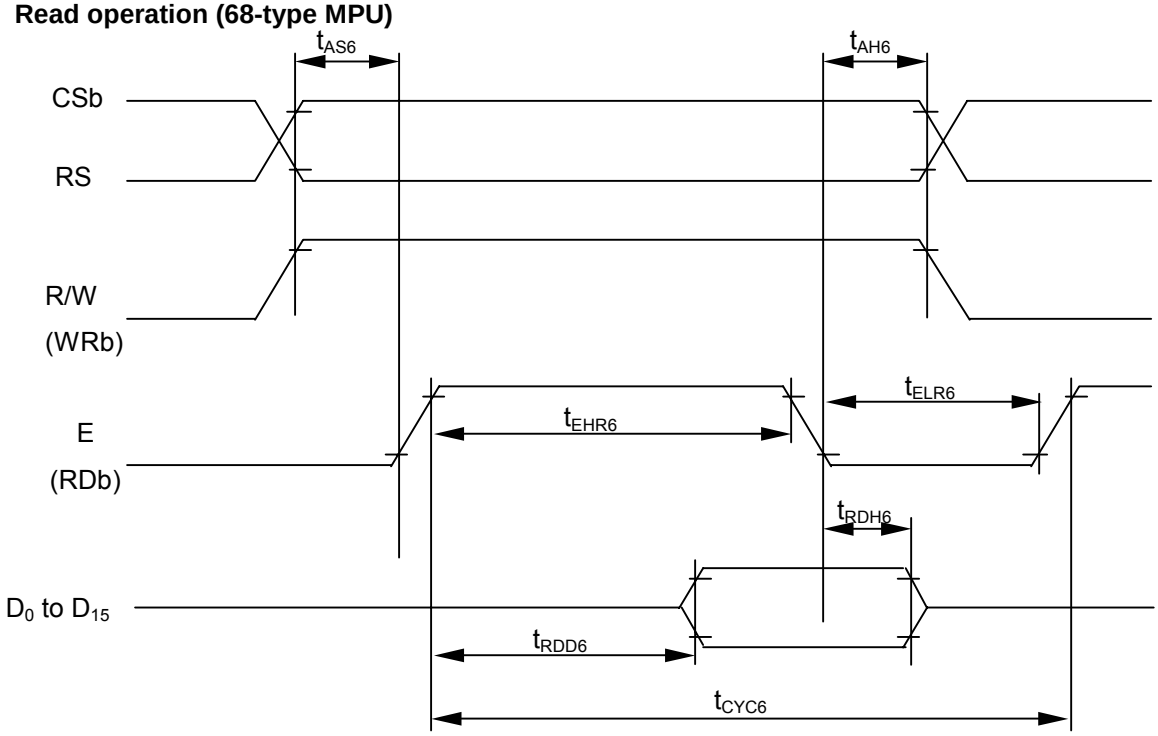
PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
Address hold time Address setup time	t_{AH6} t_{AS6}		0 0		ns ns	CSb RS
System cycle time Enable "L" level pulse width Enable "H" level pulse width	t_{CYC6} t_{ELW6} t_{EHW6}		160 70 70		ns ns ns	E
Data setup time Data hold time	t_{DS6} t_{DH6}		50 5		ns ns	D_0 to D_{15}

(V_{DD}=1.7 to 2.2V, Ta=-30 to +85°C)

PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
Address hold time Address setup time	t_{AH6} t_{AS6}		0 0		ns ns	CSb RS
System cycle time Enable "L" level pulse width Enable "H" level pulse width	t_{CYC6} t_{ELW6} t_{EHW6}		180 80 80		ns ns ns	E
Data setup time Data hold time	t_{DS6} t_{DH6}		70 10		ns ns	D_0 to D_{15}

Note) Each timing is specified based on 20% and 80% of V_{DD}.

- **Read operation (68-type MPU)**



(V_{DD}=2.5 to 3.3V, Ta=-30 to +85°C)

PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
Address hold time Address setup time	t_{AH6} t_{AS6}		0 0		ns ns	CSb RS
System cycle time Enable "L" level pulse width Enable "H" level pulse width	t_{CYC6} t_{ELR6} t_{EHR6}		180 80 80		ns ns ns	E
Read Data delay time Read Data hold time	t_{RDD6} t_{RDH6}	CL=15pF	0	70	ns ns	D_0 to D_{15}

(V_{DD}=2.2 to 2.5V, Ta=-30 to +85°C)

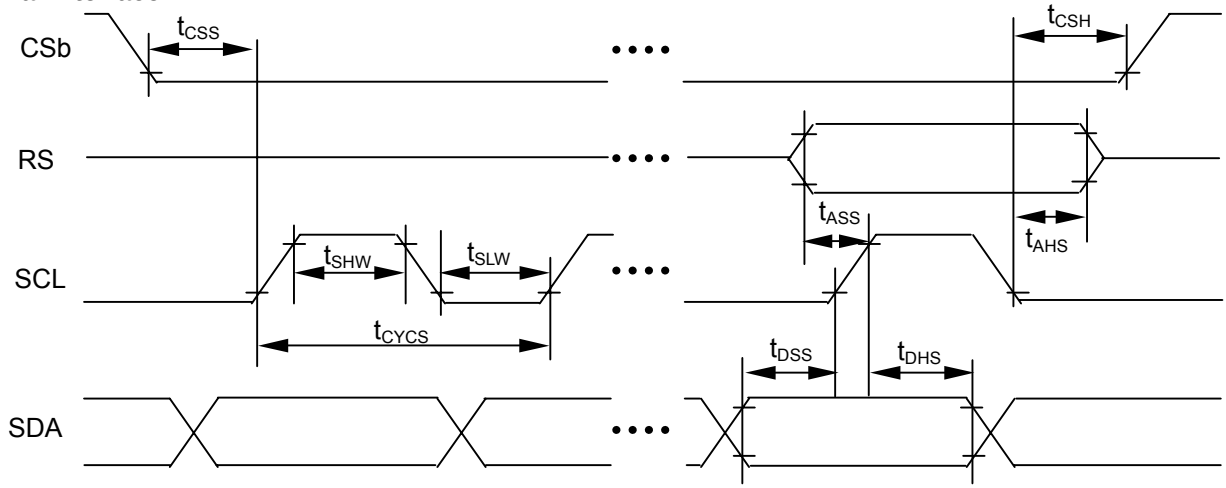
PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
Address hold time Address setup time	t_{AH6} t_{AS6}		0 0		ns ns	CSb RS
System cycle time Enable "L" level pulse width Enable "H" level pulse width	t_{CYC6} t_{ELR6} t_{EHR6}		180 80 80		ns ns ns	E
Read Data delay time Read Data hold time	t_{RDD6} t_{RDH6}	CL=15pF	0	70	ns ns	D_0 to D_{15}

(V_{DD}=1.7 to 2.2V, Ta=-30 to +85°C)

PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
Address hold time Address setup time	t_{AH6} t_{AS6}		0 0		ns ns	CSb RS
System cycle time Enable "L" level pulse width Enable "H" level pulse width	t_{CYC6} t_{ELR6} t_{EHR6}		250 120 120		ns ns ns	E
Read Data delay time Read Data hold time	t_{RDD6} t_{RDH6}	CL=15pF	0	110	ns ns	D0 to D15

Note) Each timing is specified based on 20% and 80% of V_{DD}.

- **Serial interface**



(V_{DD}=2.5 to 3.3V, Ta=-30 to +85°C)

PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
Serial clock cycle	t_{CYCS}		50		ns	SCL
SCL "H" level pulse width	t_{SHW}		20		ns	
SCL "L" level pulse width	t_{SLW}		20		ns	
Address setup time	t_{ASS}		20		ns	RS
Address hold time	t_{AHS}		20		ns	
Data setup time	t_{DSS}		20		ns	SDA
Data hold time	t_{DHS}		20		ns	
CSb – SCL time	t_{CSS}		20		ns	CSb
CSb hold time	t_{CSH}		20		ns	

(V_{DD}=2.2 to 2.5V, Ta=-30 to +85°C)

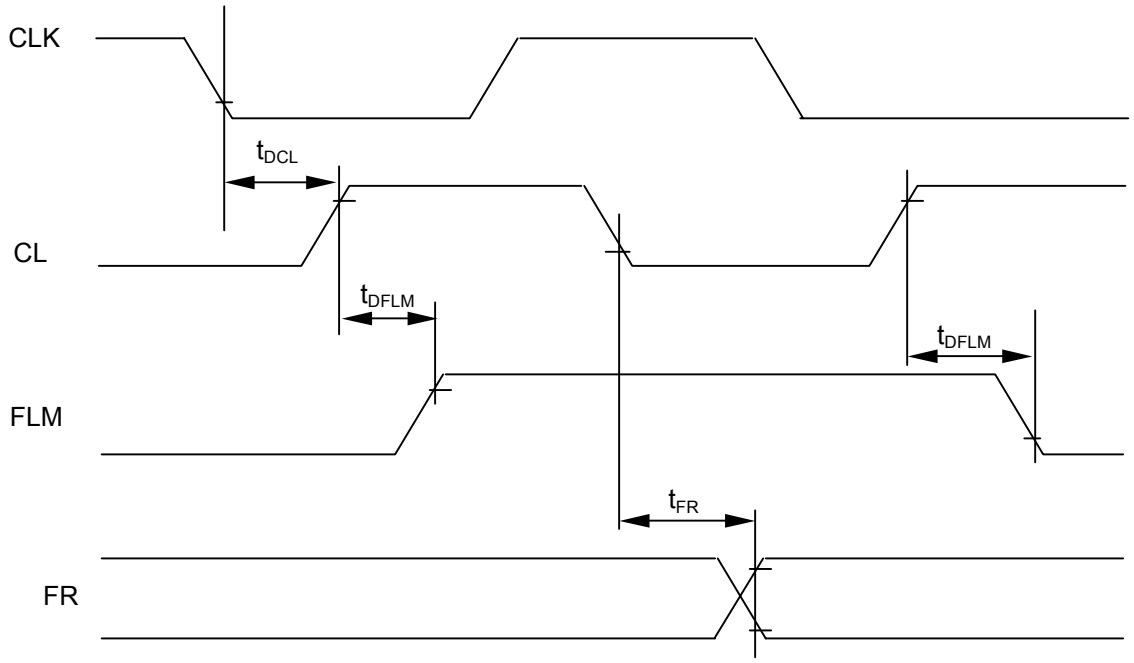
PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
Serial clock cycle	t_{CYCS}		50		ns	SCL
SCL "H" level pulse width	t_{SHW}		20		ns	
SCL "L" level pulse width	t_{SLW}		20		ns	
Address setup time	t_{ASS}		20		ns	RS
Address hold time	t_{AHS}		20		ns	
Data setup time	t_{DSS}		20		ns	SDA
Data hold time	t_{DHS}		20		ns	
CSb – SCL time	t_{CSS}		20		ns	CSb
CSb hold time	t_{CSH}		20		ns	

(V_{DD}=1.7 to 2.2V, Ta=-30 to +85°C)

PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
Serial clock cycle	t_{CYCS}		80		ns	SCL
SCL "H" level pulse width	t_{SHW}		35		ns	
SCL "L" level pulse width	t_{SLW}		35		ns	
Address setup time	t_{ASS}		35		ns	RS
Address hold time	t_{AHS}		35		ns	
Data setup time	t_{DSS}		35		ns	SDA
Data hold time	t_{DHS}		35		ns	
CSb – SCL time	t_{CSS}		35		ns	CSb
CSb hold time	t_{CSH}		35		ns	

Note) Each timing is specified based on 20% and 80% of V_{DD}.

- **Display control timing**



Output timing (V_{DD}=2.4 to 3.3V, Ta=-30 to +85°C)

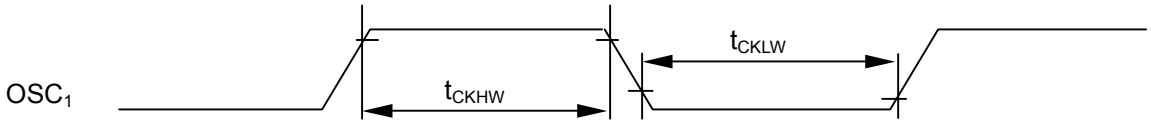
PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
FLM delay time	t_{DFLM}	CL=15pF	0	500	ns	FLM
FR delay time	t_{FR}		0	500	ns	FR
CL delay time	t_{DCL}		0	200	ns	CL

Output timing (V_{DD}=1.7 to 2.4V, Ta=-30 to +85°C)

PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
FLM delay time	t_{DFLM}	CL=15pF	0	1000	ns	FLM
FR delay time	t_{FR}		0	1000	ns	FR
CL delay time	t_{DCL}		0	200	ns	CL

Note) Each timing is specified based on 20% and 80% of V_{DD}.

- **Input clock timing**

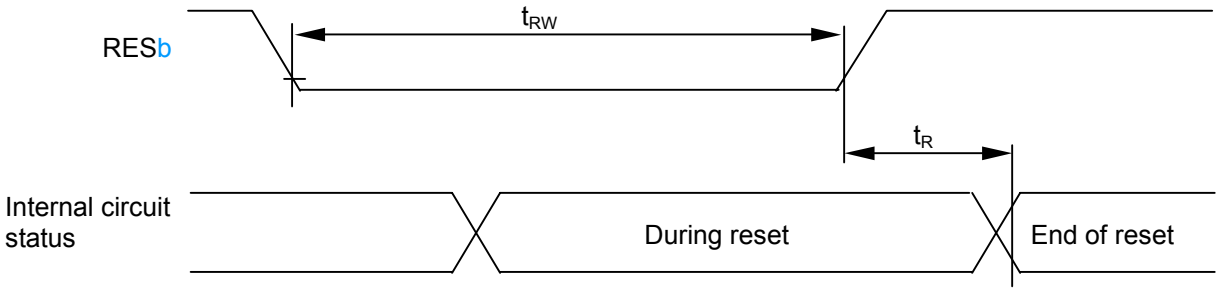


(V_{DD}=1.7 to 3.3V, Ta=-30 to +85°C)

PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
OSC_1 "H" level pulse width (1)	t_{CKHW1}		2.27	3.29	μs	OSC_1 ∗1
OSC_1 "L" level pulse width (1)	t_{CKLW1}		2.27	3.29	μs	
OSC_1 "H" level pulse width (2)	t_{CKHW2}		10	14.7	μs	OSC_1 ∗2
OSC_1 "L" level pulse width (2)	t_{CKLW2}		10	14.7	μs	
OSC_1 "H" level pulse width (3)	t_{CKHW3}		70	103	μs	OSC_1 ∗3
OSC_1 "L" level pulse width (3)	t_{CKLW3}		70	103	μs	

Note) Each timing is specified based on 20% and 80% of V_{DD}.
Note 1) Applied to the variable gradation / mode MON="0",PWM="0"
Note 2) Applied to the fixed gradation / mode MON="0",PWM="1"
Note 3) Applied to the B&W mode / MON="1"

- Reset input timing



(V_{DD}=2.4 to 3.3V, Ta=-30 to +85°C)

PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	Terminal
Reset time	t_R			1.0	µs	
RESb "L" level pulse width	t_{RW}		10.0		µs	RESb

(V_{DD}=1.7 to 2.4V, Ta=-30 to +85°C)

PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	Terminal
Reset time	t_R			1.5	µs	
RESb "L" level pulse width	t_{RW}		10.0		µs	RESb

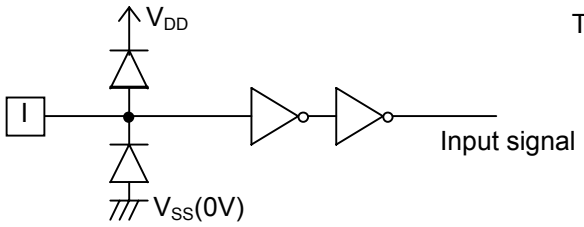
Note) Each timing is specified based on 20% and 80% of V_{DD}.

- Typical characteristic

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Basic delay time of gate	Ta=+25°C, V_{SS}=0V, V_{DD}=3.0V		10		ns

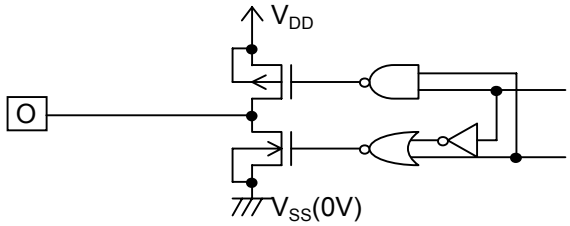
- Input output terminal type

(a) Input circuit



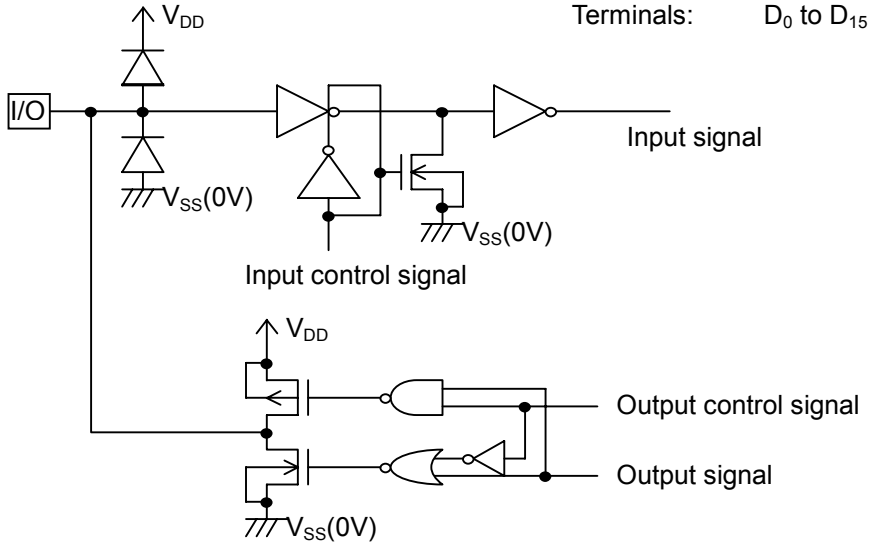
Terminals: CSb, RS, RDb, WRb, SEL68, P/S, RESb

(b) Output circuit



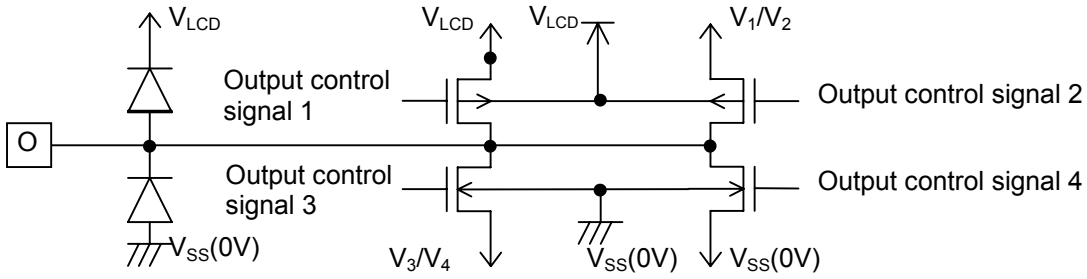
Terminals: FLM, CL, FR, CLK

(c) Input/Output circuit



Terminals: D_0 to D_{15}

(d) Display output circuit

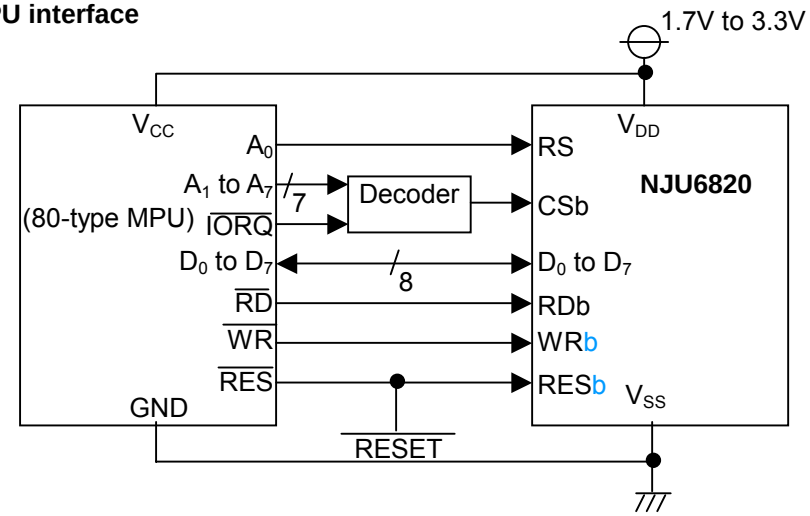


Terminals: $SEGA_0$ to $SEGA_{127}$
$SEGB_0$ to $SEGB_{127}$
$SEGC_0$ to $SEGC_{127}$
COM_0 to COM_{39}

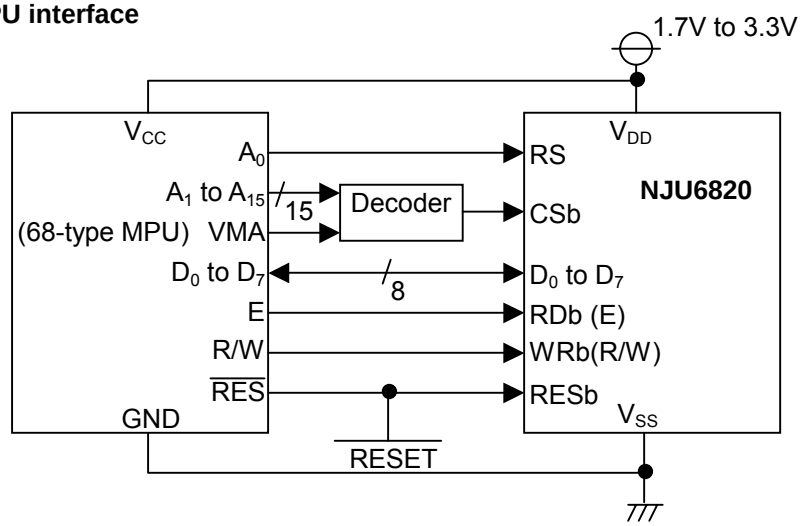
■ APPLICATION CIRCUIT EXAMPLES

(1) MPU Connections

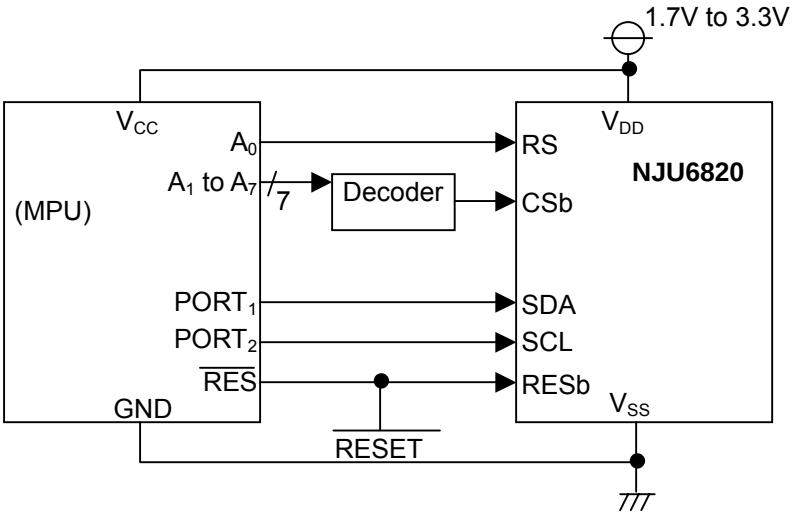
80-type MPU interface



68-type MPU interface



Serial interface



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