Highly Integrated RISController™

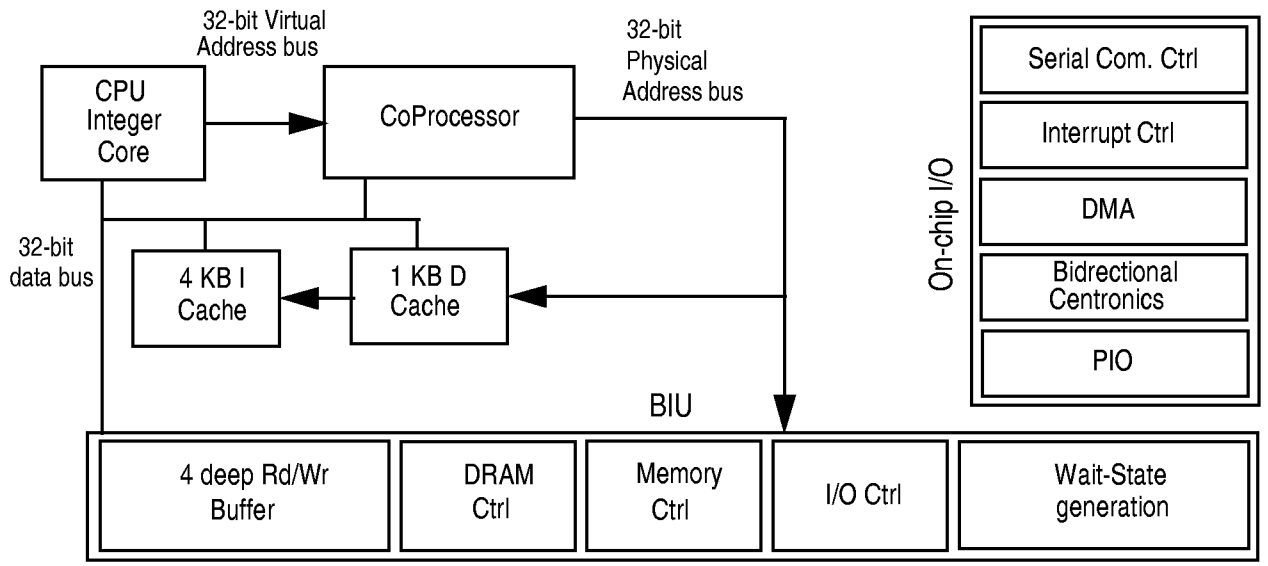
IDT79RC36100™

RISController

Features

- **Instruction set compatible with the RISCore32 family of CPUs**
- **System-level integration minimizes system cost**
  - *32-bit RISC CPU*
  - *4KB instruction cache on-chip*
  - *1KB data cache on-chip*
  - *Memory, DMA and I/O controllers*
  - *System peripherals*
- **24 MIPS/ 42K Dhrystone-2.1 at 25 MHz**
- **31 MIPS/ 55K Dhrystone-2.1 at 33 MHz**
- **Improved cache control and cache locking**
- **Flexible bus interface allows simple, low cost designs**
  - *De-multiplexed address and data bus*
  - *On-chip 4-deep Read/Write buffer*
  - *Programmable bus width (8-,16-, and 32-bit)*
- **On-chip DRAM controller with Address Multiplexer**
  - *Supports optional interleaved DRAMs*
- **On-chip memory and I/O controller**
  - *Chip selects, wait-state generator*
  - *Supports optional interleaved ROMs*
  - *Supports PCMCIA Master protocol*
- **On-chip DMA controller**
  - *4 internal channels, 2 external channels*
- **On-chip communications controller**
  - *Async*
  - *Sync (HDLC, SDLC)*
  - *2 channels*
- **On-chip Timers and interrupt controller**
- **On-chip bi-directional IEEE 1284 Centronics™ Parallel Port interface**
- **Built-in debug/emulator support**
- **QFP-208 packaging**

Block diagram



Description

The IDT79RC36100 is a highly integrated member of the IDT RISController family. The RC36100 implements a "system on a chip," which includes the CPU core, cache memory, system logic functions, and application-specific peripherals. This high level of integration greatly reduces system design challenges, substantially decreasing design risk and time to market. The RC36100 is well-suited to a wide variety of cost sensitive, space constrained embedded applications.

The RC36100 Integrated RISController is based upon the general purpose RISCore32 series CPU core and integrates a substantial amount of on-chip instruction and data cache memory. In addition to the CPU core and cache memory, the RC36100 integrates all necessary system logic functions on-chip, including DRAM, ROM, I/O and DMA controllers; counter/timers; interrupt controllers; and general purpose parallel I/O and debug support circuitry. The RC36100 also integrates printer and data communication peripherals, including an IEEE 1284 parallel port and two serial communication ports. The RC36100 includes four on-chip bus controllers, allowing seamless interface with a wide variety of standard memories and peripherals that include:

- **Standard page-mode DRAM**
- **EPROM, FLASH, SRAM, Dual-Port SRAM**
- **FIFO, SCSI, A/D, and other I/O peripherals**
- **Ethernet, data compression, and other coprocessors**

The RC36100 also integrates an IEEE 1284, RS-232C and Local Talk serial ports to serve applications that include:

- **Monochrome laser and ink-jet printers**
- **Host-based printer cards**
- **Multi-function laser/fax printer systems**

In addition, the RC36100 integrates asynchronous and synchronous serial controller channels and multiple timers, to serve data communications applications that include:

- **Local Area Network (LAN) interface cards**
- **Router, switcher, and data compression cards**

The RC36100 is also software compatible with all members of the IDT RISController family, including the low-cost 32-bit RC3000 and the RC4000 families of high-performance 64-bit embedded controllers. The common instruction set architecture (ISA) enables the same applications software to be used across a wide variety of price/performance points.

Hardware Overview

The RC36100 can be viewed as a "system on a chip"—a discrete system built around the RISCore32 series CPU. By integrating system functionality on a single chip, dramatic reductions in cost, size, and power are achieved, reducing overall system complexity and minimizing system development time. Functional units of the RC36100 are illustrated in the block diagram provided on page 1.

CPU Core

The RISCore32 series CPU core is a full 32-bit RISC integer execution engine that uses a five-stage pipeline to sustain a peak single-cycle execution rate. This CPU core contains an integer ALU unit and bit shifter with a separate integer multiplier/divider unit, address adder and program counter generator, and thirty-two orthogonal 32-bit registers. The RC36100 execution core implements the MIPS-I instruction set architecture (ISA) and is binary compatible with all other MIPS CPU engines, including the low-cost RC3000 family and the high-speed RC4000 family.

System Control Co-Processor

The RC36100 Integrated RISController also integrates an on-chip System Control Co-processor (CP0). CP0 manages the RC36100's exception handling, virtual-to-physical address memory mapping as well as various programmable bus-to-cache interface features. Details on each of these topics are provided in the *IDT79RC36100 Integrated RISController Hardware User's Manual*.

The RC36100 does not include the optional Translation Lookaside Buffer (TLB) found in other members of IDT's RC3000 family, but it does perform the same virtual-to-physical address mapping as the base versions of this product. These base version devices support distinct kernel and user mode operation without requiring page management software or an on-chip TLB, allowing a simpler operating system software model and a lower cost processor.

Clock Generator Unit

The RC36100 Integrated RISController is driven from a single, double frequency input clock. An on-chip clock generator manages the interaction between the CPU core, caches, and bus interface. The clock generator unit replaces the external delay line that was required in discrete RISCore32 series- based systems.

Instruction Cache

The RC36100 Integrated RISController integrates 4KB of on-chip instruction cache, which is organized with a line size of 16 bytes (four 32-bit entries). This relatively large cache contributes substantially to the high performance available in the RC36100 and allows even low-cost memory systems, when based on the RC36100, to achieve high performance.

The cache is implemented as a direct mapped cache, capable of caching instructions from anywhere within the 4GB physical address space. Also, because the cache is implemented by using physical addresses and physical tags, it does not require flushing on context switches.

To improve real-time performance, the RC36100 instruction cache supports a cache-locking mechanism. Each cache can be split into halves or quarters, allowing each half or quarter to service a different area of the address space. This feature enables the system software to "lock" time-critical code—such as router address hash-table lookup algorithms and interrupt service routines—into one of the halves or quarters, allowing access to the unused portions without affecting the locked time-critical code. This technique allows software to perform instruction cache locking and ensures deterministic response.

Data Cache

The RC36100 Integrated RISController incorporates an on-chip data cache of 1KB, which is organized as a line size of 4 bytes (one word). This relatively large data cache contributes substantially to the high performance inherent to the RC36100. As with the instruction cache, the data cache is also implemented as a direct mapped physical address cache, and the cache is capable of mapping any word within the 4GB physical address space.

To insure that main memory is always consistent and coherent with the internal cache, the data cache is implemented as a write-through cache. To minimize processor stalls due to data write operations, the bus interface unit incorporates a 4-deep write buffer that captures address and data at the processor execution rate. This data cache feature allows the retirement of data to main memory at a much slower rate, without impacting the internal CPU's pipeline performance.

The RC36100 also allows the data cache to be split into halves or quarters, with each half or quarter servicing a different area of the large address space. This enables the system software to lock time-critical data—such as routing address information tables and the interrupt stack—into one of the sections, while still allowing other tasks access to the unused portions without disrupting the critical data. This technique allows software to perform data cache locking without requiring memory management support.

Bus Interface Unit

The RC36100 uses its large internal caches to provide the majority of its memory bandwidth requirements to/from the execution engine. The execution engine pipeline can access both one instruction and one data load/store per clock cycle. The RC36100 requires access to main memory only on write operations and the relatively rare cache miss. Thus, the RC36100 can use a simple bus interface that connects to slow memory devices without sacrificing performance.

The RC36100 bus interface uses a de-multiplexed address and data bus. This interface readily connects to memory subsystems that are 8-, 16-, or 32-bits wide, and/or interleaved.

The RC36100 incorporates a 4-deep write buffer to decouple the speed of the execution engine from the speed of the memory system. The write buffers capture the processor's address and data information during internal store operations, storing the information as FIFO at a maximum rate of one store per clock. The write buffer then presents the bus interface write transactions at a rate the memory system can accommodate.

During main memory writes, the RC36100 can break large data—such as a 32-bit word—into a series of smaller transactions—such as bytes—according to the width of the memory port being written. This operation is transparent to the software that initiated the store and insures that the same software can run across multiple platforms that have different memory system configurations.

The RC36100 read interface performs both single data reads and quad word reads. To accommodate slower reads, the RC36100 incorporates a 4-deep read buffer FIFO, enabling the external interface to queue data within the processor before releasing it to perform a burst fill of the internal caches.

In addition, the RC36100 can perform on-chip data packing when performing large data reads—such as quad words—from narrower memory systems—such as 16-bit. Once again, this operation is transparent to the actual software, simplifying migration of software to higher performance (true 32-bit) systems and field upgrades to wider memory. Because this capability works for either instruction or data reads, the RC36100 easily supports 8-, 16-, 32-bit, or interleaved boot PROMs.

Memory Controller

The RC36100 Integrated RISController uses the on-chip memory controller to gluelessly attach external ROM (including FLASH) and/or SRAM in a number of system configurations.

For example, the memory controller supports interleaved ROM and/or SRAM, 8-bit boot ROM, 32-bit burst ROMs, and a simple 32-bit wide EPROM array. The memory controller integrates all of the control signals as well as managing the access timing and wait-state generation for multiple banks, all under the control of boot software.

DRAM Controller

The RC36100 Integrated RISController integrates an on-chip DRAM controller. The DRAM controller directly controls up to four banks of standard page mode DRAMs in a number of configurations, including systems with varying densities of DRAM, interleaved DRAM, and 16- and 32-bit wide DRAM subsystems.

I/O Controller

The RC36100 Integrated RISController has an on-chip I/O controller that performs all necessary address decoding and wait-state generation for external I/O devices. In addition, the on-chip I/O controller readily interfaces as a master to PCMCIA, including support of the large address space required and the PCMCIA chip-select protocol and timing.

DMA Control

The RC36100 Integrated RISController provides on-chip DMA control for internal peripherals, external peripherals, and external memory. Multiple internal channels allow block moves of data between any combination of memory and I/O. Each channel can also be interrupt controlled, which allows an I/O peripheral, such as the serial port, to regulate the individual transactions of a block move.

The RC36100 Integrated RISController also supports external DMA masters, which take over the external system bus via a bus request and grant handshake. Once in control of the system bus, the external DMA master can read and write to memory, I/O, and internal peripherals via the RC36100's bus controllers.

Counter/Timers

The RC36100 Integrated RISController contains three general purpose timers. Each timer consists of a 16-bit count register as well as a 16-bit compare register. The count register resets to zero and then counts upward until it equals the compare register.

When the count register equals the compare register, the TCN output is asserted and the count is reset to zero. To support intervals longer than 2^{16} ticks, the timers use a common 16-bit prescaler counter. Each timer can be programmed to select a power-of-2 divisor of the prescaler. Using these features, each timer can be used as a general purpose real-time clock, bus timeout timer, watch-dog timer, PWM/square wave/baud rate generator or gated-clock external-event counter.

PIO Interface

For controlling multi-purpose utility pins, the RC36100 Integrated RISController has a Parallel Input/Output (PIO) interface. The PIO pins can be programmed to act as general purpose inputs or outputs. Each PIO pin is also multiplexed with the inputs or outputs of other controllers .

This flexible arrangement allows system designers to customize the RC36100's resources according to their needs. Thus, designs that require a special purpose controller—such as the IEEE 1284 Centronics—can allocate pins for that purpose. However, applications that do not require the IEEE 1284 Centronics—such as data communications—can use those pins for general purpose inputs or outputs.

Serial Communications Controller

The RC36100 integrates a dual channel serial port. This peripheral controller can perform a variety of synchronous and asynchronous protocols, including RS-232C and LocalTalk. To maximize throughput, there is an option to service the on-chip serial port by the auto-initiated on-chip DMA controller, which can perform automatic block moves of data to and from the port.

Interrupt Controller

The RC36100 Integrated RISController integrates an on-chip interrupt controller to manage both external interrupts and interrupts that are signaled from the on-chip peripherals. The interrupt controller improves internal interrupt servicing speed, assists in interrupt prioritization and nesting, and interfaces with the auto-initiated DMA.

IEEE 1284 Bidirectional Parallel Port

The RC36100 Integrated RISController includes an internal IEEE1284 Centronics parallel port peripheral, which implements a true bidirectional port. Features include:

- **8-bit input target compatible protocol, for backward compatibility with legacy PCs**
- **nibble and byte mode output protocol, for backward compatibility with most PCs**
- **ECP protocol, for the emerging Laser Printer PC standard**
- **EPP protocol, for datacom applications**
- **External transceiver interface control pins**
- **Auto-initiated DMA via internal interrupts.**

Performance Overview

The following features allow the RC36100 Integrated RISController to achieve a high performance level:

- **An efficient execution engine.**
  The CPU performs ALU operations and store operations in a single cycle, has an effective load time of 1.3 cycles and branch execution rate of 1.5 cycles based on the ability of the compilers to avoid software interlocks. Thus, the RC36100 achieves over 24 dhrystone MIPS performance at 25MHz.
- **Large on-chip caches.**
  The RC36100 contains caches that are substantially larger than most embedded microprocessors. These large caches minimize the number of bus transactions required, and allow the RC36100 to achieve actual sustained performance that is very close to its peak execution rate, even with low cost memory systems.
- **Autonomous multiply and divide operations.**
  The RC36100 features an on-chip integer multiplier/divide unit that is separate from the other ALU. This allows the RC36100 to perform multiply or divide operations in parallel with other integer operations by using a single multiply or divide instruction rather than "step" operations.
- **Integrated write buffer.**
  The RC36100 features a four deep write buffer, which captures store target addresses and data at the processor execution rate and retires them to main memory at the slower main memory access rate. Use of on-chip write buffers eliminates the need for the processor to stall when performing store operations.
- **Burst read support.**
  The RC36100 enables the system designer to utilize page, static, or nibble mode RAMs when performing read operations. This minimizes the main memory read penalty and increase the effective cache hit rates.
- **Tightly coupled memory system.**
  System resources can be accessed and managed efficiently for the needs of the execution core when memory controllers are integrated on-chip.

Selectable Features

Boot-time selectable features are: 8/16 or 32-bit PROM support and Big/Little Endian selection. Other selectable, register-configurable features are:

- **Number of wait states for different memory and I/O controllers**
- **Memory and I/O map configuration**
- **16 or 32-bit DRAM and 8/16 or 32-bit memory and I/O**
- **Interleaved or non interleaved memory/DRAM**
- **Programmable control signals timing for all controllers**
- **Selectable PIO**
- **Selectable transceivers type for all controllers (FCT 260/ FCT245/FCT543)**
- **Selectable I/O style (Motorola/Intel/PCMCIA)**

Development Support

The RC36100 is supported by a rich set of development tools, ranging from system simulation tools through PROM monitor and debug support, applications software and utility libraries, logic analysis and emulator tools as well as reference evaluation boards.

Figure 1 presents an overview of the system development process that is typically used when developing RC36100 applications. The RC36100 family is supported in all phases of project development. The following list of tools allow timely, parallel development of hardware and software for RC36100 based applications:

- **IDT/c compiler, based on the GCC/GNU tool chain.**
- **Cross development tools, available for a variety of development environments.**
- **High-performance IDT floating point emulation library software.**
- **IDT Evaluation Boards, which include RAM, EPROM, I/O, and the IDT PROM Monitor.**
- **IDT/sim PROM Monitor, which implements a full PROM monitor that includes diagnostics, remote debug support, and peek/poke.**
- **IDT/kit™ (Kernel Integration Toolkit), which provides library support and a framework for the system run-time environment.**
- **Logic analyzer and in-circuit emulator support for fast debugging and hardware/software integration.**

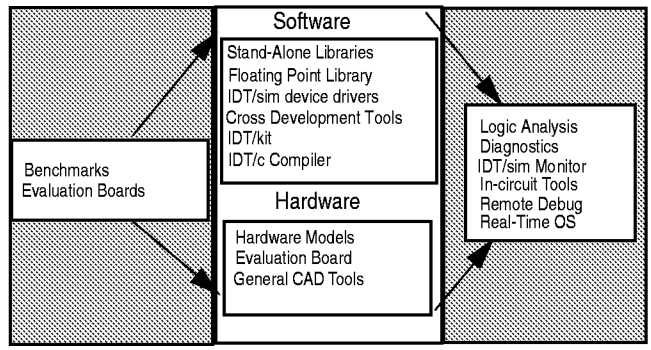


Figure 1 Development Support

Thermal Considerations

The RC36100 is now available in the QFP package, a lower cost packaging method that provides improved thermal properties for high-speed processors. The DH208 package effectively dissipates the power of the CPU and increases device reliability.

The RC36100 is guaranteed in a case temperature range of 0° to +85° C. The type of package, speed (power) of the device, and airflow conditions affect the equivalent ambient temperature conditions that will meet this specification.

The equivalent allowable ambient temperature, T_A, can be calculated using the thermal resistance from case to ambient ($\varnothing_{CA}$) of the given package. The following equation relates ambient and case temperatures (where P is the maximum power consumption at hot temperature, calculated by using the maximum I_{CC} specification for the device):

$$T_A = T_C - P * \varnothing_{CA}$$

Typical values for $\varnothing_{CA}$ at various airflows are shown in Table 1:

	∅CA					
Airflow (ft/ min)	**0**	**200**	**400**	**600**	**800**	**1000**
DH208	**17**	**9**	**7**	**5**	**4**	**3**

Table 1: Thermal Resistance (∅CA) at Various Airflows

Note: The RC36100 implements advanced power management to substantially reduce the average power dissipation of the device. This operation is described in the *IDT79RC36100 Integrated RISController Hardware User's Manual.*

Revision History

January 1996

Added 33 MHz Dhrystone data

In Figure 2, clarified directional arrows.

Reorganized AC Timing table according to Symbol parameter column

Added tsys parameter info to AC Electrical Characteristics table.

In Figure 3, ClkIn label changed to Clk.

Deleted 3.3V in DC Electrical Characteristics table.

Valid Combinations

Added 2-letter package identifier to each item.

April 1996

Signal name corrections in Logic Symbol diagram: SysALEn*, SysBurstFrame*, and SysDataRdy*.

In Package Pinout Table, Pin name changes: Pin 1 = N.C., Pin 96 = DramWrEnEven*, Pin 100 = DramWrEnOdd*,

Pin 104 = N.C., Pin 139 = LaserVideoClkIn, Pin 166 = SerialP-ClkIn*, and Pin 167 = SerialSClk*.

July 1997

In Block Diagram description, deleted Laser Printer Video Engine Interface

In Serial Communications Controller, deleted references to SDLC and HDLC application support options

Add dedicated PIO pins to Logic diagram

Delete LaserVideoData,LaserVideoClk, LaserLineSync*, and Laser-PageSync* pins from package pin-out

Delete Laser Engine Interface section of pin description table

Delete 3V DC in Electrical Characteristics table

Update 208-pin MQUAD package drawing and add reference values

Delete PQFP package references

Delete PQFP package option

December 1997

Deleted all references to JTAG and Boundary Scan

Added AC Loading diagram

Changed Tpd's

Changed Pin 144 from N.C. to ExcSint(0)

March 1998

Removed "Preliminary" label from data sheet

Adjustments to AC timing characteristics to 25 and 33 MHz

Changed CLd value to 35 pF

October 1998

Added footnote references to DC table.

January 1999

Package type, thermal characteristic description and typical thermal resistance values (∅CA).

September 1999

References to PQUAD package changed to QFP

Revised temperature values in Table 1.

Removed "Advanced Information".

Pin Description Table

The following is a list of interface, interrupt, and miscellaneous pins available on the RC36100. Pin names followed by an asterisk (*) are active when low.

Pin Name	Type	Description
System Bus Interface Pins		
SysAddr(25:0)	O	System Address Bus. Also serves as the DramAddr(13:2) Bus.
SysData(31:0)	I/O	System Data Bus.
SysClkIn	I	System Clock Input. Twice (2x) the internal CPU frequency.
SysClk*	O	System Clock Output. All other outputs are referenced to this system clock.
SysReset*	I	System Reset. Initializes entire chip, except for JTAG circuitry.
SysWait*	I	System Wait. Extends current bus transaction.
SysBusError*	I	System Bus Error. Terminates current bus transaction.
SysALEn*	I(DMA)/O	System Address Latch Enable. Indicates valid address at the beginning of a bus transaction. Input only in External DMA command phase.
SysBurstFrame*	I(DMA)/O	System Burst Frame. First indicates the beginning of a bus transaction and then indicates whether or not the bus transaction is a burst and if the next data is the last data. Input only in External DMA command phase.
SysDataRdy*	O	System Data Ready. Indicates valid data during each data of a bus transaction (except when SysWait is asserted).
SysRd*	I(DMA)/O	System Read. Indicates current bus transaction is a read. Input only in External DMA command phase.
SysWr*	I(DMA)/O	System Write. Indicates current bus transaction is a write. Input only in External DMA command phase.
DRAM Controller Pins		
DramRAS*(3:0)	O	DRAM Row Address Strobe.
DramCAS*(3:0)	O	DRAM Column Address Strobe.
DramRdEnEven*	O	DRAM Read Enable for Even FCT245/543 Type Banks. On FCT260 type banks, it is the read enable for both.
DramRdEnOdd*	O	DRAM Read Enable for Odd FCT245/543 Type Banks. On FCT260 type banks, it is the path select.
DramWrEnEven*	O	DRAM Write Enable for Even Banks.
DramWrEnOdd*	O	DRAM Write Enable for Odd Banks.

Table 2: RC36100 Pin Descriptions (Page 1 of 4)

Pin Name	Type	Description
Memory Controller Pins		
MemCS/IoCS*(7:0)	O	Memory or I/O Chip Selects. MemCS(0) and optionally MemCS(1) are reserved for the Boot PROM. IoCS(6) and/or IoCS(7) are optionally reserved for the Centronics Port if used.
MemRdEnEven*	O	Memory Read Enable for Even FCT245/543 Type Banks. On FCT260 Type banks, it is the read enable for both even and odd banks.
MemRdEnOdd*	O	Memory Read Enable for Even FCT245/543 Type Banks. On FCT260 Type Banks, it is the path select.
MemWrEn*(3:0)	I(DMA) /O	Memory Write Enable for each byte lane. Memories can directly connect their byte write enables to the RC36100 MemWrEn*(3:0) signals. During 16-bit accesses, either MemWrEn*(3:2) or MemWrEn*(1:0) are used, both pairs are equivalent. During the external DMA command phase, this signal indicates which bytes will be used in the following DMA transaction.
IoRdEn/IoDStrobe*	O	I/O Read Enable or I/O Data Strobe.
IoWrEn/IoRdWr*	O	I/O Write Enable or I/O Read/Write.
DMA Controller Pins		
DmaBusGnt*(1:0)	O	DMA Bus Grant. Indicates that the CPU has tri-stated the bus and other DMA related signals.
DmaBusReq*(1:0)	I	DMA Bus Request. Indicates that external DMA agent would like control of the bus and other DMA related signals.
DmaDone*	I	DMA Done. Indicates to the RC36100 that a burst ExtDMA read or write transaction is complete.
Serial Port Pins		
SerialPClkIn*(1:0)	I	Optional Primary Serial Clock Input.
SerialSClk*(1:0)	I/O	Optional Secondary Serial Clock Input or Output.
SerialRxData(1:0)	I	Serial Receiver Data Stream.
SerialTxData(1:0)	O	Serial Transmitter Data Stream.
SerialCTS*(1:0)	I	Serial Clear To Send.
SerialRTS*(1:0)	O	Serial Request To Send.
SerialSync*(1:0)	I/O	Serial Frame Sync.
SerialDCD*(1:0)	I	Serial Data Carrier Detect.
SerialDTR*(1:0)	O	Serial Data Terminal Ready.
Timer Pins		
TimerTC*(2:0) /TimerGate*(2:0)	I/O	Timer Terminal count output or Timer Count Gate Enable input. Terminal count asserts when Timer Count equals 0. Timer Gate enables counter to count upward or to stop.
PI0 Pins		
PI0(41:0)	I/O	Parallel Inputs or Parallel Outputs. Parallel inputs and parallel outputs are multiplexed with various peripheral inputs and peripheral outputs. If the peripheral is unused, the input or output pin can be reconfigured to be a general purpose input or output, respectively.

Table 2: RC36100 Pin Descriptions (Page 2 of 4)

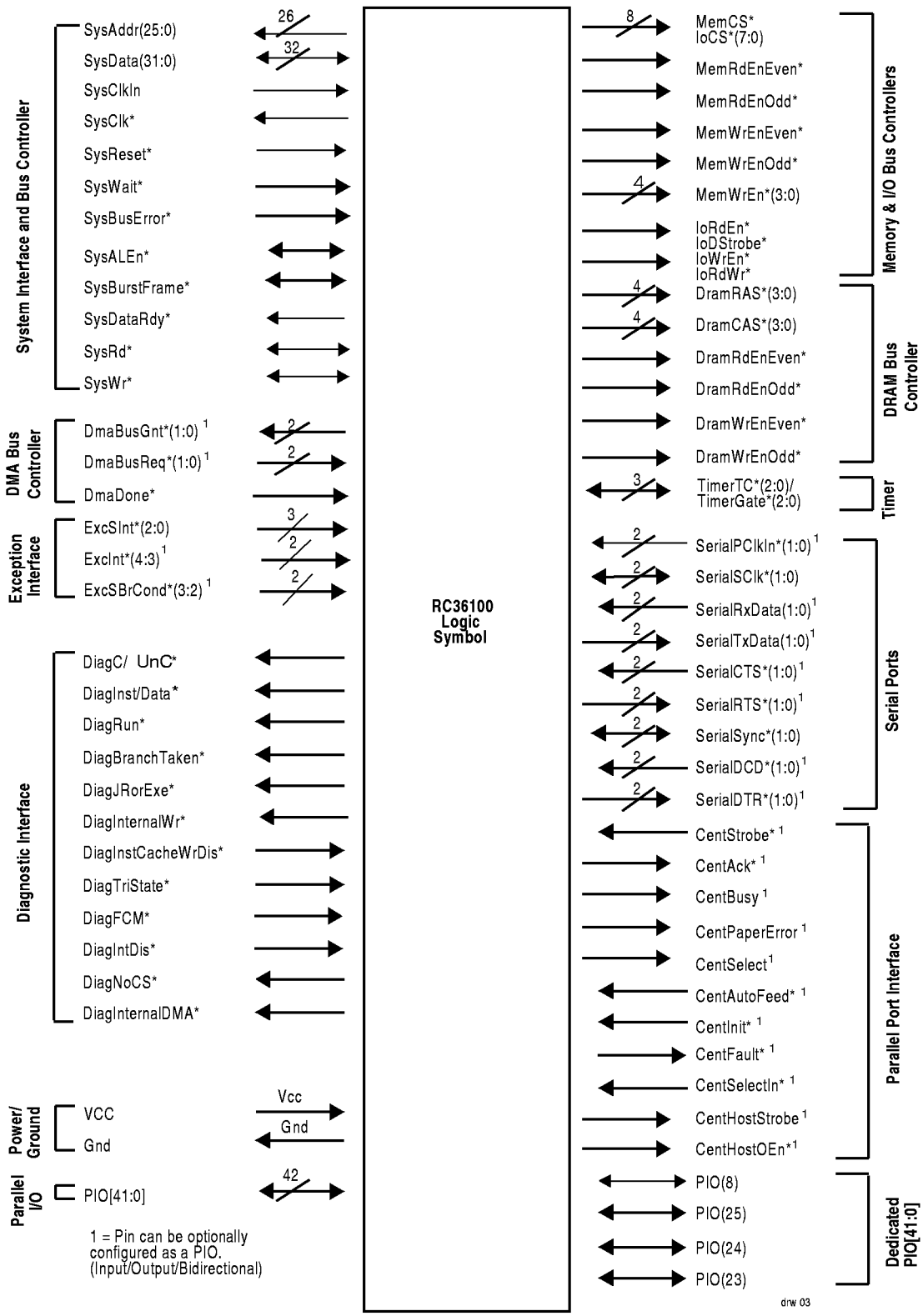
Pin Name	Type	Description
Bi-Directional Centronics Interface Pins		
CentStrobe*	I	Centronics Strobe. In compatible mode, strobes data into the printer. Has other uses for other modes.
CentAck*	O	Centronics Acknowledge. In compatible mode, acknowledges a strobe. Has other uses for other modes.
CentBusy	O	Centronics Busy. In compatible mode, delays the host from sending more data. Has other uses for other modes.
CentPaperError	O	Centronics Paper Out/Jam Error. In Compatible mode, indicates that the printer has a paper error when asserted with CentFault. Has other uses for other modes.
CentSelect	O	Centronics Select. In Compatible mode, used to indicate that this printer is on-line. Has other uses for other modes.
CentAutoFeed*	I	Centronics Auto Page Feed. In compatible mode, sends a paper feed to the printer. Has other uses for other modes.
CentInit*	I	Centronics Initialization/Reset. In Compatible mode, resets the printer. Has other uses for other modes.
CentFault*	O	Centronics Fault. In Compatible mode, indicates that the printer has a problem. Has other uses for other modes.
CentSelectIn*	I	Centronics Select In. In Compatible mode, indicates that the Host wants to select this printer on a shared cable. Has other uses for other modes
CentHostStrobe	O	Centronics Host Strobe. Used to latch Host data on the external FCT952/374 data transceiver during a Host write.
CentHostOEn*	O	Centronics Host Output Enable. Used to enable the external FCT952/374 data transceiver during a Host read.
Diagnostic Pins		
DiagC/UnC*	O	Diagnostic Cached versus Uncached. On read bus transactions, indicates whether the read is cached or uncached.
DiagInst/Data*	O	Diagnostic Instruction versus Data. On read bus transactions, indicates whether the read is for instructions or data.
DiagRun*	O	Diagnostic Run. Indicates an internal pipeline run cycle. This pin has iso-synchronous timing.
DiagBranchTaken*	O	DiagBranchTaken Indicates that a branch, jump, or exception has been taken. This pin has asynchronous timing.
DiagJRorExe*	O	Diagnostic Jump Register or Exception occurring. Indicates that a jump register or exception is executing. This pin has asynchronous timing.
DiagInternalWr*	O	Diagnostic Internal Write. Indicates that a MTCO to CP0 register $3 is occurring.
DiagInstCacheWrDis*	I	Diagnostic Cache Write Disable. Disables writes to the instruction and data cache. This pin has iso-synchronous timing and is not recommended for functional use.
DiagTriState*	I	Diagnostic Tri-State all outputs. All outputs are tri-stated including SysClk. This pin is asynchronous such that tri-stating asserts or de-asserts output enables immediately.

Table 2: RC36100 Pin Descriptions (Page 3 of 4)

Pin Name	Type	Description
DiagFCM*	I	Diagnostic Force Cache Miss. This pin has iso-synchronous timing. If used for functional board tests, it is recommended that it be (de-)asserted statically at reset time and left (de-)asserted.
DiagIntDis*	I	Diagnostic Interrupt Disable.
DiagNoCS*	O	Diagnostic No Chip Select. No internal or external chip select has occurred for the current bus transaction, therefore an external state machine should handle the bus transaction.
DiagInternalDMA*	O	Diagnostic Internal DMA. Asserts whenever any of the Internal DMA channels is generating the current bus transaction.
Exception Handling Pins		
ExcSInt*(2:0)	I	Exception Synchronized Interrupts. Also used as the reset initialization vector for 2:Boot16, 1:Boot8, and 0:BigEndian modes.
ExcInt*(4:3)	I	Exception Interrupts.
ExcSBrCond(3:2)	I	Exception Synchronized Branch Condition inputs.
Power/Ground Pins		
Vcc	I	Power pin. All power pins must be connected to 5V.
Gnd	I	Ground pin (VSS). All ground pins must be connected to 0V.

Table 2: RC36100 Pin Descriptions (Page 4 of 4)

Logic Diagram — RC36100



AC Timing Characteristics — RC36100

(Tc=0°C to +85°C, Vcc = +5V±5%)

Signal	Symbol	Reference Clock Edge	20 MHz		25 MHz		33 MHz		Unit
			Min	Max	Min	Max	Min	Max	
System Bus Interface									
SysData(31:0), SysRd*, SysWr*, SysALEn*, SysBurstFrame*, SysDataRdy*	Tpd	Sysclk rising	—	20	—	15	—	14	ns
SysData(31:0), SysRd*, SysWr*, SysALEn*, SysBurstFrame*, SysBusError	Tsetup	Sysclk rising	14	—	11	—	9	—	ns
SysWait*	Tsetup	Sysclk rising	21		17		13		ns
SysWait*	Thold	Sysclk rising	0	—	0	—	0	—	ns
SysData(31:0), SysRd*, SysWr*, SysALEn*, SysBurstFrame*, SysBusError*	Thold	Sysclk rising	0	—	0	—	0	—	ns
SysAddr(25:0)	Tpdaddr	Sysclk rising	—	13	—	12	—	11	ns
DRAM Controller									
DramRAS(3:0)*, DramRdEnEven* DramRdEnOdd*, DramWrEnEven*, DramWrEnOdd*	Tpd	Sysclk rising	—	20	—	15	—	13	ns
DramCAS(3:0)*	Tpd	Sysclk rising or falling	—	20	—	15	—	13	ns
Memory Controller									
MemCS/IoCS(7:0)*, MemRdEnEven*, MemRdEnOdd*, MemWrEnEven*, MemWrEOdd*, MemWrEn*, IoRdEn/Dstrobe*, IoWrEn/RdWr*	Tpd	Sysclk rising	—	20	—	15	—	13	ns
DMA Controller									
DmaBusGnt*	Tpd	Sysclk rising	—	20	—	15	—	13	ns
DmaBusReq(1:0)*, DmaDone*	Tsetup	Sysclk falling	14	—	11	—	9	—	ns
DmaBusReq(1:0)*, DmaDone*	Thold	Sysclk falling	0	—	0	—	0	—	ns
Serial Port									
SerialSClk(1:0)*, SerialSync(1:0)*, SerialTxData(1:0), SerialRTS(1:0), SerialDTR(1:0)	Tpdsio	Sysclk rising	—	24	—	19	—	16	ns
SerialPClkIn(1:0)*,SerialRxData(1:0),SerialDCD(1:0), SerialCTS(1:0)*, SerialSClk(1:0)*, SerialSync(1:0)*	Tsetup	Sysclk rising	14	—	11	—	9	—	ns
SerialPClkIn(1:0)*,SerialRxData(1:0),SerialDCD(1:0), SerialCTS(1:0)*, SerialSClk(1:0)*, SerialSync(1:0)*	Thold	Sysclk rising	0	—	0	—	0	—	ns
Timer									
TimerTC(2:0)/TimerGate(2:0)	Tpd	Sysclk falling	—	20	—	15	—	13	ns
TimerTC(2:0)/TimerGate(2:0)	Tsetup	Sysclk falling	14	—	11	—	9	—	ns
TimerTC(2:0)/TimerGate(2:0)	Thold	Sysclk falling	0	—	0	—	0	—	ns

Signal	Symbol	Reference Clock Edge	20 MHz		25 MHz		33 MHz		Unit
			Min	Max	Min	Max	Min	Max	
PIO									
PIO(41:0)	Tpd	SysClk falling	—	20	—	15	—	13	ns
PIO(41:0)	Tsetup	SysClk falling	14	—	11	—	9	—	ns
PIO(41:0)	Thold	SysClk falling	0	—	0	--	0	--	ns
Bidirectional Centronics Interface									
CentAck*, CentBust,CentPaperError,CentSelect,CentFault,CentHostStrobe,CentHostOEn*	Tpd	Sysclk falling	—	20	—	15	—	13	ns
CentStrobe*, CentAutoFeed*,CentInit*, CentSelectIn*	Tsetup	Sysclk falling	14	—	11	—	9	—	ns
CentStrobe*, CentAutoFeed*,CentInit*, CentSelectIn*	Thold	Sysclk falling	0	—	0	—	0	—	ns
Exception Handling									
ExcSInt(2:0)*, ExcInt(4:3)*, ExcSBrCond(3:2)	Tsetup	Sysclk falling	14	—	11	—	9	--	ns
ExcSInt(2:0)*, ExcInt(4:3)*, ExcSBrCond(3:2)	Thold	Sysclk falling	0	—	0	—	0	--	ns

AC Electrical Characteristics — RC36100

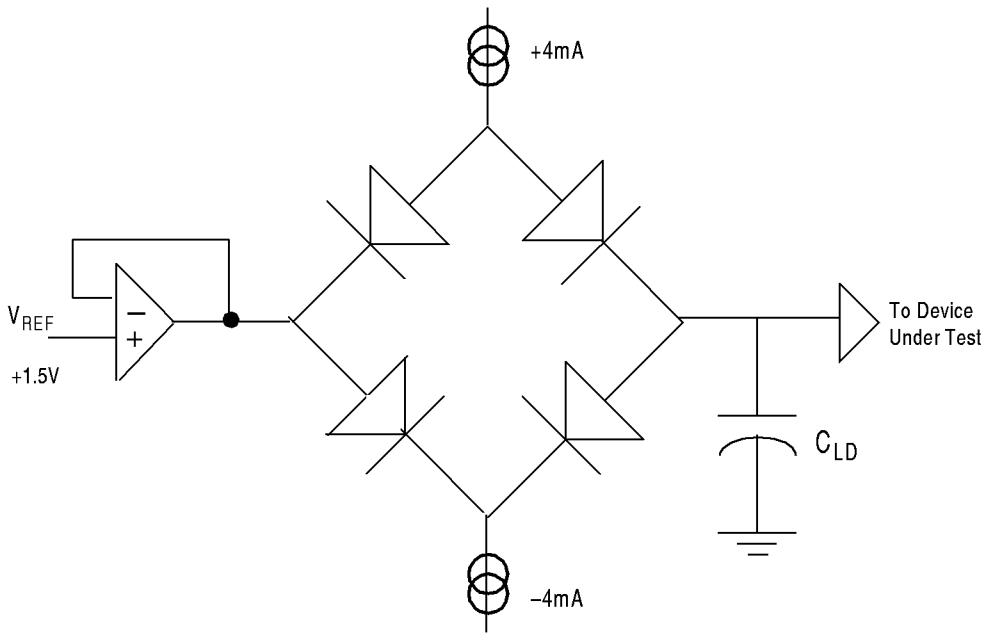
(Tc=0°C to +85°C, Vcc = +5V±5%)

Symbol	Signal	Description	20 MHz		25 MHz		33 MHz		Unit
			Min	Max	Min	Max	Min	Max	
tclkh	clkIn	Pulse Width High	10	—	8	—	6.5	—	ns
tclkl	clkIn	Pulse Width Low	10	—	8		6.5	—	ns
tClk	clkIn	Clock Period	25	250	20	250	15	250	ns
tcold	Reset	Pulse Width From Vcc Valid	200	—	200	—	200	—	µs
twarm	Reset	Minimum Pulse Width	32	—	32	—	32	—	Sys
tsysh	SysClk	Clock High Time	tClk-2	tClk+2	tClk-2	tClk+2	tClk-2	tClkh + 2	ns
tsysl	SysClk	Clock Low Time	tClk-2	tClk+2	tClk-2	tClk+2	tClk-2	tClkl+ 2	ns
tsys	SysClk	System Clock Period	2*tClk	2*tClk	tClk-2	tClk+2	tClk-2	tClk+ 2	ns

Notes to AC Characteristics:

1. AC characteristics are only measured and valid on non-idle cycles, as referred to in the *IDT79RC36100 Integrated RISController Hardware User's Manual*.
2. For timing diagrams of the ClkIn, Reset, and SysClk signals, see Figure 2 through Figure 5 on the following page.

Output Loading For AC Testing



Signal	Cld
All Signals	35 pF

Timing Diagrams for ClkIn, Reset, and SysClk Signals — RC36100

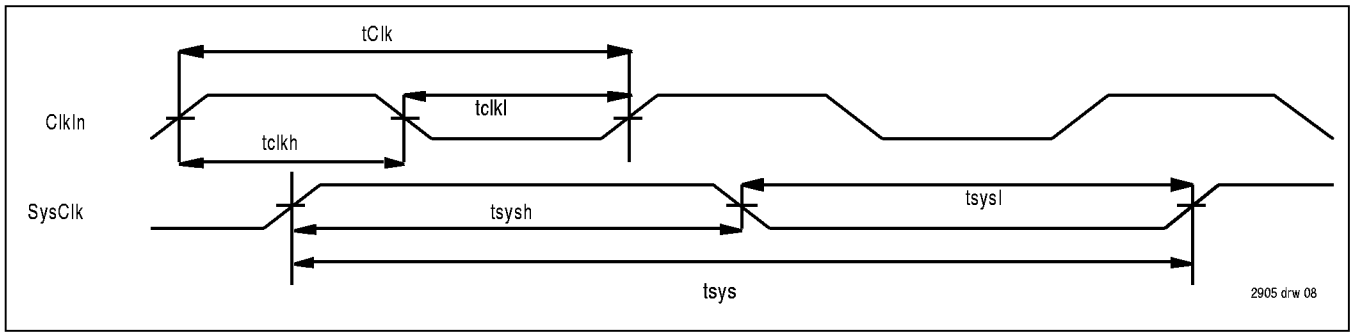


Figure 2 Clocking Sequence

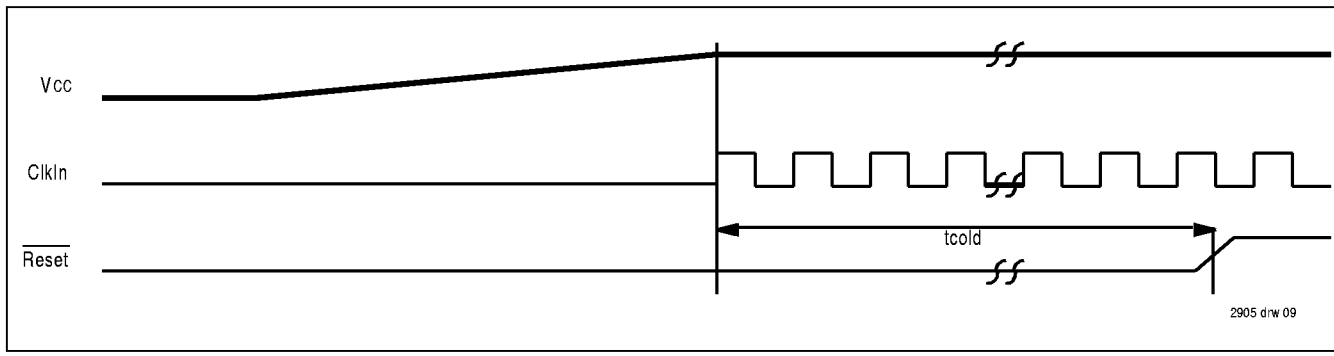


Figure 3 Power-On Reset Sequence

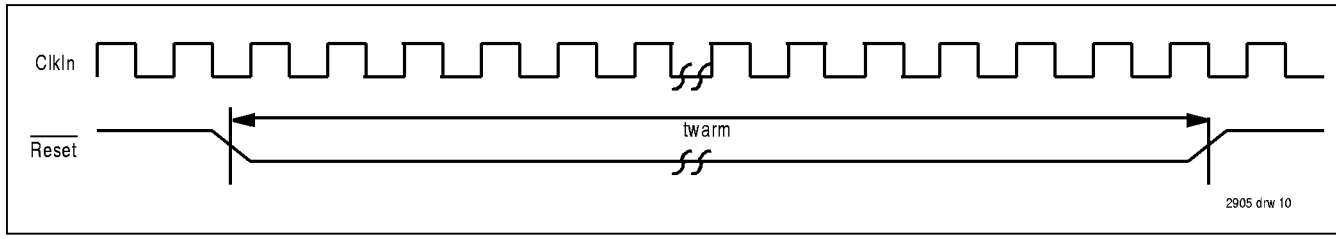


Figure 4 Warm Reset Sequence

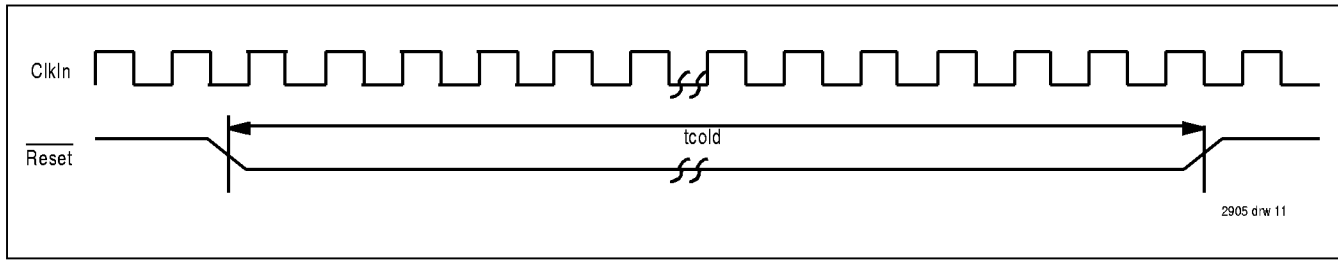


Figure 5 Warm Reset Sequence (Internal Pull-Ups Used)

DC Electrical Characteristics — RC36100

(Tc=0°C to +85°C, Vcc = +5.0V±5%)

Symbol	Parameter	Test Conditions	20 MHz		25 MHz		33 MHz		Unit
			Min	Max	Min	Max	Min	Max	
V_{OH}	Output HIGH Voltage	V_{cc} = Min., I_{OH} = –4mA	3.5	—	3.5	—	3.5	—	V
V_{OL}	Output LOW Voltage	V_{cc} = Min., I_{OL} = 4mA	—	0.4	—	0.4	—	0.4	V
V_{IH}	Input HIGH Voltage(3)	—	2.0	—	2.0	—	2.0	—	V
V_{IL}	Input LOW Voltage(1)	—	—	0.8	—	0.8	—	0.8	V
V_{IHS}	Input HIGH Voltage(2,3)	—	3.0	—	3.0	—	3.0	—	V
V_{ILS}	Input LOW Voltage(1,2)	—	—	0.4	—	0.4	—	0.4	V
C_{IN}	Input Capacitance(4)	—	—	10	—	10	—	10	pF
C_{OUT}	Output Capacitance(4)	—	—	10	—	10	—	10	pF
I_{CC}	Operating Current	V_{cc} = 5V, TC = 25°C	—	400	—	500	—	600	mA
I_{IH}	Input HIGH Leakage	V_{IH} = VCC	—	100	—	100	—	100	mA
I_{IL}	Input LOW Leakage	V_{IL} = GND	-100	—	-100	—	-100	—	mA
I_{OZ}	Output Tri-state Leakage	V_{OH} = 2.4V, V_{OL} = 0.5V	-100	100	-100	100	-100	100	mA
P_{max}	Max Power Dissipation	Calculated from V_{cc} of 5.0V and I_{cc} max		2.0		2.5		3.0	W

Notes to table:

1. V_{IL} Minimum = -3.0V for pulse width less than 15ns. V_{IL} should not fall below -0.5 volts for larger periods.
2. V_{IHS} and V_{IL} apply to ClkIn and Reset*.
3. V_{IH} should not be held above V_{cc} + 0.5 Volts.
4. Guaranteed by design.

Package Pin-Out — RC36100

Pin	Function	Pin	Function	Pin	Function	Pin	Function
1	N.C.	53	N.C	105	N.C.	157	SerialTxData(0)
2	SysAddr(0)	54	SysData(0)	106	DramRAS*(2)	158	SerialCTS*(0)
3	SysAddr(1)	55	SysData(1)	107	DramRAS*(3)	159	SerialRTS*(0)
4	DiagC_UnC*	56	SysData(2)	108	DramCAS*(0)	160	SerialSClk*(0)
5	SysAddr(2)	57	SysData(3)	109	DramCAS*(1)	161	SerialSycn*(0)
6	Vcc	58	Vcc	110	Vcc	162	Vcc
7	Vss	59	Vss	111	Vss	163	Vss
8	SysAddr(3)	60	SysData(4)	112	DramCAS*(2)	164	SerialDTR*(0)
9	SysAddr(4)	61	SysData(5)	113	DramCAS*(3)	165	SerialDCD*(0)
10	DiagRun*	62	SysData(6)	114	DramRdEnEven*	166	SerialPClkIn*(1)
11	DiagBranchTaken*	63	SysData(7)	115	DramRdEnOdd_Tr*	167	SerialSClk*(1)
12	DiagJRorExe*	64	SysData(8)	116	MemCS*_loCS*(0)	168	SerialSync*(1)

Table 3: Package Pin-Out RC36100 (Page 1 of 3)

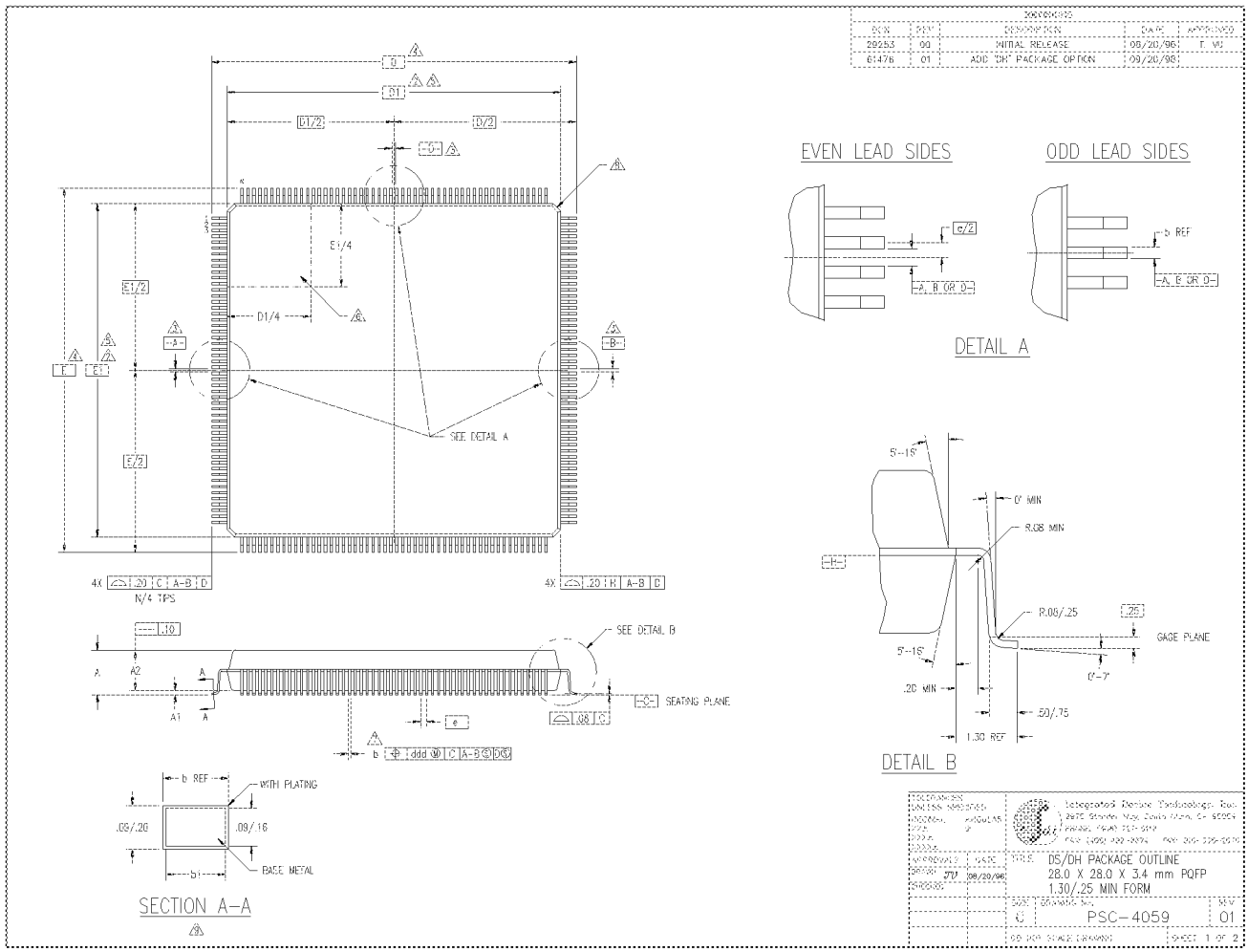
Pin	Function	Pin	Function	Pin	Function	Pin	Function
13	DiagInternalWr*	65	SysData(9)	117	MemCS*_loCS*(1)	169	SerialRxData(1)
14	SysAddr(5)	66	SysData(10)	118	MemCS*_loCS*(2)	170	SerialTxData(1)
15	SysAddr(6)	67	SysData(11)	119	MemCS*_loCS*(3)	171	SerialCTS*(1)
16	Vcc	68	Vcc	120	Vcc	172	Vcc
17	Vss	69	Vss	121	Vss	173	Vss
18	SysAddr(7)	70	SysData(12)	122	MemCS*_loCS*(4)	174	SerialRTS*(1)
19	SysAddr(8)	71	SysData(13)	123	MemCS*_loCS*(5)	175	SerialDCD*(1)
20	DiagInstCacheWrDis*	72	SysData(14)	124	MemCS*_loCS*(6)	176	SerialDTR*(1)
21	DiagTriState*	73	SysData(15)	125	MemCS*_loCS*(7)	177	TimerTC*(0)
22	DiagFCM*	74	SysData(16)	126	MemRdEnEven*	178	TimerTC*(1)
23	DiagIntDis*	75	SysData(17)	127	MemRdEnOdd*	179	TimerTC*(2)
24	SysAddr(9)	76	SysData(18)	128	MemWrEn*(0)	180	CentStrobe*
25	SysAddr(10)	77	SysData(19)	129	MemWrEn*(1)	181	CentAck*
26	Vcc	78	Vcc	130	Vcc	182	Vcc
27	Vss	79	Vss	131	Vss	183	Vss
28	SysAddr(11)	80	SysData(20)	132	MemWrEn*(2)	184	CentBusy
29	SysAddr(12)	81	SysData(21)	133	MemWrEn*(3)	185	CentPaperError
30	DiagNoCS*	82	SysData(22)	134	loRdEn*_DStrobe*	186	CentSelect
31	Diaginst_Data*	83	SysData(23)	135	loWrEn*_RdWr*	187	CentAutoFeed*
32	SysAddr(13)	84	SysData(24)	136	Vcc	188	CetInit*
33	SysAddr(14)	85	SysData(25)	137	Vss	189	CentFault*
34	SysAddr(15)	86	SysData(26)	138	PIO(8)	190	CentSelectIn*
35	SysAddr(16)	87	SysData(27)	139	PIO(26)	191	CentHostStrobe
36	Vcc	88	Vcc	140	Vcc	192	Vcc
37	Vss	89	Vss	141	Vss	193	Vss
38	SysAddr(17)	90	SysData(28)	142	PIO(25)	194	CentHostOEn*
39	SysAddr(18)	91	SysData(29)	143	PIO(24)	195	DmaBusGnt*(0)
40	SysAddr(19)	92	SysData(30)	144	ExcSint*(0)	196	DmaBusGnt*(1)
41	SysAddr(20)	93	SysData(31)	145	ExcSint*(1)	197	DmaBusReq*(0)
42	SysAddr(21)	94	SysClkIn	146	ExcSint*(2)	198	DmaBusReq*(1)
43	SysAddr(22)	95	SysReset*	147	ExcInt*(3)	199	DmaDone*
44	SysAddr(23)	96	DramWrEnEven*	148	ExcInt*(4)	200	SysAlEn*
45	SysAddr(24)	97	N.C.	149	DiagIntDma*	201	SysDataRdy*
46	Vcc	98	Vcc	150	Vcc	202	Vcc
47	Vss	99	Vss	151	Vss	203	Vss

Table 3: Package Pin-Out RC36100 (Page 2 of 3)

Pin	Function	Pin	Function	Pin	Function	Pin	Function
48	SysAddr(25)	100	DramWrEnOdd*	152	SysWait*	204	SysRd*
49	Vcc	101	N.C.	153	SysBus Error*	205	SysWr*
50	Vss	102	DramRAS*(0)	154	SysClk*	206	SysBurstFrame*
51	Vcc	103	DramRAS*(1)	155	Serial ClkIn*(0)	207	ExcSBrCond(2)
52	Vcc	104	N.C.	156	SerialRXData(0)	208	ExcSBrCond(3)

Table 3: Package Pin-Out RC36100 (Page 3 of 3)

Package Drawing — 208-pin QFP

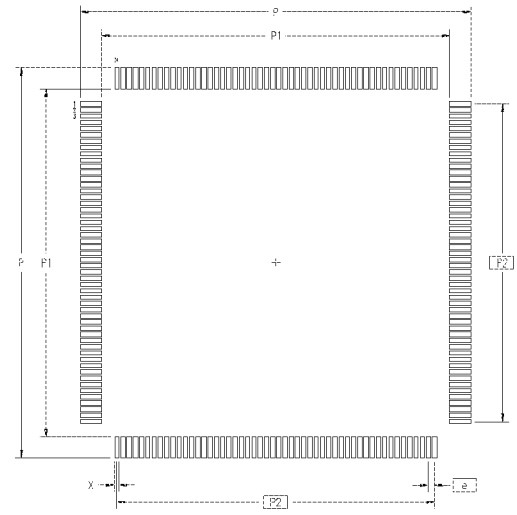


208-Pin Package Drawing — Page Two

DOCUMENT CONTROL				
ECN	REV	DESCRIPTION	DATE	APPROVED
29253	00	INITIAL RELEASE	08/20/98	T. VU
51476	01	ADD "DH" PACKAGE OPTION	05/20/99	

SYMBOL	JEDEC VARIATION FA-1 MIN	NOM	MAX	NOTE
A	--	--	4.10	
A1	.25	--	--	
A2	3.20	3.40	3.60	
D		30.60 BSC		4
D1		28.00 BSC		5,2
E		30.60 BSC		4
E1		28.00 BSC		5,2
N		208		
e		.50 BSC		
b	.17	--	.27	7
b1	.17	.20	.23	
ddd	--	--	.08	

LAND PATTERN DIMENSIONS



	MIN	MAX
P	31.20	31.40
P1	27.80	28.00
P2	25.50 BSC	
X	.30	.40
e	.50 BSC	
N	208	

NOTES:

1. ALL DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5M--1994
2. TOP PACKAGE MAY BE SMALLER THAN BOTTOM PACKAGE BY .15 mm
3. DATUMS -A-B- AND -D- TO BE DETERMINED AT DATUM PLANE -H-
4. DIMENSIONS D AND E ARE TO BE DETERMINED AT SEATING PLANE -C-
5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION IS .25 mm PER SIDE. D1 AND E1 ARE BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH
6. DETAIL OF PIN 1 IDENTIFIER IS OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED
7. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION IS .08 mm IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT.
8. EXACT SHAPE OF EACH CORNER IS OPTIONAL
9. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN .10 AND .25 mm FROM THE LEAD TIP
10. ALL DIMENSIONS ARE IN MILLIMETERS
11. THIS OUTLINE CONFORMS TO JEDEC PUBLICATION 95 REGISTRATION MO-143, VARIATION FA-1

UNLESS SPECIFIED: DECIMAL ANGULAR XXX ± XXXX ± — MATERIAL — FINISH —

Integrated Device Technology, Inc. 2975 Stender Way, Santa Clara, CA 95054 PHONE: (408) 727-6116 FAX: (408) 492-8674 TWX: 910-338-0018

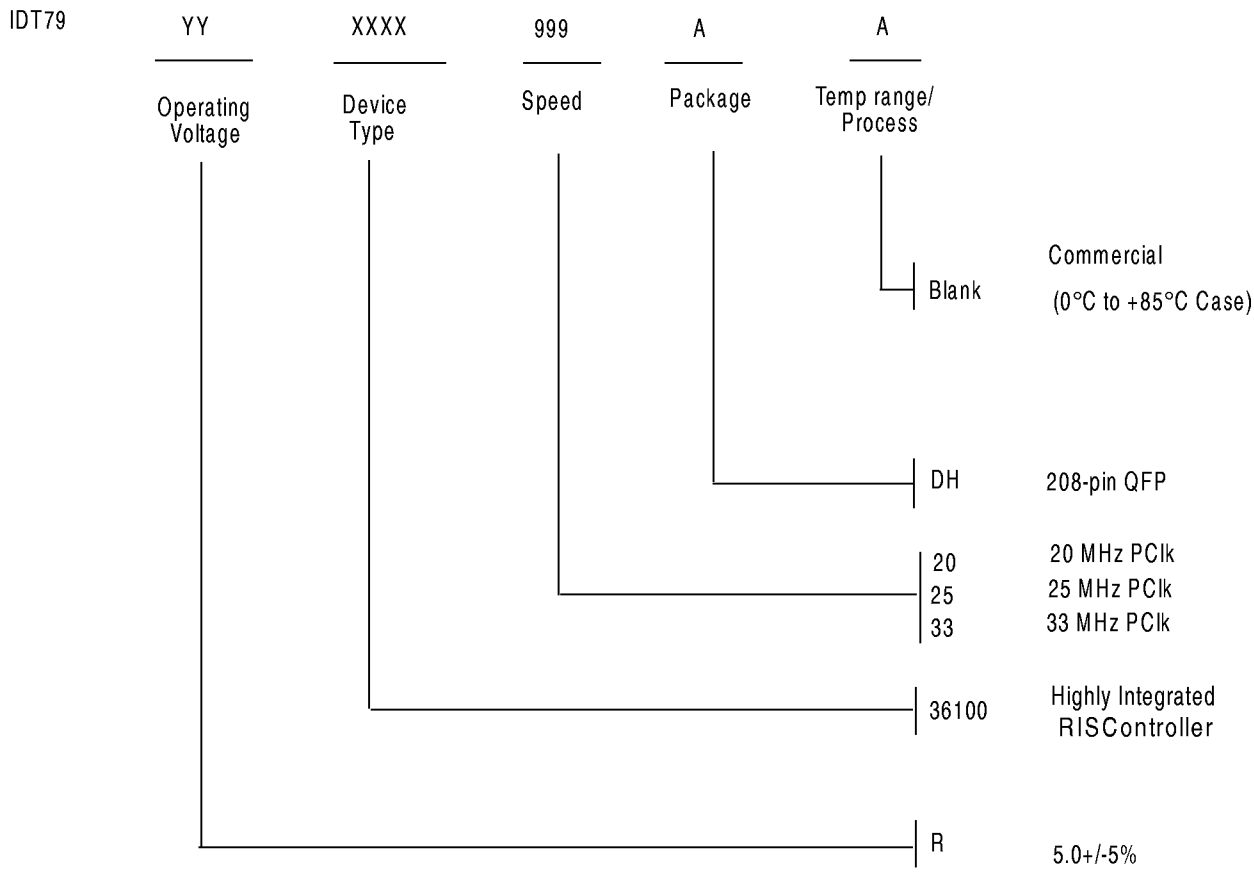
APPROVALS: DRAWN JTV 08/20/98 — CHECKED —

TITLE: DS/DH PACKAGE OUTLINE 28.0 X 28.0 X 3.4 mm PQFP 1.30/.25 MIN FORM

SIZE: D — DRAWING NO.: PSC-4059 — REV: 01

DO NOT SCALE DRAWING — SHEET 2 OF 2

Ordering Information



Valid Combinations

IDT79RC36100 - 20, 25, 33MHz DH 208-pin QFP package, Commercial Temperature

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