Dual P-Channel 20-V (D-S) MOSFET

CHARACTERISTICS

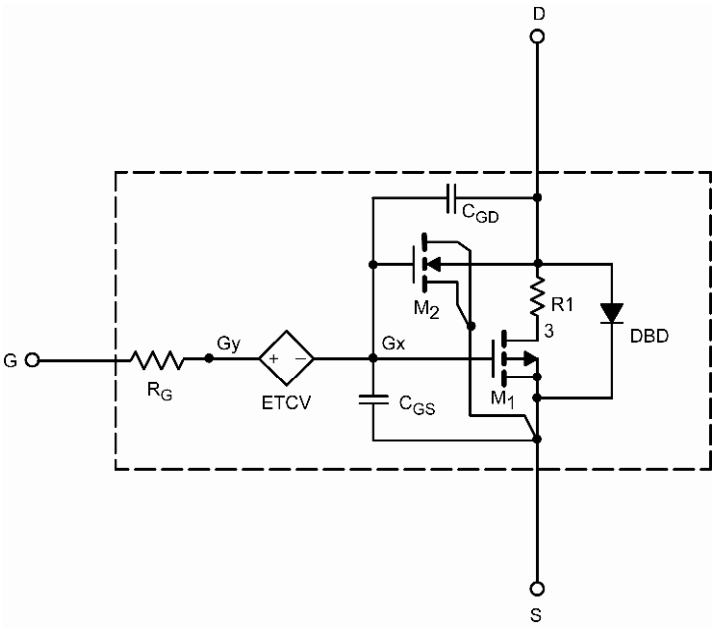
- P-Channel Vertical DMOS
- Macro Model (Subcircuit Model)
- Level 3 MOS
- Apply for both Linear and Switching Application
- Accurate over the −55 to 125°C Temperature Range
- Model the Gate Charge, Transient, and Diode Reverse Recovery Characteristics

DESCRIPTION

The attached spice model describes the typical electrical characteristics of the p-channel vertical DMOS. The subcircuit model is extracted and optimized over the −55 to 125°C temperature ranges under the pulsed 0-V to 5-V gate drive. The saturated output impedance is best fit at the gate bias near the threshold voltage.

A novel gate-to-drain feedback capacitance network is used to model the gate charge characteristics while avoiding convergence difficulties of the switched C_{gd} model. All model parameter values are optimized to provide a best fit to the measured electrical data and are not intended as an exact physical interpretation of the device.

SUBCIRCUIT MODEL SCHEMATIC

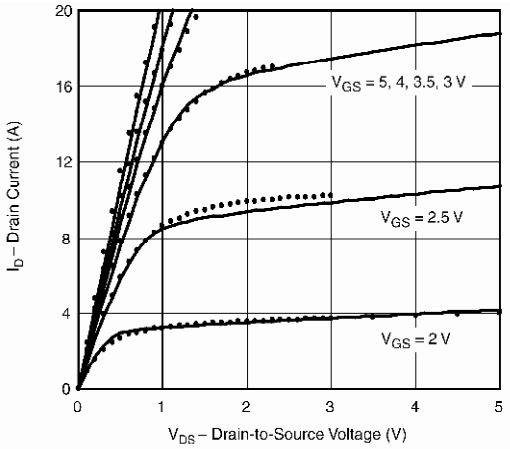


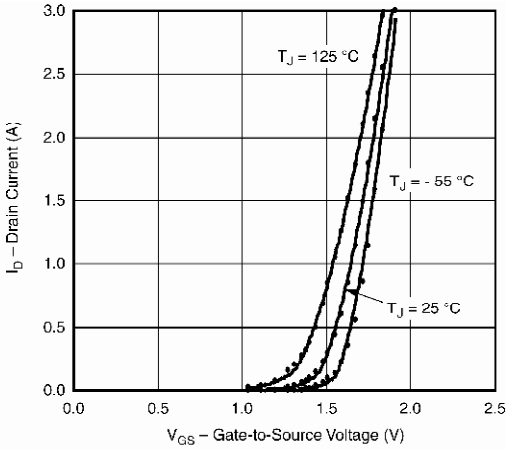
This document is intended as a SPICE modeling guideline and does not constitute a commercial product data sheet. Designers should refer to the appropriate data sheet of the same number for guaranteed specification limits.

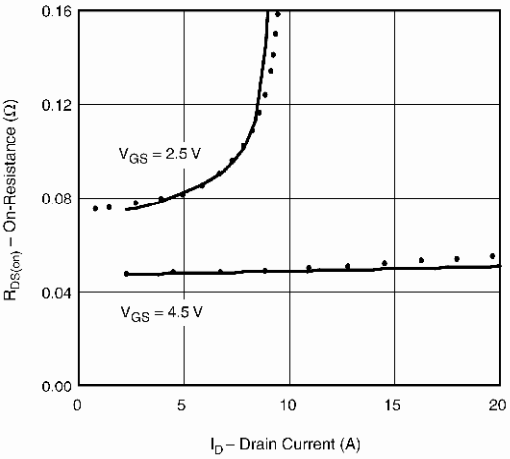
SPECIFICATIONS (T_J = 25°C UNLESS OTHERWISE NOTED)					
Parameter	**Symbol**	**Test Condition**	**Simulated Data**	**Measured Data**	**Unit**
Static					
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = -250\ \mu A$	0.89		V
Drain-Source On-State Resistance[a]	$r_{DS(on)}$	$V_{GS} = -4.5$ V, $I_D = -4.8$ A	0.048	0.048	Ω
		$V_{GS} = -2.5$ V, $I_D = -1$ A	0.072	0.075	
Forward Transconductance[a]	g_{fs}	$V_{DS} = -10$ V, $I_D = -4.8$ A	12	11	S
Diode Forward Voltage	V_{SD}	$I_S = -3.8$ A	−0.84	−0.77	V
Dynamic[b]					
Input Capacitance	C_{iss}	$V_{DS} = -10$ V, $V_{GS} = 0$ V, f = 1 MHz	662	665	pF
Output Capacitance	C_{oss}		140	140	
Reverse Transfer Capacitance	C_{rss}		113	115	
Total Gate Charge	Q_g	$V_{DS} = -10$ V, $V_{GS} = -10$ V, $I_D = -4.8$ A	14	17	nC
		$V_{DS} = -10$ V, $V_{GS} = -4.5$ V, $I_D = -4.8$ A	7	8	
Gate-Source Charge	Q_{gs}		2	2	
Gate-Drain Charge	Q_{gd}		3	3	

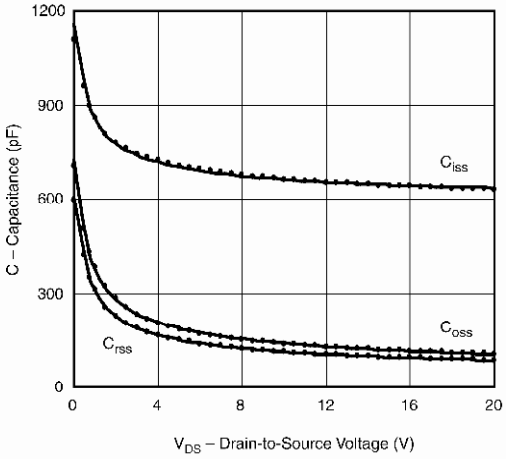
Notes
a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%.
b. Guaranteed by design, not subject to production testing.

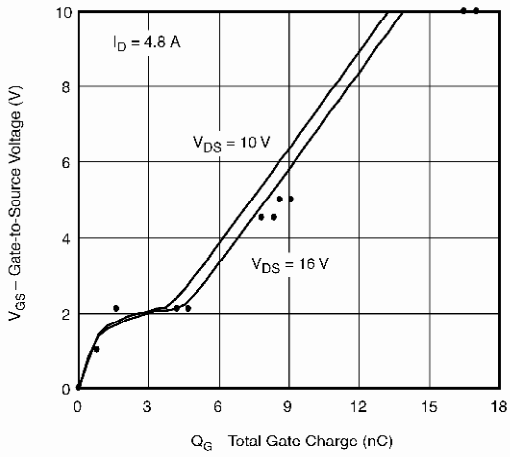
COMPARISON OF MODEL WITH MEASURED DATA (T_J=25°C UNLESS OTHERWISE NOTED)

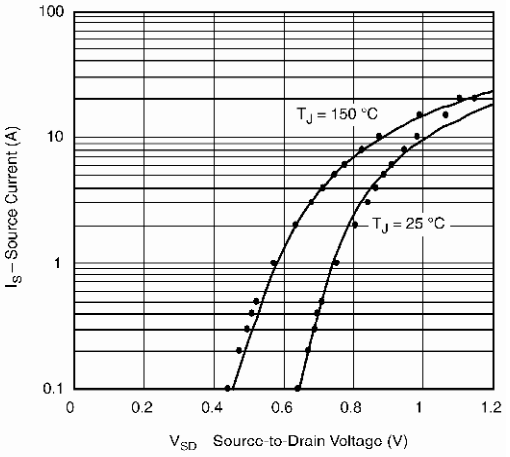






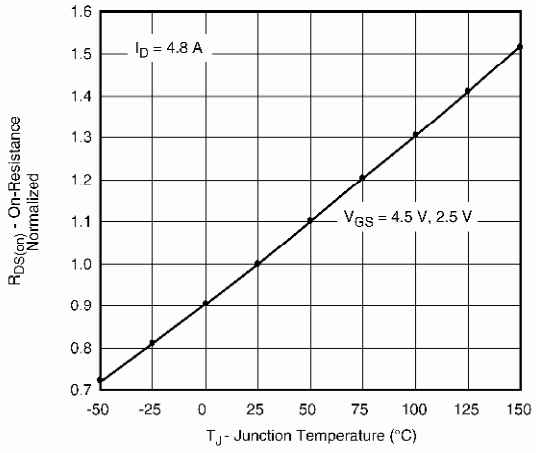


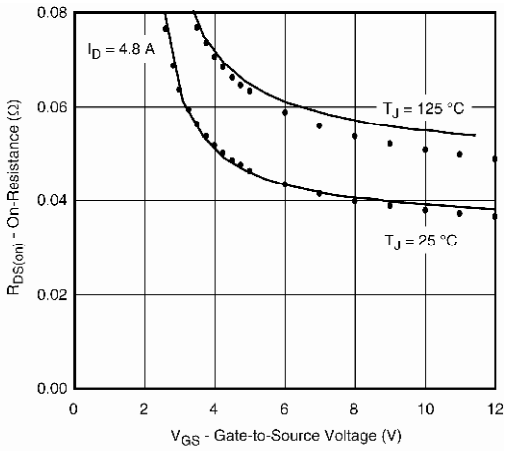




Note: Dots and squares represent measured data.

COMPARISON OF MODEL WITH MEASURED DATA (TJ=25°C UNLESS OTHERWISE NOTED)





Note: Dots and squares represent measured data.

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