CLEAR LOGIC

# CL7256A
# CL7256AE

**Link Processed Logic Device Family**

## Key Features

- Patented High Fidelity Conversion Technology
- Link Processed Logic Device (LPLD®) technology offers the ultimate combination of performance, flexibility, and low cost
- Functionally, architecturally, and electrically compatible with industry-standard Altera® MAX® 7000
- High Density
  - 5,000 Usable gates
  - 256 Macrocells
  - 164 Maximum user I/O pins
- Metal Link technology provides very fast, dense interconnect routing
- Low current consumption
- Supports 3.3 volt operation
- Alpha particle immune

## CL7000 Product Family Overview

| Feature | CL7128A<br>CL7128AE | CL7256A<br>CL7256AE | CL7512AE |
|---|---|---|---|
| Useable Gates | 2,500 | 5,000 | 10,000 |
| Macrocells | 128 | 256 | 512 |
| Logic array Blocks | 8 | 16 | 32 |
| Max user I/O pins | 100 | 164 | 212 |
| Speed Grades | -4, -5, -6, -7, -10, -12 | -4, -5, -6, -7, -10, -12 | -6, -7, -10, -12 |
| Packages | 84-Pin PLCC<br>100-Pin TQFP<br>100-Pin BGA<br>144-Pin TQFP | 100-Pin TQFP<br>100-Pin BGA<br>144-Pin TQFP<br>208-Pin PQFP<br>256-Pin BGA | 144-Pin TQFP<br>208-Pin PQFP<br>256-Pin BGA<br>256-Pin FBGA |

7KA tbl 01A

## Description

The Clear Logic CL7000 Laser Processed Logic Device (LPLD®) family offers the ultimate combination of performance, flexibility, and cost. This family is a system level second source to Altera MAX® 7000A products. For designs not requiring in-system reprogrammability, design verification can be performed using the programmable Altera devices, and Clear Logic LPLDs can be used for low cost, high volume production.

Clear Logic's innovative laser-based technology eliminates NRE costs, test vector development, ordering minimums and long lead times. No re-simulation or re-layout is required, as the device uses a cell-based, PLD-like architecture. Clear Logic's NoFault® technology ensures complete test coverage through the use of specialized testing modes which are transparent to the user.

The Clear Logic CL7000 Laser Processed Logic Device family is based upon a large array of macrocells. Each macrocell contains a logic array with five product terms, a product-term select matrix, and a configurable register. A group of sixteen macrocells forms a block. Laser-configured metal fuses implement logical functions and control signal routing.

Laser configuration provides reduced cost and enhanced performance. These inherent performance benefits include extremely consistent propagation delays, reduced power consumption, and improved immunity to noise and upset events.

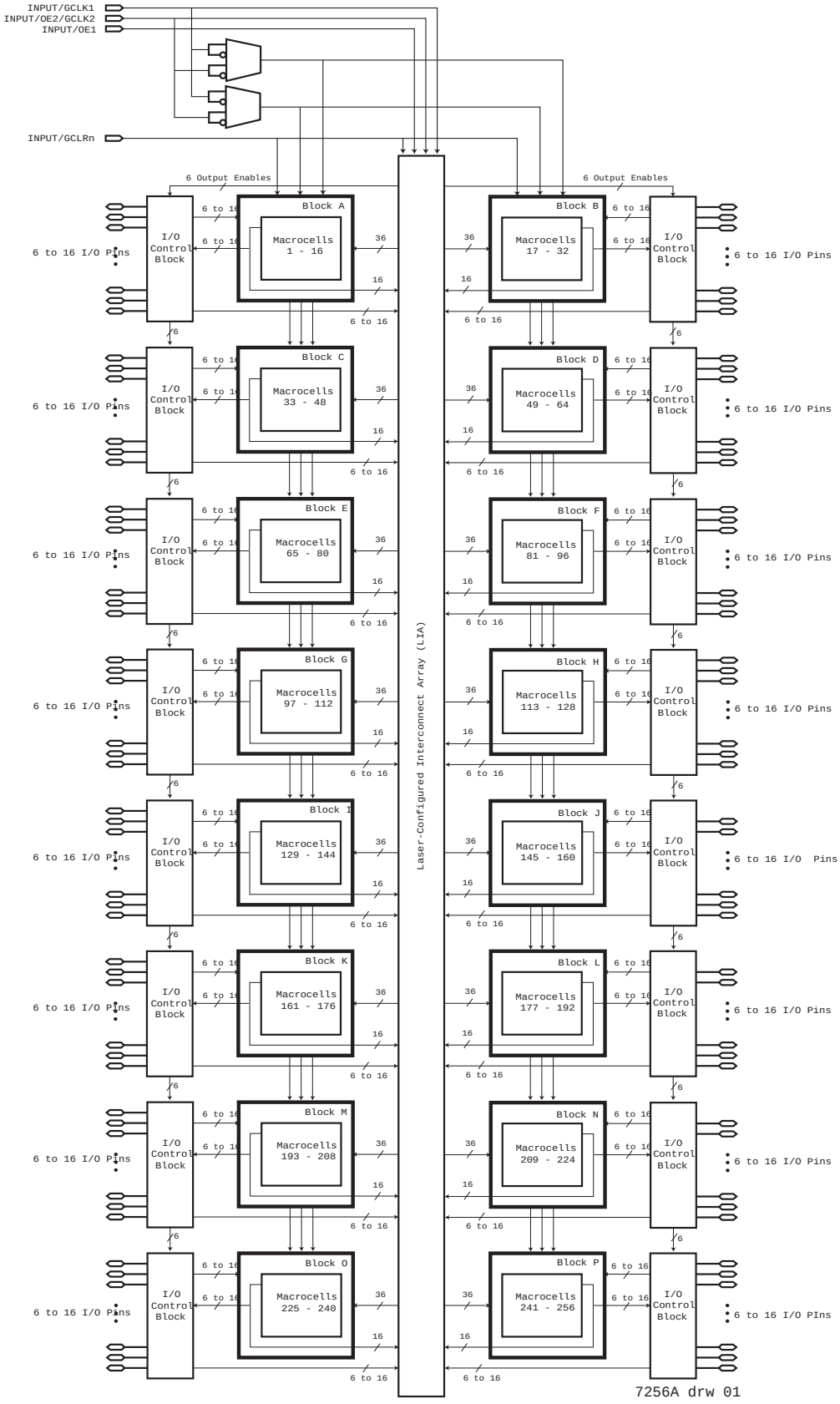
## Additional Information

For further information on designing with the CL7000 LPLD family, please consult the following documents:

- AN-01: Requesting a First Article. This document provides instructions on how to submit a bitstream file for generation of first articles.
- AN-02: Clear Logic Packaging Guide. This document provides specifications and drawings for packages used by the CL7000 family.
- AN-09: CL7000 Technology White Paper. This document outlines the technologies employed by the CL7000 LPLD family.
- AN-10: Calculating CL7000 Power Consumption. This document provides guidelines for calculating power consumption based on design characteristics.
- AN-11: CL7000 Test Methodology. This document describes how Clear Logic provides 100% stuck-at fault coverage.

- AN-12: CL7000 LPLD Timing and Function Compatibility. This document shows how a seamless conversion from CPLD to ASIC can be achieve with no additional engineering with Clear Logic.

# Block Diagram



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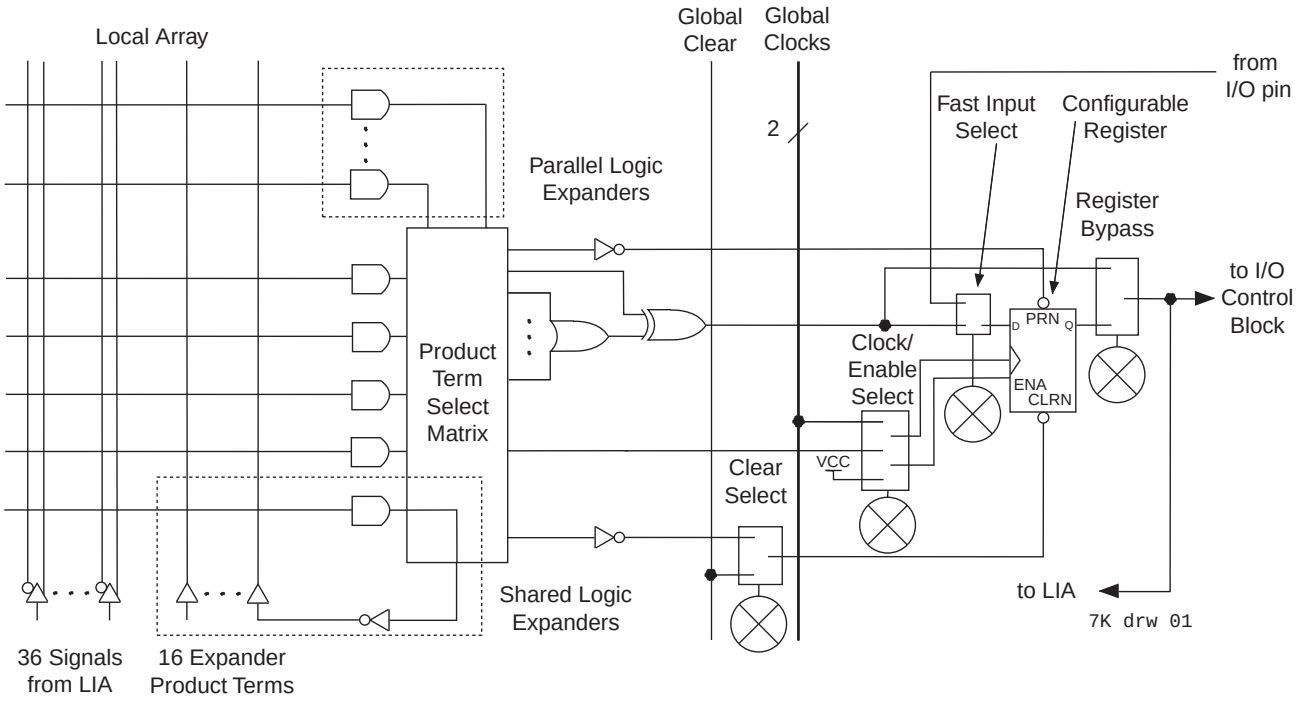
## Macrocell Diagram



## Pin Configuration

| Pin Name | 100 pin TQFP | 100 pin FBGA | 144 pin TQFP | 208 pin PQFP | 256 pin FBGA |
|---|---|---|---|---|---|
| INPUT/GCLK1 | 87 | A6 | 125 | 184 | D9 |
| INPUT/GCLRn | 89 | B5 | 127 | 182 | E8 |
| INPUT/OE1 | 88 | B6 | 126 | 183 | E9 |
| INPUT/OE2/GCLK2 | 90 | A5 | 128 | 181 | D8 |
| TDI | 4 | A1 | 4 | 176 | D4 |
| TMS | 15 | F3 | 20 | 127 | J6 |
| TCK | 62 | F8 | 89 | 30 | J11 |
| TDO | 73 | A10 | 104 | 189 | D13 |
| GNDINT | 38, 86 | D6, G5 | 52, 57, 124, 129 | 75, 82, 180, 185 | A8, C9, G9, K8, P9 |
| GND | 11, 26, 43, 59, 74, 95 | C3, D7, E5, F6, G4, H8 | 3, 13, 17, 33, 59, 64, 85, 105, 135 | 14, 32, 50, 72, 94, 116, 134, 152, 174, 200 | A3, B10, C2, D14, F6, G10, H8, J9, K7, L11, M3, P6, P10, R2, R3, T1, T15 |
| VCCINT | 39, 91 | D5, G6 | 51, 58, 123, 130 | 74, 83, 179, 186 | B9, C8, G8, K9, P8 |
| VCCIO | 3, 18, 34, 51, 66, 82 | C8, D4, E6, F5, G7, H3 | 24, 50, 73, 76, 95, 115, 144 | 5, 23, 41, 63, 85, 107, 125, 143, 165, 191 | B3, B5, C14, E15, F11, G3, G7, G15, H9, J8, K10, L3, L6, M15, P14, T2, T3 |
| NC (No Connect) | - | - | - | 1, 2, 51, 52, 53, 54, 103, 104, 105, 106, 155, 156, 157, 158, 207, 208 | A1, A2, A6, A12, A13, A14, A15, A16, B1, B2, B15, B16, C1, C15, C16, D1, D3, D15, D16, G1, G16, H15, H16, J1, K1, L1, L2, M1, M16, N1, N2, N14, N15, N16, P1, P2, P15, P16, R1, R14, R15, R16, T7, T8, T10, T11, T14, T16 |
| **Total user I/O pins** | **84** | **84** | **120** | **164** | **164** |

7256A tbl 01

# DC Electrical Specifications

## Recommended Operating Conditions

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{CCINT}$ | Supply voltage, internal logic and input buffers | | 3.0 | 3.6 | V |
| $V_{CCIO}$ | Supply voltage for output drivers<br>3.3 volt operation<br>2.5 volt operation | | <br>3.0<br>2.3 | <br>3.6<br>2.7 | <br>V<br>V |
| $V_I$ | Input voltage | | -0.5 | 5.75 | V |
| $V_O$ | Output voltage | | 0 | $V_{CCIO}$ | V |
| $T_A$ | Ambient Operating temperature<br>Commercial temperature range<br>Industrial temperature range | | <br>0<br>-40 | <br>70<br>85 | <br>°C<br>°C |
| $T_J$ | Ambient Operating temperature<br>Commercial temperature range<br>Industrial temperature range | | <br>0<br>-40 | <br>90<br>105 | <br>°C<br>°C |
| $t_R$ | Input signal rise time | | | 40 | ns |
| $t_F$ | Input signal fall time | | | 40 | ns |
| $t_{RVCC}$ | $V_{CC}$ rise time | | | 100 | ms |

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## Absolute Maximum Ratings

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | With respect to ground | -0.5 | 4.6 | V |
| $V_I$ | DC input voltage[1] | With respect to ground | -2.0 | 5.8 | V |
| $I_{OUT}$ | DC output current, per pin | | -25 | 25 | mA |
| $T_{STG}$ | Storage temperature | No bias | -65 | 150 | °C |
| $T_A$ | Ambient temperature | Under bias | -65 | 135 | °C |
| $T_J$ | Junction temperature | Fineline BGA, PQFP, and TPFP packages, Under bias | | 135 | °C |

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## DC Electrical Specifications cont.

### DC Electrical Characteristics (over the operating range)

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{IH}$ | High-level input Voltage | | 1.7 | 5.75 | V |
| $V_{IL}$ | Input LOW Voltage[1] | | -0.5 | 0.8 | V |
| $V_{OH}$ | 3.3-V high-level TTL output Voltage | $I_{OH}$ = -8 mA DC, $V_{CCIO}$ = 3.00 V | 2.4 | | V |
| | 3.3-V high-level CMOS output Voltage | $I_{OH}$ = -0.1 mA DC, $V_{CCIO}$ = 3.00 V | $V_{CCIO}$-0.2 | | V |
| | 2.5-V high-level output Voltage | $I_{OH}$ = -100 µA DC, $V_{CCIO}$ = 2.30 V | 2.1 | | V |
| | | $I_{OH}$ = -1 mA DC, $V_{CCIO}$ = 2.30 V | 2.0 | | |
| | | $I_{OH}$ = -2 mA DC, $V_{CCIO}$ = 2.30 V | 1.7 | | |
| $V_{OL}$ | 3.3-V high-level TTL output Voltage | $I_{OH}$ = 8 mA DC, $V_{CCIO}$ = 3.00 V | | 0.45 | V |
| | 3.3-V high-level CMOS output Voltage | $I_{OH}$ = 0.1 mA DC, $V_{CCIO}$ = 3.00 V | | 0.2 | V |
| | 2.5-V high-level output Voltage | $I_{OH}$ = 100 µA DC, $V_{CCIO}$ = 2.30 V | | 0.2 | V |
| | | $I_{OH}$ = 1 mA DC, $V_{CCIO}$ = 2.30 V | | 0.4 | V |
| | | $I_{OH}$ = 2 mA DC, $V_{CCIO}$ = 2.30 V | | 0.7 | V |
| $I_{IN}$ | Input Leakage Current | $V_I$ = VCC or GND | -10 | 10 | µA |
| $I_{OZ}$ | Output Leakage Current | $V_O$ = VCC or GND | -10 | 10 | µA |

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### Capacitance

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | $V_{IN}$ = 0 V, f = 1.0 MHz | | 8 | pF |
| $C_{OUT}$ | Output Capacitance | $V_{OUT}$ = 0 V, f = 1.0 MHz | | 8 | pF |

7KA tbl 05

# AC Electrical Specifications

## I/O Element Timing Parameters

| | | | Speed: -4 | | Speed: -5 | | Speed: -6 | | |
|---|---|---|---|---|---|---|---|---|---|
| **Symbol** | **Parameter** | **Conditions** | **Min** | **Max** | **Min** | **Max** | **Min** | **Max** | **Unit** |
| $t_{PD1}$ | Input to non-registered output | $C_L$ = 35 pF | | 4.5 | | 5.0 | | 6.0 | ns |
| $t_{PD2}$ | I/O input to non-registered output | $C_L$ = 35 pF | | 4.5 | | 5.0 | | 6.0 | ns |
| $t_{SU}$ | Global clock setup time | | 3.0 | | 3.2 | | 3.7 | | ns |
| $t_{H}$ | Global clock hold time | | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{FSU}$ | Global clock setup time of fast input | | 2.5 | | 2.5 | | 2.5 | | ns |
| $t_{FH}$ | Global clock hold time of fast input | | 0.0 | | 0.0 | | 0.5 | | ns |
| $t_{CO1}$ | Global clock to output delay | $C_L$ = 35 pF | 1.0 | 2.8 | 1.0 | 3.0 | 1.0 | 3.3 | ns |
| $t_{CH}$ | Global clock high time | | 2.0 | | 2.0 | | 3.0 | | ns |
| $t_{CL}$ | Global clock low time | | 2.0 | | 2.0 | | 3.0 | | ns |
| $t_{ASU}$ | Array clock setup time | | 1.4 | | 1.0 | | 0.8 | | ns |
| $t_{AH}$ | Array clock hold time | | 0.8 | | 0.8 | | 1.9 | | ns |
| $t_{ACO1}$ | Array clock to output delay | $C_L$ = 35 pF | | 4.4 | | 5.2 | 1.0 | 6.2 | ns |
| $t_{ACH}$ | Array clock high time | | 2.0 | | 2.0 | | 3.0 | | ns |
| $t_{ACL}$ | Array clock low time | | 2.0 | | 2.0 | | 3.0 | | ns |
| $t_{CNT}$ | Minimum global clock period | | | 5.2 | | 5.5 | | 6.4 | ns |
| $f_{CNT}$ | Max. internal global clock frequency | | 192.3 | | 181.8 | | 156.3 | | MHz |
| $t_{ACNT}$ | Minimum array clock period | | | 5.2 | | 5.5 | | 6.4 | ns |
| $f_{ACNT}$ | Max. internal array clock frequency | | 192.3 | | 181.8 | | 156.3 | | MHz |

7KA tbl 06A1

# AC Electrical Specifications cont.

## External Timing Parameters

| | | | Speed: -7 | | Speed: -10 | | Speed: -12 | | |
|---|---|---|---|---|---|---|---|---|---|
| **Symbol** | **Parameter** | **Conditions** | **Min** | **Max** | **Min** | **Max** | **Min** | **Max** | **Unit** |
| $t_{PD1}$ | Input to non-registered output | $C_L$ = 35 pF | | 7.5 | | 10.0 | | 12.0 | ns |
| $t_{PD2}$ | I/O input to non-registered output | $C_L$ = 35 pF | | 7.5 | | 10.0 | | 12.0 | ns |
| $t_{SU}$ | Global clock setup time | | 4.9 | | 6.6 | | 7.8 | | ns |
| $t_H$ | Global clock hold time | | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{FSU}$ | Global clock setup time of fast input | | 3.0 | | 3.0 | | 3.0 | | ns |
| $t_{FH}$ | Global clock hold time of fast input | | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{CO1}$ | Global clock to output delay | $C_L$ = 35 pF | 1.0 | 4.5 | 1.0 | 5.9 | 1.0 | 7.1 | ns |
| $t_{CH}$ | Global clock high time | | 3.0 | | 4.0 | | 5.0 | | ns |
| $t_{CL}$ | Global clock low time | | 3.0 | | 4.0 | | 5.0 | | ns |
| $t_{ASU}$ | Array clock setup time | | 1.6 | | 2.1 | | 2.4 | | ns |
| $t_{AH}$ | Array clock hold time | | 2.1 | | 3.4 | | 4.4 | | ns |
| $t_{ACO1}$ | Array clock to output delay | $C_L$ = 35 pF | | 7.8 | | 10.4 | | 12.5 | ns |
| $t_{ACH}$ | Array clock high time | | 3.0 | | 4.0 | | 5.0 | | ns |
| $t_{ACL}$ | Array clock low time | | 3.0 | | 4.0 | | 5.0 | | ns |
| $t_{CNT}$ | Minimum global clock period | | | 8.4 | | 11.2 | | 13.3 | ns |
| $f_{CNT}$ | Max. internal global clock frequency | | 119.0 | | 89.3 | | 75.2 | | MHz |
| $t_{ACNT}$ | Minimum array clock period | | | 8.4 | | 11.2 | | 13.3 | ns |
| $f_{ACNT}$ | Max. internal array clock frequency | | 119.0 | | 89.3 | | 75.2 | | MHz |

7KA tbl 06A2

## AC Electrical Specifications cont.

### Internal Timing Parameters[4]

| Symbol | Parameter | Conditions | Speed: -7 Min | Speed: -7 Max | Speed: -10 Min | Speed: -10 Max | Speed: -12 Min | Speed: -12 Max |
|---|---|---|---|---|---|---|---|---|
| $t_{IN}$ | Input pad and buffer delay | | | 0.4 | | 0.6 | | 0.7 |
| $t_{IO}$ | I/O input pad and buffer delay | | | 0.4 | | 0.6 | | 0.7 |
| $t_{FIN}$ | Fast input delay | | | 3.3 | | 3.7 | | 4.1 |
| $t_{SEXP}$ | Shared expander delay | | | 3.6 | | 4.9 | | 5.9 |
| $t_{PEXP}$ | Parallel expander delay | | | 0.8 | | 1.1 | | 1.3 |
| $t_{LAD}$ | Logic array delay | | | 3.7 | | 5.0 | | 6.0 |
| $t_{LAC}$ | Logic control array delay | | | 3.4 | | 4.6 | | 5.6 |
| $t_{IOE}$ | Internal output enable delay | | | 0.0 | | 0.0 | | 0.0 |
| $t_{OD1}$ | Output buffer and pad delay Slow slew rate = off, $V_{CCIO}$ = 5.0 V | $C_L$ = 35 pF | | 0.6 | | 0.7 | | 0.9 |
| $t_{OD2}$ | Output buffer and pad delay Slow slew rate = off, $V_{CCIO}$ = 3.3 V | $C_L$ = 35 pF | | 1.1 | | 1.2 | | 0.4 |
| $t_{OD3}$ | Output buffer and pad delay Slow slew rate = on, $V_{CCIO}$ = 5.0 V or 3.3 V | $C_L$ = 35 pF | | 5.6 | | 5.7 | | 5.9 |
| $t_{ZX1}$ | Output buffer enable delay Slow slew rate = off, $V_{CCIO}$ = 5.0 V | $C_L$ = 35 pF | | 4.0 | | 5.0 | | 5.0 |
| $t_{ZX2}$ | Output buffer enable delay Slow slew rate = off, $V_{CCIO}$ = 3.3 V | $C_L$ = 35 pF | | 4.5 | | 5.5 | | 5.5 |
| $t_{ZX3}$ | Output buffer enable delay Slow slew rate = on, $V_{CCIO}$ = 5.0 V or 3.3 V | $C_L$ = 35 pF | | 9.0 | | 10.0 | | 10.0 |
| $t_{XZ}$ | Output buffer disable delay | $C_L$ = 5 pF[3] | | 4.0 | | 5.0 | | 5.0 |
| $t_{SU}$ | Register setup time | | 1.3 | | 1.7 | | 2.0 | |
| $t_H$ | Register hold time | | 2.4 | | 3.8 | | 4.8 | |
| $t_{FSU}$ | Register setup time of fast input | | 1.1 | | 1.1 | | 1.1 | |
| $t_{FH}$ | Register hold time of fast input | | 1.9 | | 1.9 | | 1.9 | |
| $t_{RD}$ | Register delay | | | 2.1 | | 2.8 | | 3.3 |
| $t_{COMB}$ | Combinatorial delay | | | 1.5 | | 2.0 | | 2.4 |
| $t_{IC}$ | Array clock delay | | | 3.4 | | 4.6 | | 5.6 |
| $t_{EN}$ | Register enable time | | | 3.4 | | 4.6 | | 5.6 |
| $t_{GLOB}$ | Global control delay | | | 1.4 | | 1.8 | | 2.2 |
| $t_{PRE}$ | Register preset time | | | 3.9 | | 5.2 | | 6.2 |
| $t_{CLR}$ | Register clear time | | | 3.9 | | 5.2 | | 6.2 |

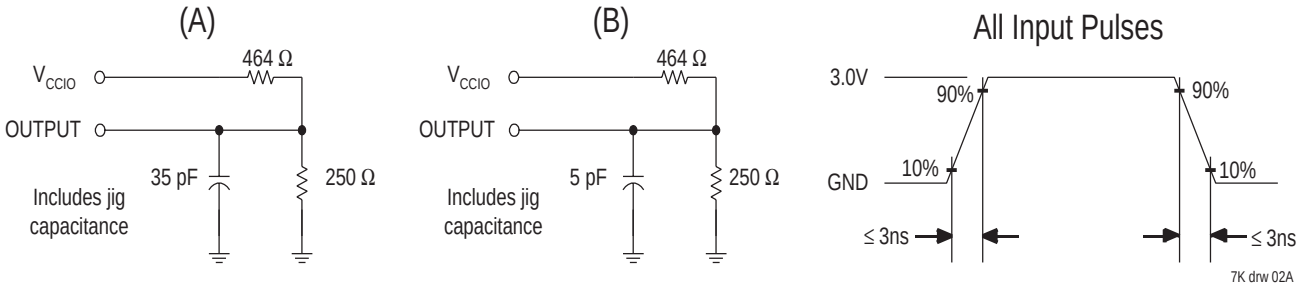
# AC Electrical Specifications cont.

## Internal Timing Parameters[4]

| Symbol | Parameter | Conditions | Speed: -7 Min | Speed: -7 Max | Speed: -10 Min | Speed: -10 Max | Speed: -12 Min | Speed: -12 Max | Unit |
|---|---|---|---|---|---|---|---|---|---|
| $t_{IN}$ | Input pad and buffer delay | | | 0.4 | | 0.6 | | 0.7 | ns |
| $t_{IO}$ | I/O input pad and buffer delay | | | 0.4 | | 0.6 | | 0.7 | ns |
| $t_{FIN}$ | Fast input delay | | | 3.3 | | 3.7 | | 4.1 | ns |
| $t_{SEXP}$ | Shared expander delay | | | 3.6 | | 4.9 | | 5.9 | ns |
| $t_{PEXP}$ | Parallel expander delay | | | 0.8 | | 1.1 | | 1.3 | ns |
| $t_{LAD}$ | Logic array delay | | | 3.7 | | 5.0 | | 6.0 | ns |
| $t_{LAC}$ | Logic control array delay | | | 3.4 | | 4.6 | | 5.6 | ns |
| $t_{IOE}$ | Internal output enable delay | | | 0.0 | | 0.0 | | 0.0 | ns |
| $t_{OD1}$ | Output buffer and pad delay Slow slew rate = off, $V_{CCIO}$ = 5.0 V | $C_L$ = 35 pF | | 0.6 | | 0.7 | | 0.9 | ns |
| $t_{OD2}$ | Output buffer and pad delay Slow slew rate = off, $V_{CCIO}$ = 3.3 V | $C_L$ = 35 pF | | 1.1 | | 1.2 | | 0.4 | ns |
| $t_{OD3}$ | Output buffer and pad delay Slow slew rate = on, $V_{CCIO}$ = 5.0 V or 3.3 V | $C_L$ = 35 pF | | 5.6 | | 5.7 | | 5.9 | ns |
| $t_{ZX1}$ | Output buffer enable delay Slow slew rate = off, $V_{CCIO}$ = 5.0 V | $C_L$ = 35 pF | | 4.0 | | 5.0 | | 5.0 | ns |
| $t_{ZX2}$ | Output buffer enable delay Slow slew rate = off, $V_{CCIO}$ = 3.3 V | $C_L$ = 35 pF | | 4.5 | | 5.5 | | 5.5 | ns |
| $t_{ZX3}$ | Output buffer enable delay Slow slew rate = on, $V_{CCIO}$ = 5.0 V or 3.3 V | $C_L$ = 35 pF | | 9.0 | | 10.0 | | 10.0 | ns |
| $t_{XZ}$ | Output buffer disable delay | $C_L$ = 5 pF[3] | | 4.0 | | 5.0 | | 5.0 | ns |
| $t_{SU}$ | Register setup time | | 1.3 | | 1.7 | | 2.0 | | ns |
| $t_{H}$ | Register hold time | | 2.4 | | 3.8 | | 4.8 | | ns |
| $t_{FSU}$ | Register setup time of fast input | | 1.1 | | 1.1 | | 1.1 | | ns |
| $t_{FH}$ | Register hold time of fast input | | 1.9 | | 1.9 | | 1.9 | | ns |
| $t_{RD}$ | Register delay | | | 2.1 | | 2.8 | | 3.3 | ns |
| $t_{COMB}$ | Combinatorial delay | | | 1.5 | | 2.0 | | 2.4 | ns |
| $t_{IC}$ | Array clock delay | | | 3.4 | | 4.6 | | 5.6 | ns |
| $t_{EN}$ | Register enable time | | | 3.4 | | 4.6 | | 5.6 | ns |
| $t_{GLOB}$ | Global control delay | | | 1.4 | | 1.8 | | 2.2 | ns |
| $t_{PRE}$ | Register preset time | | | 3.9 | | 5.2 | | 6.2 | ns |
| $t_{CLR}$ | Register clear time | | | 3.9 | | 5.2 | | 6.2 | ns |
| $t_{LIA}$ | LIA delay | | | 1.3 | | 1.7 | | 2.0 | ns |

7KA tbl 07A2

## AC Test Conditions




## Notes to Tables

1. During transitions, inputs may undershoot to -2.0V for periods shorter than 20ns. Otherwise, minimum DC input voltage is 0.3V.

2. Typical values are at $V_{CC}$ of 5.0 volts and ambient temperature of 25 ºC.

3. Guaranteed but not tested. Characterized initially, and after any design changes which may affect these parameters.

4. Internal timing delays are based on characterization, and cannot be explicitly tested. Internal timing parameters should be used for performance estimation only.

## Revision History

| | |
|---|---|
| 11 Jan. 1999: | Created preliminary document. |
| 31 July 1999: | Created full document. |
| 13 Oct. 1999: | Corrected typographical error in AC Test Condition diagram (W changed to Ω) also corrected timing in 10ns External Timing Paramiters |
| 1 Dec. 2000: | Updated application note reference. |

## Ordering Information

| Part Number | Temperature Range | Package Type | Speed | Altera Equivalent |
|---|---|---|---|---|
| CL7256ATC100-12 | Commercial | 100-pin Thin QFP | -12 | EPM7256ATC100-12 |
| CL7256ATC100-10 | | | -10 | EPM7256ATC100-10 |
| CL7256ATC100-7 | | | -7 | EPM7256ATC100-7 |
| CL7256ATC100-6 | | | -6 | N/A |
| CL7256ATC100-5 | | | -5 | N/A |
| CL7256ATC100-4 | | | -4 | N/A |
| CL7256ATC144-12 | | 144-pin Thin QFP | -12 | EPM7256ATC144-12 |
| CL7256ATC144-10 | | | -10 | EPM7256ATC144-10 |
| CL7256ATC144-7 | | | -7 | EPM7256ATC144-7 |
| CL7256ATC144-6 | | | -6 | N/A |
| CL7256ATC144-5 | | | -5 | N/A |
| CL7256ATC144-4 | | | -4 | N/A |
| CL7256ATI144-10 | Industrial | | -10 | EPM7256ATI144-10 |
| CL7256AQC208-12 | Commercial | 208-pin Plastic QFP | -12 | EPM7256AQC208-12 |
| CL7256AQC208-10 | | | -10 | EPM7256AQC208-10 |
| CL7256AQC208-7 | | | -7 | EPM7256AQC208-7 |
| CL7256AQC208-6 | | | -6 | N/A |
| CL7256AQC208-5 | | | -5 | N/A |
| CL7256AQC208-4 | | | -4 | N/A |
| CL7256AQI208-10 | Industrial | | -10 | EPM7256AQI208-10 |
| CL7256AFC256-12 | Commercial | 256-pin FBGA | -12 | EPM7256AFC256-12 |
| CL7256AFC256-10 | | | -10 | EPM7256AFC256-10 |
| CL7256AFC256-7 | | | -7 | EPM7256AFC256-7 |
| CL7256AFC256-6 | | | -6 | N/A |
| CL7256AFC256-5 | | | -5 | N/A |
| CL7256AFC256-4 | | | -4 | N/A |
| CL7256AFI256-10 | Industrial | | -10 | EPM7256AFI256-10 |

7256A tbl 02B

## Ordering Information (cont.)

| Part Number | Temperature Range | Package Type | Speed | Altera Equivalent |
|---|---|---|---|---|
| CL7256AETC100-10 | Commercial | 100-pin Thin QFP | -10 | EPM7256AETC100-10 |
| CL7256AETC100-7 | | | -7 | EPM7256AETC100-7 |
| CL7256AETC100-6 | | | -6 | EPM7256AETC100-6 |
| CL7256AETC100-5 | | | -5 | EPM7256AETC100-5 |
| CL7256AETC100-4 | | | -4 | N/A |
| CL7256AETI100-7 | Industrial | | -7 | EPM7256AETI100-7 |
| CL7256AEFC100-10 | Commercial | 100-pin FBGA | -10 | EPM7256AEFC100-10 |
| CL7256AEFC100-7 | | | -7 | EPM7256AEFC100-7 |
| CL7256AEFC100-6 | | | -6 | EPM7256AEFC100-6 |
| CL7256AEFC100-5 | | | -5 | EPM7256AEFC100-5 |
| CL7256AEFC100-4 | | | -4 | N/A |
| CL7256AETC144-10 | | 144-pin Thin QFP | -10 | EPM7256AETC144-10 |
| CL7256AETC144-7 | | | -7 | EPM7256AETC144-7 |
| CL7256AETC144-6 | | | -6 | EPM7256AETC144-6 |
| CL7256AETC144-5 | | | -5 | EPM7256AETC144-5 |
| CL7256AETC144-4 | | | -4 | N/A |
| CL7256AETI144-7 | Industrial | | | EPM7256AETI144-7 |
| CL7256AEQC208-10 | Commercial | 208-pin Plastic QFP | -10 | EPM7256AEQC208-10 |
| CL7256AEQC208-7 | | | -7 | EPM7256AEQC208-7 |
| CL7256AEQC208-6 | | | -6 | EPM7256AEQC208-6 |
| CL7256AEQC208-5 | | | -5 | EPM7256AEQC208-5 |
| CL7256AEQC208-4 | | | -4 | N/A |
| CL7256AEQI208-7 | Industrial | | -7 | EPM7256AEQI208-7 |
| CL7256AEFC256-10 | Commercial | 256-pin FBGA | -10 | EPM7256AEFC256-10 |
| CL7256AEFC256-7 | | | -7 | EPM7256AEFC256-7 |
| CL7256AEFC256-6 | | | -6 | EPM7256AEFC256-6 |
| CL7256AEFC256-5 | | | -5 | EPM7256AEFC256-5 |
| CL7256AEFC256-4 | | | -4 | N/A |
| CL7256AEFI256-7 | Industrial | | -7 | EPM7256AEFI256-7 |

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