

Indium Gallium Phosphorus HBT WLAN Power Amplifier

Designed for 802.11g and dual mode applications with frequencies from 2400 to 2500 MHz.

- 26.5 dBm P1dB @ 2450 MHz
- Power Gain: 27.5 dB Typ (@ f = 2450 MHz, Class AB)
- High Gain, High Efficiency and High Linearity
- EVM = 3% Typ @ P_{out} = +19 dBm, 14% PAE
- Pb-Free Leads
- In Tape and Reel. R2 Suffix = 1,500 Units per 12 mm, 7 inch Reel.



**2400-2500 MHz, 27.5 dB, 26.5 dBm
 802.11g WLAN POWER AMPLIFIER
 InGaP HBT**

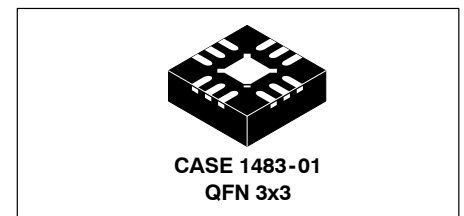


Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Collector Supply	V _{CC}	5	V
Base Supply First Stage	V _{B1}	5	V
Base Supply Second Stage	V _{B2}	5	V
Detector Bias Supply	V _{BIAS}	5	V
DC Current	I _{DC}	171	mA

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Ambient	R _{θJA}	185 (1)	°C/W
Case Operating Temperature Range	T _C	- 40 to +85	°C
Storage Temperature Range	T _{stg}	- 55 to +150	°C

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22-A114)	2 (Minimum)
Machine Model (per EIA/JESD22-A115)	A (Minimum)
Charge Device Model (per JESD22-C101)	II (Minimum)

Table 4. Moisture Sensitivity Level

Test Methodology	Rating	Package Peak Temperature	Unit
Per JESD 22-A113, IPC/JEDEC J-STD-020	1	260	°C

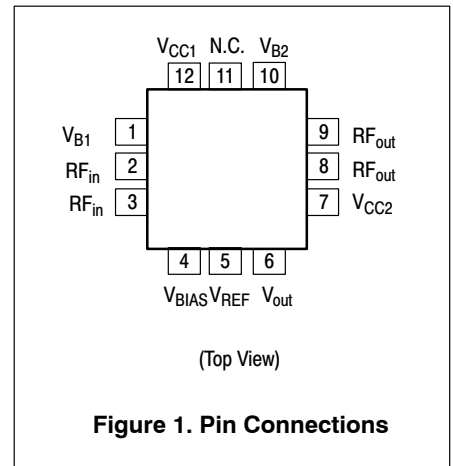
1. Simulated.

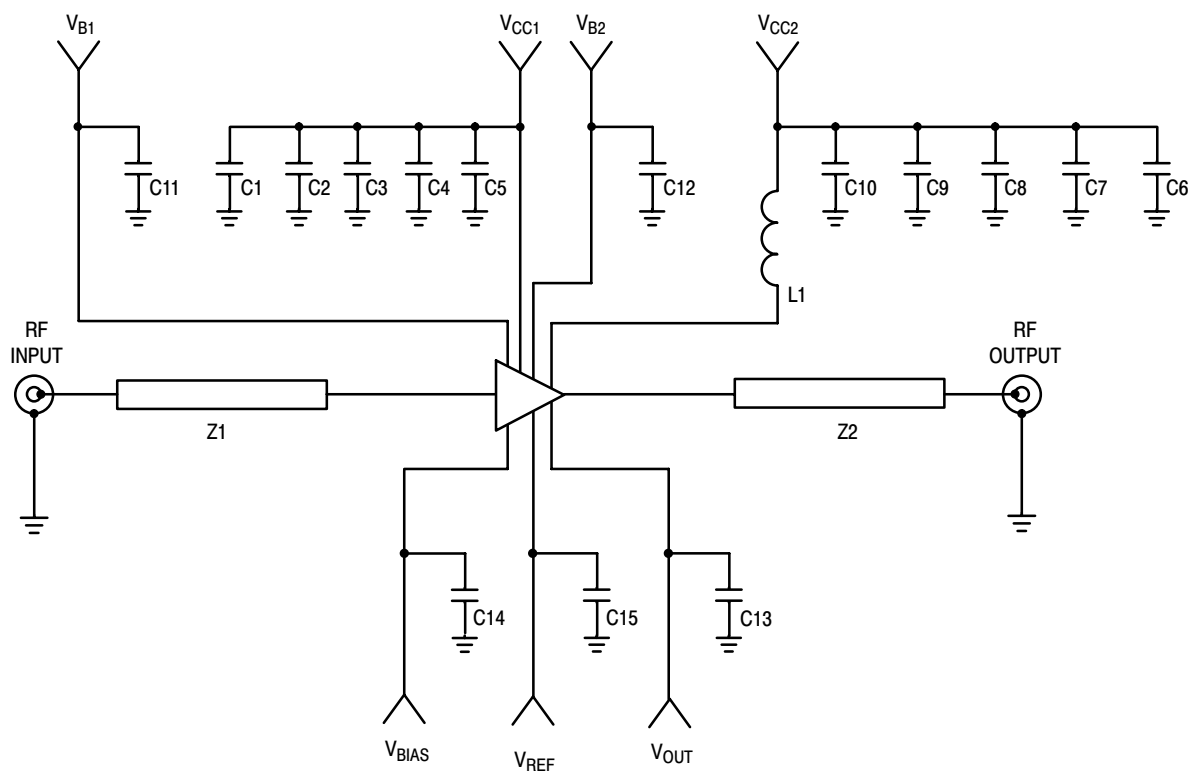
Table 5. Electrical Characteristics ($T_A = 25^\circ\text{C}$ unless otherwise noted.) $V_{CC} = 3.3\text{ Vdc}$, $V_{BIAS} = 3\text{ Vdc}$, $I_{CQ} = 83\text{ mA}$, $f = 2450\text{ MHz}$

Characteristic	Symbol	Min	Typ	Max	Unit
Output Power at 1dB Compression	P1dB	24	26.5	—	dBm
Power Gain ($P_{out} = 19\text{ dBm}$)	G_p	26	27.5	29	dB
Error Vector Magnitude ($P_{out} = 19\text{ dBm}$, 64 QAM/54 Mbps)	EVM	—	3	—	%
Total Current ($P_{out} = 19\text{ dBm}$)	I_{Ctotal}	—	210	—	mA
Quiescent Current	I_{DCQ}	—	156	—	mA
Bias Control Reference Current ($I_{CQ} = 66\text{ mA}$)	I_{ref}	—	8.4	—	mA
Gain Flatness (Over 100 MHz)	G_F	—	± 0.2	—	dB
Gain Variation over Temperature (-40 to 85°C)	—	—	± 1	—	dB
Input Return Loss	IRL	—	-10	-7.5	dB
Reverse Isolation	—	—	-35	—	dB
Second Harmonic ($P_{out} = 19\text{ dBm}$)	—	—	-45	—	dBc
Third Harmonic ($P_{out} = 19\text{ dBm}$)	—	—	-35	—	dBc
Ramp-On Time (10-90%)	t_{ON}	—	100	—	ns

Table 6. Functional Pin Description

Name	Pin Number	Description
V _{B1}	1	Base power supply for first stage amplifier.
RF _{in}	2, 3	RF input for the power amplifier. This pin is DC-shorted to GND and AC-coupled to the transistor base of the first stage.
V _{BIAS}	4	Detector bias voltage supply.
V _{REF}	5	Detector output voltage reference. V _{out} - V _{REF} is useful for tracking detector performance over temperature.
V _{out}	6	Detector output voltage.
V _{CC2}	7	Collector power supply for second stage amplifier.
RF _{OUT}	8, 9	RF output for the power amplifier. This pin is DC-coupled and requires a DC-blocking series capacitor.
V _{B2}	10	Base power supply for second stage amplifier.
N.C.	11	Not connected.
V _{CC1}	12	Collector power supply for first stage amplifier.
GND	Backside Center Metal	The center metal base of the QFN 3x3 package provides both DC and RF ground as well as heat sink contact for the power amplifier.



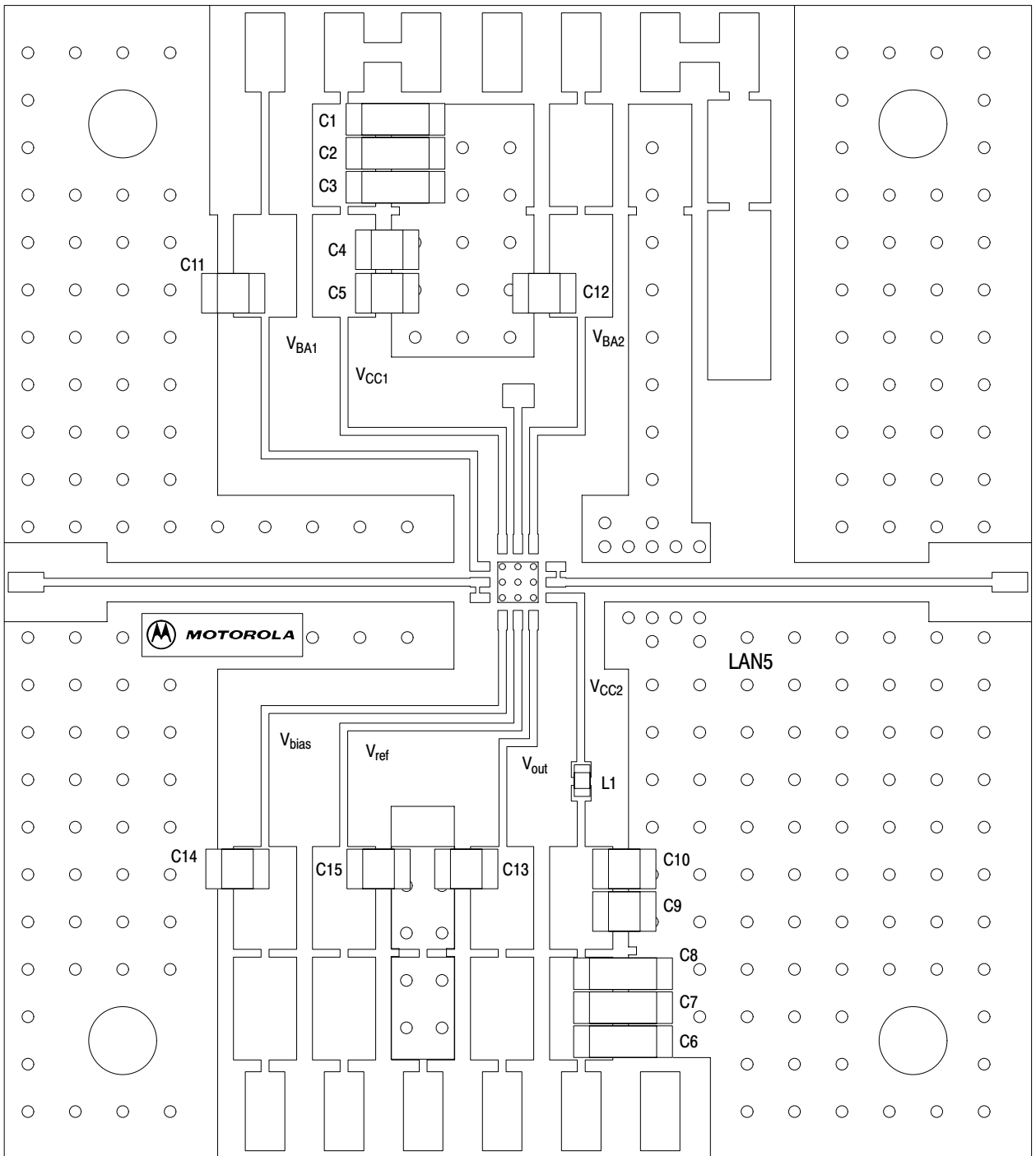


Z1, Z2 0.10" x 0.5395" Microstrip
 PCB Getek ML200M, 0.005", $\epsilon_r = 3.8$

Figure 2. MMG2401NR2 Test Circuit Schematic

Table 7. MMG2401NR2 Test Circuit Component Designations and Values

Part	Description	Part Number	Manufacturer
C1, C6	1 μ F Chip Capacitor	12065A105JAT2A	AVX
C2, C7	0.1 μ F Chip Capacitor	12065A104JAT2A	AVX
C3, C8	0.01 μ F Chip Capacitor	12065A103JAT2A	AVX
C4, C9, C11, C12	100 pF Chip Capacitor	08055A101FAT2A	AVX
C5, C10, C13, C14, C15	20 pF Chip Capacitor	12065A200CAT2A	AVX
L1	7.5 nH Chip Inductor	0402CS-7N5XJBC	Coilcraft



Freescale has begun the transition of marking Printed Circuit Boards (PCBs) with the Freescale Semiconductor signature/logo. PCBs may have either Motorola or Freescale markings during the transition period. These changes will have no impact on form, fit or function of the current product.

Figure 3. MMG2401NR2 Test Circuit Component Layout

TYPICAL CHARACTERISTICS

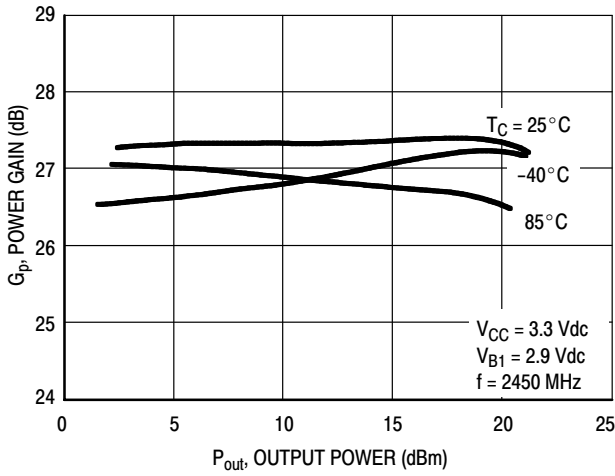


Figure 4. Power Gain versus Output Power

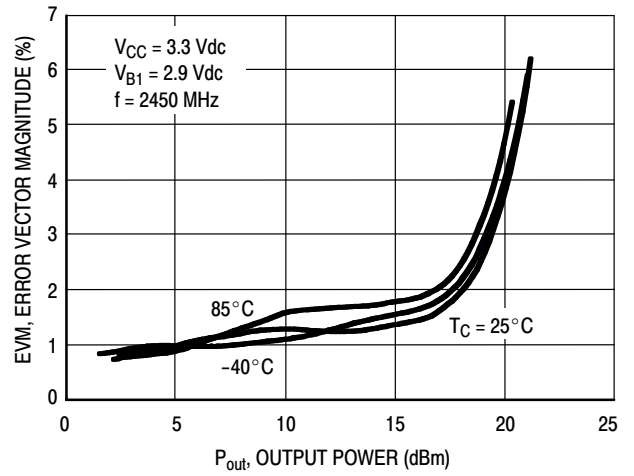


Figure 5. Error Vector Magnitude versus Output Power

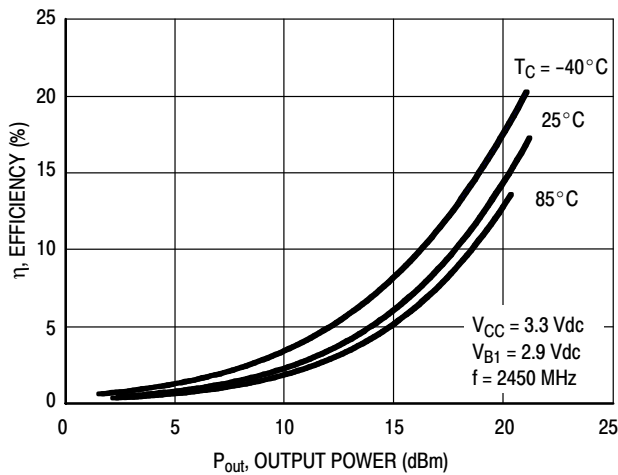


Figure 6. Efficiency versus Output Power

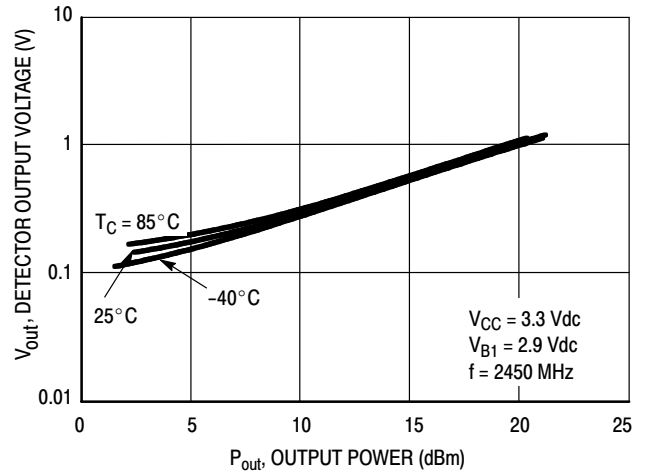


Figure 7. Detector Output Voltage versus Output Power

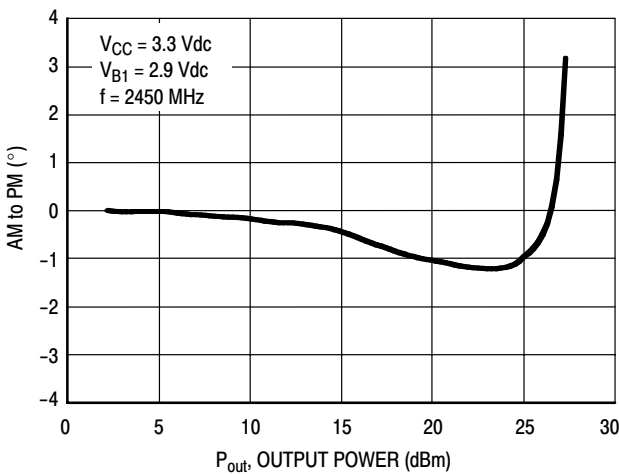


Figure 8. AM to PM versus Output Power

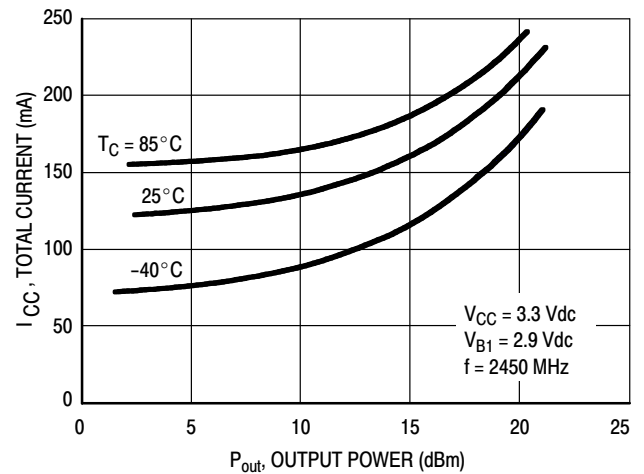


Figure 9. Total Current versus Output Power

TYPICAL CHARACTERISTICS

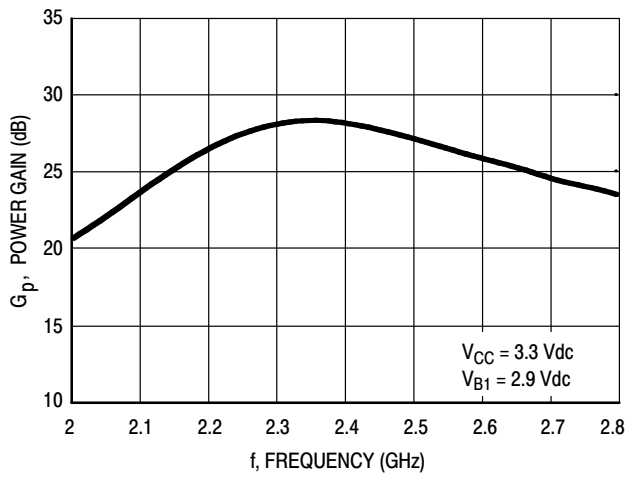


Figure 10. Power Gain (S21) versus Frequency

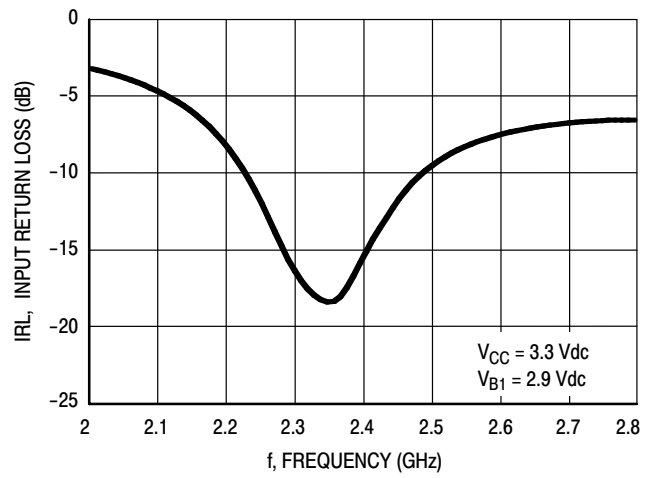


Figure 11. Input Return Loss (S11) versus Frequency

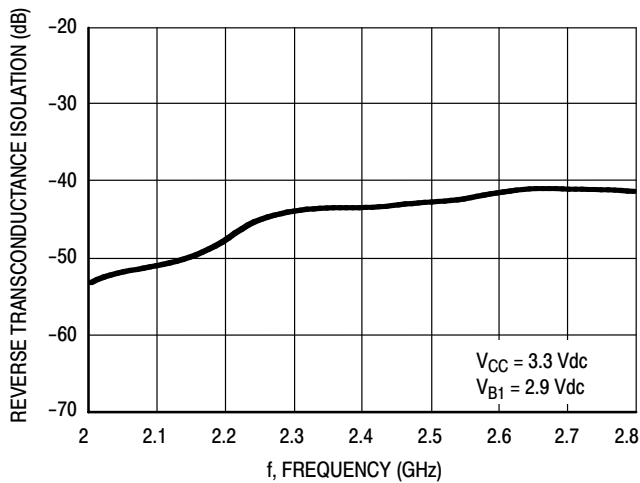


Figure 12. Reverse Transconductance Isolation (S12) versus Frequency

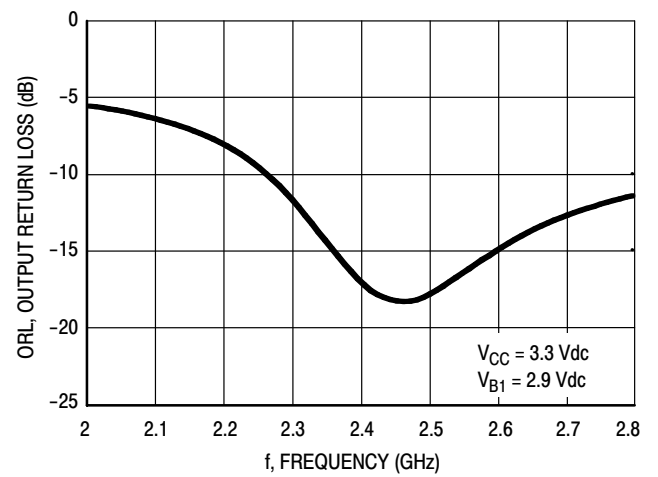
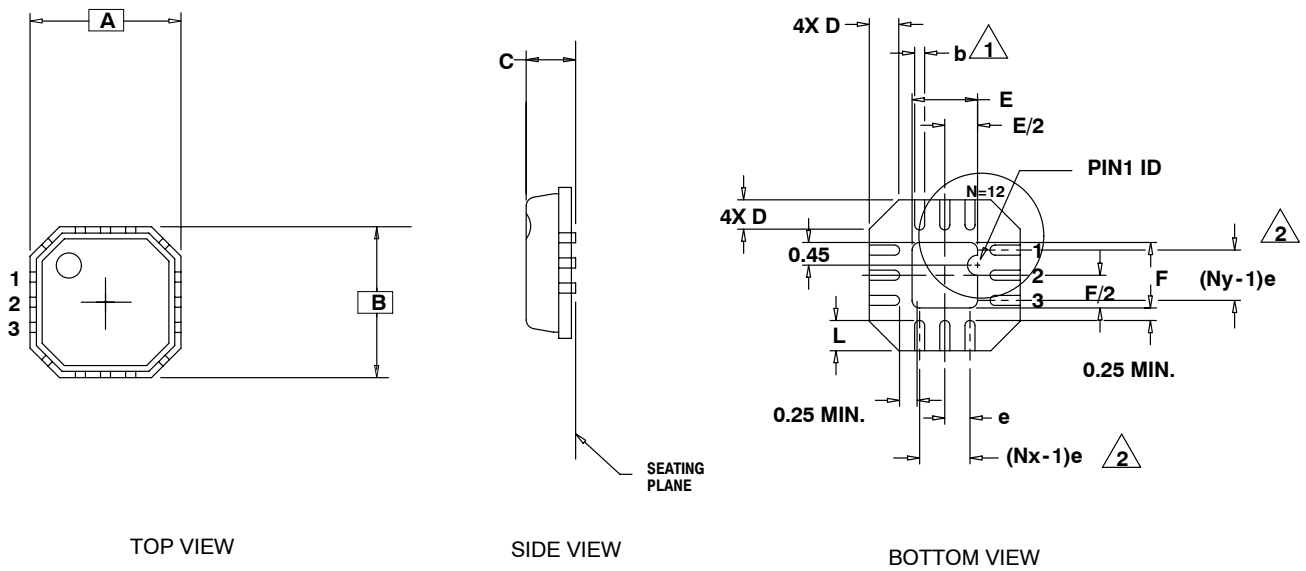


Figure 13. Output Return Loss (S22) versus Frequency

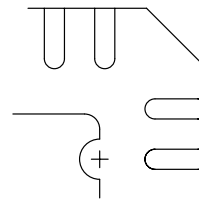


NOTES:

- 1. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.20 AND 0.25 MM FROM TERMINAL TIP.
- 2. N IS THE NUMBER OF TERMINALS (12).
Nx IS THE NUMBER OF TERMINALS IN X-DIRECTION AND
Ny IS THE NUMBER OF TERMINALS IN Y-DIRECTION.
- 3. ALL DIMENSIONS ARE IN MILLIMETERS.

DIM	MIN	NOM	MAX
A		3.00 BSC	
B		3.00 BSC	
C	-	0.85	1.00
D	0.24	0.42	0.60
E	SEE EXPOSED PAD		
F	SEE EXPOSED PAD		
b	0.18	0.23	0.30
e	0.50 BSC		
Nx	3		
Ny	3		

SYMBOLS	E			F		
	MIN	NOM	MAX	MIN	NOM	MAX
EXPOSED PAD	1.15	1.30	1.45	1.15	1.30	1.45

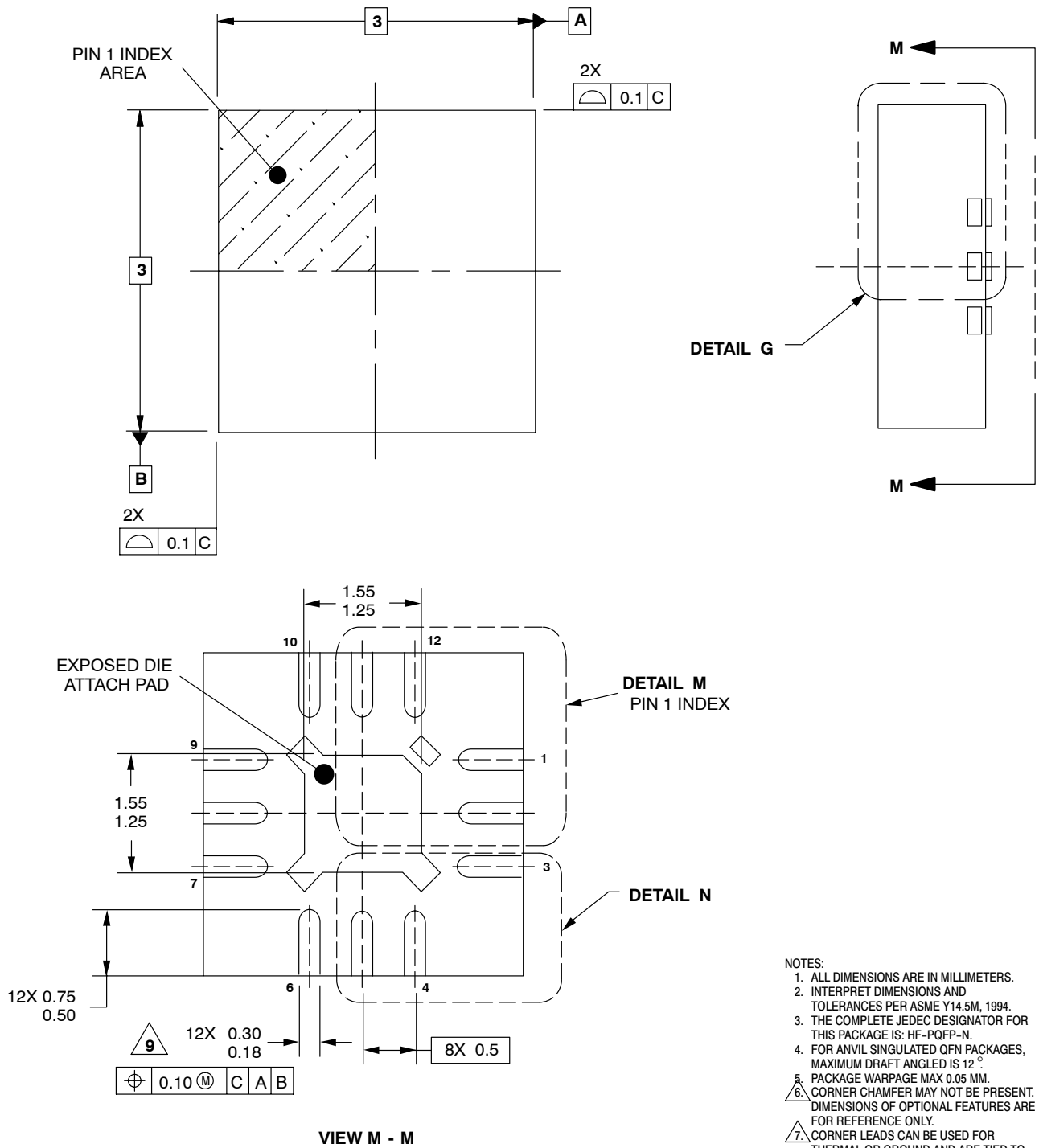


STANDARD

DETAIL "A" - PIN #1 ID AND TIE BAR MARK OPTION

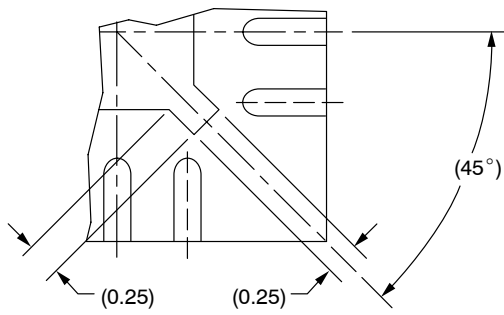
Figure 14. MMG2401NR2 Specific Mechanical Outline Information

PACKAGE DIMENSIONS

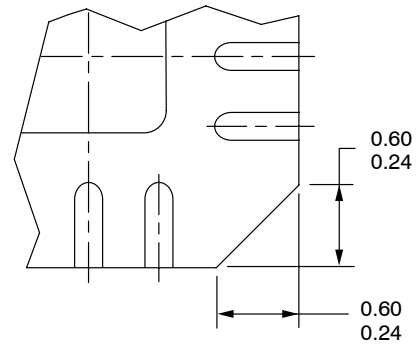


- NOTES:**
1. ALL DIMENSIONS ARE IN MILLIMETERS.
 2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
 3. THE COMPLETE JEDEC DESIGNATOR FOR THIS PACKAGE IS: HF-PQFP-N.
 4. FOR ANVIL SINGULATED QFN PACKAGES, MAXIMUM DRAFT ANGLED IS 12°.
 5. PACKAGE WARPAGE MAX 0.05 MM.
 6. CORNER CHAMFER MAY NOT BE PRESENT. DIMENSIONS OF OPTIONAL FEATURES ARE FOR REFERENCE ONLY.
 7. CORNER LEADS CAN BE USED FOR THERMAL OR GROUND AND ARE TIED TO THE DIE ATTACH PAD. THESE LEADS ARE NOT INCLUDED IN THE LEAD COUNT.
 8. COPLANARITY APPLIES TO LEAD, CORNER LEADS, AND DIE ATTACH PAD.
 9. THIS DIMENSION APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.20 MM AND 0.25 MM FROM TERMINAL TIP.

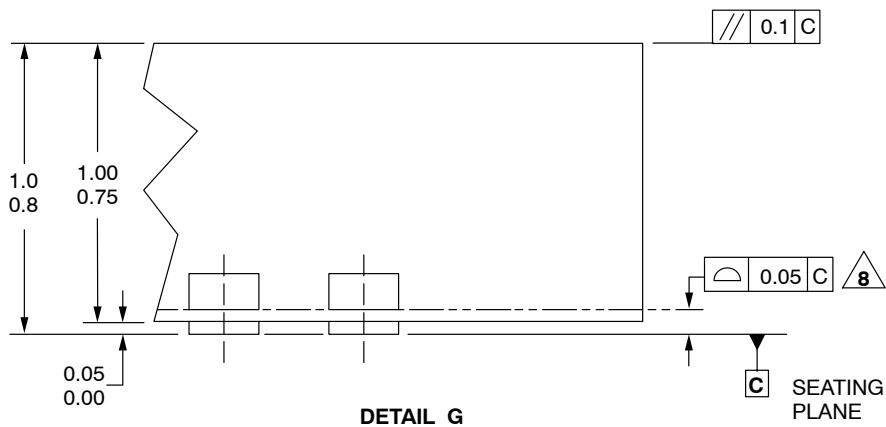
**CASE 1483-01
ISSUE O
QFN 3x3**



DETAIL N
PREFERRED CORNER CONFIGURATION

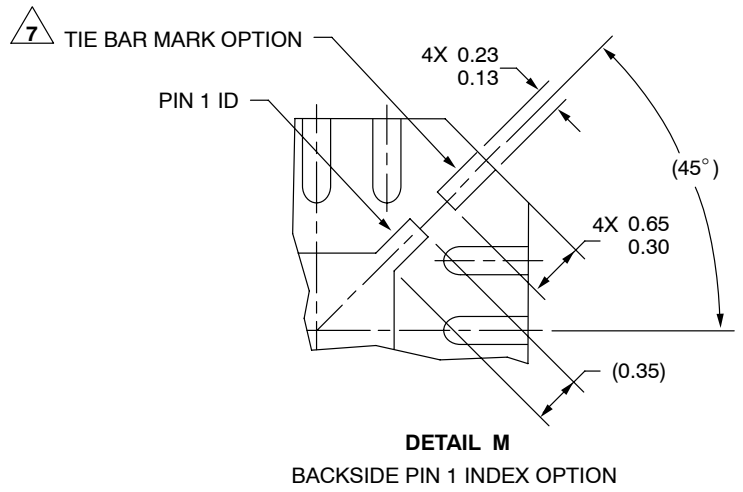
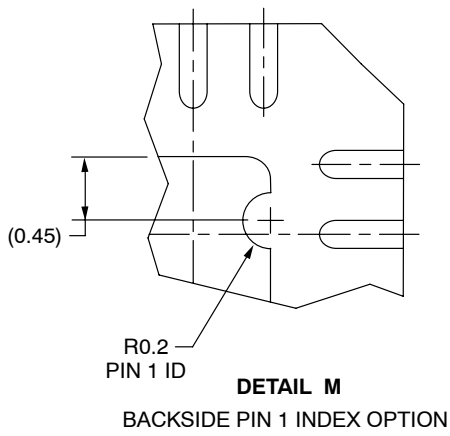
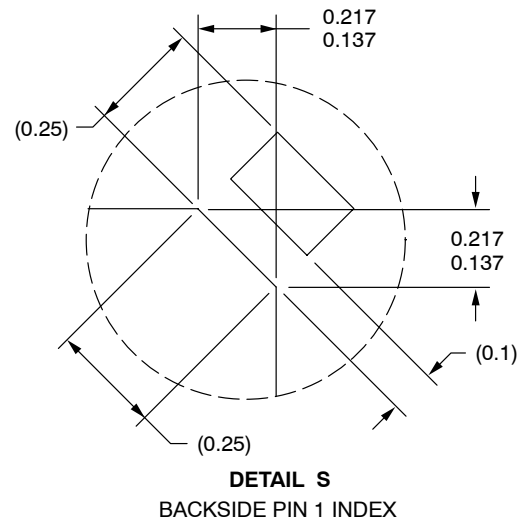
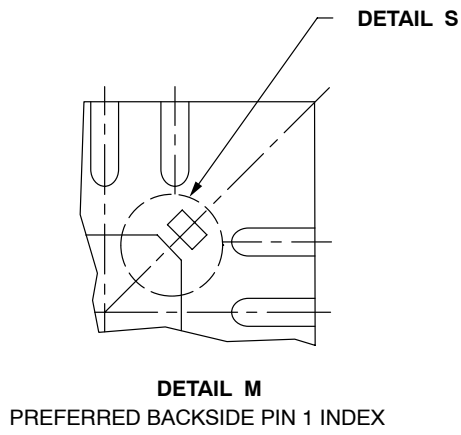


DETAIL N
CORNER CONFIGURATION



DETAIL G
VIEW ROTATED 90° CW

CASE 1483-01
ISSUE O
QFN 3x3



**CASE 1483-01
ISSUE O
QFN 3x3**

How to Reach Us:

Home Page:

www.freescale.com

E-mail:

support@freescale.com

USA/Europe or Locations Not Listed:

Freescale Semiconductor
Technical Information Center, CH370
1300 N. Alma School Road
Chandler, Arizona 85224
+1-800-521-6274 or +1-480-768-2130
support@freescale.com

Europe, Middle East, and Africa:

Freescale Halbleiter Deutschland GmbH
Technical Information Center
Schatzbogen 7
81829 Muenchen, Germany
+44 1296 380 456 (English)
+46 8 52200080 (English)
+49 89 92103 559 (German)
+33 1 69 35 48 48 (French)
support@freescale.com

Japan:

Freescale Semiconductor Japan Ltd.
Headquarters
ARCO Tower 15F
1-8-1, Shimo-Meguro, Meguro-ku,
Tokyo 153-0064
Japan
0120 191014 or +81 3 5437 9125
support.japan@freescale.com

Asia/Pacific:

Freescale Semiconductor Hong Kong Ltd.
Technical Information Center
2 Dai King Street
Tai Po Industrial Estate
Tai Po, N.T., Hong Kong
+800 2666 8080
support.asia@freescale.com

For Literature Requests Only:

Freescale Semiconductor Literature Distribution Center
P.O. Box 5405
Denver, Colorado 80217
1-800-441-2447 or 303-675-2140
Fax: 303-675-2150
LDCForFreescaleSemiconductor@hibbertgroup.com

Information in this document is provided solely to enable system and software implementers to use Freescale Semiconductor products. There are no express or implied copyright licenses granted hereunder to design or fabricate any integrated circuits or integrated circuits based on the information in this document.

Freescale Semiconductor reserves the right to make changes without further notice to any products herein. Freescale Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does Freescale Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. "Typical" parameters that may be provided in Freescale Semiconductor data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals", must be validated for each customer application by customer's technical experts. Freescale Semiconductor does not convey any license under its patent rights nor the rights of others. Freescale Semiconductor products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the Freescale Semiconductor product could create a situation where personal injury or death may occur. Should Buyer purchase or use Freescale Semiconductor products for any such unintended or unauthorized application, Buyer shall indemnify and hold Freescale Semiconductor and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that Freescale Semiconductor was negligent regarding the design or manufacture of the part.

Freescale™ and the Freescale logo are trademarks of Freescale Semiconductor, Inc. All other product or service names are the property of their respective owners.

© Freescale Semiconductor, Inc. 2005. All rights reserved.

