National Semiconductor

93L422A
256 x 4-Bit Static Random Access Memory

General Description

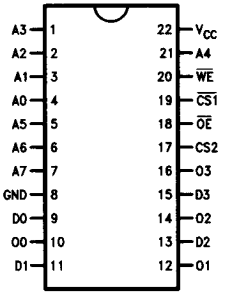
The 93L422A is a 1024-bit read/write Random Access Memory (RAM) organized 256 words by four bits. It is designed for high speed cache, control and buffer storage applications. The device includes full on-chip decoding, separate Data input and non-inverting Data output, as well as two Chip Select Lines.

Features

- New design to replace old 93422/93L422
- Improved ESD thresholds
- Alpha hard without die coat
- Commercial address access time
  93L422A 25 ns
- Fully TTL compatible
- Features TRI-STATE® outputs
- Power dissipation decreases with increasing temperature

Connection Diagram

22-Pin DIP



TL/D/9996-1

Top View

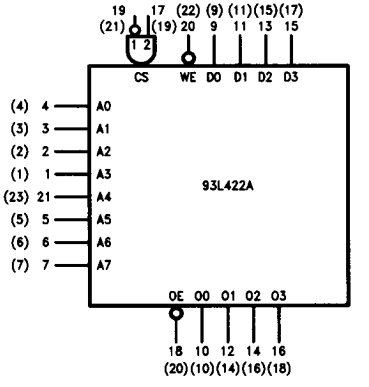
Order Number 93L422ADC or 93L422APC
See NS Package Number J22A* or N22A*

Optional Processing QR = Burn-In
*For most current package information, contact product marketing

Pin Names

A0–A7	Address Inputs
D0–D3	Data Inputs
$\overline{CS1}$	Chip Select Input (Active LOW)
CS2	Chip Select Input (Active HIGH)
$\overline{WE}$	Write Enable Input (Active LOW)
$\overline{OE}$	Output Enable Input (Active LOW)
O0–O3	Data Outputs

Logic Symbol



TL/D/9996-3

Absolute Maximum Ratings

Above which the useful life may be impaired

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Supply Voltage Range	−0.5V to +7.0V
Input Voltage (DC) (Note 1)	−0.5V to V_{CC}
Input Current (DC)	−12 mA to +5.0 mA
Voltage Applied to Outputs (Note 2)	−0.5V to +5.5V
Lead Temperature (Soldering, 10 sec.)	300°C
Maximum Junction Temperature (T_J)	+175°C
Output Current	+20 mA

Guaranteed Operating Ranges

Supply Voltage (V_{CC})	5.0V ±5%
Case Temperature (T_C)	0°C to +75°C

DC Characteristics over operating temperature ranges (Note 3)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{OL}	Output LOW Voltage	V_{CC} = Min, I_{OL} = 8 mA		0.3	0.45	V
V_{IH}	Input HIGH Voltage	Guaranteed Input HIGH Voltage for All Inputs (Notes 4, 5 & 6)	2.1			
V_{IL}	Input LOW Voltage	Guaranteed Input LOW Voltage for All Inputs (Notes 4, 5 & 6)			0.8	
V_{OH}	Output HIGH Voltage	V_{CC} = Min, I_{OH} = −5.2V	2.4			V
I_{IL}	Input LOW Current	V_{CC} = Max, V_{IN} = 0.4V		−150	−300	μA
I_{IH}	Input HIGH Current	V_{CC} = Max, V_{IN} = 4.5V		1.0	40	μA
I_{IHB}	Input Breakdown Current	V_{CC} = Max, V_{IN} = V_{CC}			1.0	mA
V_{IC}	Input Diode Clamp Voltage	V_{CC} = Max, I_{IN} = −10 mA		−1.0	−1.5	V
I_{OZH}	Output Current (HIGH Z)	V_{CC} = Max, V_{OUT} = 2.4V			50	μA
I_{OZL}		V_{CC} = Max, V_{OUT} = 0.5V			−50	μA
I_{OS}	Output Current Short Circuit to Ground	V_{CC} = Max (Note 7)	−10		−70	mA
I_{CC}	Power Supply Current	V_{CC} = Max, All Outputs Open, All Inputs = GND			80	mA

AC Electrical Characteristics (Note 6) V_{CC} = 5.0V ±5%, GND = 0V, T_C = 0°C to +75°C

Symbol	Parameter	Conditions	Min	Max	Units
READ TIMING					
t_{ACS}	Chip Select Access Time	*Figures 3a, 3b, 3c*		20	ns
t_{ZRCS}	Chip Select to High Z			20	ns
t_{AOS}	Output Enable Access Time			20	ns
t_{ZROS}	Output Enable to HIGH Z			20	ns
t_{AA}	Address Access Time (Note 8)			25	ns
WRITE TIMING					
t_W	Write Pulse Width to Guarantee Writing (Note 9)	*Figure 4*	20		ns
t_{WSD}	Data Setup Time prior to Write		5		ns
t_{WHD}	Data Hold Time after Write		5		ns
t_{WSA}	Address Setup Time prior to Write (Note 9)		5		ns
t_{WHA}	Address Hold Time after Write		5		ns
t_{WSCS}	Chip Select Setup Time prior to Write		5		ns
t_{WHCS}	Chip Select Hold Time after Write		5		ns
t_{ZWS}	Write Enable to Output Disable			20	ns
t_{WR}	Write Recovery Time			20	ns

Note 1: Either input voltage limit or input current limit sufficient to protecting inputs.

Note 2: Output current limit required.

Note 3: Typical values are at V_{CC} = 5.0V, t_C = +25°C and maximum loading.

Note 4: Static condition only.

Note 5: Functional testing done at input levels V_{IL} = 0.45V (V_{OL} Max) and V_{IH} = 2.4V (V_{OH} Min).

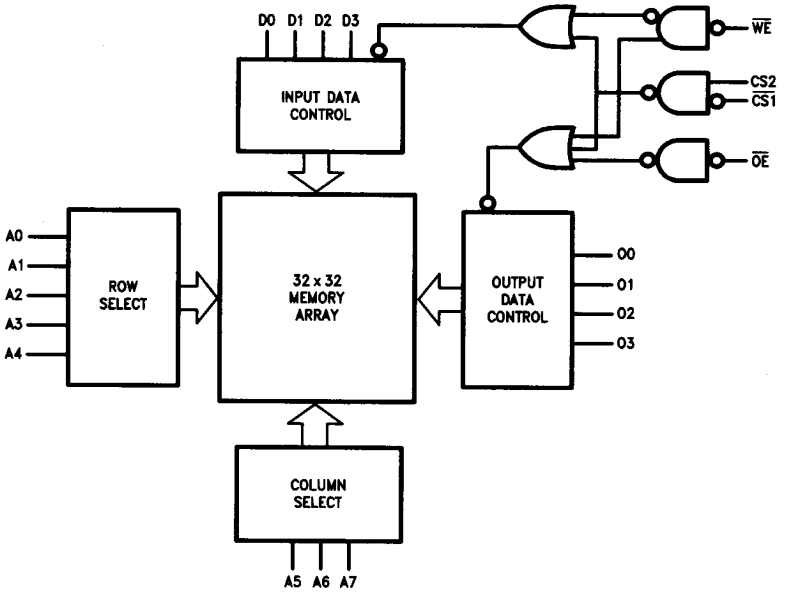
Note 6: AC testing done at input levels V_{IH} = 3V, V_{IL} = 0V.

Note 7: Short circuit to ground not to exceed one second; ground only one output at a time.

Note 8: The maximum address access time is guaranteed to be the worst case bit in the memory using a pseudorandom testing pattern.

Note 9: t_W measured at t_{WSA} = Min. t_{WSA} measured at t_W = Min.

Logic Diagram



TL/D/9996–2

Truth Table

Inputs				Outputs	
$\overline{OE}$	$\overline{CS1}$	CS2	$\overline{WE}$	TRI-STATE	Mode
X	H	X	X	HIGH Z	Not Selected
X	X	L	X	HIGH Z	Not Selected
L	L	H	H	D_{OUT}	READ
X	L	H	L	HIGH Z	WRITE
H	X	X	X	HIGH Z	Output Disabled

H = HIGH Voltage Level 2.4V
L = LOW Voltage Level 0.45V
X = Don't Care HIGH or LOW
HIGH Z = High-Impedance

Functional Description

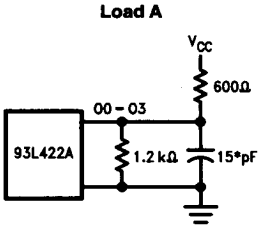
The 93L422A is a fully decoded 1024-bit Random Access Memory organized 256 words by four bits. Word selection is achieved by means of an 8-bit address A0–A7.

Two Chip Select inputs, inverting and non-inverting, are provided for logic flexibility. For larger memories, the fast chip select access time permits the decoding of the chip selects from the address without increasing address access time.

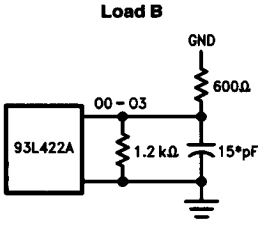
The read and write operations are controlled by the state of the active LOW Write Enable $\overline{WE}$ input. When $\overline{WE}$ is held LOW and the chip is selected, the data at D0–D3 is written into the address location. Since the write function is level-triggered, data must be held stable for at least $t_{WSD\ (Min)}$ plus $t_{W\ (Min)}$ plus $t_{WHD\ (Min)}$ to insure a valid write. To read, $\overline{WE}$ is held high, the chip is selected, and the data is transferred to the outputs (O0–O3).

The 93L422A has TRI-STATE outputs which provide active pull-ups when enabled and high output impedance when disabled. This allows optimization of word expansion in bus organized systems.

Functional Description (Continued)



TL/D/9996–4

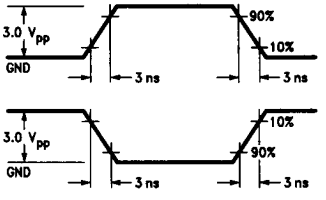


TL/D/9996–5

*Includes jig and probe capacitance

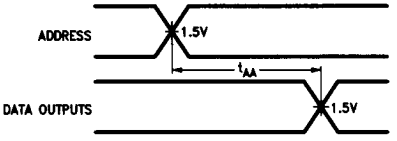
Note: Load A is used for all production testing.

FIGURE 1. AC Test Output Load



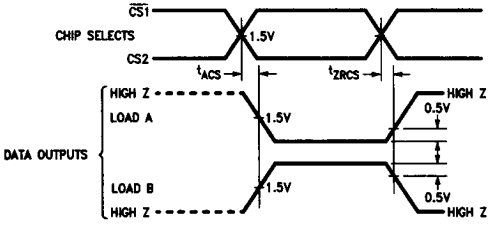
TL/D/9996–6

FIGURE 2. AC Test Input Levels



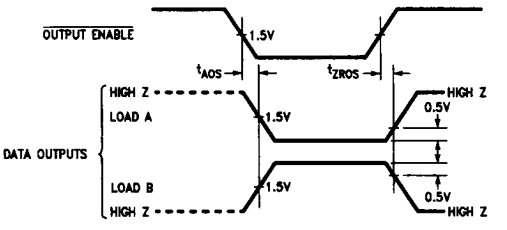
TL/D/9996–7

3a. Read Mode Propagation Delay from Address



TL/D/9996–8

3b. Read Mode Propagation Delay from Chip Select

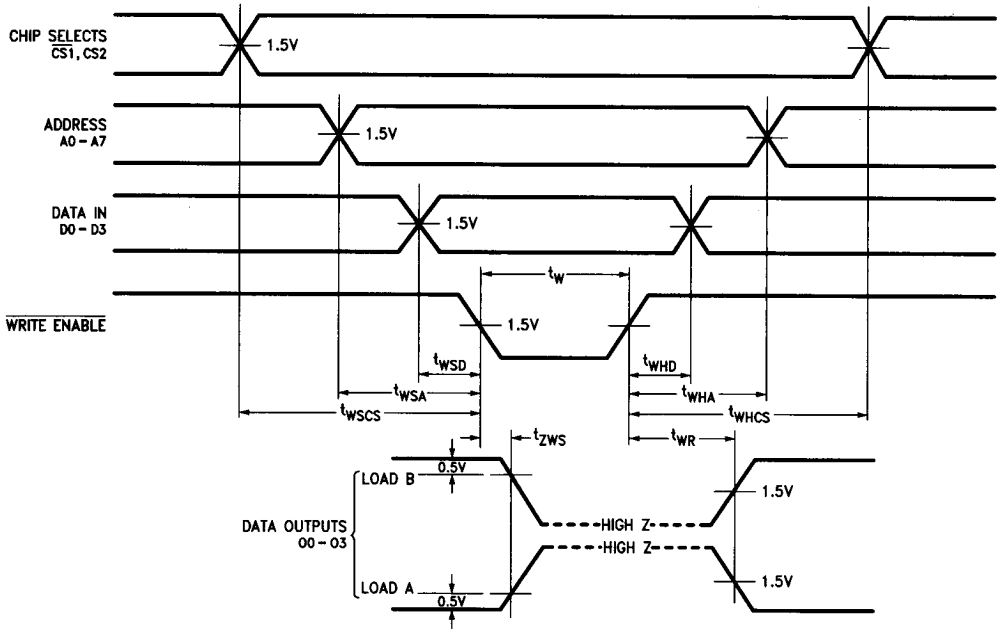


TL/D/9996–9

3c. Read Mode Propagation Delay from Output Enable

FIGURE 3. Read Mode Testing

Functional Description (Continued)



TL/D/9996–10

FIGURE 4. Write Mode Timing

Note 1: Timing Diagram represents one solution which results in an optimium cycle time. Timing may be changed to fit various applications as long as the worst case limits are not violated.

Note 2: Input voltage levels for worst case AC test are 3.0V–0V.

5