BUK653R7-30C

N-channel TrenchMOS intermediate level FET

Rev. 3 — 13 October 2010

Product data sheet

1. Product profile

1.1 General description

Intermediate level gate drive N-channel enhancement mode Field-Effect Transistor (FET) in a plastic package using advanced TrenchMOS technology. This product has been designed and qualified to the appropriate AEC Q101 standard for use in high performance automotive applications.

1.2 Features and benefits

- AEC Q101 compliant
- Suitable for standard and logic level gate drive sources
- Suitable for thermally demanding environments due to 175 °C rating

1.3 Applications

- 12 V Automotive systems
- Electric and electro-hydraulic power steering
- Motors, lamps and solenoid control
- Start-Stop micro-hybrid applications
- Transmission control
- Ultra high performance power switching

1.4 Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Тур	Max	Unit
V_{DS}	drain-source voltage	$T_j \ge 25 \text{ °C}; T_j \le 175 \text{ °C}$		-	-	30	V
I _D	drain current	$V_{GS} = 10 \text{ V}; T_{mb} = 25 \text{ °C};$ see Figure 1	<u>[1]</u>	-	-	100	Α
P _{tot}	total power dissipation	T _{mb} = 25 °C; see <u>Figure 2</u>		-	-	158	W
Static characteristics							
R _{DSon}	drain-source on-state resistance	$V_{GS} = 10 \text{ V}; I_D = 25 \text{ A};$ $T_j = 25 \text{ °C}; \text{ see } \frac{\text{Figure 11}}{\text{ or } 100 \text{ c}}$		-	3.3	3.9	mΩ



Table 1. Quick reference data ...continued

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
Avalanche	ruggedness					
E _{DS(AL)S}	non-repetitive drain-source avalanche energy	$I_D = 100 \text{ A; } V_{sup} \le 30 \text{ V;}$ $R_{GS} = 50 \Omega; V_{GS} = 10 \text{ V;}$ $T_{j(init)} = 25 ^{\circ}\text{C; unclamped}$	-	-	242	mJ
Dynamic cl	naracteristics					
Q_{GD}	gate-drain charge	$I_D = 25 \text{ A}$; $V_{DS} = 24 \text{ V}$; $V_{GS} = 10 \text{ V}$; see Figure 13; see Figure 14	-	20	-	nC

^[1] Continuous current is limited by package.

2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate		_
2	D	drain	mb	D
3	S	source		_G (ET)
mb	D	mounting base; connected to drain	1 2 3	mbb076 S
			SOT78A (TO-220AB)	

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BUK653R7-30C	TO-220AB	plastic single-ended package; heatsink mounted; 1 mounting hole; 3-lead TO-220AB	SOT78A

4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DS}	drain-source voltage	T _j ≥ 25 °C; T _j ≤ 175 °C		-	30	V
V_{GS}	gate-source voltage	DC	<u>[1]</u>	-16	16	V
		Pulsed	[2]	-20	20	V
I _D	drain current	T_{mb} = 25 °C; V_{GS} = 10 V; see <u>Figure 1</u>	[3]	-	100	Α
		$T_{mb} = 100 ^{\circ}\text{C}; V_{GS} = 10 \text{V}; \text{see} \frac{\text{Figure 1}}{}$	[3]	-	100	Α
I _{DM}	peak drain current	T_{mb} = 25 °C; t_p ≤ 10 μs; pulsed; see <u>Figure 3</u>		-	583	Α
P _{tot}	total power dissipation	T _{mb} = 25 °C; see <u>Figure 2</u>		-	158	W
T_{stg}	storage temperature			-55	175	°C
T_j	junction temperature			-55	175	°C
Source-drain	diode					
Is	source current	$T_{mb} = 25 ^{\circ}C$	[3]	-	100	Α
I _{SM}	peak source current	$t_p \le 10 \mu\text{s}; \text{ pulsed}; T_{mb} = 25 ^{\circ}\text{C}$		-	583	Α
Avalanche rug	ggedness					
E _{DS(AL)S}	non-repetitive drain-source avalanche energy	I_D = 100 A; $V_{sup} \le$ 30 V; R_{GS} = 50 Ω ; V_{GS} = 10 V; $T_{j(init)}$ = 25 °C; unclamped		-	242	mJ
$E_{DS(AL)R}$	repetitive drain-source avalanche energy		[4][5][6]	-	-	J

^{[1] -16}V accumulated duration not to exceed 168 hrs

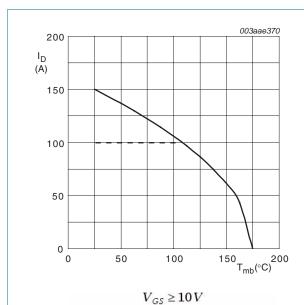
^[2] Accumulated pulse duration not to exceed 5mins.

^[3] Continuous current is limited by package.

^[4] Single-pulse avalanche rating limited by maximum junction temperature of 175 °C.

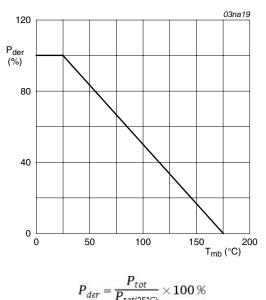
^[5] Repetitive avalanche rating limited by an average junction temperature of 170 °C.

^[6] Refer to application note AN10273 for further information.



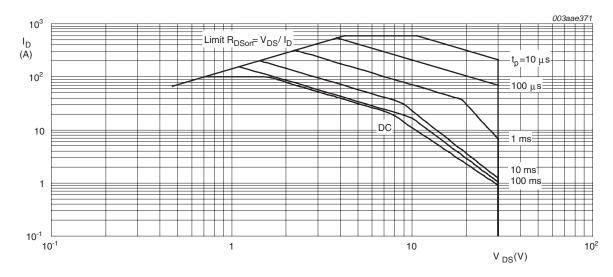
(1) Capped at 100 A due to package.

Continuous drain current as a function of mounting base temperature



$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}C)}} \times 100\%$$

Fig 2. Normalized total power dissipation as a function of mounting base temperature



 $T_{mb} = 25$ °C; I_{DM} is a single pulse

Safe operating area; continuous and peak drain currents as a function of drain-source voltage Fig 3.

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	see Figure 4	-	-	0.95	K/W
R _{th(j-a)}	thermal resistance from junction to ambient	vertical in free air	-	60	-	K/W

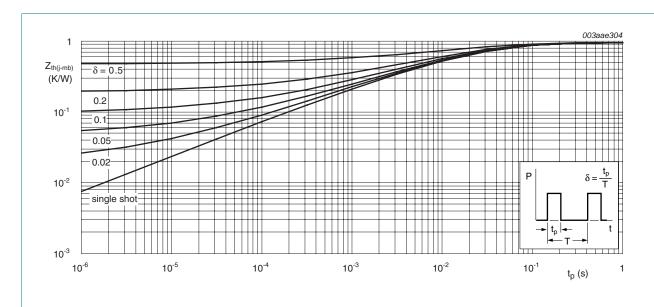


Fig 4. Transient thermal impedance from junction to mounting base as a function of pulse duration

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N-channel TrenchMOS intermediate level FET

6. Characteristics

Table 6. Characteristics

BUK653R7-30C

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
Static cha	aracteristics					
V _{(BR)DSS}	drain-source	$I_D = 250 \mu A; V_{GS} = 0 V; T_j = 25 °C$	30	-	-	V
	breakdown voltage	$I_D = 250 \mu A; V_{GS} = 0 V; T_j = -55 °C$	27	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1 \text{ mA}$; $V_{DS} = V_{GS}$; $T_j = 25 \text{ °C}$; see <u>Figure 9</u> ; see <u>Figure 10</u>	1.8	2.3	2.8	V
		$I_D = 1$ mA; $V_{DS} = V_{GS}$; $T_j = -55$ °C; see Figure 9	-	-	3.3	V
		$I_D = 1$ mA; $V_{DS} = V_{GS}$; $T_j = 175$ °C; see Figure 9	0.8	-	-	V
I _{DSS}	drain leakage current	$V_{DS} = 30 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 175 ^{\circ}\text{C}$	-	-	500	μΑ
		$V_{DS} = 30 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ °C}$	-	0.02	1	μΑ
I _{GSS}	gate leakage current	$V_{DS} = 0 \text{ V}; V_{GS} = 20 \text{ V}; T_j = 25 \text{ °C}$	-	2	100	nA
		$V_{DS} = 0 \text{ V}; V_{GS} = -20 \text{ V}; T_j = 25 \text{ °C}$	-	2	100	nA
R _{DSon}	drain-source on-state resistance	$V_{GS} = 10 \text{ V}; I_D = 25 \text{ A}; T_j = 25 ^{\circ}\text{C};$ see Figure 11	-	3.3	3.9	mΩ
		$V_{GS} = 5 \text{ V}; I_D = 25 \text{ A}; T_j = 25 \text{ °C};$ see Figure 11	-	4.6	5.8	mΩ
		$V_{GS} = 4.5 \text{ V}; I_D = 25 \text{ A}; T_j = 25 ^{\circ}\text{C};$ see Figure 11	-	5.3	7.2	mΩ
		V_{GS} = 10 V; I_D = 25 A; T_j = 175 °C; see Figure 12; see Figure 11	-	-	7.4	mΩ
Dynamic	characteristics					
Dynamic Q _{G(tot)}	characteristics total gate charge	I _D = 25 A; V _{DS} = 24 V; V _{GS} = 10 V; see Figure 13; see Figure 14	-	78	-	nC
			-	78 45	-	nC nC
Q _{G(tot)}		see <u>Figure 13</u> ; see <u>Figure 14</u> $I_D = 25 \text{ A}$; $V_{DS} = 24 \text{ V}$; $V_{GS} = 5 \text{ V}$;			-	
	total gate charge	see Figure 13; see Figure 14 $I_D = 25 \text{ A}$; $V_{DS} = 24 \text{ V}$; $V_{GS} = 5 \text{ V}$; see Figure 13; see Figure 14	-	45		nC
$Q_{G(tot)}$	total gate charge	see Figure 13; see Figure 14 $I_D = 25 \text{ A}; V_{DS} = 24 \text{ V}; V_{GS} = 5 \text{ V};$ see Figure 13; see Figure 14 $I_D = 25 \text{ A}; V_{DS} = 24 \text{ V}; V_{GS} = 10 \text{ V};$	-	45 15	-	nC nC
$Q_{G(tot)}$ Q_{GS} Q_{GD}	total gate charge gate-source charge gate-drain charge	see Figure 13; see Figure 14 $I_D = 25 \text{ A}; V_{DS} = 24 \text{ V}; V_{GS} = 5 \text{ V};$ see Figure 13; see Figure 14 $I_D = 25 \text{ A}; V_{DS} = 24 \text{ V}; V_{GS} = 10 \text{ V};$ see Figure 13; see Figure 14 $V_{GS} = 0 \text{ V}; V_{DS} = 25 \text{ V}; f = 1 \text{ MHz};$ $T_j = 25 \text{ °C}; \text{ see Figure 15}$ $V_{GS} = 0 \text{ V}; V_{DS} = 25 \text{ V}; f = 1 \text{ MHz};$	-	45 15 20	-	nC nC
Q _{G(tot)} Q _{GS} Q _{GD} C _{iss} C _{oss}	gate-source charge gate-drain charge input capacitance	see Figure 13; see Figure 14 $I_D = 25 \text{ A}$; $V_{DS} = 24 \text{ V}$; $V_{GS} = 5 \text{ V}$; see Figure 13; see Figure 14 $I_D = 25 \text{ A}$; $V_{DS} = 24 \text{ V}$; $V_{GS} = 10 \text{ V}$; see Figure 13; see Figure 14 $V_{GS} = 0 \text{ V}$; $V_{DS} = 25 \text{ V}$; $f = 1 \text{ MHz}$; $T_j = 25 \text{ °C}$; see Figure 15	- - - -	45 15 20 3530	- - 4707	nC nC nC
Q _{G(tot)} Q _{GS} Q _{GD} C _{iss} C _{oss} C _{rss}	gate-source charge gate-drain charge input capacitance output capacitance reverse transfer	see Figure 13; see Figure 14 $I_{D} = 25 \text{ A}; V_{DS} = 24 \text{ V}; V_{GS} = 5 \text{ V};$ see Figure 13; see Figure 14 $I_{D} = 25 \text{ A}; V_{DS} = 24 \text{ V}; V_{GS} = 10 \text{ V};$ see Figure 13; see Figure 14 $V_{GS} = 0 \text{ V}; V_{DS} = 25 \text{ V}; f = 1 \text{ MHz};$ $T_{j} = 25 \text{ °C}; \text{ see Figure 15}$ $V_{GS} = 0 \text{ V}; V_{DS} = 25 \text{ V}; f = 1 \text{ MHz};$ $T_{j} = 25 \text{ °C}; \text{ see Figure 14}$ $V_{GS} = 0 \text{ V}; V_{DS} = 25 \text{ V}; f = 1 \text{ MHz};$	- - - -	45 15 20 3530 623	- - 4707 748	nC nC nC pF
Q _G (tot) Q _{GS} Q _{GD} C _{iss} C _{oss} C _{rss}	gate-source charge gate-drain charge input capacitance output capacitance reverse transfer capacitance	see Figure 13; see Figure 14 $I_{D} = 25 \text{ A}; V_{DS} = 24 \text{ V}; V_{GS} = 5 \text{ V};$ see Figure 13; see Figure 14 $I_{D} = 25 \text{ A}; V_{DS} = 24 \text{ V}; V_{GS} = 10 \text{ V};$ see Figure 13; see Figure 14 $V_{GS} = 0 \text{ V}; V_{DS} = 25 \text{ V}; f = 1 \text{ MHz};$ $T_{j} = 25 \text{ °C}; \text{ see Figure 15}$ $V_{GS} = 0 \text{ V}; V_{DS} = 25 \text{ V}; f = 1 \text{ MHz};$ $T_{j} = 25 \text{ °C}; \text{ see Figure 14}$ $V_{GS} = 0 \text{ V}; V_{DS} = 25 \text{ V}; f = 1 \text{ MHz};$ $T_{j} = 25 \text{ °C}$	- - - -	45 15 20 3530 623 381	- - 4707 748 522	nC nC nC pF
QG(tot) QGS QGD Ciss Coss td(on)	gate-source charge gate-drain charge input capacitance output capacitance reverse transfer capacitance turn-on delay time	see Figure 13; see Figure 14 $I_{D} = 25 \text{ A; } V_{DS} = 24 \text{ V; } V_{GS} = 5 \text{ V; }$ see Figure 13; see Figure 14 $I_{D} = 25 \text{ A; } V_{DS} = 24 \text{ V; } V_{GS} = 10 \text{ V; }$ see Figure 13; see Figure 14 $V_{GS} = 0 \text{ V; } V_{DS} = 25 \text{ V; } f = 1 \text{ MHz; }$ $T_{j} = 25 \text{ °C; see Figure 15}$ $V_{GS} = 0 \text{ V; } V_{DS} = 25 \text{ V; } f = 1 \text{ MHz; }$ $T_{j} = 25 \text{ °C; see Figure 14}$ $V_{GS} = 0 \text{ V; } V_{DS} = 25 \text{ V; } f = 1 \text{ MHz; }$ $T_{j} = 25 \text{ °C}$ $V_{DS} = 25 \text{ V; } R_{L} = 1 \text{ \Omega; } V_{GS} = 10 \text{ V; }$	- - - -	45 15 20 3530 623 381 19	- - 4707 748 522	nC nC nC pF pF
$Q_{G(tot)}$ Q_{GS} Q_{GD} C_{iss}	gate-source charge gate-drain charge input capacitance output capacitance reverse transfer capacitance turn-on delay time rise time	see Figure 13; see Figure 14 $I_{D} = 25 \text{ A; } V_{DS} = 24 \text{ V; } V_{GS} = 5 \text{ V; }$ see Figure 13; see Figure 14 $I_{D} = 25 \text{ A; } V_{DS} = 24 \text{ V; } V_{GS} = 10 \text{ V; }$ see Figure 13; see Figure 14 $V_{GS} = 0 \text{ V; } V_{DS} = 25 \text{ V; } f = 1 \text{ MHz; }$ $T_{j} = 25 \text{ °C; see Figure 15}$ $V_{GS} = 0 \text{ V; } V_{DS} = 25 \text{ V; } f = 1 \text{ MHz; }$ $T_{j} = 25 \text{ °C; see Figure 14}$ $V_{GS} = 0 \text{ V; } V_{DS} = 25 \text{ V; } f = 1 \text{ MHz; }$ $T_{j} = 25 \text{ °C}$ $V_{DS} = 25 \text{ V; } R_{L} = 1 \text{ \Omega; } V_{GS} = 10 \text{ V; }$	- - - -	45 15 20 3530 623 381 19 54	- 4707 748 522 -	nC nC nC pF pF ns
QG(tot) QGS QGD Ciss Crss td(on) tr	gate-source charge gate-drain charge input capacitance output capacitance reverse transfer capacitance turn-on delay time rise time turn-off delay time	see Figure 13; see Figure 14 $I_{D} = 25 \text{ A; } V_{DS} = 24 \text{ V; } V_{GS} = 5 \text{ V; }$ see Figure 13; see Figure 14 $I_{D} = 25 \text{ A; } V_{DS} = 24 \text{ V; } V_{GS} = 10 \text{ V; }$ see Figure 13; see Figure 14 $V_{GS} = 0 \text{ V; } V_{DS} = 25 \text{ V; } f = 1 \text{ MHz; }$ $T_{j} = 25 \text{ °C; see Figure 15}$ $V_{GS} = 0 \text{ V; } V_{DS} = 25 \text{ V; } f = 1 \text{ MHz; }$ $T_{j} = 25 \text{ °C; see Figure 14}$ $V_{GS} = 0 \text{ V; } V_{DS} = 25 \text{ V; } f = 1 \text{ MHz; }$ $T_{j} = 25 \text{ °C}$ $V_{DS} = 25 \text{ V; } R_{L} = 1 \text{ \Omega; } V_{GS} = 10 \text{ V; }$	- - - - -	45 15 20 3530 623 381 19 54 135	- 4707 748 522 - -	nC nC pF pF ns ns ns

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Table 6. Characteristics ...continued

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
Source-drain diode						
V _{SD}	source-drain voltage	$I_S = 25 \text{ A}; V_{GS} = 0 \text{ V}; T_j = 25 ^{\circ}\text{C};$ see <u>Figure 16</u>	-	0.8	1.2	V
t _{rr}	reverse recovery time	$I_S = 20 \text{ A}; dI_S/dt = -100 \text{ A/}\mu\text{s}; V_{GS} = 0 \text{ V};$	-	46	-	ns
Q _r	recovered charge	$V_{DS} = 25 \text{ V}$	-	57	-	nC

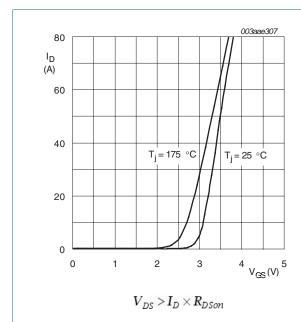


Fig 5. Transfer characteristics: drain current as a function of gate-source voltage; typical values

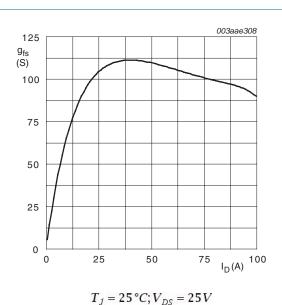


Fig 6. Forward transconductance as a function of drain current; typical values

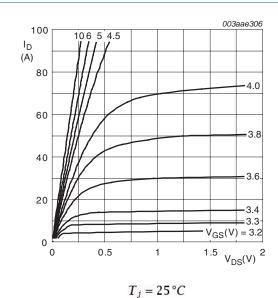


Fig 7. Output characteristics: drain current as a function of drain-source voltage; typical values

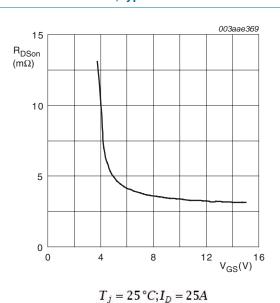
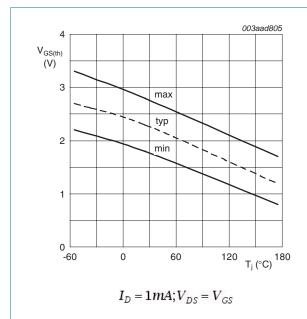


Fig 8. Drain-source on-state resistance as a function of gate-source voltage; typical values.

BUK653R7-30C

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Gate-source threshold voltage as a function of Fig 9. junction temperature

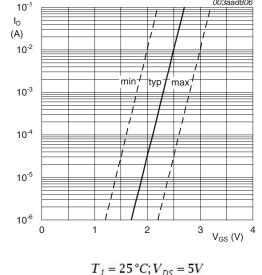


Fig 10. Sub-threshold drain current as a function of gate-source voltage

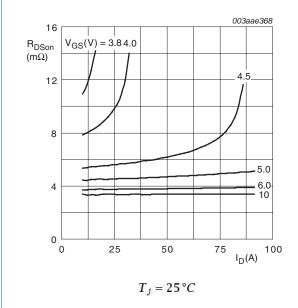


Fig 11. Drain-source on-state resistance as a function of drain current; typical values

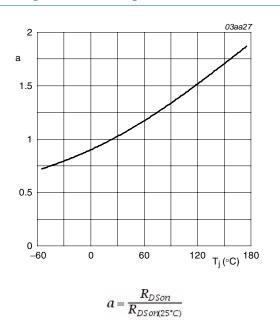
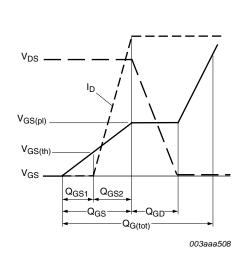
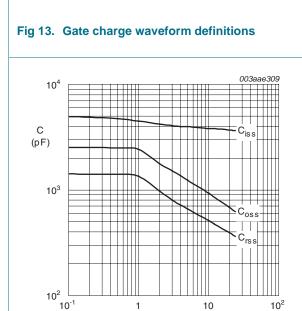


Fig 12. Normalized drain-source on-state resistance factor as a function of junction temperature

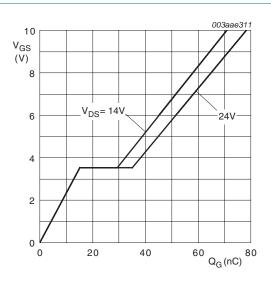




 $V_{GS} = 0V; f = 1MHz$

Fig 15. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

 $V_{DS}(V)$



 $T_j = 25 \,^{\circ}C; I_D = 25A$

Fig 14. Gate-source voltage as a function of gate charge; typical values

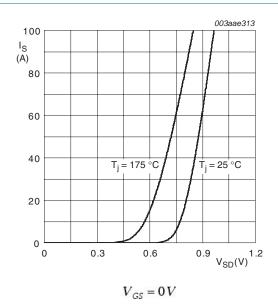


Fig 16. Source current as a function of source-drain voltage; typical values

7. Package outline

Plastic single-ended package; heatsink mounted; 1 mounting hole; 3-lead TO-220AB

SOT78A

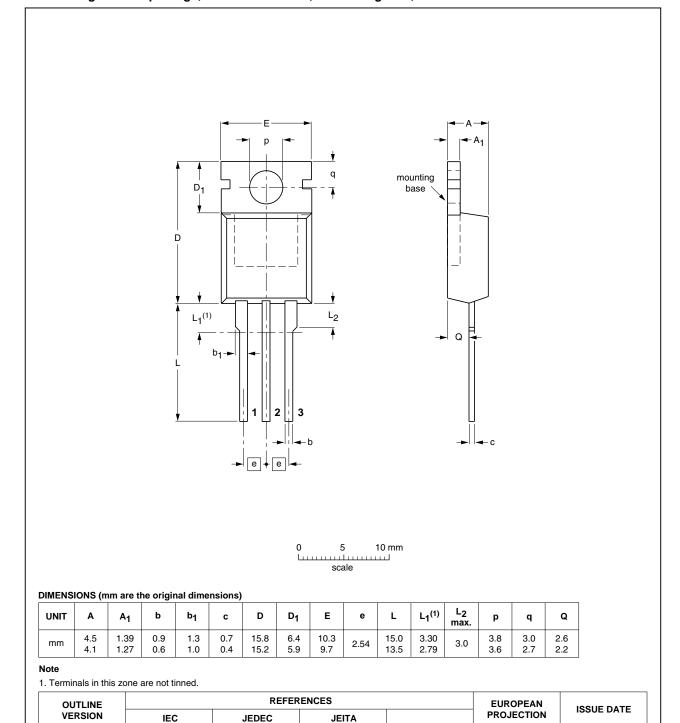


Fig 17. Package outline SOT78A (TO-220AB)

BUK653R7-30C

SC-46

3-lead TO-220AB

03-01-22

05-03-14

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SOT78A

8. Revision history

Table 7. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BUK653R7-30C v.3	20101013	Product data sheet	-	BUK653R7-30C v.2
Modifications:	 Status change 	ed from objective to product.		
BUK653R7-30C v.2	20100705	Objective data sheet	-	BUK653R7-30C v.1

9. Legal information

9.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
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10. Contact information

For more information, please visit: http://www.nxp.com

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