R1LA1616R Series

16Mb superSRAM (1M wordx16bit)

REJ03C0100-0002Z
Rev.0.02
2003.10.24

Description

The R1LA1616R Series is a family of low voltage 16-Mbit static RAMs organized as 1048576-words by 16-bit, fabricated by Renesas's high-performance 0.15um CMOS and TFT technologies.

The R1LA1616R Series is suitable for memory applications where a simple interfacing , battery operating and battery backup are the important design objectives.

The R1LA1616R Series is packaged in a 52pin micro thin small outline mount device[µ TSOP / 10.79mm x 10.49mm with the pin-pitch of 0.4mm] or a 48balls fine pitch ball grid array [f-BGA / 7.5mmx8.5mm with the ball-pitch of 0.75mm and 6x8 array] . It gives the best solution for a compaction of mounting area as well as flexibility of wiring pattern of printed circuit boards.

Features

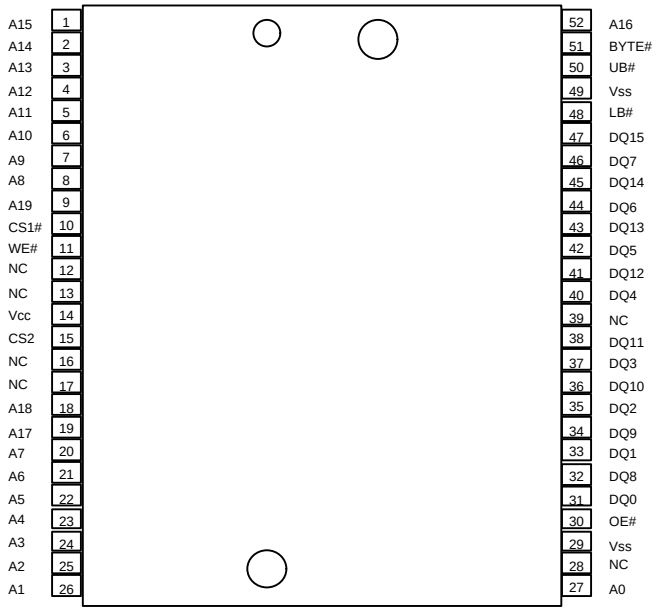
- Single 1.65-2.3V power supply
- Small stand-by current:3µA (1.8V, typ.)
- Smaller stand-by current by "Data retention mode"(“CS2"='L') : 1µA (1.8V, typ.)
- Data retention supply voltage =1.5V
- No clocks, No refresh
- Easy memory expansion by CS1#, CS2, LB# and UB#
- Common Data I/O
- Three-state outputs: OR-tie capability
- OE# prevents data contention on the I/O bus
- Process technology: 0.15um CMOS

Ordering Information

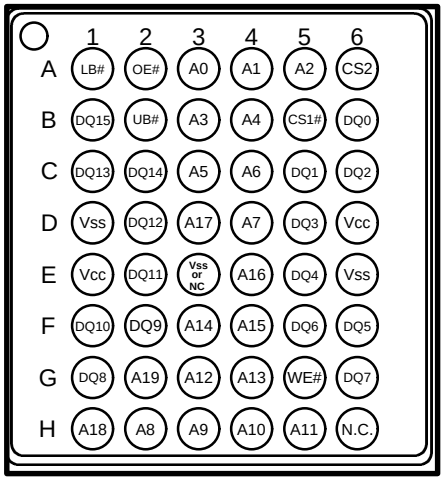
Type No.	Access time	Package
R1LA1616RSD-7SI	70 ns	350-mil 52-pin plastic µ - TSOP(II) (normal-bend type) (52PTG)
R1LA1616RSD-8SI	85 ns	
R1LA1616RBG-7SI	70 ns	7.5mmx8.5mm f-BGA 0.75mm pitch 48ball
R1LA1616RBG-8SI	85 ns	

Pin Arrangement

52-pin µ TSOP



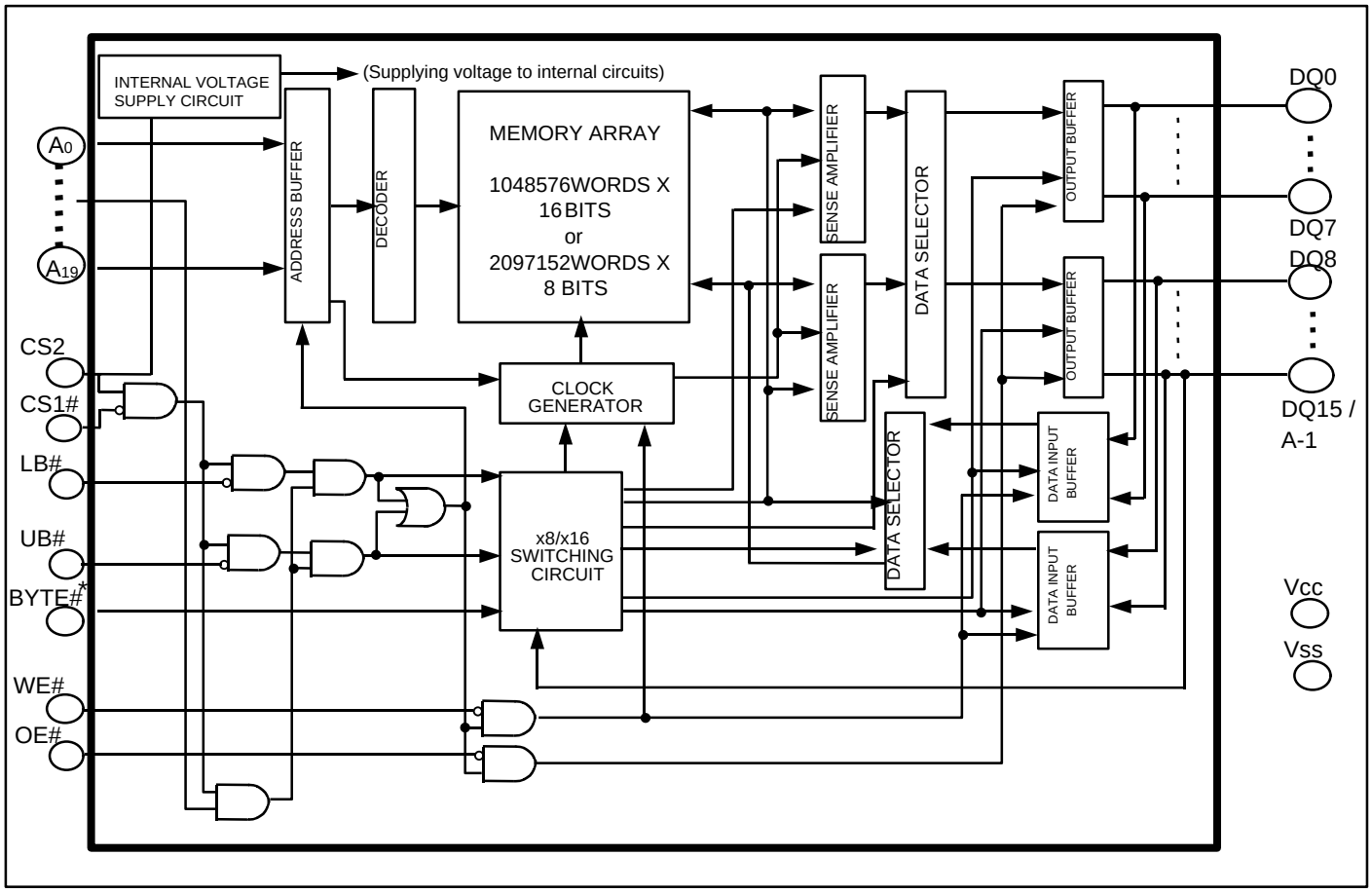
48-pin fBGA



Pin Description

Pin name	Function
A0 to A19	Address input
DQ 0 to DQ15	Data input/output
CS1# &CS2	Chip select
WE#	Write enable
OE#	Output enable
LB#	Lower byte select
UB#	Upper byte select
Vcc	Power supply
Vss	Ground
BYTE#	Byte control mode enable input
NC	Non connection

Block Diagram



Note, BYTE# pin supported by only TSOP type.

Operating Table

CS1#	CS2*3	BYTE#*2	LB#	UB#	WE#	OE#	DQ0~7	DQ8~14	DQ15	Operation
H	H	X	X	X	X	X	High-Z	High-Z	High-Z	Stand-by
X	L	X	X	X	X	X	High-Z	High-Z	High-Z	Data retention
X	H	X	H	H	X	X	High-Z	High-Z	High-Z	Stand-by
L	H	H	L	H	L	X	Din	High-Z	High-Z	Write in lower byte
L	H	H	L	H	H	L	Dout	High-Z	High-Z	Read from lower byte
L	H	H	L	H	H	H	High-Z	High-Z	High-Z	Output disable
L	H	H	H	L	L	X	High-Z	Din	Din	Write in upper byte
L	H	H	H	L	H	L	High-Z	Dout	Dout	Read from upper byte
L	H	H	H	L	H	H	High-Z	High-Z	High-Z	Output disable
L	H	H	L	L	L	X	Din	Din	Din	Write
L	H	H	L	L	H	L	Dout	Dout	Dout	Read
L	H	H	L	L	H	H	High-Z	High-Z	High-Z	Output disable
L	H	L	L	L	L	X	Din	High-Z	A-1	Write
L	H	L	L	L	H	L	Dout	High-Z	A-1	Read
L	H	L	L	L	H	H	High-Z	High-Z	A-1	Output disable

Note 1,H:VIH L:VIL X: VIH or VIL
2, BYTE# pin supported by only TSOP type. When apply BYTE# =“L” ,please assign LB#=UB#=“L”.

*3 Notification about a new function of CS2 signal

R1LA1616R Series use CS2 signal to control the internal voltage for as 'Data retention mode'. In case of conventional SRAM products, both CS1# and CS2 signals are used as control signals for device operation of active and stand-by modes. In terms of R1LA1616R Series, CS1# is an ordinary function that controls device operation, but CS2 function is to make a switch device status between 'Stand-by mode' and 'Data retention mode', based on the input level of CS2 signal. In the concrete, when setting CS2 at a high level, a device status is changed from 'Data retention mode' to 'Stand-by mode'. And when setting CS2 at a low level, it's changed from 'Stand-by mode' to 'Data retention mode'. The latter is a new function. During 'Data retention mode' with CS2='L', the reduction of current consumption is achieved by turning off the internal voltage supply except memory cell array. Therefore in case of using with CS2 signal as for 'back up control with battery' , it will be realized the most suitable system.
With regard to the detailed specifications for CS2 signal, please refer to the item of "Timing diagram" in p.11~p.14 and that of "Data retention characteristics" in p.15.

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Power supply voltage relative to Vss	Vcc	-0.5 to +2.7	V
Terminal voltage on any pin relation toVss	V_T	-0.5*1 to Vcc+0.3*2	V
Power dissipation	P_T	0.7	W
Operation temperature	Topr	-40 to + 85	ºC
Storage temperature range	Tstg	-65 to + 150	ºC
Storage temperature range under bias	Tbias	-40 to + 85	ºC

Note 1: -1.0V in case of AC (Pulse width ≤ 30ns)
2:Maximum voltage is +2.7V

DC Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	Vcc	1.65	1.80	2.30	V	
	Vss	0	0	0	V	
Input high voltage	V_{IH}	0.7 x Vcc	——	Vcc+0.2	V	
Input low voltage	V_{IL}	-0.2	——	0.4	V	1
Ambient temperature range	Ta	-40	——	85	ºC	

Note 1 –1.0V in case of AC (Pulse width ≤ 30ns)

DC Characteristics

Parameter	Symbol	Min	Typ*1	Max	Unit	Test conditions*2	
Input leakage current	$\|I_{LI}\|$	——	——	1	µA	Vin=Vss to Vcc	
Output leakage current	$\|I_{LO}\|$	——	——	1	µA	CS1# =V_{IH} or CS2=V_{IL} or OE# = V_{IH} or WE# =V_{IL} or LB# =UB# =V_{IH},$V_{I/O}$=Vss to Vcc	
Operating current	Icc	——	1.5	3	mA	CS1#=V_{IL} , CS2=V_{IH} Others = V_{IH} / V_{IL} $I_{I/O}$ = 0 mA	
Average operating current	I_{CC1}	——	20	40	mA	Min. cycle, duty =100% $I_{I/O}$ = 0 mA,CS1# =V_{IL}, CS2=V_{IH} Others = V_{IH} / V_{IL}	
	I_{CC2}	——	1.5	8	mA	Cycle time = 1µs,duty=100% $I_{I/O}$ = 0 mA,CS1# =V_{IL}, CS2=V_{IH} Others = V_{IH} / V_{IL}	
Standby current	I_{SB}	——	0.1	0.3	mA	CS1#=CS2=V_{IH}	
Standby current	I_{SB1}	——	3	5	µA	~+25ºC	0V≤Vin CS2 ≥ Vcc-0.2V (1)CS1# ≥ Vcc-0.2V or (2)LB# = UB# ≥ Vcc-0.2V CS1# ≤ 0.2V
			5	10	µA	~+40ºC	
				20	µA	~+70ºC	
				40	µA	~+85ºC	
Output hige voltage	V_{OH}	1.3	——	——	V	I_{OH} = -0.1mA	
Output Low voltage	V_{OL}	——	——	0.2	V	I_{OL} = 0.1mA	

Note 1: Typical parameter indicates the value for the center of distribution at 1.8V (Ta=25ºC), and not 100% tested.
2: BYTE# pin supported by only TSOP type.
BYTE# ≥ Vcc-0.2V or BYTE# ≤ 0.2V

Capacitance

(Ta=+25ºC, f=1MHz)

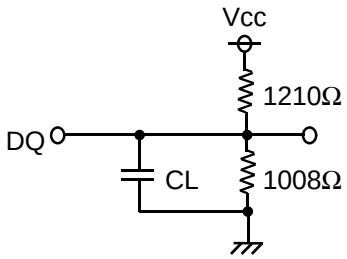
Parameter	Symbol	Min	Typ	Max	Unit	Test conditions	Note
Input capacitance	C in	——	——	10	pF	V in =0V	1
Input / output capacitance	C I/O	——	——	10	pF	V I/O=0V	1

Note 1: This parameter is sampled and not 100% tested.

AC Characteristics

Test Conditions (Vcc=1.65V~2.3V , Ta = - 40~+85 ºC)

- Input pulse levels : VIL= 0.2V, VIH=Vcc - 0.2V
- Input rise and fall time : 5ns
- Input and output timing reference levels : 0.9V
- Output load : See figures (Including scope and jig)



CL=30pF

CL=5FpF (for t_{CLZ}, t_{BLZ}, t_{OLZ}, t_{CHZ}, t_{CLZ}, t_{BHZ}, t_{OHZ}, t_{OWZ}, t_{OHZ}, t_{WHZ})

Read Cycle

Parameter	Symbol	R1LA1616R**-7SI		R1LA1616R**-8SI		Unit	Notes
		Min	Max	Min	Max		
Read cycle time	t_{RC}	70	——	85	——	ns	
Address access time	t_{AA}	——	70	——	85	ns	
Chip select access time	t_{ACS}	——	70	——	85	ns	
Output enable to output valid	t_{OE}	——	35	——	45	ns	
Output hold from address change	t_{OH}	10	——	10	——	ns	
LB#,UB# access time	t_{BA}	——	70	——	85	ns	
Chip select to output in low-Z	t_{CLZ}	10	——	10	——	ns	2,3
LB#,UB# enable to low-Z	t_{BLZ}	5	——	5	——	ns	2,3
Output enable to output in low-Z	t_{OLZ}	5	——	5	——	ns	2,3
Chip deselect to output in high-Z	t_{CHZ}	0	25	0	30	ns	1,2,3
LB#,UB# disable to high-Z	t_{BHZ}	0	25	0	30	ns	1,2,3
Output disable to output in high-Z	t_{OHZ}	0	25	0	30	ns	1,2,3

Write Cycle

Parameter	Symbol	R1LA1616R**-7SI		R1LA1616R**-8SI		Unit	Notes
		Min	Max	Min	Max		
Write cycle time	t_{WC}	70	——	85	——	ns	
Address valid to end of write	t_{AW}	65		70		ns	
Chip selection to end of write	t_{CW}	65		70		ns	5
Write pulse width	t_{WP}	55		60		ns	4
LB#,UB# valid to end of write	t_{BW}	65		70		ns	
Address setup time	t_{AS}	0		0		ns	6
Write recovery time	t_{WR}	0	——	0	——	ns	7
Data to write time overlap	t_{DW}	35	——	40	——	ns	
Data hold from write time	t_{DH}	0	——	0	——	ns	
Output active from end of write	t_{OW}	5		5		ns	2
Output disable to output in high -Z	t_{OHZ}	0	25	0	30	ns	1,2
Write to output in high-Z	t_{WHZ}	0	25	0	30	ns	1,2

Note1. t_{CHZ}, t_{OHZ}, t_{WHZ} and t_{BHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referred to output voltage levels.

2.This parameter is sampled and not 100% tested.

3.AT any given temperature and voltage condition, t_{HZ} max is less than t_{HZ} min both for a given device and form device to device.

4. A write occurs during the overlap of a low CS1#, a high CS2, a low WE# and a low LB# or a low UB#. A write begins at the latest transition among CS1# going low, WE# going low and LB# going low or UB# going low . A write ends at the earliest transition among CS1# going high, WE# going high and LB# going high or UB# going high. t_{WP} is measured from the beginning of write to the end of write.

5. t_{CW} is measured from the later of CS1# going low to end of write.

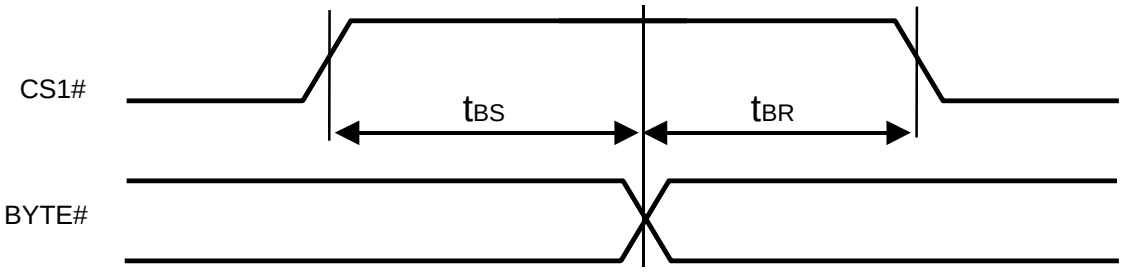
6. t_{AS} is measured the address valid to the beginning of write.

7. t_{WR} is measured from the earliest of CS1# or WE# going high to the end of write cycle.

Byte Control

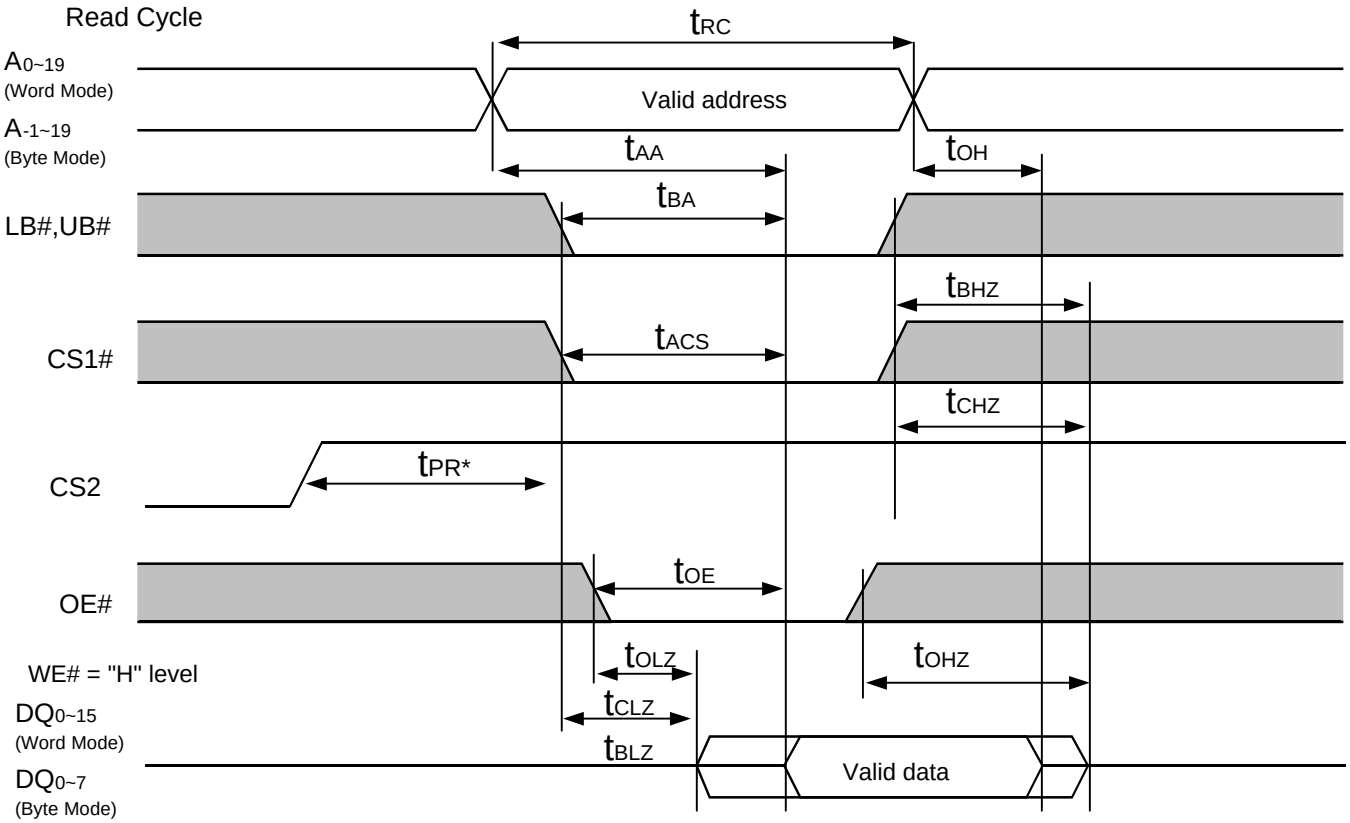
Parameter	Symbol	R1LA1616R**-7SI		R1LA1616R**-8SI		Unit	Notes
		Min	Max	Min	Max		
Byte setup time	t_{BS}	5	——	5	——	ms	
Byte recovery time	t_{BR}	5	——	5	——	ms	

BYTE# Timing Waveform



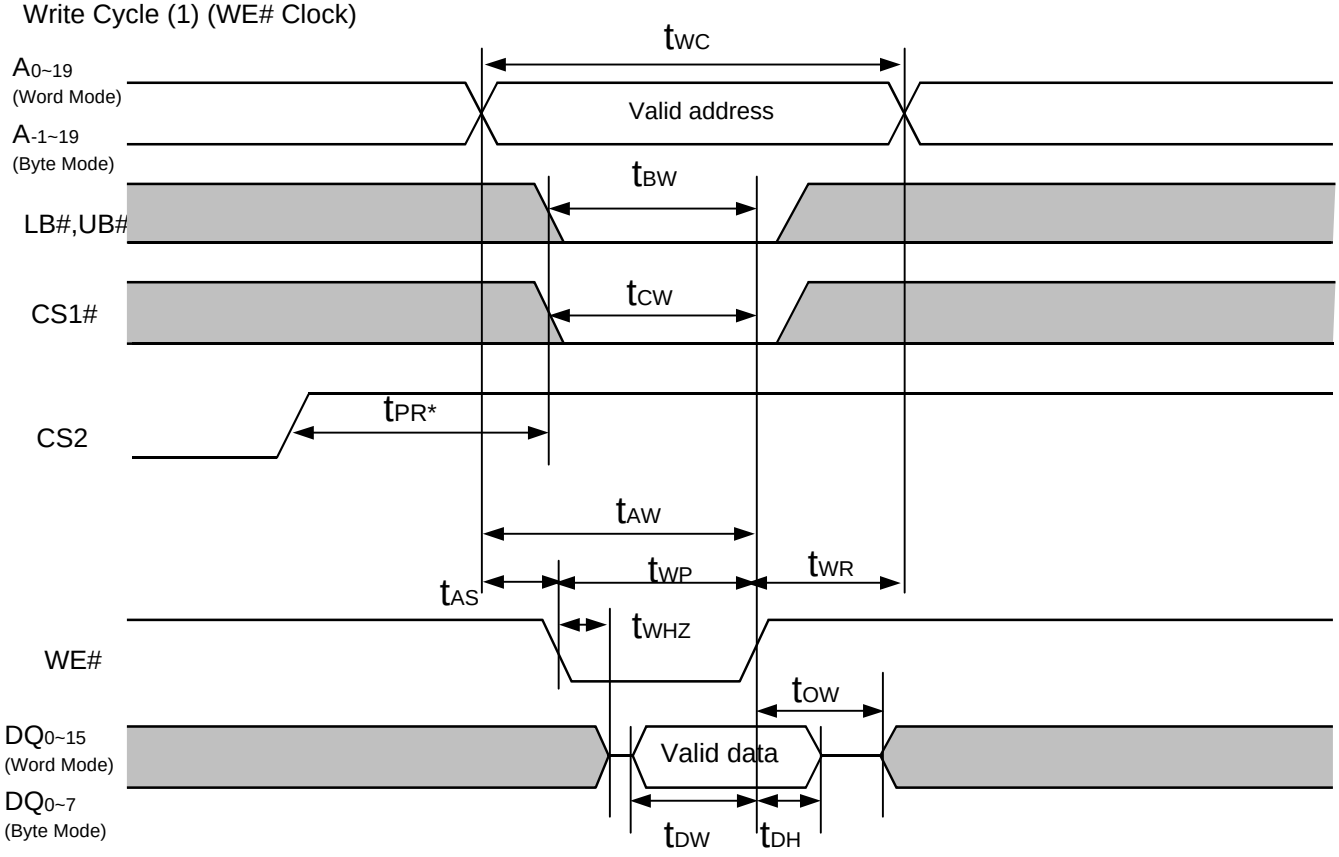
Timing Waveform

Read Cycle



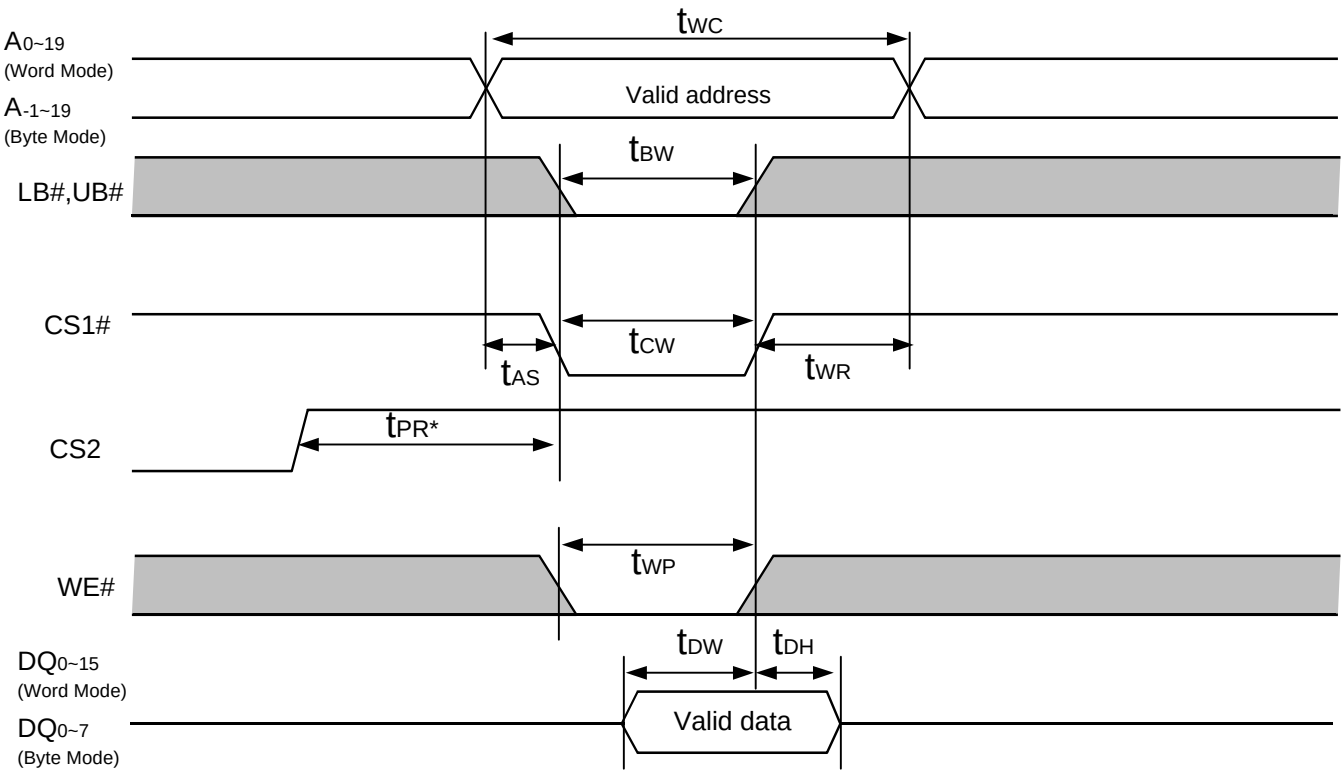
Note , About t_{PR}, See Data Retention Characteristics p.15

Write Cycle (1) (WE# Clock)



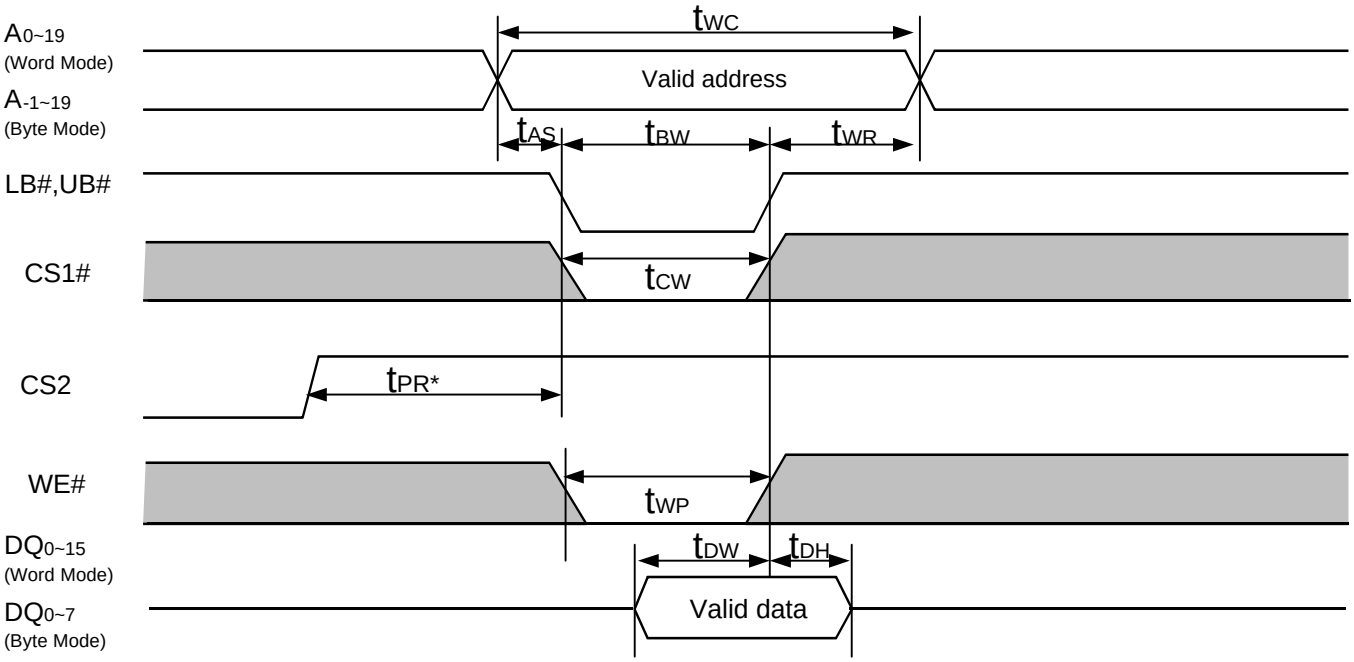
Note , About t_{PR}, See Data Retention Characteristics p.15

Write Cycle (2) (CS1# ,CS2 Clock, OE#=V_{IH})



Note , About t_{PR}, See Data Retention Characteristics p.15

Write Cycle (3) (LB#,UB# Clock, OE#=V_{IH})



Note , About t_{PR}, See Data Retention Characteristics p.15

Data Retention Characteristics *1

(Ta= -40~+85ºC)

Parameter	Symbol	Min	Typ*2	Max	Unit	Test conditions*3,4	
Vcc for data retention	V_{DR}	1.5V	——	2.3V	V	V in ≥ 0V 0V≤CS2≤0.2V	
Data retention current	I_{CCDR}	——	1.0	3.0	µA	~+25ºC	Vcc=1.8V V in ≥ 0V CS2≤0.2V
		——	3.0	8.0	µA	~+40ºC	
		——	——	17	µA	~+70ºC	
		——	——	37	µA	~+85ºC	
Chip deselect to data retention time	t_{CDR}	0	——	——	ns	See retention waveform	
Operation recovery time	t_R	5	——	——	ms		
Power off setup time	t_{PS}	0	——	——	ns	See retention waveform	
Power supply recovery time	t_{PR}	200	——	——	µs		

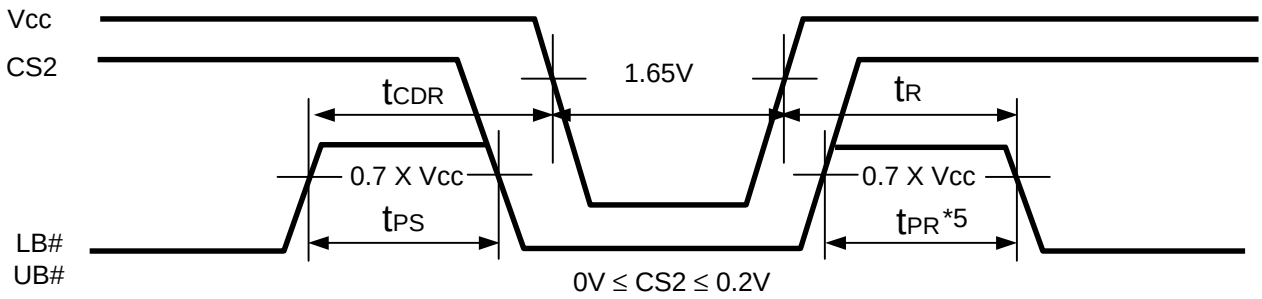
Note 1. Different from conventional SRAM products, this is the reduction mode of Data retention current when CS2 is low. During CS2 low , Internal voltage supply circuit is turned off except memory cell array.

2.Typical parameter of I_{CCDR} indicates the value for the center of distribution at Vcc=1.8V and not 100% tested.

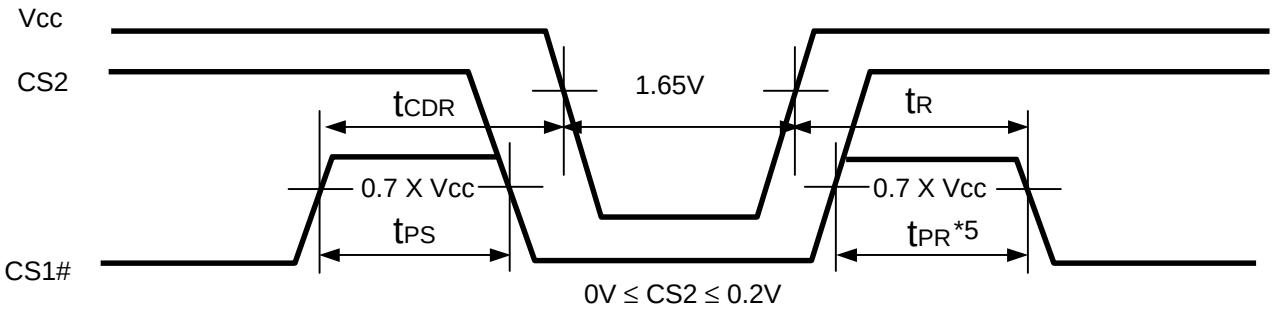
3. BYTE# pin supported by TSOP type. BYTE# ≥ Vcc-0.2V or BYTE# ≤ 0.2V

4. Also CS2 controls address buffer, WE# buffer ,CS1# buffer ,OE# buffer ,LB# ,UB# buffer and Din buffer . In the data retention mode (0V ≤ CS2 ≤ 0.2V) , Vin levels (address, WE# ,OE#,CS1#,LB#,UB#,I/O) can be in the high impedance state.

Data Retention timing Waveform (1) (LB#,UB# Controlled)



Data Retention timing Waveform (2) (CS1# Controlled)



Note 5. On the UB#,LB# control mode or the CS1# control mode ,when recovering from the Data retention mode , the level of UB# and LB# or CS1# during t_{PR} period must be fixed 0.7V x Vcc ~ Vcc.

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REVISION HISTORY	R1LA1616R Series Data Sheet

Rev.	Date	Description	
		Page	Summary
0.01	Jul. 04, 2003	—	First edition issued
0.02	Oct. 24, 2003	9	Revise Removed “CS2 signal operation” from Note 4,5 & 7 as follows. Note 4. Former A write occurs during the overlap of a low CS1#, a high CS2, a low WE# and a low LB# or a low UB#.A write begins at the latest transition among CS1# going low, CS2 going high , WE# going low and LB# going low or UB# going low . A write ends at the earliest transition among CS1# going high ,CS2 going low, WE# going high and LB# going high or UB# going high. tWP is measured from the beginning of write to the end of write. Note 4. Revision A write occurs during the overlap of a low CS1#, a high CS2, a low WE# and a low LB# or a low UB#.A write begins at the latest transition among CS1# going low, WE# going low and LB# going low or UB# going low . A write ends at the earliest transition among CS1# going high , WE# going high and LB# going high or UB# going high. tWP is measured from the beginning of write to the end of write. Note 5. Former tCW is measured from the later of CS1# going low or CS2 going high to end of write Note 5. Revision tCW is measured from the later of CS1# going low to end of write. Note 7. Former tWR is measured from the earliest of CS1# or WE# going high or CS2 going low to the end of write cycle. Note 7. Revision tWR is measured from the earliest of CS1# or WE# going high to the end of write cycle.
		5	In “Note 2” , Add instructions “When apply BYTE# =“L” ,please assign LB#=UB#=“L”.”
		3	Change Pin name “I/O 0 to I/O15” to “DQ 0 to DQ15” in “Pin Description”.