High Reliability Series Serial EEPROM Series

WL-CSP EEPROMs family
SPI BUS

BR25S128GUZ-W

No.10001JAT06

●Description

BR25S128GUZ-W is a 16K×8bit serial EEPROM of SPI BUS interface method.

●Features

1) High speed clock action up to 10MHz (Max.)
2) Wait function by HOLDB terminal
3) Part or whole of memory arrays settable as read only memory area by program
4) 1.7～5.5V single power source action most suitable for battery use
5) 64Byte page write mode useful for initial value write at factory shipment
6) For SPI bus interface (CPOL, CPHA)=(0, 0), (1, 1)
7) Auto erase and auto end function at data rewrite
8) Low current consumption
   - At write action (5.0V) : 1.5mA (Typ.)
   - At read action (5.0V) : 1.0mA (Typ.)
   - At standby action (5.0V) : 0.1μA (Typ.)
9) Address auto increment function at read action
10) Write mistake prevention function
    - Write prohibition at power on
    - Write prohibition by command code (WRDI)
    - Write prohibition by WPB pin
    - Write prohibition block setting by status registers (BP1, BP0)
    - Write mistake prevention function at low voltage
11) VCSP35L2 Package
12) Data at shipment Memory array: FFh, status register WPEN, BP1, BP0 : 0
13) Data kept for 40 years
14) Data rewrite up to 1,000,000 times

●Absolute maximum ratings (Ta=25°C)

Parameter	Symbol	Limits		Unit
Impressed voltage	Vcc	-0.3～+6.5		V
Permissible dissipation	Pd	VCSP35L2	220 ※1	mW
Storage temperature range	Tstg	-65～+125		℃
Operating temperature range	Topr	-40～+85		℃
Terminal voltage	—	-0.3～Vcc+0.3 ※2		V

※1 Degradation is done at 4.5mW, for operation above 25℃.
※2 The Max value of Terminal Voltage is not over 6.5V.

●Memory cell characteristics (Ta=25°C , Vcc=1.7V～5.5V)

Parameter	Limits			Unit
	Min.	Typ.	Max.	
Number of data rewrite times ※1	1,000,000	—	—	Time
Data hold years ※1	40	—	—	Year

※1 Not 100% TESTED.

●Recommended action conditions

Parameter	Symbol	Limits	Unit
Power source voltage	Vcc	1.7～5.5	V
Input voltage	V_{IN}	0～Vcc	

●Input / output capacity (Ta=25°C, frequency=5MHz)

Parameter	Symbol	Conditions	Min.	Max.	Unit
Input capacity ※1	C_{IN}	V_{IN}=GND	—	8	pF
Output capacity ※1	C_{OUT}	V_{OUT}=GND	—	8	

※1 Not 100% TESTED.

●Electrical characteristics (Unless otherwise specified, Ta=-40～+85°C, Vcc=1.7～5.5V)

Parameter	Symbol	Limits			Unit	Conditions
		Min.	Typ.	Max.		
“H” Input Voltage1	VIH1	0.7xVcc	—	Vcc+0.3	V	1.7≦Vcc≦5.5V
“L” Input Voltage1	VIL1	-0.3	—	0.3xVcc	V	1.7≦Vcc≦5.5V
“L” Output Voltage1	VOL1	0	—	0.4	V	IOL=2.1mA, 2.5≦Vcc<5.5V
“L” Output Voltage2	VOL2	0	—	0.2	V	IOL=1.0mA, 1.7≦Vcc<2.5V
“H” Output Voltage1	VOH1	Vcc-0.2	—	Vcc	V	IOH=-0.4mA, 2.5V≦Vcc<5.5V
“H” Output Voltage2	VOH2	Vcc-0.2	—	Vcc	V	IOH=-100μA, 1.7≦Vcc<2.5V
Input Leakage Current	ILI	-1	—	1	μA	V_{IN}=0～Vcc
Output Leakage Current	ILO	-1	—	1	μA	V_{OUT}=0～Vcc, CSB=Vcc
Operating Current Write	ICC1	—	—	0.5	mA	Vcc=1.8V,fSCK=5MHz, tE/W=5ms Byte Write, Page Write
	ICC2	—	—	1	mA	Vcc=2.5V,fSCK=10MHz, tE/W=5ms Byte Write, Page Write
	ICC3	—	—	2	mA	Vcc=5.5V,fSCK=10MHz, tE/W=5ms Byte Write, Page Write
Operating Current Read	ICC4	—	—	1	mA	Vcc=1.8V,fSCK=5MHz, SO=OPEN Read, Read Status Register
	ICC5	—	—	1	mA	Vcc=2.5V,fSCK=2MHz, SO=OPEN Read, Read Status Register
	ICC6	—	—	1.5	mA	Vcc=2.5V,fSCK=5MHz, SO=OPEN Read, Read Status Register
	ICC7	—	—	2	mA	Vcc=2.5V,fSCK=10MHz, SO=OPEN Read, Read Status Register
	ICC8	—	—	2	mA	Vcc=5.5V,fSCK=5MHz, SO=OPEN Read, Read Status Register
	ICC9	—	—	4	mA	Vcc=5.5V,fSCK=10MHz, SO=OPEN Read, Read Status Register
	ICC10	—	—	8	mA	Vcc=5.5V,fSCK=20MHz, SO=OPEN Read, Read Status Register
Standby Current	ISB	—	—	2	μA	Vcc=5.5V, CSB=Vcc, SCK=SI=Vcc or GND HOLDB=WPB=Vcc, SO=OPEN

○Radiation resistance design is not made

●Block diagram

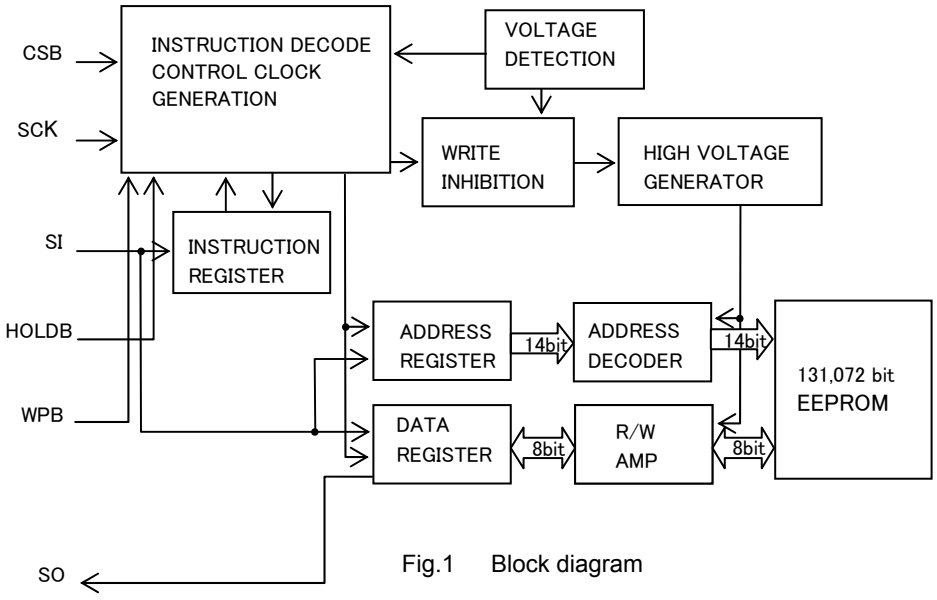


Fig.1 Block diagram

●Operating timing characteristics (Ta=-40～+85°C, unless otherwise specified, load capacity C_L=30pF)

Parameter	Symbol	1.7≦Vcc<2.5V			1.8≦Vcc<2.5V			2.5≦Vcc≦5.5V			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
SCK frequency	f_{SCK}	-	-	3	-	-	5	-	-	10	MHz
SCK high time	t_{SCKWH}	125	-	-	80	-	-	40	-	-	ns
SCK low time	t_{SCKWL}	125	-	-	80	-	-	40	-	-	ns
CSB high time	t_{CS}	250	-	-	90	-	-	40	-	-	ns
CSB setup time	t_{CSS}	100	-	-	60	-	-	30	-	-	ns
CSB hold time	t_{CSH}	100	-	-	60	-	-	30	-	-	ns
SCK setup time	t_{SCKS}	100	-	-	50	-	-	20	-	-	ns
SCK hold time	t_{SCKH}	100	-	-	50	-	-	20	-	-	ns
SI setup time	t_{DIS}	30	-	-	20	-	-	10	-	-	ns
SI hold time	t_{DIH}	50	-	-	20	-	-	10	-	-	ns
Data output delay time	t_{PD}	-	-	125	-	-	80	-	-	40	ns
Output hold time	t_{OH}	0	-	-	0	-	-	0	-	-	ns
Output disable time	t_{OZ}	-	-	200	-	-	80	-	-	40	ns
HOLDB setting setup time	t_{HFS}	100	-	-	0	-	-	0	-	-	ns
HOLDB setting hold time	t_{HFH}	100	-	-	20	-	-	10	-	-	ns
HOLDB release setup time	t_{HRS}	100	-	-	0	-	-	0	-	-	ns
HOLDB release hold time	t_{HRH}	100	-	-	20	-	-	10	-	-	ns
Time from HOLDB to output High-Z	t_{HOZ}	-	-	100	-	-	80	-	-	40	ns
Time from HOLDB to output change	t_{HPD}	-	-	100	-	-	80	-	-	40	ns
SCK rise time ※1	t_{RC}	-	-	1	-	-	1	-	-	1	μs
SCK fall time ※1	t_{FC}	-	-	1	-	-	1	-	-	1	μs
OUTPUT rise time ※1	t_{RO}	-	-	100	-	-	50	-	-	40	ns
OUTPUT fall time ※1	t_{FO}	-	-	100	-	-	50	-	-	40	ns
Write time	$t_{E/W}$	-	-	5	-	-	5	-	-	5	ms

※1 NOT 100% TESTED

● Pin assignment and description

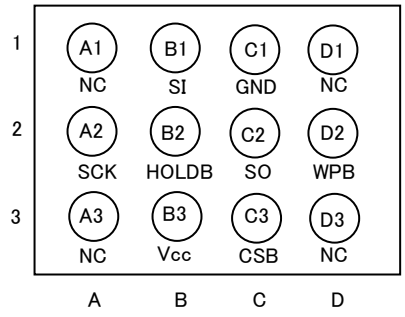


Fig.2 Pin assignment diagram

Terminal name	Input/Output	Function
CSB	Input	Chip select input
SO	Output	Serial data output
WPB	Input	Write protect input Write command is prohibited Write status register command is prohibited
GND	-	All input / output reference voltage, 0V
SI	Input	Start bit, ope code, address, and serial data input
SCK	Input	Serial clock input
HOLDB	Input	Hold input Command communications may be suspended temporarily (HOLD status)
Vcc	-	Power source to be connected

●Sync data input / output timing

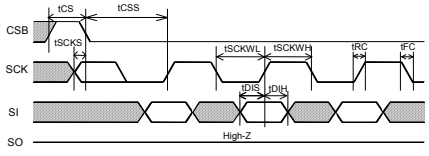


Fig.3 Input timing

SI is taken into IC inside in sync with data rise edge of SCK. Input address and data from the most significant bit MSB

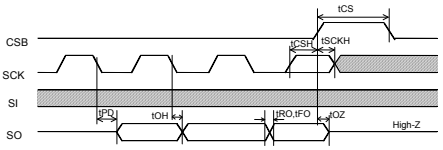


Fig.4 Input / Output timing

SO is output in sync with data fall edge of SCK. Data is output from the most significant bit MSB.

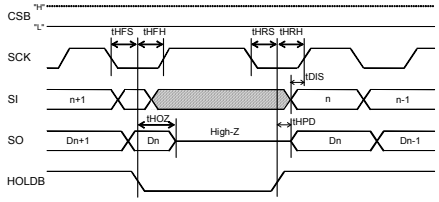


Fig.5 HOLD timing

●AC measurement conditions

Parameter	Symbol	Limits			Unit
		Min.	Typ.	Max.	
Load capacity	C_L	-	-	30	pF
Input rise time	-	-	-	50	ns
Input fall time	-	-	-	50	ns
Input voltage	-	0.2Vcc/0.8Vcc			V
Input / Output judgment voltage	-	0.3Vcc/0.7Vcc			V

●Characteristic data (The following characteristic data are Typ. Values.)

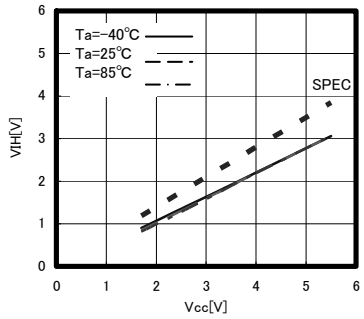


Fig.6 "H" input voltage VIH(CSB,SCK,SI,HOLDB,WPB)

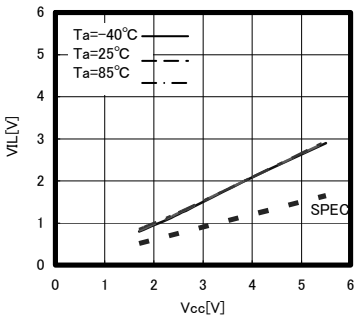


Fig.7 "L" input voltage VIL(CSB,SCK,SI,HOLDB,WPB)

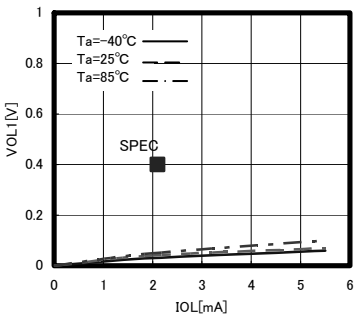


Fig.8 "L" output voltage VOL1 (Vcc=2.5V)

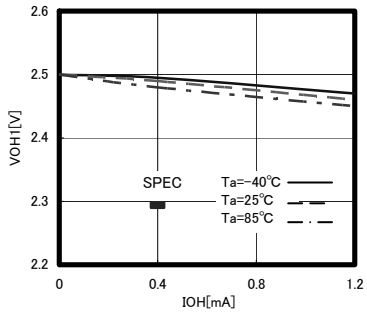


Fig.9 "H" output voltage VOH1 (Vcc=2.5V)

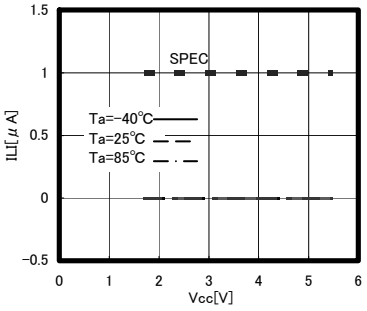


Fig.10 Input leak current ILI(CSB,SCK,SI,HOLDB,WPB)

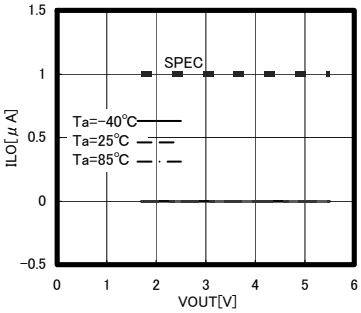


Fig.11 Output leak current ILO(SO)

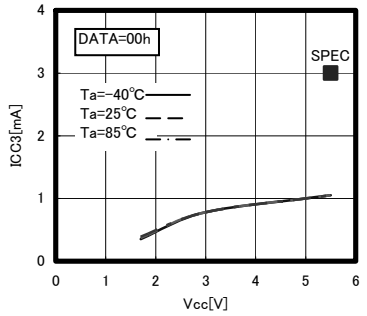


Fig.12 Current consumption at WRITE operation ICC3

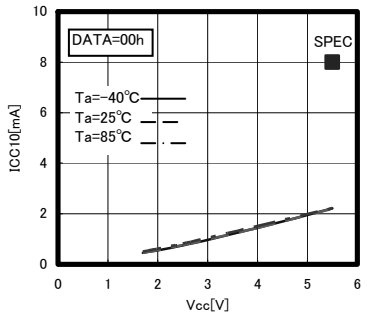


Fig.13 Current Consumption at READ operation ICC10

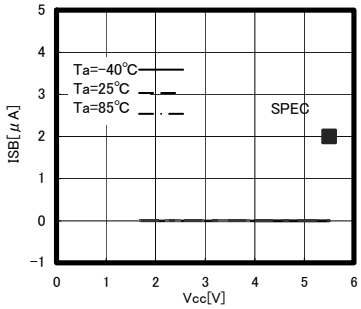


Fig.14 Current Consumption at standby operation IS

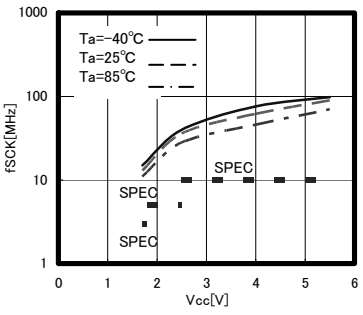


Fig.15 SCK frequency fSCK

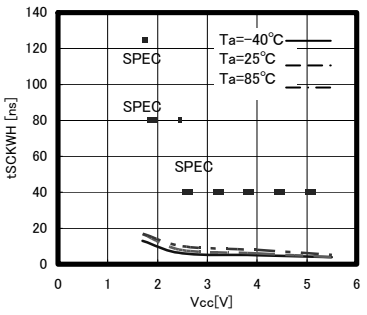


Fig.16 SCK high time tSCKWH

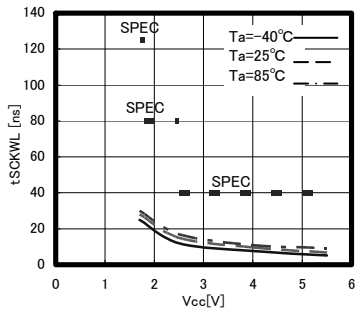


Fig.17 SCK low time tSCKWL

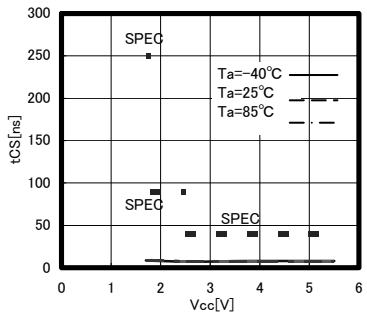


Fig.18 CSB high time tCS

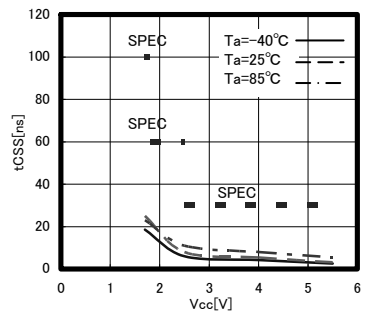


Fig.19 CSB setup time tCSS

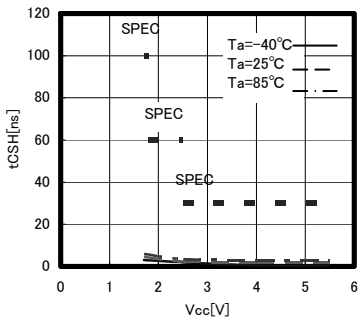


Fig.20 CSB hold time tCSH

●Characteristic data (The following characteristic data are Typ. Values.)

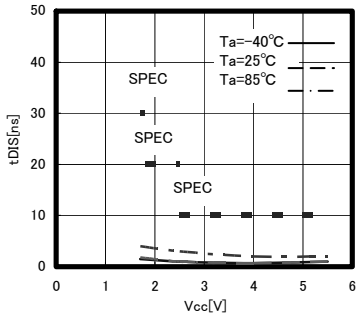


Fig.21 SI setup time tDIS

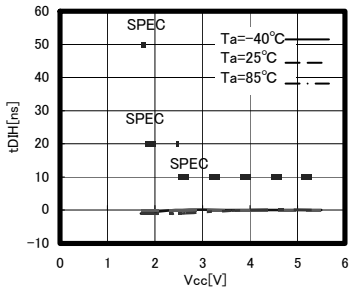


Fig.22 SI hold time tDIH

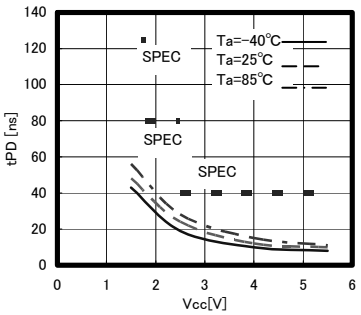


Fig.23 Data output delay time tPD

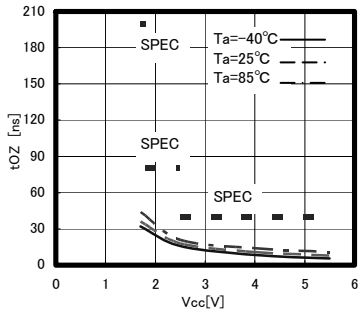


Fig.24 Output disable time tOZ

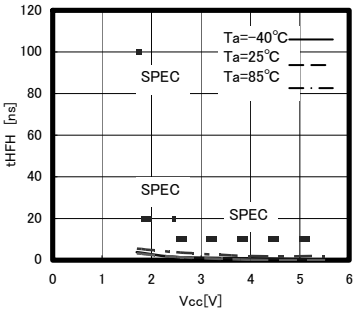


Fig.25 HOLDB setting hold time tHFH

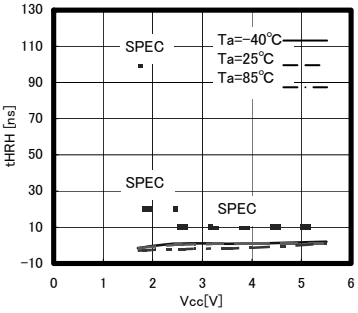


Fig.26 HOLDB release hold time tHRH

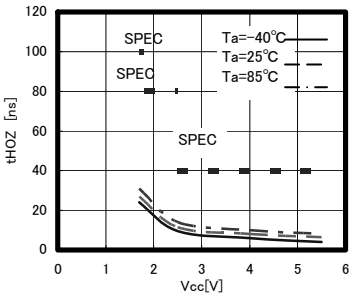


Fig.27 Time from HOLDB to output High-Z tHOZ

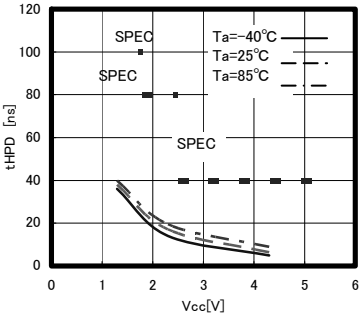


Fig.28 Time from HOLDB to output change tHPD

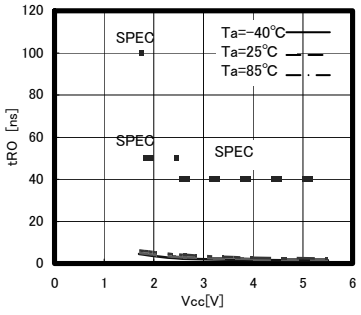


Fig.29 Output rise time tRO

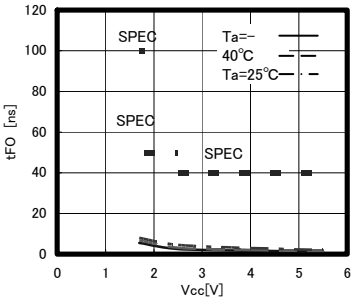


Fig.30 Output fall time tFO

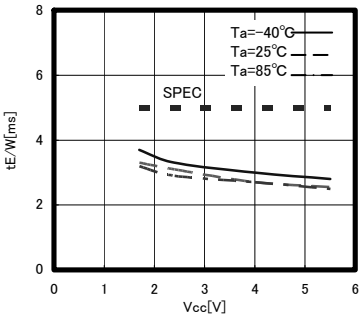


Fig.31 Write cycle time tE/W

●Features

○Status registers

This IC has status register. The status register expresses the following parameters of 8 bits.
BP0 and BP1 can be set by write status register command. These 2 bits are memorized into the EEPROM, therefore are valid even when power source is turned off.
Rewrite characteristics and data hold time are same as characteristics of the EEPROM.
WEN can be set by write enable command and write disable command. WEN becomes write disable status when power source is turned off. $\overline{R}$/B is for write confirmation, therefore cannot be set externally.
The value of status register can be read by read status register command.

1. Contexture of status register

Product number	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
BR25S128GUZ-W	WPEN	0	0	0	BP1	BP0	WEN	$\overline{R}$/B

bit	Memory location	Function
WPEN	EEPROM	WPB pin enable / disable designation bit WPEN=0=invalid WPEN=1=valid
BP1 BP0	EEPROM	EEPROM write disable block designation bit
WEN	registers	Write and write status register write enable / disable status confirmation bit WEN=0=prohibited WEN=1=permitted
$\overline{R}$/B	registers	Write cycle status (READY / BUSY) status confirmation bit $\overline{R}$/B=0=READY $\overline{R}$/B=1=BUSY

2. Write disable block setting

BP1	BP0	Write disable block
		BR25S128GUZ-W
0	0	None
0	1	3000h-3FFFh
1	0	2000h-3FFFh
1	1	0000h-3FFFh

○WPB pin

By setting WPB=LOW, write command is prohibited. And the write command to be disabled at this moment is WRSR. However, when write cycle is in execution, no interruption can be made.

Product number	WRSR	WRITE
BR25S128GUZ-W	Prohibition possible but WPEN bit “1”	Prohibition impossible

○HOLDB pin

By HOLDB pin, data transfer can be interrupted. When SCK=”0”, by making HOLDB from “1” into”0”, data transfer to EEPROM is interrupted. When SCK = “0”, by making HOLDB from “0” into “1”, data transfer is restarted.

●Command mode

Command	Contents	Ope code	
WREN	Write enable command	0000	0110
WRDI	Write disable command	0000	0100
READ	Read command	0000	0011
WRITE	Write command	0000	0010
RDSR	Read status register command	0000	0101
WRSR	Write status register command	0000	0001

●Timing chart

1. Write enable (WREN) / disable (WRDI) command

WREN (WRITE ENABLE): Write enable

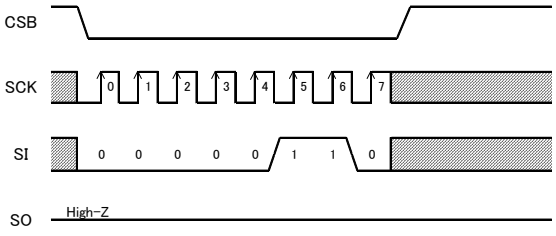


Fig.32 Write enable command

WRDI (WRITE DISABLE): Write disable

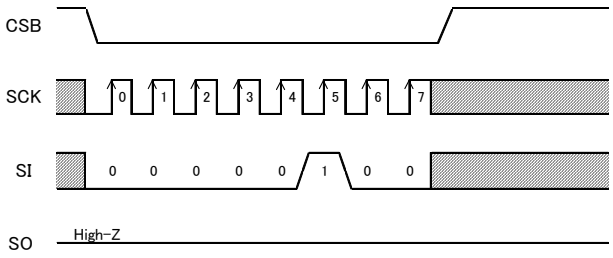


Fig.33 Write disable command

This IC has write enable status and write disable status. It is set to write enable status by write enable command, and it is set to write disable status by write disable command. As for these commands, set CSB LOW, and then input the respective ope codes. The respective commands are accepted at the 7-th clock rise. Even with input over 7 clocks, command becomes valid.
When to carry out write command, it is necessary to set write enable status by the write enable command. If write command is input in the write disable status, the command is cancelled. And even in the write enable status, once write command is executed, it gets in the write disable status. After power on, this IC is in write disable status.

2. Read command (READ)

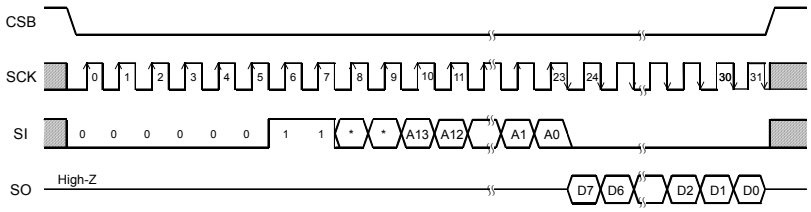


Fig.34 Read command

By read command, data of EEPROM can be read. As for this command, set CSB LOW, then input address after read ope code. EEPROM starts data output of the designated address. Data output is started from SCK fall of 23-th clock, and from D7 to D0 sequentially. This IC has increment read function. After output of data for 1 byte (8bits), by continuing input of SCK, data of the next address can be read. Increment read can read all the addresses of EEPROM. After reading data of the most significant address, by continuing increment read, data of the most insignificant address is read.

3. Write command (WRITE)

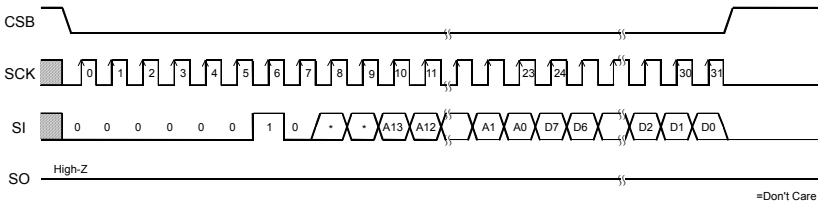


Fig.35 Write command

By write command, data of EEPROM can be written. As for this command, set CSB LOW, then input address and data after write ope code. Then, by making CSB HIGH, the EEPROM starts writing. The write time of EEPROM requires time of tE/W (Max 5ms). During tE/W, other than read status register command is not accepted. Set CSB HIGH between taking the last data (D0) and rising the next SCK clock. At the other timing, write command is not executed, and this write command is cancelled. This IC has page write function, and after input of data for 1 byte (8 bits), by continuing data input without setting CSB HIGH, 2byte or more data can be written for one tE/W. Up to 64 arbitrary bytes can be written. In page write, the insignificant 6 bit of the designated address is incremented internally at every time when data of 1 byte is input and data is written to respective addresses. When data of the maximum bytes or higher is input, address rolls over, and previously input data is overwritten.

4. Read status register command (RDSR)

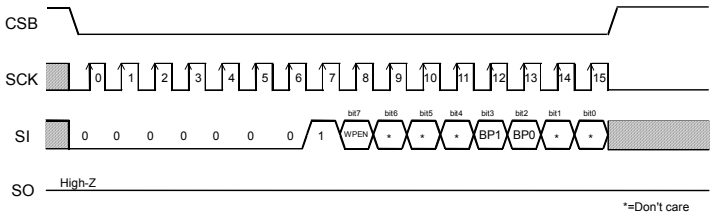


Fig.36 Write status register

Write status register command can write data of status register. The data can be written by this command are 3 bits, that is, WPEN(bit7), BP1 (bit3) and BP0 (bit2) among 8 bits of status register. By BP1 and BP0, write disable block of EEPROM can be set. As for this command, set CSB LOW, and input ope code of write status register, and input data. Then, by making CSB HIGH, EEPROM starts writing. Write time requires time of tE/W as same as write. As for CSB rise, set CSB HIGH between taking the last data bit (bit0) and the next SCK clock rising. At the other timing, command is cancelled. Write disable block is determined by BP1 BP0, and the block can be selected from 1/4 , 1/2, and entire of memory array (Refer to the write disable block setting table.). To the write disabled block, write cannot be made, and only read can be made.

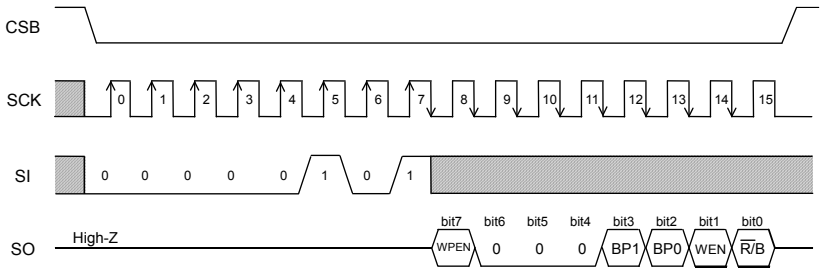


Fig.37 Read status register command

●WPB cancel valid area

WPB is normally fixed to “H” or “L” for use, but when WPB is controlled so as to cancel write status register command, pay attention to the following WPB valid timing.

While write status register command is executed, by setting WPB = “L” in cancel valid area, command can be cancelled. The area from command ope code to CSB rise at internal automatic write start becomes the cancel valid area. However, once write is started, by any input write cycle cannot be cancelled. WPB input becomes Don’t Care, and cancellation becomes invalid.

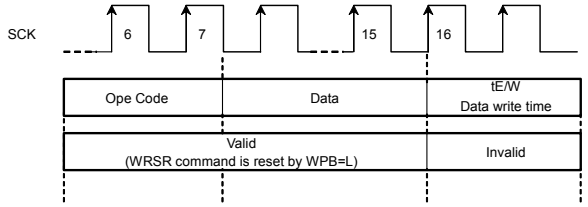


Fig.38 WPB valid timing (At inputting WRSR command)

●HOLDB pin

By HOLDB pin, command communication can be stopped temporarily (HOLD status). The command communications are carried out when the HOLDB pin is HIGH. To get in HOLD status, at command communication, when SCK=LOW, set the HOLDB pin LOW. At HOLD status, SCK and SI become Don’t Care, and SO becomes high impedance (High-Z). To release the HOLD status, set the HOLDB pin HIGH when SCK=LOW. After that, communication can be restarted from the point before the HOLD status. For example, when HOLD status is made after A5 address input at read, after release of HOLD status, by starting A4 address input, read can be restarted. When in HOLD status, keep CSB LOW. When it is set CSB=HIGH in HOLD status, the IC is reset, therefore communication after that cannot be restarted.

●Method to cancel each command

○READ, RDSR

・Method to cancel : cancel by CSB = “H”.

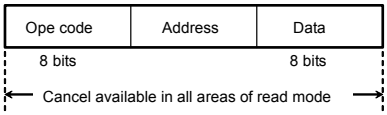


Fig.39 READ cancel valid timing

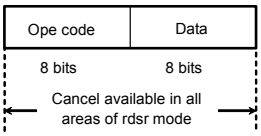


Fig.40 RDSR cancel valid timing

○WRITE、PAGE WRITE

a：Ope code or address input area
Cancellation is available by CSB=”H”.

b：Data input area (D7～D1 input area)
Cancellation is available by CSB=”H”.

c：Data input area (D0 area)
In this area, cancellation is not available.
When CSB is set HIGH, write starts.
By continuing to input SCK clock without rising CSB, the command will be page write command.
In page write mode, there is write enable area at every 8 clocks.

d：tE/W area
In the area c, by rising CSB, write starts.
While writting, by any input, cancellation cannot be made.

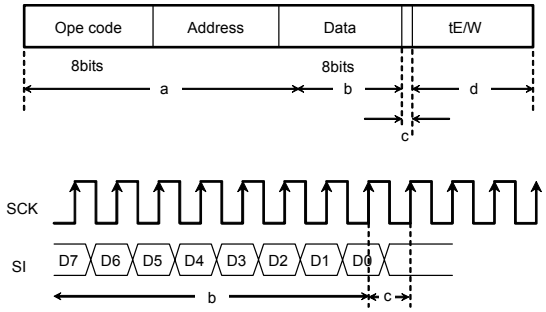


Fig.41 WRITE cancel valid timing

Note1) If Vcc is made OFF during write execution, designated address data is not guaranteed, therefore write it once again.

Note2) If CSB is rised at the same timing as that of the SCK rise, write execution / cancel becomes unstable, therefore, it is recommended to rise in SCK = “L” area. As for SCK rise, assure timing of tCSS / tCSH or more.

○WRSR

a：From ope code to 15-th clock rise
Cancellation is available by CSB=”H”.

b：From 15-th clock rise to 16-th clock rise (write enable area)
In this area, cancellation is not available.
When CSB is set HIGH, write starts.

c：After 16-th clock rise.
Cancellation is available by CSB=”H”.
However, if write starts (CSB is rised) in the area b, cancellation cannot be made by any means.
And, by inputting on SCK clock, cancellation cannot be made.

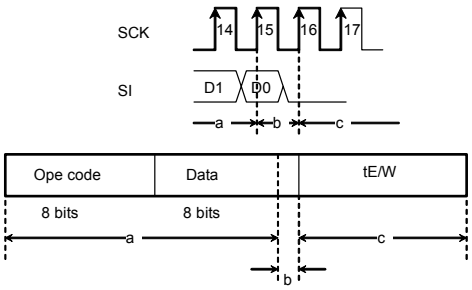


Fig.42 WRSR cancel valid timing

Note1) If Vcc is made OFF during write execution, designated address data is not guaranteed, therefore write it once again

Note2) If CSB is rised at the same timing as that of the SCK rise, write execution / cancel becomes unstable, therefore, it is recommended to rise in SCK = “L” area. As for SCK rise, assure timing of tCSS / tCSH or more.

○WREN/WRDI

a：From ope code to 7-th clock rise, cancellation is available by CSB = “H”.

b：Cancellation is not available 7-th clock.

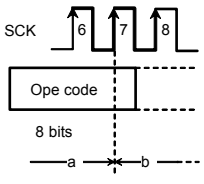


Fig.43 WREN/WRDI cancel valid timing

●I/O peripheral circuits

In order to realize stable high speed operations, pay attention to the following input / output pin conditions.

○Input pin pull up, pull down resistance

When to attach pull up, pull down resistance to EEPROM input pin, select an appropriate value for the microcontroller VOL, IOL with considering VIL characteristics of this IC.

1. Pull up resistance

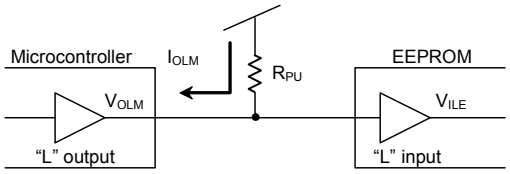


Fig.44 Pull up resistance

$$R_{PU} \geqq \frac{V_{CC}-V_{OLM}}{I_{OLM}} \quad \cdots ①$$

$$V_{OLM} \leqq V_{ILE} \quad \cdots ②$$

Example) When Vcc=5V, V_{ILE}=1.5V, V_{OLM}=0.4V, I_{OLM}=2mA, from the equation ①,

$$R_{PU} \geqq \frac{5-0.4}{2\times10^{-3}}$$

$$\therefore R_{PU} \geqq 2.3[k\Omega]$$

With the value of Rpu to satisfy the above equation, V_{OLM} becomes 0.4V or lower, and with V_{ILE} (=1.5V), the equation ② is also satisfied.

- V_{ILE} :EEPROM V_{IL} specifications
- V_{OLM} :Microcontroller V_{OL} specifications
- I_{OLM} :Microcontroller I_{OL} specifications

And, in order to prevent malfunction or erroneous write at power ON/OFF, be sure to make CSB pull up.

2.Pull down resistance

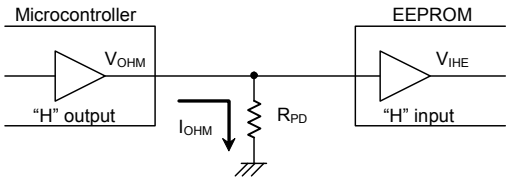


Fig.45 Pull down resistance

$$R_{PD} \geqq \frac{V_{OHM}}{I_{OHM}} \quad \cdots ③$$

$$V_{OHM} \geqq V_{IHE} \quad \cdots ④$$

Example) When V_{CC}=5V, V_{OHM}=V_{CC}-0.5V, I_{OHM}=0.4mA, V_{IHE}=V_{CC}×0.7V, from the equation③,

$$R_{PD} \geqq \frac{5-0.5}{0.4\times10^{-3}}$$

$$\therefore R_{PD} \geqq 11.3[k\Omega]$$

Further, by amplitude VIHE, VILE of signal input to EEPROM, operation speed changes. By inputting Vcc/GND level amplitude of signal, more stable high speed operations can be realized. On the contrary, when amplitude of 0.8VCC / 0.2Vcc is input, operation speed becomes slow.*1

In order to realize more stable high speed operation, it is recommended to make the values of R_{PU}, R_{PD} as large as possible, and make the amplitude of signal input to EEPROM close to the amplitude of VCC / GND level.

(★1 In this case, guaranteed value of operating timing is guaranteed.)

○SO load capacity condition

Load capacity of SO output pin affects upon delay characteristic of SO output (Data output delay time, time from HOLDB to High-Z, Output rise time, Output fall time.). In order to make output delay characteristic into better, make SO load capacity small.

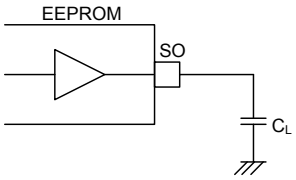


Fig.46 SO load capacity of data output delay time tPD

○Other cautions

Make the each wire length from the microcontroller to EEPROM input pin same length, in order to prevent setup / hold violation to EEPROM, owing to difference of wire length of each input.

●Equivalent circuit

○Output circuit

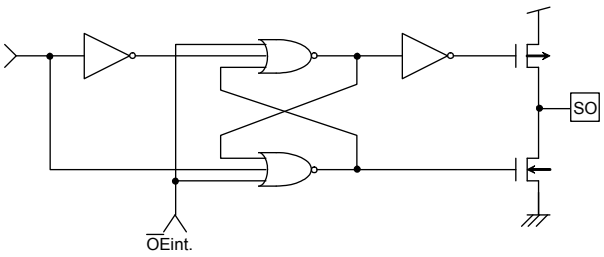


Fig.47 SO output equivalent circuit

○Input circuit

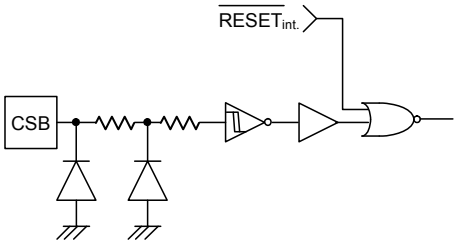


Fig.48 CSB input equivalent circuit

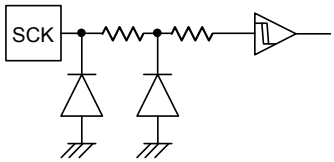


Fig.49 SCK input equivalent circuit

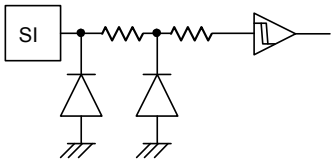


Fig.50 SI input equivalent circuit

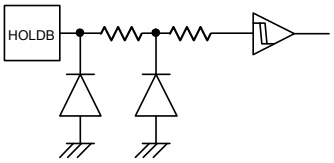


Fig.51 HOLDB input equivalent circuit

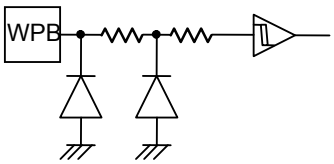


Fig.52 WPB input equivalent circuit

●Notes on power ON/OFF

○At standby

Set CSB “H”, and be sure to set SCK, SI input “L” or “H”. Do not input intermediate electric potantial.

○At power ON/OFF

When Vcc rise or fall, set CSB=”H” (=Vcc).

When CSB is “L”, this IC gets in input accept status (active). If power is turned on in this status, noises and the likes may cause malfunction, erroneous write or so. To prevent these, at power ON, set CSB “H”. (When CSB is in “H” status, all inputs are canceled.)

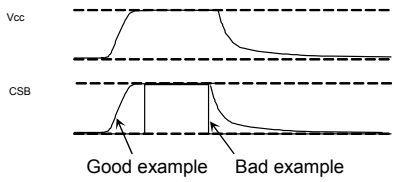


Fig.53 CSB timing at power ON/OFF

(Good example) CSB terminal is pulled up to Vcc.

At power OFF, take 10ms or more before supply. If power is turned on without observing this condition, the IC internal circuit may not be reset.

(Bad example) CSB terminal is “L” at power ON/OFF.

In this case, CSB always becomes “L” (active status), and EEPROM may have malfunction or erroneous write owing to noises and the likes.

Even when CSB input is High-Z, the status becomes like this case.

○Operating timing after power ON

As shown in Fig.55, at standby, when SCK is “H”, even if CSB is fallen, SI status is not read at fall edge. SI status is read at SCK rise edge after fall of CSB. At standby and at power ON/OFF, set CSB “H” status.

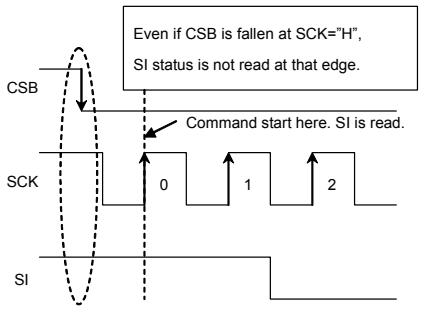


Fig.54 Operating timing

○At power on malfunction preventing function

This IC has a POR (Power On Reset) circuit as mistake write countermeasure. After POR action, it gets in write disable status. The POR circuit is valid only when power is ON, and does not work when power is OFF. When power is ON, if the recommended conditions of the following tR, tOFF, and Vbot are not satisfied, it may become write enable status owing to noises and the likes.

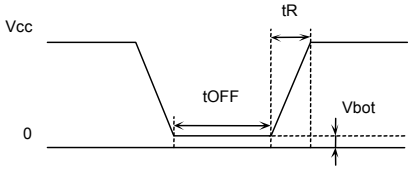


Fig.55 Rise waveform

Recommended conditions of t_R, t_{OFF}, Vbot

t_R	t_{OFF}	Vbot
10ms or below	10ms or higher	0.3V or below
100ms or below	10ms or higher	0.2V or below

○Low voltage malfunction preventing function

LVCC (Vcc-Lockout) circuit prevents data rewrite action at low power, and prevents wrong write.

At LVCC voltage (Typ. =1.2V) or below, it prevent data rewrite.

●Noise countermeasures

○Vcc noise (bypass capacitor)

When noise or surge gets in the power source line, malfunction may occur, therefore, for removing these, it is recommended to attach a bypass capacitor (0.1μF) between IC Vcc and GND. At that time, attach it as close to IC as possible.
And, it is also recommended to attach a bypass capacitor between board Vcc and GND.

○SCK noise

When the rise time of SCK (tRC) is long, and a certain degree or more of noise exists, malfunction may occur owing to clock bit displacement. To avoid this, a Schmitt trigger circuit is built in SCK input. The hysterisis width of this circuit is set about 0.2V, if noises exist at SCK input, set the noise amplitude 0.2Vp-p or below. And it is recommended to set the rise time of SCK (tRC) 100ns or below. In the case when the rise time is 100ns or higher, take sufficient noise countermeasures. Make the clock rise, fall time as small as possible.

○WPB noise

During execution of write status register command, if there exist noises on WPB pin, mistake in recognition may occur and forcible cancellation may result. To avoid this, a Schmitt trigger circuit is built in WPB input. In the same manner, a Schmitt trigger circuit is built in CSB input, SI input and HOLDB input too.

●Cautions on use

(1) Described numeric values and data are design representative values, and the values are not guaranteed.

(2) We believe that application circuit examples are recommendable, however, in actual use, confirm characteristics further sufficiently. In the case of use by changing the fixed number of external parts, make your decision with sufficient margin in consideration of static characteristics and transition characteristics and fluctuations of external parts and our LSI.

(3) Absolute maximum ratings

If the absolute maximum ratings such as impressed voltage and operating temperature range and so forth are exceeded, LSI may be destructed. Do not impress voltage and temperature exceeding the absolute maximum ratings. In the case of fear exceeding the absolute maximum ratings, take physical safety countermeasures such as fuses, and see to it that conditions exceeding the absolute maximum ratings should not be impressed to LSI.

(4) GND electric potential

Set the voltage of GND terminal lowest at any action condition. Make sure that each terminal voltage is higher than that of GND terminal.

(5) Heat design

In consideration of permissible dissipation in actual use condition, carry out heat design with sufficient margin.

(6) Terminal to terminal short circuit and wrong packaging

When to package LSI onto a board, pay sufficient attention to LSI direction and displacement. Wrong packaging may destruct LSI. And in the case of short circuit between LSI terminals and terminals and power source, terminal and GND owing to foreign matter, LSI may be destructed.

(7) Use in a strong electromagnetic field may cause malfunction, therefore, evaluate design sufficiently.

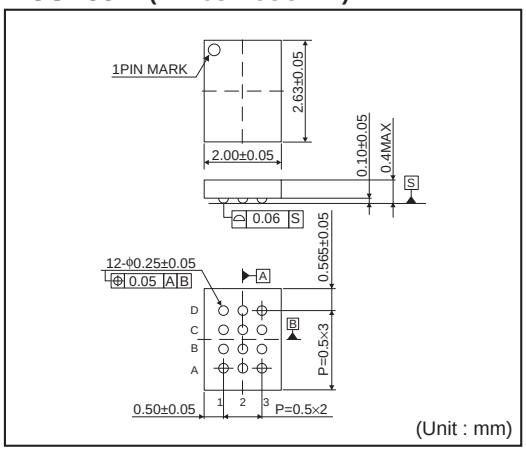
●Selection of order type

B	R	2	5	S	1	2	8	G	U	Z	-	W	E	2

Part No.	BUS Type	Operating Temperature / Power source voltage	Capacity	Package	Double cell	Packaging and forming specification
	25:SPI	S: -40℃~ +85℃ / 1.7V~5.5V	128=128Kbit	GUZ:VCSP35L2		E2: Embossed tape and reel

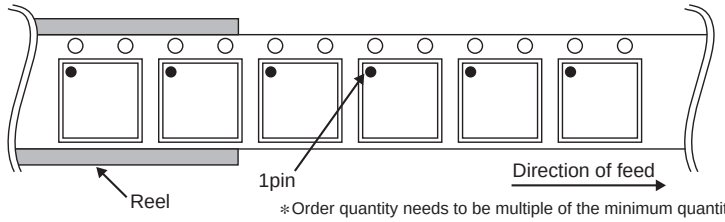
●Package specifications

VCSP35L2(BR25S128GUZ-W)



<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	3000pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



∗Order quantity needs to be multiple of the minimum quantity.

Notes

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If you intend to export or ship overseas any Product or technology specified herein that may be controlled under the Foreign Exchange and the Foreign Trade Law, you will be required to obtain a license or permit under the Law.

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