

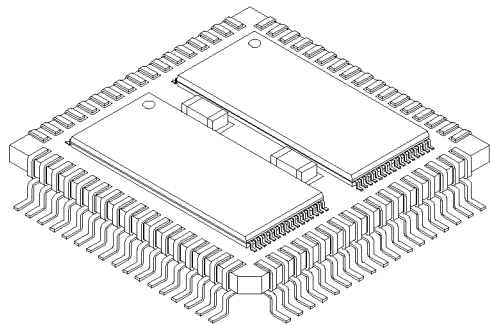
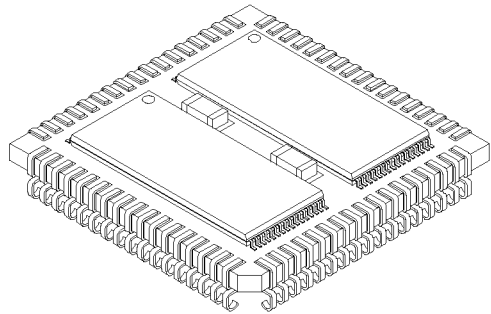
DESCRIPTION:

The DPS128X24XP/XHP is a 68-pin surface mount module consisting of three 128K x 8 SRAM devices in plastic TSOP packages surface mounted on a FR-4 substrate.

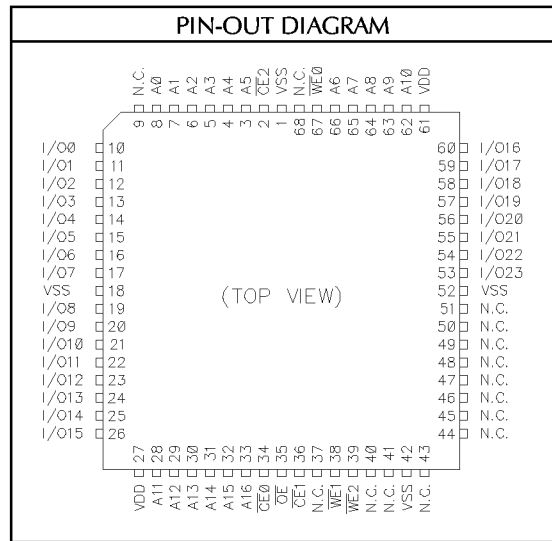
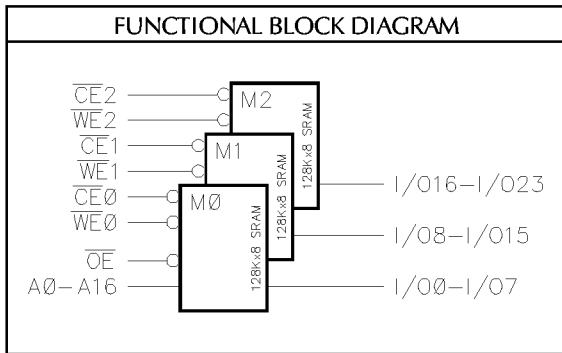
The module is available with either "J"-Leads or "Gull"-Leads.

FEATURES:

- Organizations Available:
384K x 8 or 128K x 24
- Access Times:
15, 20, 25, 35ns
- Fully Static Operation - No clock or refresh required
- TTL-compatible
- 68-Pin Surface Mount Module



PIN NAMES	
A0 - A16	Address Inputs
I/O0 - I/O23	Data Input/Output
CE0 - CE2	Low Chip Enables
WE0 - WE2	Write Enables
OE	Output Enable
VDD	Power (+5V)
Vss	Ground
N.C.	No Connect



RECOMMENDED OPERATING RANGE ³						
Symbol	Characteristic	Min.	Typ.	Max.	Unit	
V _{DD}	Supply Voltage	4.5	5.0	5.5	V	
V _{IH}	Input HIGH Voltage	2.2		V _{DD} +0.3	V	
V _{IL}	Input LOW Voltage	-0.5 ²		0.8	V	
T _A	Operating Temperature	C	0	+25	+70	°C
		CI	-40	+25	+85	

TRUTH TABLE					
Mode	\overline{CE}	\overline{WE}	\overline{OE}	I/O Pin	Supply Current
Not Selected	X	X	X	High-Z	Standby
Not Selected	H	X	X	High-Z	Standby
D _{OUT} Disable	L	H	H	High-Z	Active
Read	L	H	L	D _{OUT}	Active
Write	L	L	X	D _{IN}	Active

H = HIGH L = LOW X = Don't Care
 * If \overline{OE} is LOW during Write, t_{WHZ} must be observed before data is presented to the device.

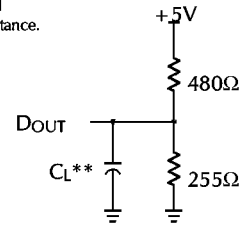
DC OUTPUT CHARACTERISTICS					
Symbol	Parameter	Conditions	Min.	Max.	Unit
V _{OH}	HIGH Voltage	I _{OH} = -4.0mA	2.4		V
V _{OL}	LOW Voltage	I _{OL} = 8.0mA		0.4	V

CAPACITANCE ⁴ : T _A = 25°C, F = 1.0MHz				
Symbol	Parameter	Max.	Unit	Condition
C _{ADR}	Address Input	30	pF	V _{IN} ² = 0V
C _{CE}	Chip Enable	12		
C _{WE}	Write Enable	12		
C _{OE}	Output Enable	30		
C _{I/O}	Data Input/Output	12		

ABSOLUTE MAXIMUM RATINGS ³			
Symbol	Parameter	Value	Unit
T _{STC}	Storage Temperature	-55 to +125	°C
T _{BIAS}	Temperature Under Bias	-55 to +125	°C
V _{DD}	Supply Voltage ¹	-0.5 to +7.0	°C
V _{I/O}	Input/Output Voltage ¹	-0.5 to +7.0	V

AC TEST CONDITIONS		
Input Pulse Levels		0V to 3.0V
Input Pulse Rise and Fall Times		5ns
Input and Output Timing Reference Levels		1.5V

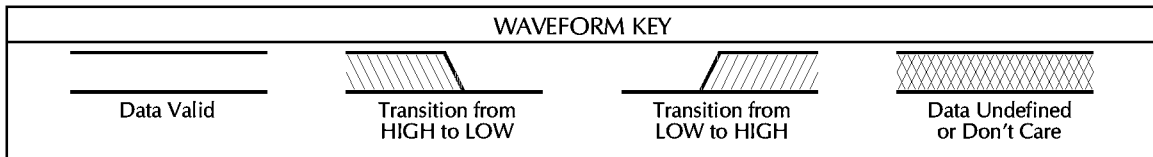
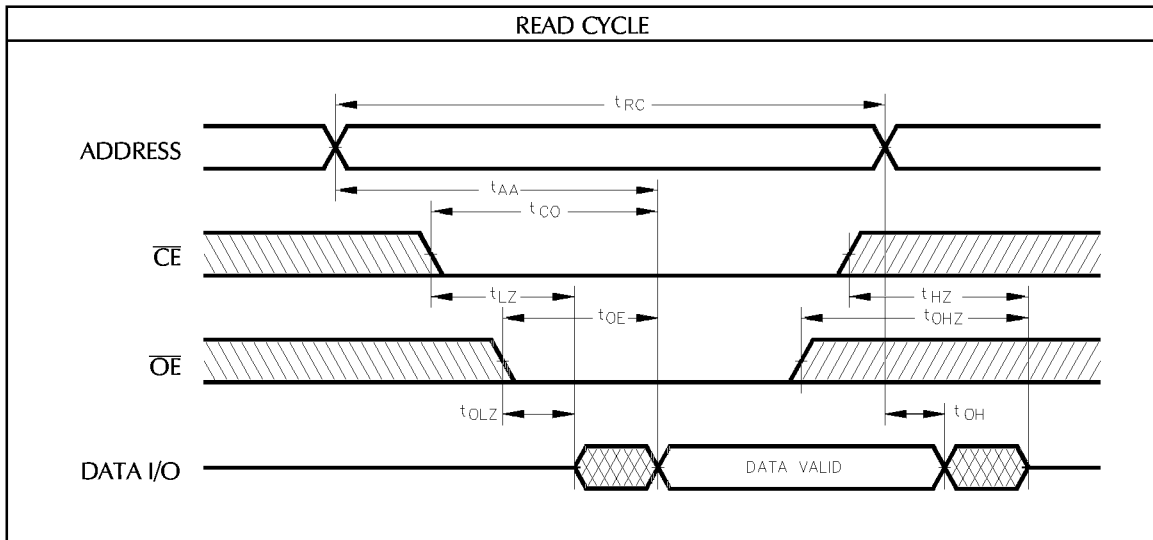
Figure 1. Output Load
 ** Including Probe and Jig Capacitance.



OUTPUT LOAD		
Load	C _L	Parameters Measured
1	30pF	except t _{IZ} , t _{HZ} , t _{OHZ} , t _{OLZ} , and t _{WHZ}
2	5pF	t _{IZ} , t _{HZ} , t _{OHZ} , t _{OLZ} , and t _{WHZ}

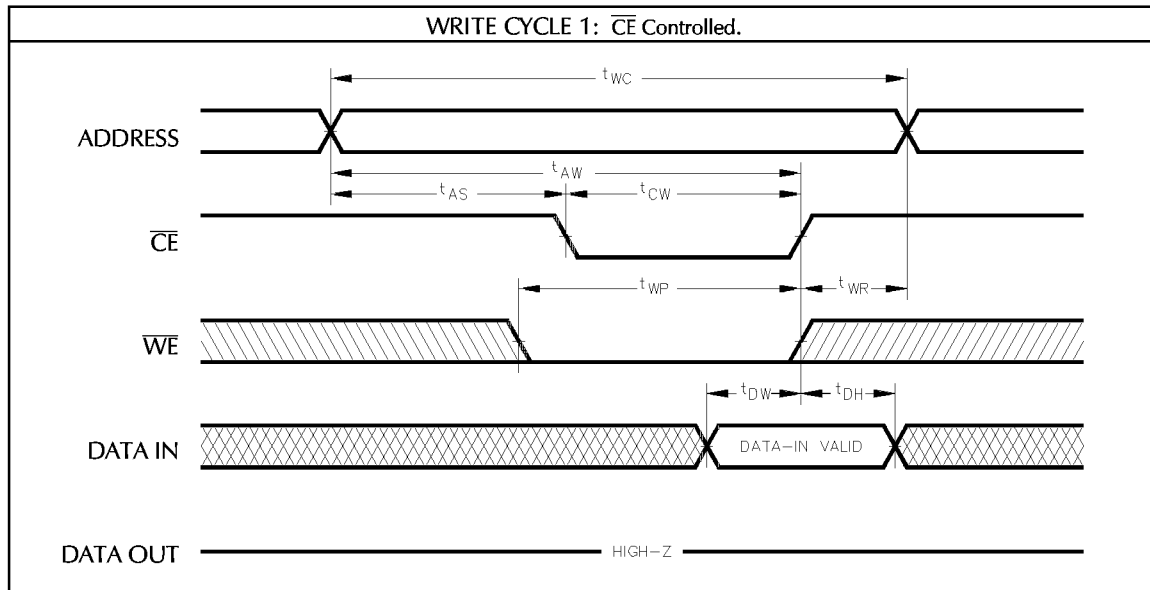
DC OPERATING CHARACTERISTICS: Over operating ranges							
Symbol	Characteristics	Test Conditions	x8		x24		Unit
			Min.	Max.	Min.	Max.	
I _{IN}	Input Leakage Current	V _{IN} = 0V to V _{DD} , V _{DD} = max.	-20	+20	-20	+20	μA
I _{OUT}	Output Leakage Current	V _{I/O} = 0V to V _{DD} , V _{DD} = max., \overline{CE} = V _{IH}	-20	+20	-5	+5	μA
I _{CC}	Dynamic Operating Current	\overline{CE} = V _{IL} , V _{DD} = max. I _{OUT} = 0mA, f = f max.		340		540	mA
I _{SB1}	Full Standby Supply Current (CMOS)	f = 0, V _{IN} ≥ V _{DD} -0.2V or V _{IN} ≤ V _{SS} +0.2V, \overline{CE} ≥ V _{DD} -0.2V		40		40	mA
I _{SB2}	Standby Current (TTL)	\overline{CE} = V _{IH} , f = f max.		160		160	mA
V _{OL}	Output Low Voltage	I _{OUT} = 8.0mA		0.4		0.4	V
V _{OH}	Output High Voltage	I _{OUT} = -4.0mA	2.4		2.4		V

AC OPERATING CONDITIONS AND CHARACTERISTICS - READ CYCLE: Over operating ranges											
No.	Symbol	Parameter	15ns		20ns		25ns		35ns		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
1	t_{RC}	Read Cycle Time	15		20		25		35		ns
2	t_{AA}	Address Access Time		15		20		25		35	ns
3	t_{CO}	\overline{CE} to Output Valid		15		20		25		35	ns
4	t_{OE}	Output Enable to Output Valid		7		9		10		12	ns
5	t_{LZ}	\overline{CE} to Output in LOW-Z ^{4,5}	3		3		3		3		ns
6	t_{OLZ}	Output Enable to Output in LOW-Z ^{4,5}	0		0		0		0		ns
7	t_{HZ}	\overline{CE} to Output in HIGH-Z ^{4,5}		8		9		10		12	ns
8	t_{OHZ}	Output Enable to Output in HIGH-Z ^{4,5}		7		8		10		12	ns
9	t_{OH}	Output Hold from Address Change	4		4		4		4		ns



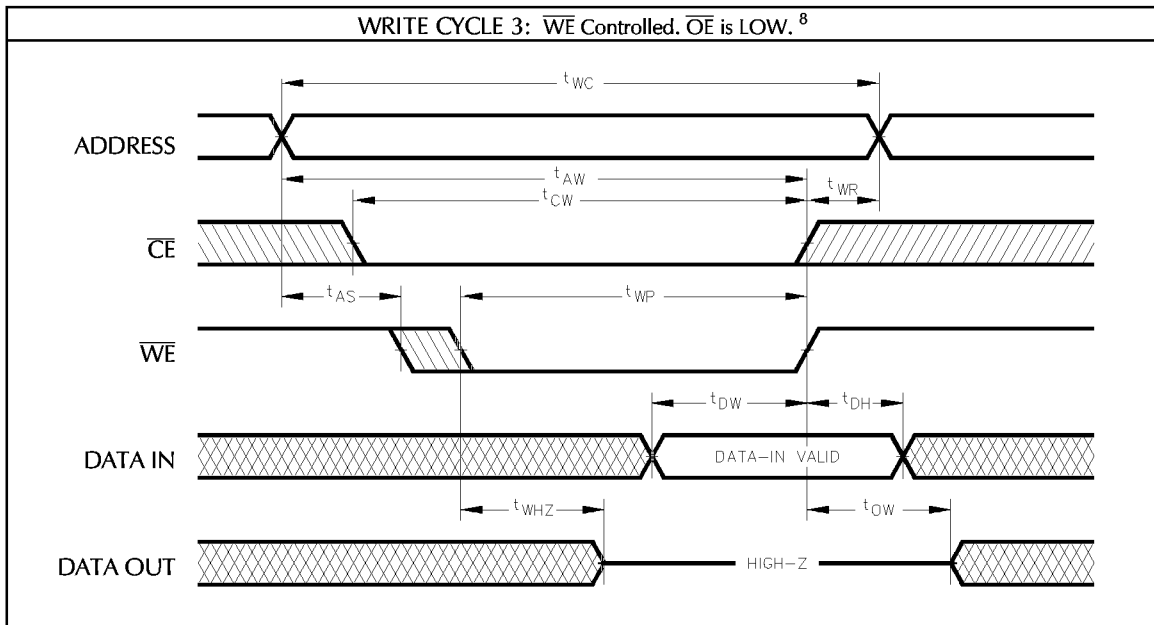
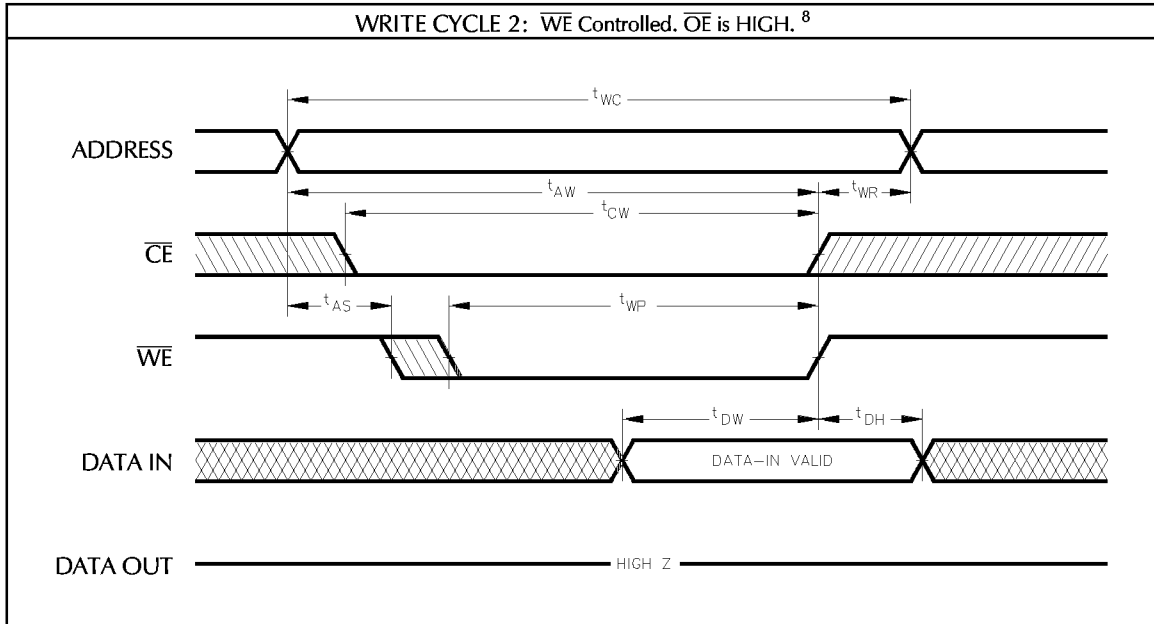
AC OPERATING CONDITIONS AND CHARACTERISTICS - WRITE CYCLE ^{6,7} : Over operating ranges											
No.	Symbol	Parameter	15ns		20ns		25ns		35ns		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
10	t _{WC}	Write Cycle Time	15		20		25		35		ns
11	t _{AW}	Address Valid to End of Write	12		15		20		30		ns
12	t _{CW}	Chip Enable to End of Write	12		15		20		30		ns
13	t _{AS}	Address Set-Up Time *	0		0		0		0		ns
14	t _{WP}	Write Pulse Width	11		12		15		20		ns
15	t _{WR}	Write Recovery Time, \overline{CE} , \overline{WE}	0		0		0		0		ns
16	t _{WHZ}	Write Enable to Output in HIGH-Z ^{4,5}		7		10		12		15	ns
17	t _{DW}	Data to Write Time Overlap	8		10		12		12		ns
18	t _{DH}	Data Hold from Write Time	0		0		0		0		ns
19	t _{OW}	Output Active from End of Write	2		2		2		2		ns

* Valid for both Read and Write Cycles.

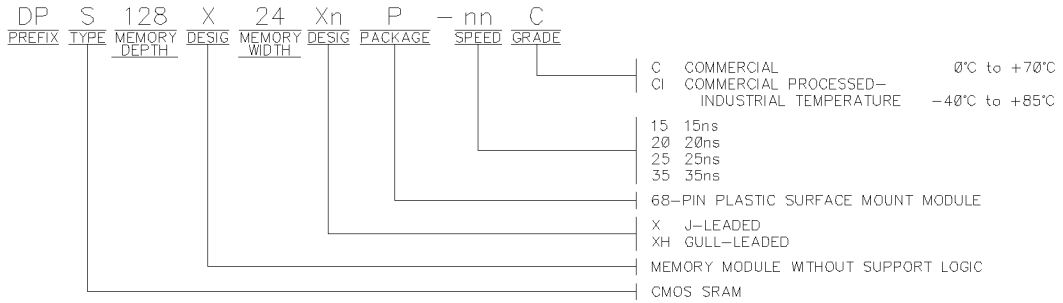


NOTES:

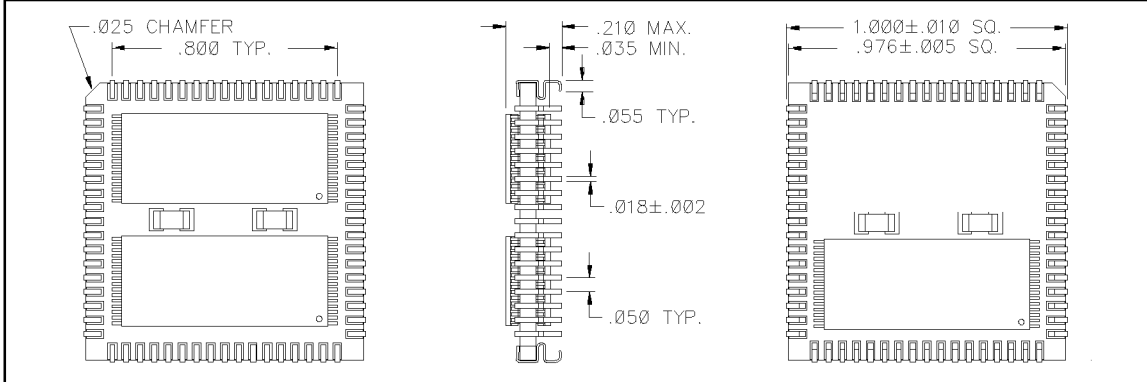
1. All voltages are with respect to V_{ss}.
2. -2.0V min. for pulse width less than 20ns (V_{IL} min. = -0.5V at DC level).
3. Stresses greater than those under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
4. This parameter is guaranteed and not 100% tested.
5. Transition is measured at the point of ±500mV from steady state voltage.
6. When \overline{OE} and \overline{CE} are LOW and \overline{WE} is HIGH, I/O pins are in the output state, and input signals of opposite phase to the outputs must not be applied.
7. The outputs are in a high impedance state when \overline{WE} is LOW.



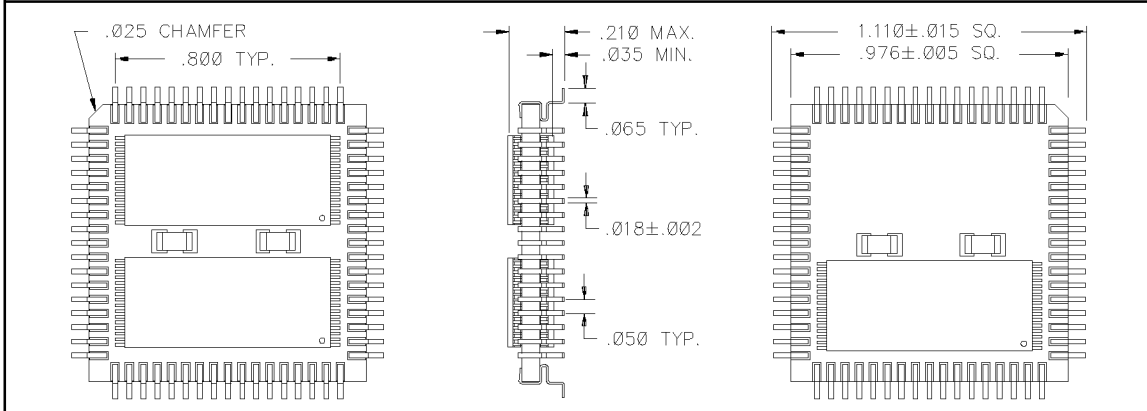
ORDERING INFORMATION



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