



Monolithic N-Channel JFET Dual

PRODUCT SUMMARY				
$V_{GS(off)}$ (V)	$V_{(BR)GSS}$ Min (V)	g_{fs} Min (mS)	I_G Typ (μ A)	$ V_{GS1} - V_{GS2} _{Max}$ (mV)
-1 to -6	-25	4.5	-1	20

FEATURES

- Monolithic Design
- High Slew Rate
- Low Offset/Drift Voltage
- Low Gate Leakage: 1 pA
- Low Noise
- High CMRR: 90 dB

BENEFITS

- Tight Differential Match vs. Current
- Improved Op Amp Speed, Settling Time Accuracy
- High-Speed Performance
- Minimum Input Error/Trimming Requirement
- Insignificant Signal Loss/Error Voltage
- High System Sensitivity
- Minimum Error with Large Input Signal

APPLICATIONS

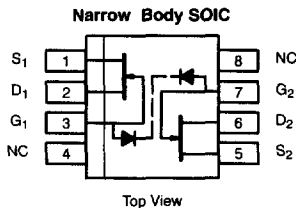
- Wideband Differential Amps
- High-Speed, Temp-Compensated, Single-Ended Input Amps
- High Speed Comparators
- Impedance Converters

DESCRIPTION

The SST441 is a monolithic high-speed dual JFET mounted in a single SO-8 package. This JFET is an excellent choice for use as wideband differential amplifiers in demanding test and measurement applications.

The SO-8 package is available with tape-and-reel options to support automated assembly (see Packaging Information).

For similar products in TO-71 packaging, see the U441 data sheet.



ABSOLUTE MAXIMUM RATINGS

Gate-Drain, Gate-Source Voltage	-25 V
Gate Current	50 mA
Lead Temperature ($1/16''$ from case for 10 sec.)	300°C
Storage Temperature	-55 to 150°C

Operating Junction Temperature	-55 to 150°C
Power Dissipation :	Per Side ^a 300 mW
	Total ^a 500 mW

Notes
a. Derate 2.4 mW/°C above 25°C

For applications information see AN102.



SPECIFICATIONS ($T_A = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)						
Parameter	Symbol	Test Conditions	Limits			Unit
			Min	Typ ^a	Max	
Static						
Gate-Source Breakdown Voltage	$V_{(BR)GSS}$	$I_G = -1\ \mu\text{A}$, $V_{DS} = 0\ \text{V}$	-25	-35		V
Gate-Source Cutoff Voltage	$V_{GS(off)}$	$V_{DS} = 10\ \text{V}$, $I_D = 1\ \text{nA}$	-1	-3.5	-6	
Saturation Drain Current ^b	I_{DSS}	$V_{DS} = 10\ \text{V}$, $V_{GS} = 0\ \text{V}$	6	15	30	mA
Gate Reverse Current	I_{GSS}	$V_{GS} = -15\ \text{V}$, $V_{DS} = 0\ \text{V}$		-1	-500	pA
		$T_A = 125^\circ\text{C}$		-0.2		nA
Gate Operating Current	I_G	$V_{DG} = 10\ \text{V}$, $I_D = 5\ \text{mA}$		-1	-500	pA
		$T_A = 125^\circ\text{C}$		-0.2		nA
Gate-Source Forward Voltage	$V_{GS(F)}$	$I_G = 1\ \text{mA}$, $V_{DS} = 0\ \text{V}$		0.7		V
Dynamic						
Common-Source Forward Transconductance	g_{fs}	$V_{DS} = 10\ \text{V}$, $I_D = 5\ \text{mA}$ $f = 1\ \text{kHz}$	4.5	6	9	mS
Common-Source Output Conductance	g_{os}				20	200
Common-Source Forward Transconductance	g_{fs}	$V_{DS} = 10\ \text{V}$, $I_D = 5\ \text{mA}$ $f = 100\ \text{MHz}$		5.5		mS
Common-Source Output Conductance	g_{os}				30	
Common-Source Input Capacitance	C_{iss}	$V_{DS} = 10\ \text{V}$, $I_D = 5\ \text{mA}$ $f = 1\ \text{MHz}$		3.5		pF
Common-Source Reverse Transfer Capacitance	C_{rss}				1	
Equivalent Input Noise Voltage	\bar{e}_n	$V_{DS} = 10\ \text{V}$, $I_D = 5\ \text{mA}$ $f = 10\ \text{kHz}$		4		nV/ $\sqrt{\text{Hz}}$
Matching						
Differential Gate-Source Voltage	$ V_{GS1} - V_{GS2} $	$V_{DG} = 10\ \text{V}$, $I_D = 5\ \text{mA}$		7	20	mV
Gate-Source Voltage Differential Change with Temperature	$\frac{\Delta V_{GS1} - V_{GS2} }{\Delta T}$	$V_{DG} = 10\ \text{V}$, $I_D = 5\ \text{mA}$ $T_A = -55$ to 125°C		10		$\mu\text{V}/^\circ\text{C}$
Saturation Drain Current Ratio ^c	$\frac{I_{DSS1}}{I_{DSS2}}$	$V_{DS} = 10\ \text{V}$, $V_{GS} = 0\ \text{V}$		0.98		
Transconductance Ratio ^c	$\frac{g_{fs1}}{g_{fs2}}$	$V_{DS} = 10\ \text{V}$, $I_D = 5\ \text{mA}$ $f = 1\ \text{kHz}$		0.98		
Common Mode Rejection Ratio	CMRR	$V_{DG} = 10$ to $15\ \text{V}$, $I_D = 5\ \text{mA}$		90		dB

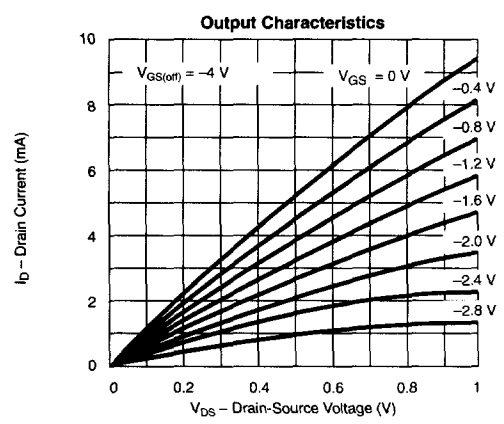
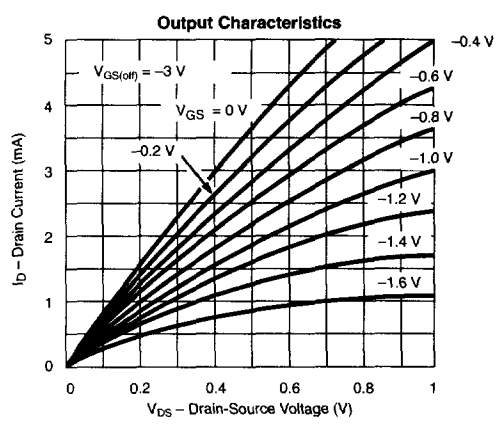
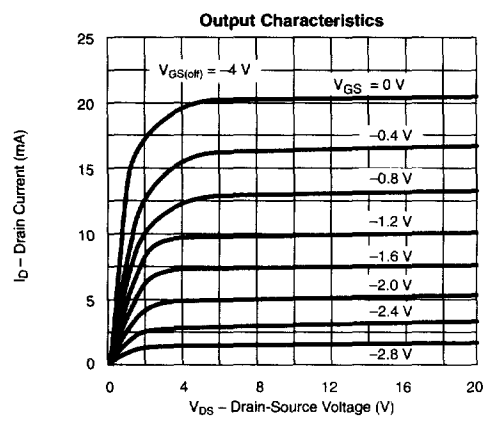
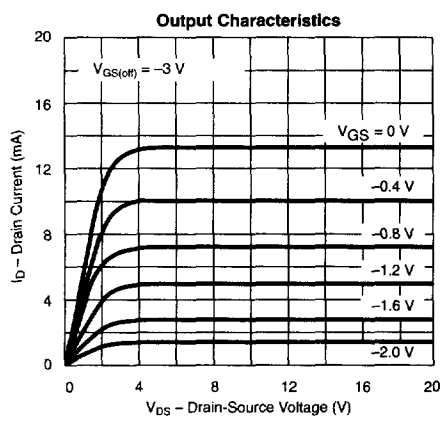
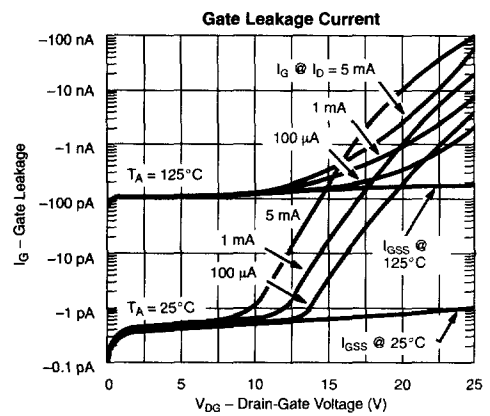
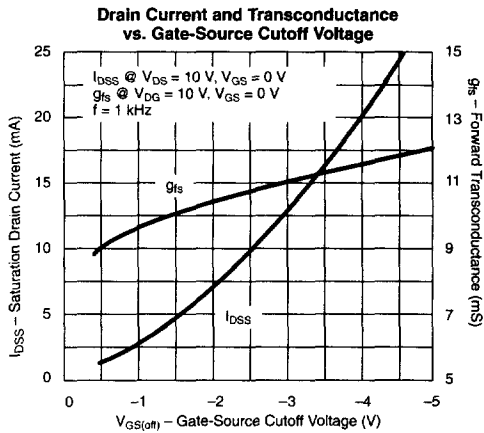
Notes

- a. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
 b. Pulse test: $PW \leq 300\ \mu\text{s}$ duty cycle $\leq 3\%$.
 c. Assumes smaller value in the numerator.

NNZ

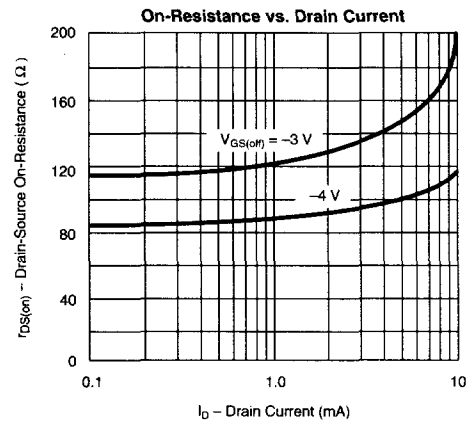
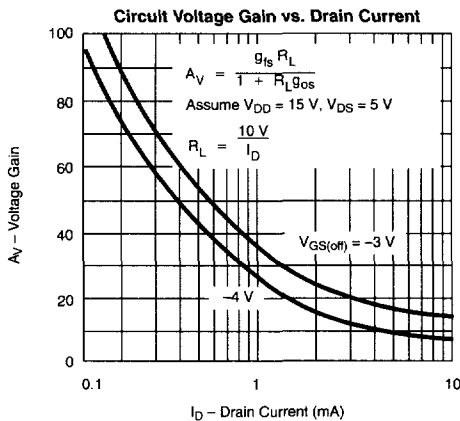
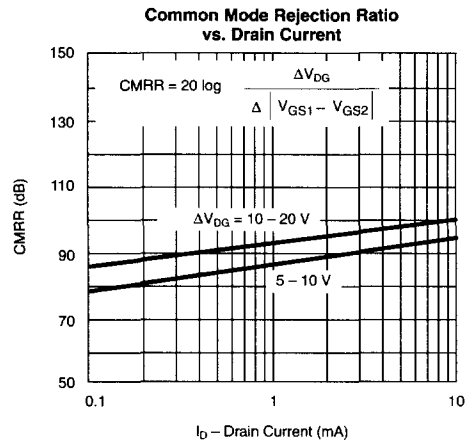
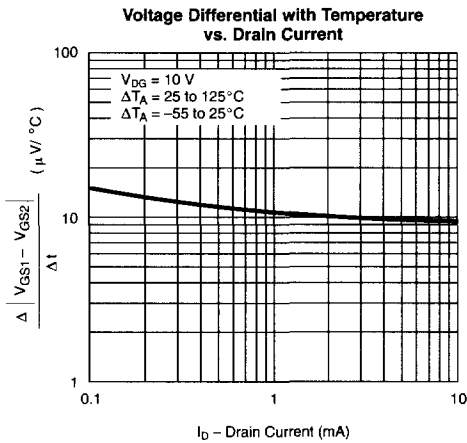
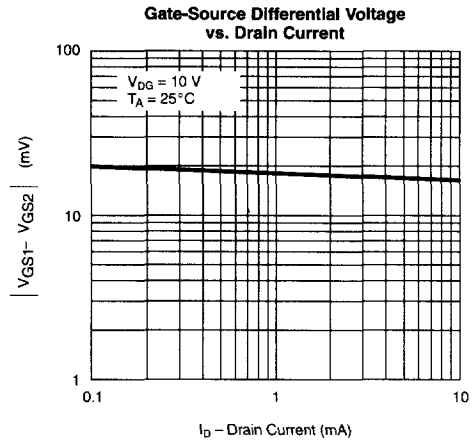
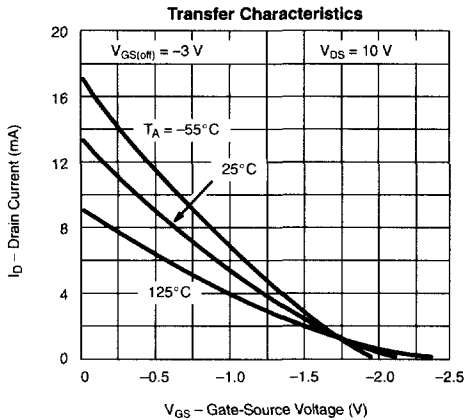


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