TENTATIVE TOSHIBA MOS DIGITAL INTEGRATED CIRCUIT SILICON GATE CMOS

1,048,576-WORD BY 18-BIT SYNCHRONOUS DDR STATIC RAM

DESCRIPTION

The TC55YK1618AYB is a 18,874,368-bit synchronous static random access memory (SRAM) organized as 1,048,576 words by 18 bits. It is designed for use as a secondary cache in applications where high speed operation is required.

The TC55YK1618AYB is a double data rate (DDR) SRAM which transfers read/write data in response to both the rising edge and falling edge of the clock. The TC55YK1618AYB can also operate at single data rate and operations are dynamically controlled by the control inputs (B1, B2, B3).

TC55YK1618AYB uses an HSTL (high speed transceiver logic) interface to minimize switching noise and power consumption in the output buffers.

The TC55YK1618AYB uses single power supply (1.8 V) and is available in a 153-bump ball grid array (BGA) package which is suitable for high-density surface mounting.

FEATURES

- Organized as 1M words × 18 bits.
- Fast cycle time of 4 ns minimum
  Clock: 400 MHz maximum
  Data: 800 MHz maximum
- Fast access time of 1.8 ns maximum (from clock edge to echo clock edge)
- Differential clock inputs
- Complement echo clock outputs
- Double data rate or single data rate Operations
- Synchronous self-timed write
- Full data coherency
- Programmable impedance output buffer
- Interleaved burst or linear burst sequences
- Stop-clock standby
- HSTL interface
- JTAG boundary scan
- Available in 153-bump BGA package (C-BGA153-1422-1.27BZF, Weight : 2.00 grams(typical))
- Power Supply : $V_{DD} = V_{DDQ} = 1.8\ V \pm 0.09\ V\ (\pm 5\%)$

PIN ASSIGNMENT (TOP VIEW)

	1	2	3	4	5	6	7	8	9
A	V_{SS}	V_{DDQ}	A11	A10	ZQ	A9	A8	V_{DDQ}	V_{SS}
B	NC	I/O10	A12	V_{SS}	B1	V_{SS}	A7	NC	I/O9
C	V_{SS}	V_{DDQ}	A14	A13	$\overline{G}$	A6	A5	V_{DDQ}	V_{SS}
D	I/O11	NC	A19	V_{SS}	V_{DD}	V_{SS}	A18	I/O8	NC
E	V_{SS}	V_{DDQ}	V_{SS}	V_{DD}	VREF	V_{DD}	V_{SS}	V_{DDQ}	V_{SS}
F	NC	CQ	NC	V_{DD}	V_{DD}	V_{DD}	I/O7	NC	I/O6
G	V_{SS}	V_{DDQ}	V_{SS}	V_{SS}	CK	V_{SS}	V_{SS}	V_{DDQ}	V_{SS}
H	I/O13	NC	I/O12	V_{DD}	$\overline{CK}$	V_{DD}	NC	I/O5	NC
J	V_{SS}	V_{DDQ}	V_{SS}	V_{DD}	V_{DD}	V_{DD}	V_{SS}	V_{DDQ}	V_{SS}
K	NC	I/O14	NC	V_{SS}	B2	V_{SS}	I/O3	NC	I/O4
L	V_{SS}	V_{DDQ}	V_{SS}	$\overline{LBO}$	B3	V_{SS}	V_{SS}	V_{DDQ}	V_{SS}
M	I/O15	NC	I/O16	V_{DD}	V_{DD}	V_{DD}	NC	$\overline{CQ}$	NC
N	V_{SS}	V_{DDQ}	V_{SS}	V_{DD}	VREF	V_{DD}	V_{SS}	V_{DDQ}	V_{SS}
P	NC	I/O17	A17	V_{SS}	V_{DD}	V_{SS}	A4	NC	I/O2
R	V_{SS}	V_{DDQ}	V_{DD}	A15	A1	A2	V_{DD}	V_{DDQ}	V_{SS}
T	I/O18	NC	A16	V_{SS}	A0	V_{SS}	A3	I/O1	NC
U	V_{SS}	V_{DDQ}	TMS	TDI	TCK	TDO	NC	V_{DDQ}	V_{SS}

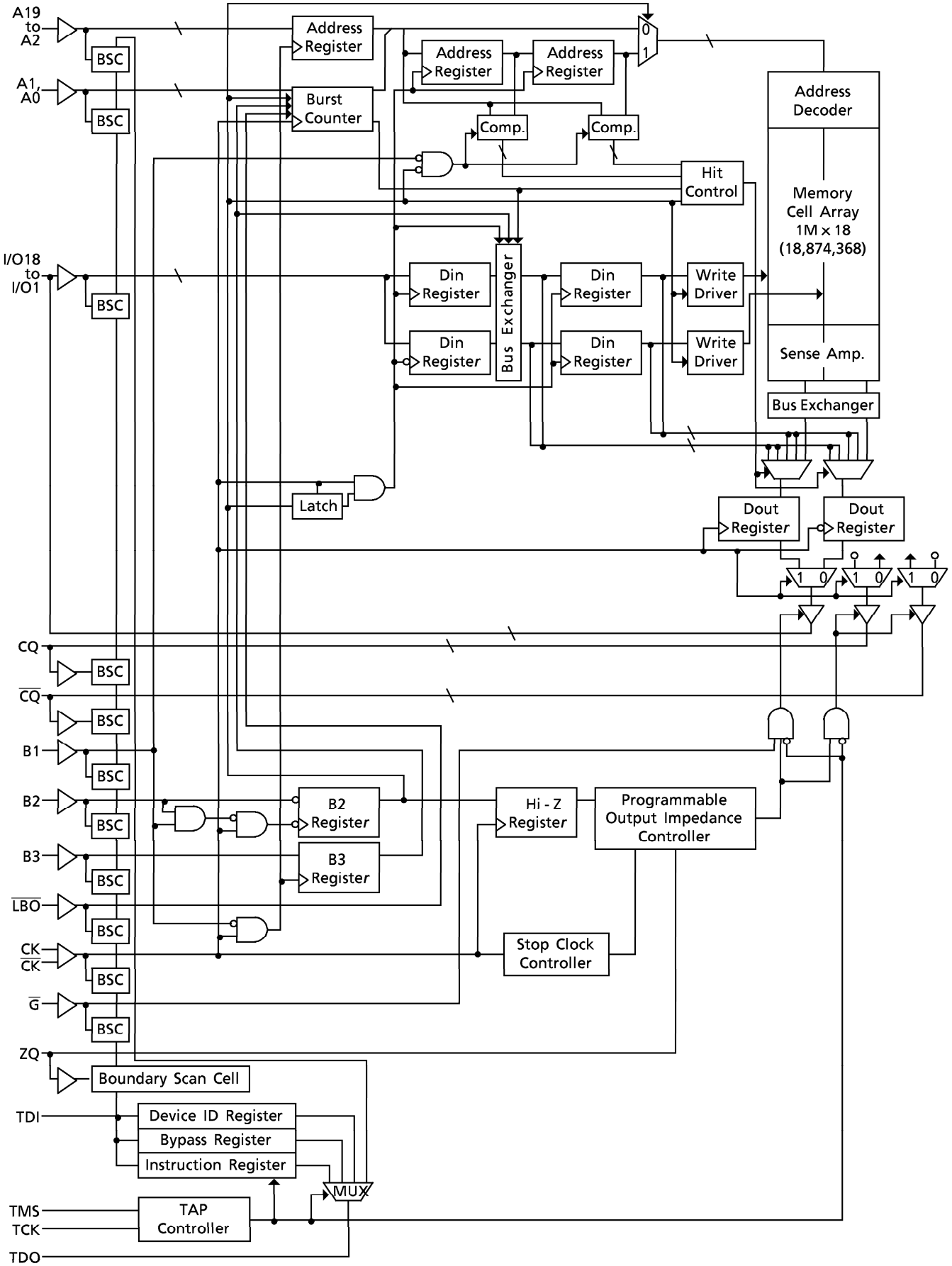
PIN NAMES

A0 to A19	Address Inputs
I/O1 to I/O18	Data Inputs / Outputs
VREF	Reference Voltage Input
CK, $\overline{CK}$	Differential Clock Inputs
B1, B2, B3	Control Inputs
CQ, $\overline{CQ}$	Complement Echo Clock Outputs
$\overline{G}$	Output Enable Input
ZQ	Output Buffer Impedance Control Input
$\overline{LBO}$	Burst Order Select Input
V_{DD}	Power Supply (1.8 V)
V_{DDQ}	Output Power Supply (1.8 V)
V_{SS}	Ground
NC	No Connection
TMS, TDI, TCK, TDO	Boundary Scan Test Access Ports

⟨The information contained herein is subject to change without notice.⟩

000707EBA2

BLOCK DIAGRAM



PIN DESCRIPTIONS

PIN NUMBER	SYMBOL	TYPE	DESCRIPTION
5T, 5R, 6R, 7T, 7P, 7C, 6C, 7B, 7A, 6A, 4A, 3A, 3B, 4C, 3C, 4R, 3T, 3P, 7D, 3D	A0 to A19	Input (synchronous)	**Address Inputs** Registered on the rising edge of CK (falling edge of $\overline{CK}$).
8T, 9P, 7K, 9K, 8H, 9F, 7F, 8D, 9B, 2B, 1D, 3H, 1H, 2K, 1M, 3M, 2P, 1T	I/O1 to I/O18	Input/Output (synchronous)	**Data Inputs/ Outputs** Write data are registered on both the rising and falling edges of CK (both the falling and rising edges of $\overline{CK}$) in double data rate operation. In single data rate operation, write data are registered on the rising edge of CK (the falling edge of $\overline{CK}$).
5E, 5N	VREF	Input	**Reference Voltage Input** for input buffers. The inputs must be tied together.
5G, 5H	CK, $\overline{CK}$	Differential Input	**Differential Reference Clock** for both input and output signals. $\overline{CK}$ clock input must be the complement of the CK clock input.
5B, 5K, 5L	B1, B2, B3	Input (synchronous)	**Control Input** Registered on the rising edge of CK (falling edge of $\overline{CK}$). These inputs control the chip operations according to the truth table and the bus state diagram.
2F, 8M	CQ, $\overline{CQ}$	Complement Output (synchronous)	**Echo Clock Output** Echoes the reference clock (CK, $\overline{CK}$) when the reference clock is running regardless of read/write operations.
5C	$\overline{G}$	Input (asynchronous)	**Output Enable Input**
5A	ZQ	Input	**Output Impedance Control Input** Output buffer impedance is programmed using an external resistor connected between the ZQ and V_{SS} pins. The value of the resistor should be five times the expected output buffer impedance.
4L	$\overline{LBO}$	Input	**Burst Sequence Select Input** If High, the burst sequence is an interleaved burst. If Low, the burst sequence is a linear burst. Do not alter the input state during operation.
3U, 4U, 5U	TMS, TDI, TCK	Input (synchronous)	**Test Inputs for Test Access Port**
6U	TDO	Output (synchronous)	**Test Data Output from Test Access Port**
3R, 4E, 4F, 4H, 4J, 4M, 4N, 5D, 5F, 5J, 5M, 5P, 6E, 6F, 6H, 6J, 6M, 6N, 7R	V_{DD}	Supply	**Power Supply** (1.8 V)
2A, 2C, 2E, 2G, 2J, 2L, 2N, 2R, 2U, 8A, 8C, 8E, 8G, 8J, 8L, 8N, 8R, 8U	V_{DDQ}	Supply	**Output Buffer Power Supply** (1.8 V)

PIN DESCRIPTIONS (CONTINUED)

PIN NUMBER	SYMBOL	TYPE	DESCRIPTION
1A, 1C, 1E, 1G, 1J, 1L, 1N, 1R, 1U, 3E, 3G, 3J, 3L, 3N, 4B, 4D, 4G, 4K, 4P, 4T, 6B, 6D, 6G, 6K, 6L, 6P, 6T, 7E, 7G, 7J, 7L, 7N, 9A, 9C, 9E, 9G, 9J, 9L, 9N, 9R, 9U	V_{SS}	Ground	**Ground** All V_{SS} inputs must be connected to ground level.
1B, 1F, 1K, 1P, 2D, 2H, 2M, 2T, 3F, 3K, 7H, 7M, 7U, 8B, 8F, 8K, 8P, 9D, 9H, 9M, 9T	NC	—	**No connection** There is a ball for each pin but it is not connected.

OPERATING MODES

(1) Synchronous Input Truth Table

OPERATION	CK (n)	B1 (n)	B2 (n)	B3 (n)	I/O1 to I/O18	
					CK (n + 1) ↑	CK (n + 1) ↓
Load External Address, Double Data Write	L→H	L	L	L	Din	Din
Load External Address, Single Data Write	L→H	L	L	H	Din	×
Load External Address, Double Data Read	L→H	L	H	L	Dout	Dout
Load External Address, Single Data Read	L→H	L	H	H	Dout	Previous data held
NOP, Pipeline Hi-Z	L→H	H	L	×	Hi - Z	Hi - Z
Increment Internal Burst Address, Continue Previous Operation	L→H	H	H	×	Dout (n) or Din (n)	
Stop-Clock Standby [5)]	L	×	×	×	Hi - Z or Dout	

Notes: 1. H means logical High and L means logical Low. × means Don't Care.
2. (n) and (n+1) indicate the n-th cycle and (n+1)-th cycle. ↑ and ↓ mean the rising edge and falling edge respectively.
3. $\overline{CK}$ is the complement of CK.
4. Operation is controlled according to the bus cycle state diagram.
5. Stop-clock standby
The TC55YK1618AYB has a stop clock standby circuit for reducing power dissipation. The TC55YK1618AYB enters Standby mode when the clock is stopped in the specified state (CK = Low and $\overline{CK}$ = High). Any write cycle is not allowed at the cycle just prior to stop clock. In the Stop-Clock state, the echo clock outputs (CQ, $\overline{CQ}$) are held active. When the TC55YK1618AYB is woken up from Standby mode by restarting the clock, a recovery time of at least 2 clocks is required.

(2) Asynchronous Truth Table

OPERATION	$\overline{G}$	I/O1 to I/O18
Write	×	Din, Hi - Z
Read	L	Dout
	H	Hi - Z
Stop-clock standby	L	Dout
	H	Hi - Z

(3) Burst Address Sequence

The TC55YK1618AYB has a burst counter circuit for Burst Read and Burst Write operations. The TC55YK1618AYB supports both interleaved burst and linear burst sequences using $\overline{LBO}$. The internal burst address is incremented on the rising edge of CK at the single data rate and on both the rising and falling edges of CK at the double data rate. The burst length is controlled by an interval of an assertion of B1 = L. A mode mixing between single and double data mode during burst is not allowed.

Bit Order: A_{19} A_{18} ..... A_3 A_2 A_1 A_0
The lower 2 bits are internally generated from the external address.
The burst address wraps around to its initial state after 4 counts.

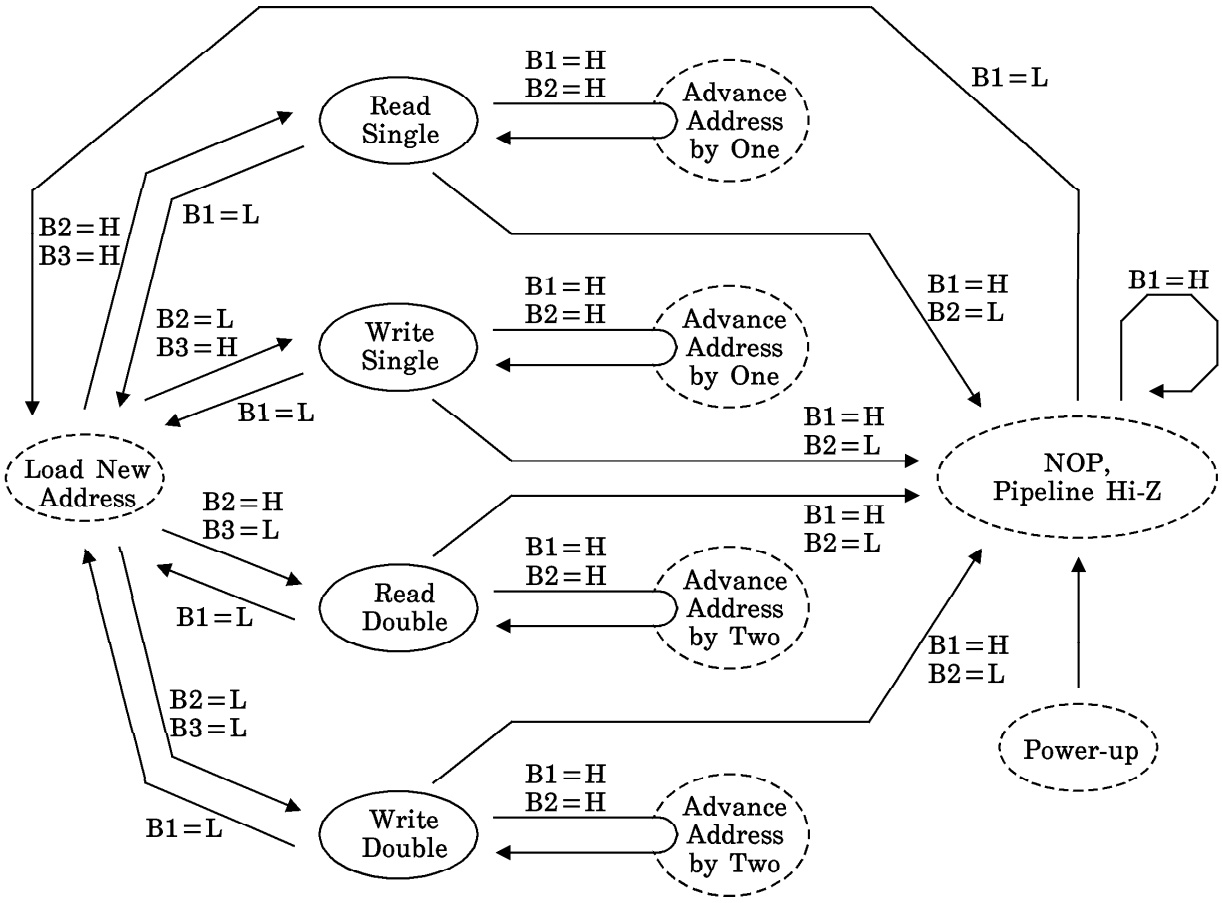
Interleaved burst sequence ($\overline{LBO}$ = H)

1st Address	2nd Address	3rd Address	4th Address
XX ····· XX00	XX ····· XX01	XX ····· XX10	XX ····· XX11
XX ····· XX01	XX ····· XX00	XX ····· XX11	XX ····· XX10
XX ····· XX10	XX ····· XX11	XX ····· XX00	XX ····· XX01
XX ····· XX11	XX ····· XX10	XX ····· XX01	XX ····· XX00

Linear burst sequence ($\overline{LBO}$ = L)

1st Address	2nd Address	3rd Address	4th Address
XX ····· XX00	XX ····· XX01	XX ····· XX10	XX ····· XX11
XX ····· XX01	XX ····· XX10	XX ····· XX11	XX ····· XX00
XX ····· XX10	XX ····· XX11	XX ····· XX00	XX ····· XX01
XX ····· XX11	XX ····· XX00	XX ····· XX01	XX ····· XX10

BUS CYCLE STATE DIAGRAM



Notes: 1. ⬭ indicates a transition stage, and does not take up a cycle.
2. The burst address wraps around to its initial state after 4 counts.
3. No NOP is necessary when the bus changes from Write to Read.
4. At least 1 NOP is necessary when the bus changes from Read to Write when $\overline{G}$ is fixed Low.

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{DD}	Power Supply Voltage	– 0.5 to 2.5	V
V_{DDQ}	Output Buffer Power Supply Voltage	– 0.5 to V_{DD} + 0.5 (2.5V maximum)	V
V_{IN}	Input Terminal Voltage	– 0.5* to 2.5	V
$V_{I/O}$	Input / Output Terminal Voltage	– 0.5 * to V_{DDQ} + 0.5** (2.5V maximum)	V
P_D	Power Dissipation	2.1	W
T_{strg}	Storage Temperature	– 55 to 125	°C
T_{opr}	Operating Temperature	– 10 to 85	°C

* : −1 V with a pulse width of 20% · t_{KHKH} minimum (1.0 ns maximum)
** : V_{DDQ} + 1 V with a pulse width of 20% · t_{KHKH} minimum (1.0 ns maximum)

DC RECOMMENDED OPERATING CONDITIONS (Ta = 0 to 70°C)

(1) DC Supply Voltage

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
V_{DD}	Power Supply Voltage	1.71	1.8	1.89	V
V_{DDQ}	Output Buffer Power Supply Voltage	1.71	1.8	1.89	V
VREF	Input Reference Voltage	0.68	0.9	1.0	V

Note: 1. Peak-to-peak AC noise on VREF may not exceed 2% Vref (DC).

(2) Single-ended Inputs

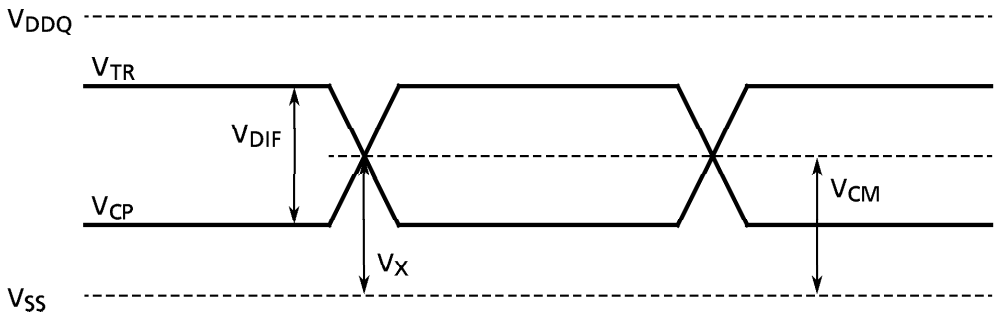
SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
V_{IH}	Input High Voltage	VREF + 0.1	–	V_{DDQ} + 0.3**	V
V_{IL}	Input Low Voltage	– 0.3*	–	VREF – 0.1	V
$V_{IH - I/O}$	Input High Voltage for I/O	VREF + 0.1	–	V_{DDQ} + 0.3**	V
$V_{IL - I/O}$	Input Low Voltage for I/O	– 0.3*	–	VREF – 0.1	V

* : −0.5 V with a pulse width of 20% · t_{KHKH} minimum (1.0 ns maximum)
** : V_{DDQ} + 0.5 V with a pulse width of 20% · t_{KHKH} minimum (1.0 ns maximum)

(3) Differential Inputs (CK, $\overline{CK}$)

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
V_{IN}	Input Signal Voltage	– 0.3	–	V_{DDQ} + 0.3	V
V_{DIF}	Differential Input Voltage	0.2	–	V_{DDQ} + 0.6	V
V_{CM}	Common Mode Input Voltage	0.6	–	1.1	V
V_X	Differential Cross Point Voltage	0.6	0.9	1.0	V

Notes: 1. V_{DIF} specifies the maximum input differential voltage (V_{TR}-V_{CP}) required for switching, where V_{TR} is the "true" input level and V_{CP} is the "complement" of the input level.
2. V_{CM} specifies the maximum allowable range of (V_{TR} + V_{CP})/ 2.
3. V_X specifies the voltage at which differential input signals must cross.
4. The CK and $\overline{CK}$ click inputs must be used as differential inputs..



(4) Static Inputs

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
V_{IH1}	Input Voltage for $\overline{LBO}$ Pin	V_{DD} – 0.3	V_{DD}	V_{DD} + 0.3	V
V_{IL1}	Input Voltage for $\overline{LBO}$ Pin	– 0.3	0.0	0.3	V

Note: The $\overline{LBO}$ pin must not be changed during operation.

DC CHARACTERISTICS (Ta = 0 to 70°C, $V_{DD} = V_{DDQ} = 1.8\ V \pm 0.09\ V\ (\pm 5\%)$)

SYMBOL	PARAMETER	TEST CONDITION		MIN	TYP	MAX	UNIT
I_{IL}	Input Leakage Current	$V_{IN} = 0$ to V_{DD}		– 10	–	10	μA
I_{LO}	Output Leakage Current	Write Status, or $\overline{G} = V_{IH}$, $V_{OUT} = 0$ to V_{DDQ}		– 10	–	10	μA
V_{OH}	Output High Voltage	$I_{OH} = -(V_{DDQ}/2) / (RQ/5) \pm 15\%$ & $RQ = 250\ \Omega$		$V_{DDQ}/2$	–	V_{DDQ}	V
		$I_{OH} = -100\ \mu A$		$V_{DDQ} - 0.2$	–	V_{DDQ}	
V_{OL}	Output Low Voltage	$I_{OL} = (V_{DDQ}/2) / (RQ/5) \pm 15\%$ & $RQ = 250\ \Omega$		0.0	–	$V_{DDQ}/2$	V
		$I_{OL} = 100\ \mu A$		0.0	–	0.2	
$I_{DDO}S$	Operating Current [1), 2)]	Read or Write Status, Single, $I_{OUT} = 0$ mA, All Inputs = 1.5 V/0.3 V, Clock ≧ t_{KHKH} Minimum	2.5 ns			1000	mA
			3.0 ns	–	–	850	
			4.0 ns	–	–	650	
$I_{DDO}D$		Read or Write Status, Double, $I_{OUT} = 0$ mA, All Inputs = 1.5 V/0.3 V, Clock ≧ t_{KHKH} Minimum	2.5 ns			1000	mA
			3.0 ns	–	–	850	
			4.0 ns	–	–	650	
I_{DDS}	Stop-Clock Standby Current	CK = 0.2 V, $\overline{CK} = V_{DDQ} - 0.2$ V, Read Status Double or Single, All Inputs = $V_{DD} - 0.2$ V or 0.2 V		–	–	100	mA

Notes: 1. Operating current is calculated with 50% Read cycles and 50% Write cycles.
2. Refer to AC test conditions for input level.

PROGRAMMABLE IMPEDANCE OUTPUT BUFFER DC CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
RQ	RQ Resistor	–	175	–	350	Ω
Buffer - Z	Output Buffer Impedance	Measured at $V_{DDQ}/2$	(RQ/5) – 15%	–	(RQ/5) + 15%	Ω

Note: The TC55YK1618AYB has programmable impedance output buffers which can be programmed to between 35 Ω and 70 Ω. The impedance is programmed by connecting an external RQ resistor between ZQ and V_{SS} which is 5 times the intended output impedance. The output impedance is periodically updated while the output is Hi-Z due to the NOP or Write cycle. The output impedance of the echo outputs (CQ, $\overline{CQ}$) are also updated during the NOP or Write cycle. The TC55YK1618AYB requires at least 256 NOP cycles after power-up to adjust the output impedance to the intended value.

CAPACITANCE (Ta = 25°C, f = 1.0 MHz)

SYMBOL	PARAMETER	TEST CONDITION	MAX	UNIT
C_{IN}	Input Capacitance	$V_{IN} = V_{SS}$	6	pF
$C_{I/O}$	Input/Output Capacitance	$V_{I/O} = V_{SS}$	8	pF

Note: This parameter is periodically sampled and is not tested for every device.

AC CHARACTERISTICS

(Ta = 0 to 70°C, V_{DD} = 1.8 V ± 0.09 V(± 5%))

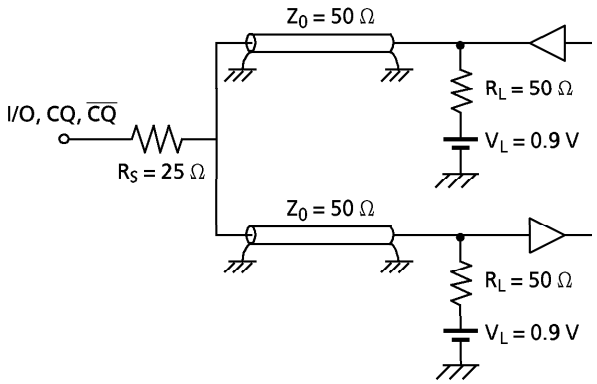
SYMBOL	PARAMETER	TC55YK1618AYB-800		TC55YK1618AYB-666		TC55YK1618AYB-500		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{KHKH}	Clock (CK, $\overline{CK}$) Cycle Time	2.5	–	3.0	–	4.0	–	ns
t_{KHKL}	Clock (CK, $\overline{CK}$) High Pulse Width	1.2	–	1.4	–	1.6	–	
t_{KLKH}	Clock (CK, $\overline{CK}$) Low Pulse Width	1.2	–	1.4	–	1.6	–	
t_{CHCL}	CQ High Pulse Width	t_{KHKL} – 0.1	t_{KHKL} + 0.1	t_{KHKL} – 0.1	t_{KHKL} + 0.1	t_{KHKL} – 0.1	t_{KHKL} + 0.1	
t_{CLCH}	CQ Low Pulse Width	t_{KLKH} – 0.1	t_{KLKH} + 0.1	t_{KLKH} – 0.1	t_{KLKH} + 0.1	t_{KLKH} – 0.1	t_{KLKH} + 0.1	
t_{KHCH} t_{KLCL}	CK High to CQ High CK Low to CQ Low	–	1.8	–	1.9	–	2.3	
t_{CHQV} t_{CLQV}	CQ High to Output Valid CQ Low to Output Valid	–	0.2	–	0.2	–	0.3	
t_{CHQX} t_{CLQX}	CQ High to Output Hold CQ Low to Output Hold	– 0.2	–	– 0.2	–	– 0.4	–	
t_{CHQLZ}	CQ High to Output Low-Z	– 0.2	–	– 0.2	–	– 0.4	–	
t_{CHQHZ}	CQ High to Output High-Z	–	0.2	–	0.2	–	0.3	
t_{GLQV}	$\overline{G}$ Low to Output Valid	–	2.0	–	2.0	–	2.3	
t_{GHQX}	$\overline{G}$ High to Output Hold	0	–	0	–	0	–	
t_{GLQLZ}	$\overline{G}$ Low to Output Low-Z	0	–	0	–	0	–	
t_{GHQHZ}	$\overline{G}$ High to Output High-Z	–	2.0	–	2.0	–	2.3	
t_S	Input Setup Time from Clock (CK, $\overline{CK}$)	0.3	–	0.4	–	0.5	–	
t_{DS}	Data Setup Time from Clock (CK, $\overline{CK}$)	0.25	–	0.3	–	0.5	–	
t_H	Input Hold Time from Clock (CK, $\overline{CK}$)	0.3	–	0.4	–	0.5	–	
t_{DH}	Data Hold Time from Clock (CK, $\overline{CK}$)	0.25	–	0.3	–	0.5	–	

Notes: 1. The operating temperature (Ta) is guaranteed while a transverse air flow exceeding 400 linear feet per minute is flowing.
2. Do not apply opposite phase data to the I/O pins when they are in the Output state.
3. Output Low-Z and output High-Z times are measured at ±200 mV from the steady-state voltage.

AC TEST CONDITIONS

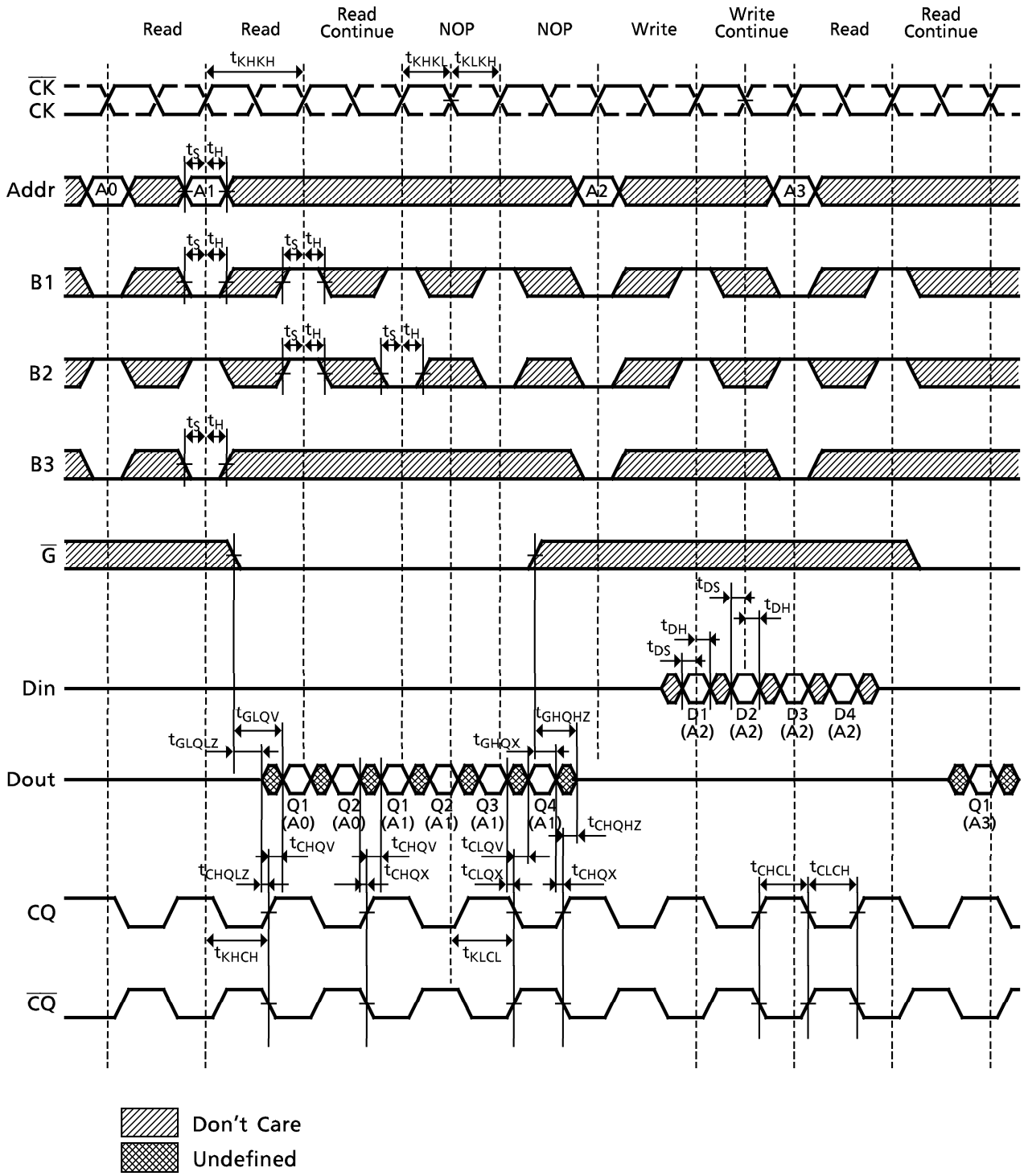
Input Pulse Level	1.5 V/0.3 V
Input Pulse Rise and Fall Time	0.5 ns
Input Timing Measurement Reference Level	0.9 V
Output Timing Measurement Reference Level	0.9 V
Output Buffer Power Supply (V_{DDQ})	1.8 V
Refernce Voltage Input (VREF)	0.9 V
Output Buffer Impedance	50 Ω (RQ = 250 Ω)
Output Load	Fig. 1

Fig. 1



TIMING DIAGRAMS

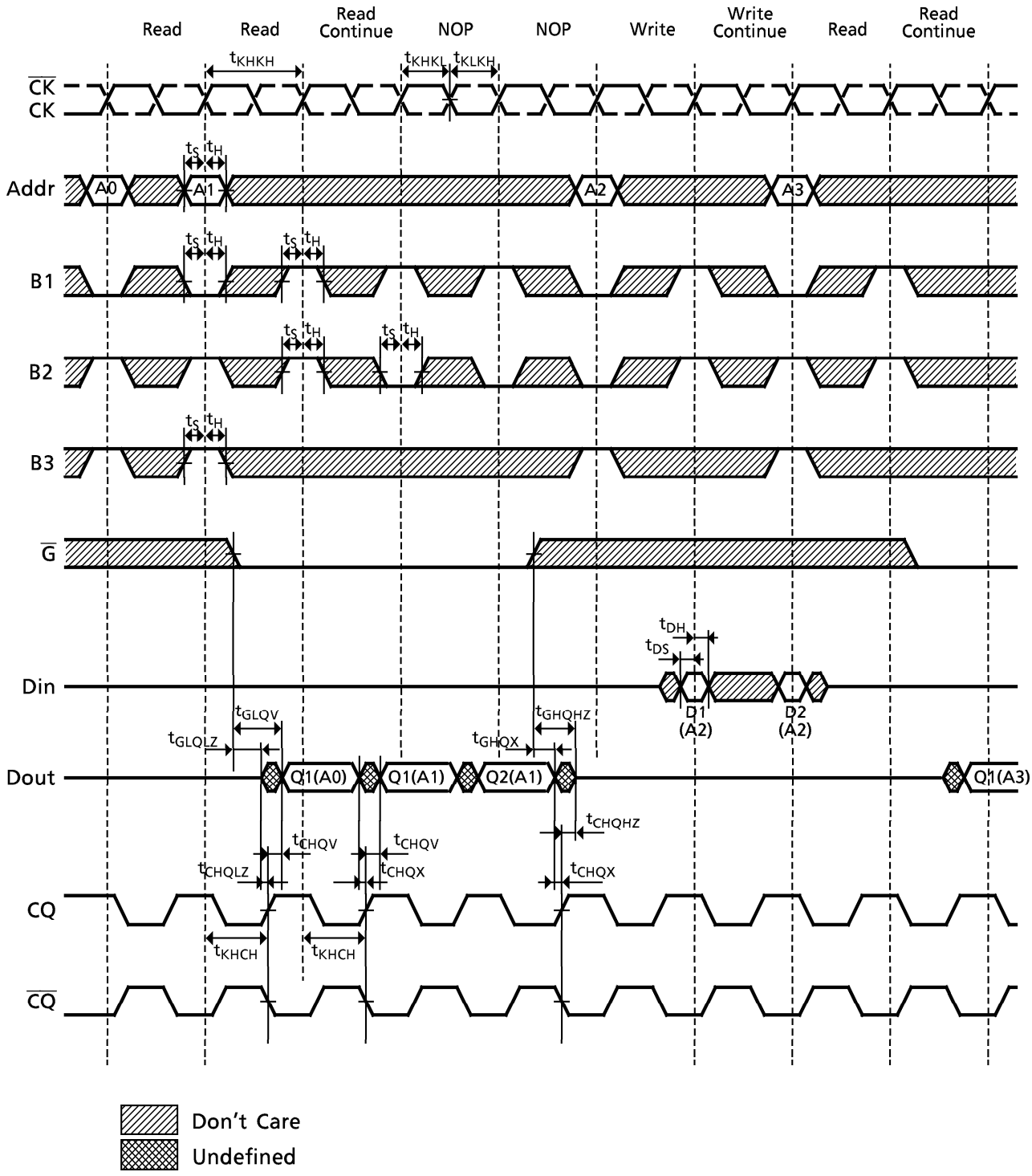
(1) READ/ WRITE CYCLE (DOUBLE DATA RATE)



Notes:

1. D1(A2) represents input data for 1st burst address starting from address A2.
   D2(A2) represents input data for 2nd burst address starting from address A2.
2. Q1(A1) represents output data from 1st burst address starting from address A1.
   Q2(A1) represents output data from 2nd burst address starting from address A1.
3. The 2nd NOP is not necessary if the bus turn-around time is long enough.

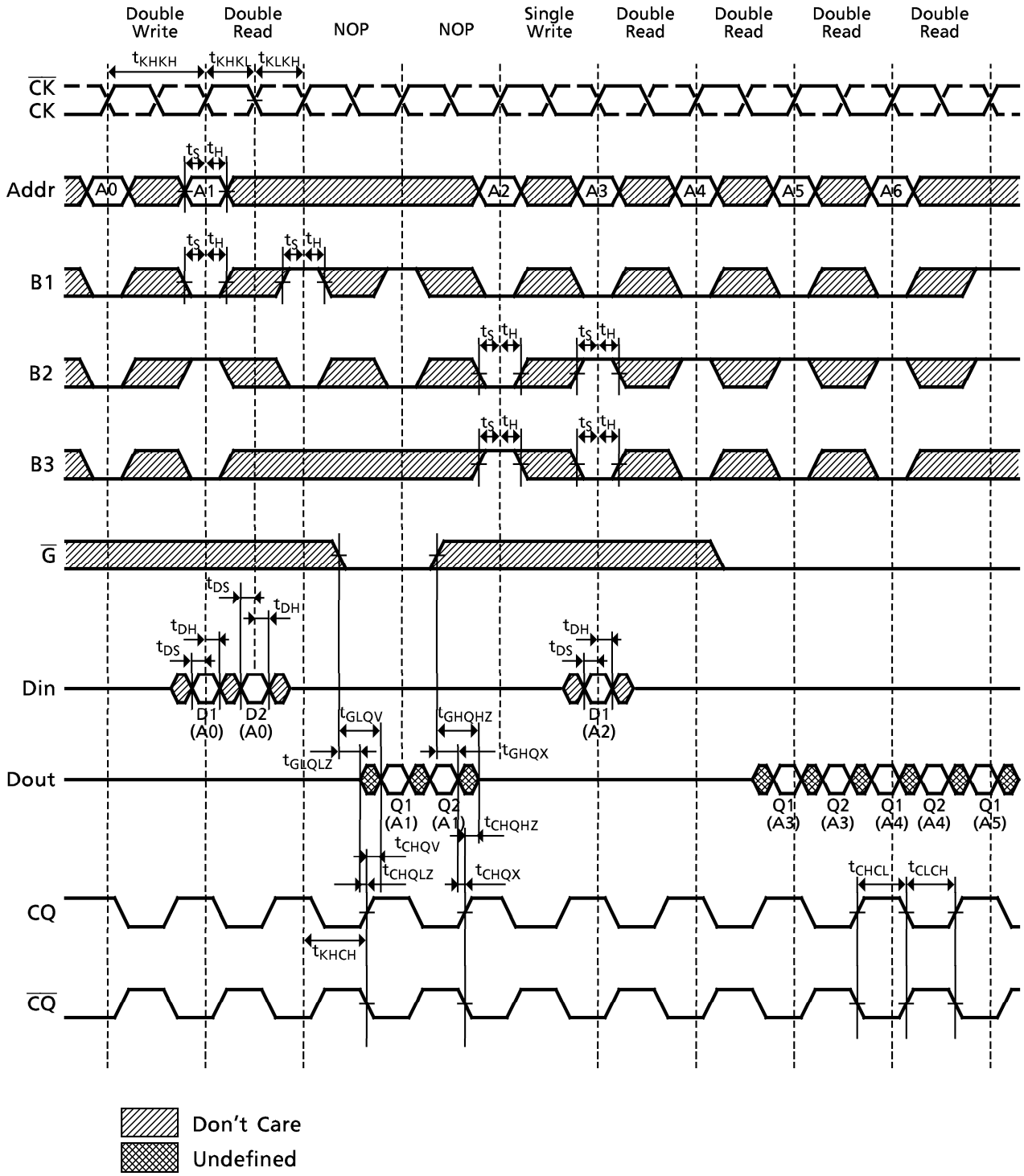
(2) READ/ WRITE CYCLE (SINGLE DATA RATE)



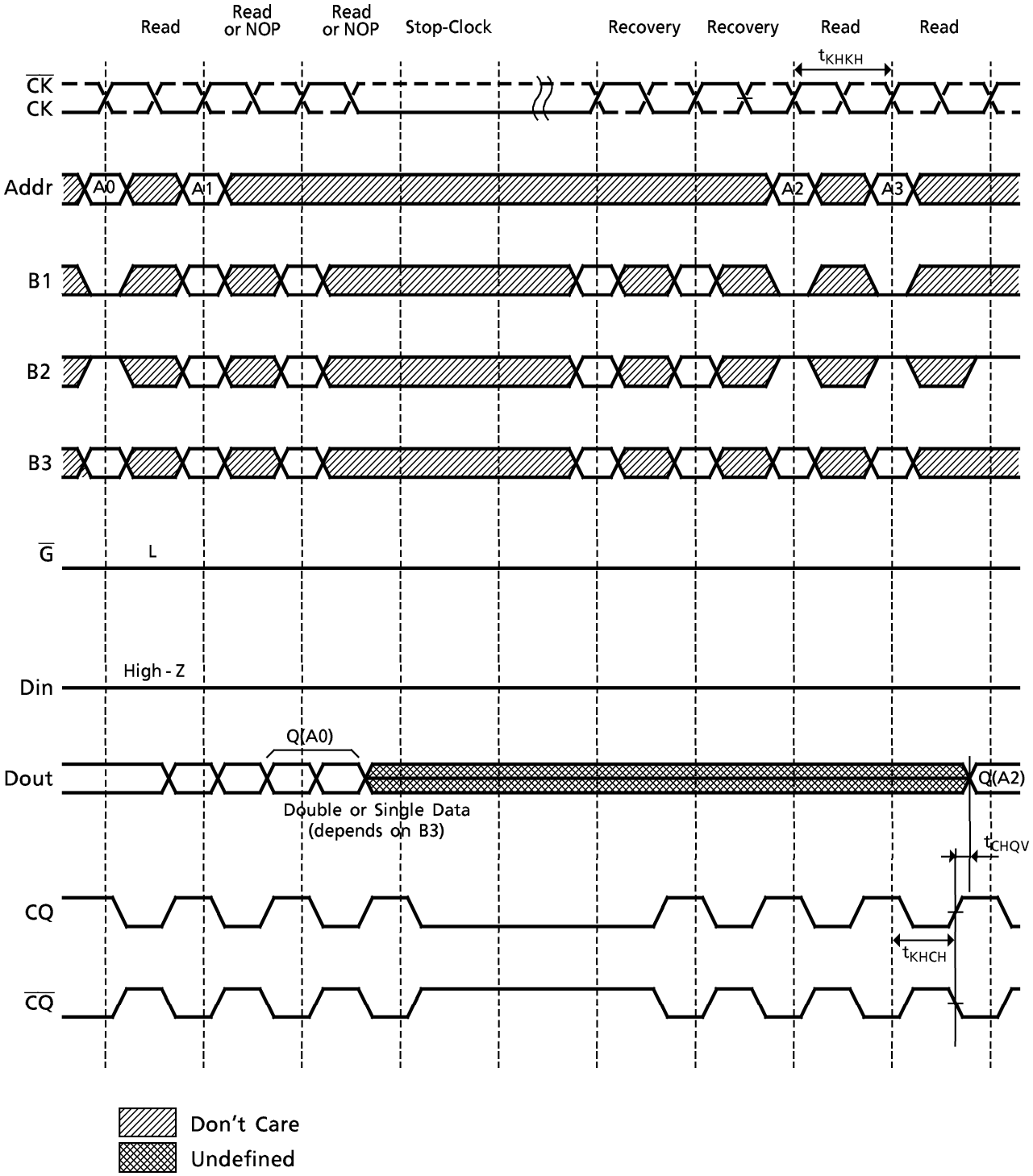
Notes:

1. D1(A2) represents input data for 1st burst address starting from address A2.
   D2(A2) represents input data for 2nd burst address starting from address A2.
2. Q1(A1) represents output data from 1st burst address starting from address A1.
   Q2(A1) represents output data from 2nd burst address starting from address A1.
3. The 2nd NOP is not necessary if the bus turn-around time is long enough.

(3) READ/ WRITE CYCLE (DOUBLE AND SINGLE DATA RATE MIXED)



(4) STOP-CLOCK CYCLE



Notes: The TC55YK1618AYB has a stop clock standby circuit for reducing power dissipation. The TC55YK1618AYB enters Standby mode when the clock is stopped in the specified state (CK = Low and $\overline{CK}$ = High). Any write cycle is not allowed at the cycle just prior to stop clock. In the Stop-Clock state, the echo clock outputs (CQ, $\overline{CQ}$) are held active. When the TC55YK1618AYB is woken up from Standby mode by restarting the clock, a recovery time of at least 2 clocks is required.

BOUNDARY SCAN TEST ACCESS PORT OPERATIONS

The TC55YK1618AYB has a serial boundary scan test access port (TAP) which is compatible with IEEE Standard 1149.1 - 1990, but which does not implement all the functions required for 1149.1 - 1990 compliance. TCK must be tied to V_{SS} or V_{DD} to disable the TAP when TAP operation is not required.

Test Access Port Signals

SYMBOL	DESCRIPTION	
TCK	Test Clock Input	All Test Access Port inputs are sampled on the rising edge of TCK. To disable the TAP, TCK must be tied to V_{SS} or V_{DD}.
TMS	Test Mode Select Input	The signal presented at TMS is sampled on the rising edge of TCK. This input is internally pulled up so as to recognize a floating input as a logical High (Test-Logic-Reset).
TDI	Test Data Input	Values presented at TDI are clocked into the selected register on the rising edge of TCK. This input is internally pulled up. This enables detection of when the TDI input to the board is open-circuit.
TDO	Test Data Output	TDO is the serial output for test instructions and data from the test logic. This output is controlled by the falling edge of TCK.

Test Access Port Registers

REGISTER		SYMBOL	LENGTH (bits)	DESCRIPTION
Instruction Register		IR [2 : 0]	3	The Instruction register controls five states (EXTEST, Sample-Z, Sample, Bypass, ID code).
Test Data Register				
	ID Register	IDR [31 : 0]	32	The register includes information on revision number, organization and TOSHIBA ID number.
	Bypass Register	BR	1	The register connects TDI and TDO.
	Boundary Scan Register	BSR [48 : 0]	49	The Boundary Scan register is comprised of boundary scan cells at each input and I/O pin. The BSCs are serially connected between TDI and TDO.

TAP Controller Instruction Set

IR2	IR1	IR0	INSTRUCTION	DESCRIPTION
0	0	0	EXTEST	Moves the Preloaded data on to the output pins. Samples the inputs connected to the BSCs.
0	0	1	ID CODE	Access ID code.
0	1	0	SAMPLE - Z	Tristates the RAM outputs and samples the inputs connected to the BSCs.
0	1	1	RESERVED	This instruction is reserved for future use.
1	0	0	SAMPLE	Samples the inputs connected to the BSCs. Load the sampled data at I/Os to the parallel output of the BSCs. Does not affect RAM operation.
1	0	1	RESERVED	This instruction is reserved for future use.
1	1	0	RESERVED	This instruction is reserved for future use.
1	1	1	BYPASS	Bypassse TDI and TDO using the Bypass register.

The first bit to be scanned into TDI is taken to be the least significant bit (IR0).

ID Register

BIT #	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Value	0	0	1	0	0	1	0	1	0	1	0	1	1	0	0	1	0	0	0	1	0	0	0	1	0	0	1	1	0	0	0	1
Content	Memory Type																				TOSHIBA ID number											Fix -ed

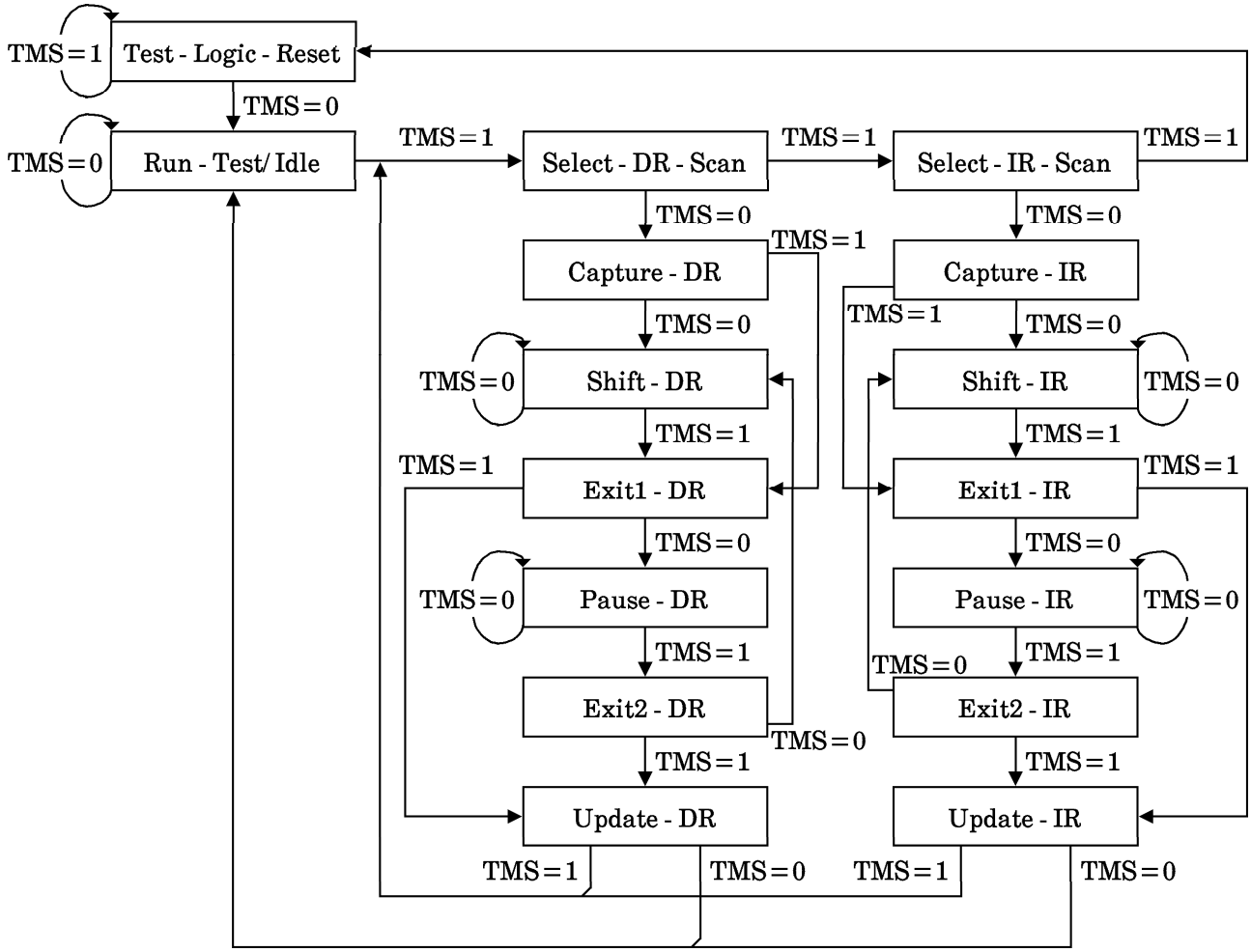
Boundary Scan Order

BIT #	BUMP LOCATION	SYMBOL
0	5R	A1
1	5T	A0
2	6R	A2
3	7T	A3
4	7P	A4
5	8T	I/O1
6	9P	I/O2
7	8M	$\overline{CQ}$
8	7K	I/O3
9	9K	I/O4
10	6L	V_{SS}
11	5H	$\overline{CK}$
12	5G	CK
13	5C	$\overline{G}$
14	8H	I/O5
15	9F	I/O6
16	7F	I/O7
17	8D	I/O8
18	9B	I/O9
19	7D	A18
20	7C	A5
21	7B	A7
22	7A	A8
23	6C	A6
24	6A	A9
25	4A	A10

BIT #	BUMP LOCATION	SYMBOL
26	4C	A13
27	3A	A11
28	3B	A12
29	3C	A14
30	3D	A19
31	2B	I/O10
32	1D	I/O11
33	2F	CQ
34	3H	I/O12
35	1H	I/O13
36	5A	ZQ
37	5B	B1
38	5K	B2
39	5L	B3
40	4L	$\overline{LBO}$
41	2K	I/O14
42	1M	I/O15
43	3M	I/O16
44	2P	I/O17
45	1T	I/O18
46	3P	A17
47	3T	A16
48	4R	A15

Notes: 1. The first bit to be shifted out from TDO is taken to be bit 0.
2. The $\overline{CK}$ clock input must be the complement of the CK clock input.

TAP CONTROLLER STATE DIAGRAM



Notes: 1. To enter the Test-Logic-Reset state in order to initialize the device, keep TMS High for at least five rising edges of the TCK.

2. The TDO output buffer is active only during shift operations (the Shift-DR and Shift-IR states) and is inactive (High-Z) during other states.

TAP DC OPERATING CHARACTERISTICS (Ta = 0 to 70°C, V_{DD} = 1.8 V ± 0.09 V (± 5%))

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
I_{LO}	Output Leakage Current (TDO pin)	Output Deselected V_{OUT} = 0 to V_{DD}	– 10	–	10	μA
I_I	Input Current (TMS, TDI pins)	V_{IN} = 1.7 V to V_{DD}	– 20	–	10	μA
		V_{IN} = 0 to 0.7 V	– 100	–	10	μA
V_{IH}	Input High Voltage (TCK, TMS, TDI pins)	–	1.05	–	V_{DD} + 0.3	V
V_{IL}	Input Low Voltage (TCK, TMS, TDI pins)	–	– 0.3	–	0.7	V
V_{OH}	Output High Voltage (TDO pin)	I_{OH} = – 2 mA	1.5	–	–	V
V_{OL}	Output Low Voltage (TDO pin)	I_{OL} = 2 mA	–	–	0.45	V

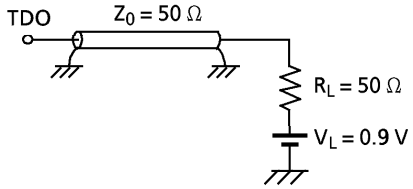
AC CHARACTERISTICS (Ta = 0 to 70°C, V_{DD} = 1.8 V ± 0.09 V (± 5%))

SYMBOL	PARAMETER	TC55YK1618AYB		UNIT
		MIN	MAX	
t_{THTH}	TCK Cycle Time	50	–	ns
t_{THTL}	TCK High Pulse Width	20	–	
t_{TLTH}	TCK Low Pulse Width	20	–	
t_{MVTH}	TMS Setup Time to TCK	10	–	
t_{THMX}	TMS Hold Time from TCK	10	–	
t_{CS}	Capture Setup time to TCK	10	–	
t_{CH}	Capture Hold time from TCK	10	–	
t_{DVTH}	TDI Setup Time to TCK	10	–	
t_{THDX}	TDI Hold Time from TCK	10	–	
t_{TLQV}	Output Valid Time from TCK Low	–	20	
t_{TLQX}	Output Hold Time from TCK Low	0	–	
t_{TLQLZ}	Output Low - Z Time from TCK Low	5	–	
t_{TLQHZ}	Output High - Z Time from TCK Low	–	5	

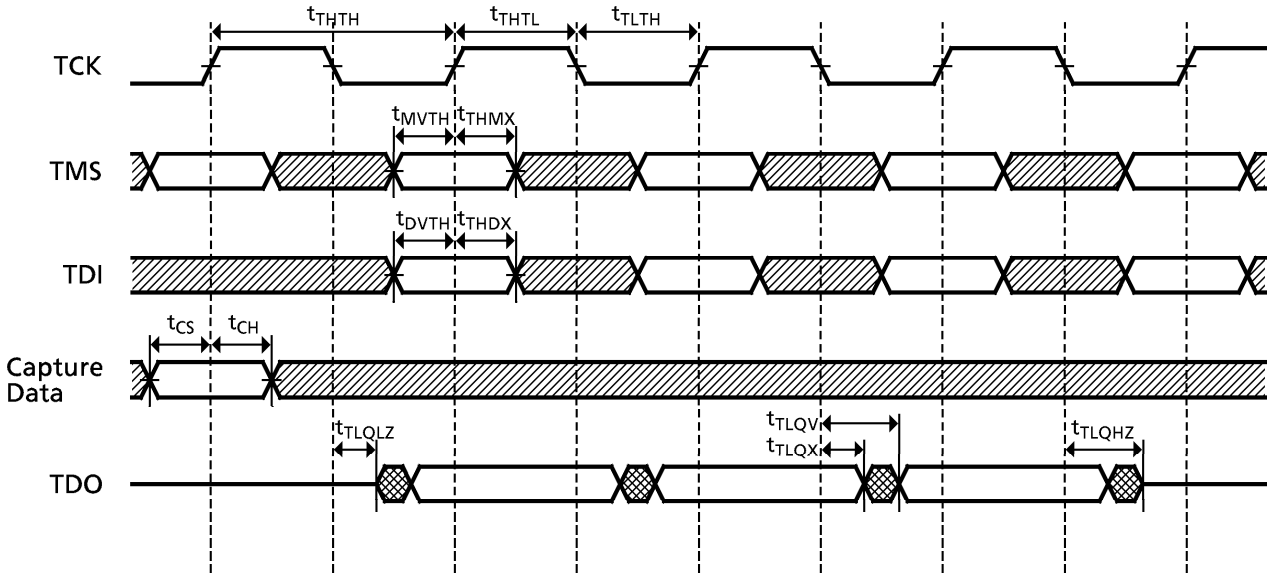
TAP AC TEST CONDITIONS

Input Pulse Level	1.8 V/0.0 V
Input Pulse Rise and Fall Time	2 ns
Input Timing Measurement Reference Level	0.9 V
Output Timing Measurement Reference Level	0.9 V
Output Load	Fig. 2

Fig. 2



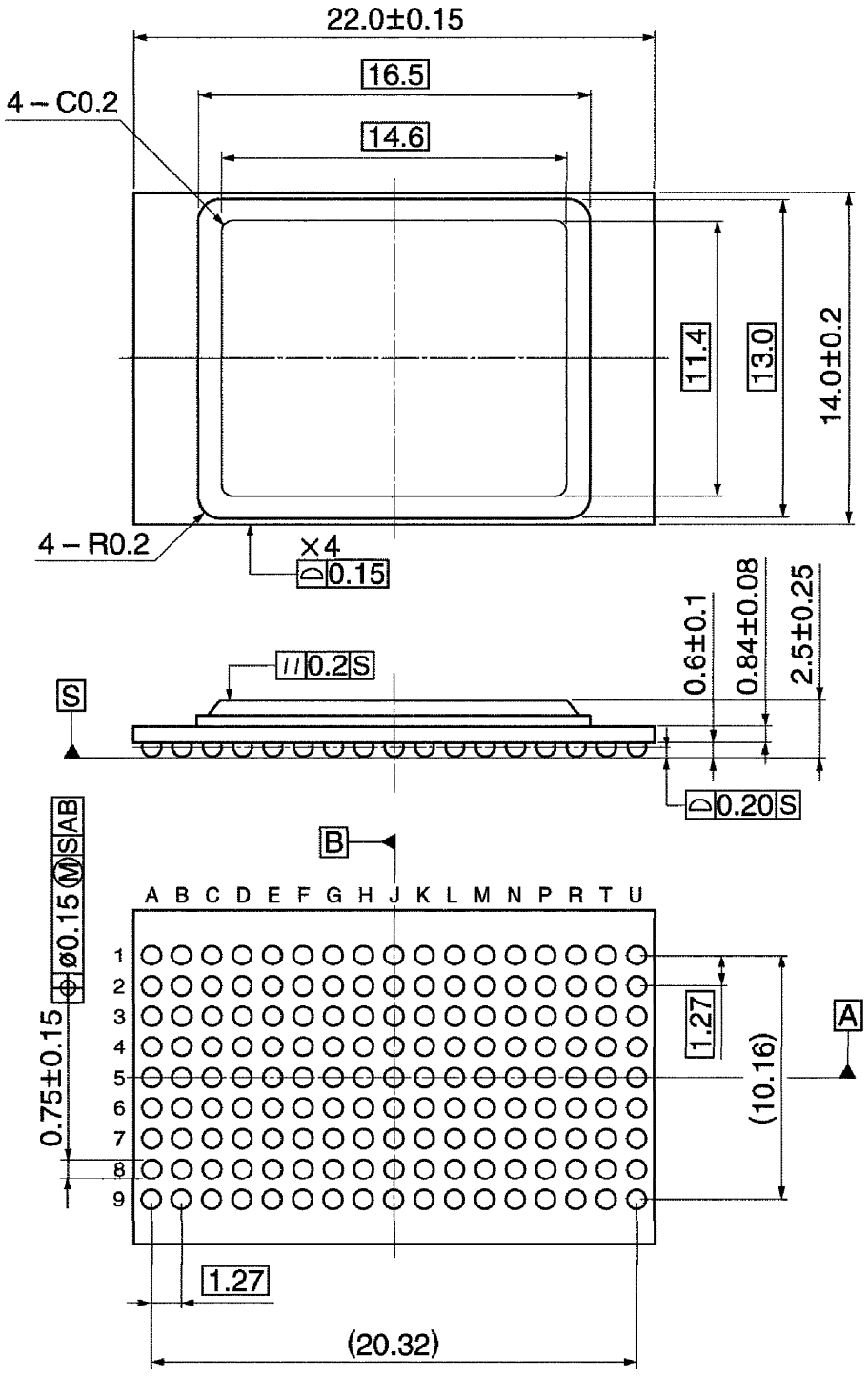
TAP TIMING DIAGRAMS



PACKAGE DIMENSIONS

C-BGA153-1422-1.27BZF

Unit: mm



Weight : 2.00 g (Typ)