# CMOS Floating-Point Divider
32-Bit, 2.5MFLOPS

The TMC3210 is a CMOS monolithic device which is capable of performing a full 32-bit floating-point division in
400 nanoseconds. The floating-point device divides normalized numbers expressed in IEEE 32-bit single-precision format and can also accommodate denormalized operands if they are first "wrapped" by a companion TMC3033 arithmetic unit. The user can select either FAST mode (output zero) or IEEE mode (output a wrapped quotient) to handle underflows. With wrapping and unwrapping externally provided, the TMC3210 is fully compliant with the number format and single-precision division operation described in Version 10.0 of IEEE Standard 754. The TMC3210 is built using TRW's OMICRON-C™ one-micron CMOS process.

All data and instruction inputs are registered. The two input operands (divisor and dividend) are each loaded in two 16-bit words through the dedicated half-width bus and the output is produced in two 16-bit words through the dedicated output port. With a clock rate of 20MHz, the divider has a 2.5 Megaflop pipelined throughput rate with a latency on any given operation of 6 internal clock cycles (600ns). Renormalizing, rounding and limiting functions are all generated per IEEE specification. The output quotient and status flag ports are driven by three-state buffers.

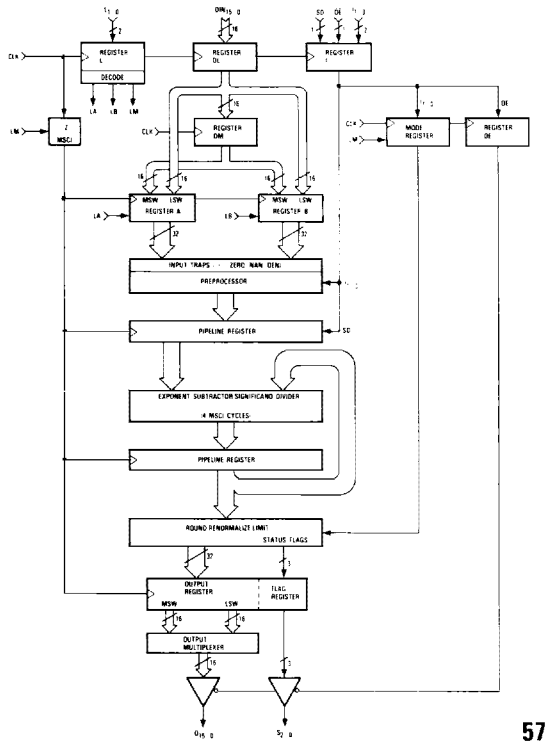
## Features

- IEEE Standard 754 Version 10.0 32-Bit Floating-Point Data Format
- 20MHz Bus Clock Rate; 2.5 Megaflop Pipelined Throughput Rate
- IEEE Unbiased Round To Nearest, Round Toward Zero, Round Toward Positive Infinity And Round Toward Negative Infinity Modes
- Supports Denormalized Operands/Results Through "Wrapping/Unwrapping" By External TMC3033 Arithmetic Unit
- Two-Bus Architecture (Dedicated Input And Output) Works With Single Bus Or Data Flow Systems
- IEEE Exception Flags Including Inexact Result, Overflow, Underflow, Divide By Zero, Invalid Operation And Denormalized Operands
- Automatic Limiting For Overflow Or Underflow
- Input Traps For Infinity, Zero, Not-A-Number And Denormalized Operand
- All Inputs And Outputs Registered And TTL Compatible
- Low Power CMOS Construction
- Available In A 48 Pin Hermetic Ceramic DIP

## Applications

- Graphics And Image Processors
- Solids Modeling
- Matrix Operations And Geometric Transforms
- Microcomputers/Minicomputers

## Functional Block Diagram



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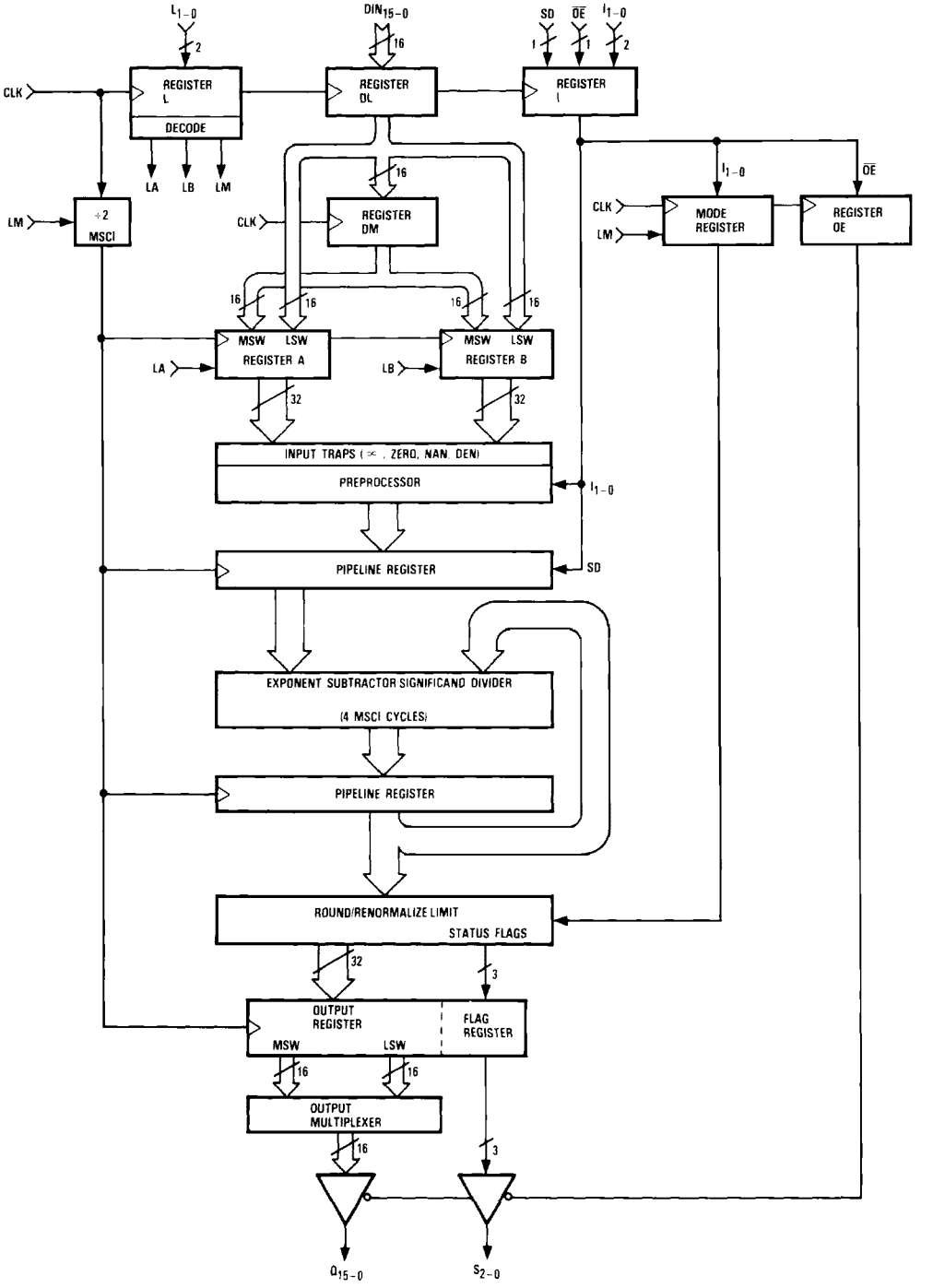
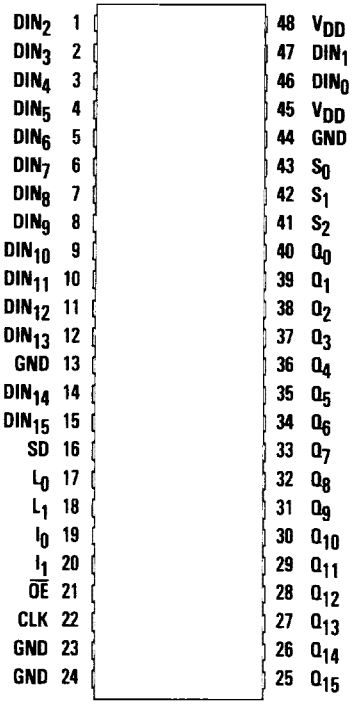
40G05346 Rev. B – 11/90
Printed in the U.S.A.

## Functional Block Diagram



## Pin Assignments




48 Lead DIP - J4 Package

## Functional Description

### General Information

The TMC3210 consists of five sections: the input registers, the input preprocessor, the exponent subtractor/significand divider, the round/renormalize/limit block, and the output multiplexer, registers and drivers.

### Input Registers

The input section accepts the data input (DIN) operand for the divisor (B) or dividend (A) along with an instruction which sets the mode (rounding) or format (wrapped or normalized number) depending on the load instructions. The external clock (CLK) strobes the DL and DM input preload registers, as well as the Load (L), Instruction (I) and Mode registers. CLK is internally divided by two to support an internal pipeline rate which is half the external bus clock rate.

The Most Significant Word (MSW) and the Least Significant Word (LSW) of both operands enter through the single 16-bit half-width input bus. The input preload register DL latches in the contents on the bus on the rising edge of CLK. The load instruction $L_{1-0}$ enables the A, B or Mode register and must be input at the same time as the A operand (dividend), B operand (divisor) or selected rounding mode instruction $I_{1-0}$ respectively. $L_{1-0}$ must be held for two clock cycles while the MSW and then the LSW of the dividend or divider is loaded. The two operands may be loaded in either order, but each always enters on two consecutive rising edges of CLK with the MSW first. If either operand is not updated, the next division will use the respective value from the previous operation, facilitating repeated divisions by or into a constant.

**Table 1. Load Instructions**

| $I_{1-0}$ | Mnemonic | Operation |
|---|---|---|
| 00 | NOP | No loading of A, B, or Mode registers |
| 01 | LA | Load register A from DL and DM preload registers |
| 10 | LB | Load register B from DL and DM preload registers |
| 11 | LM | Load Mode register from I register |

One of the four IEEE rounding modes is selected by $I_{1-0}$ when the Mode register is enabled through the LM load instruction. During a Load Mode, the Start Divide (SD) control selects either FAST or IEEE mode for the handling of underflowing results.

**Table 2. Mode Instructions**

| $I_{1-0}$[1] | Mnemonic | Operation |
|---|---|---|
| 00 | RN | Round to nearest number, or nearest even number if distances are equal (IEEE Standard 754 default) |
| 01 | RZ | Round toward zero (truncate product significand) |
| 10 | RP | Round toward positive infinity |
| 11 | RM | Round toward negative infinity |

Note:
1. $I_{1-0}$ selects the rounding mode during a Load Mode (LM) instruction.

**Table 3. Mode Control**

| SD[1] | Mnemonic | Operation |
|---|---|---|
| 0 | IEEE | Gradual Underflow (wrap exponent underflow values) |
| 1 | FAST | Flush-to-zero (replace exponent underflow numbers with zero) |

Note:
1. SD selects IEEE or FAST mode during a Load Mode (LM) instruction.

The registered Start Divide control initiates a division. SD must remain HIGH for two CLK cycles and may be asserted during the loading of the second operand. After SD is exercised, the user may load the next set of operands without interfering with the operation in progress. Another SD may occur every four internal MSCI clock cycles (eight external CLK cycles).

The format instructions $I_{1-0}$ select the dividend and divisor format and must be input with the loading of the second operand. If only one operand needs to be loaded for a division, $I_{1-0}$ is registered at the same time as the operand. Wrapped operands are too small to be expressed as standard IEEE normalized values, therefore instead of being denormalized with an exponent and hidden bit of 0, they are represented with a nonpositive two's complement exponent and a hidden bit of 1. A wrapped number is normalized, but has a special exponent. This special format allows the divider to handle denormalized numbers without large on-board normalizing shifters.

**Table 4. Format Instructions**

| $I_{1-0}$ | Mnemonic | Operation |
|---|---|---|
| 00 | A/B | Divide normalized A by normalized B |
| 01 | WA/B | Divide wrapped A by normalized B |
| 10 | A/WB | Divide normalized A by wrapped B |
| 11 | WA/WB | Divide wrapped A by wrapped B |

### Input Preprocessor

This section includes the input traps which detect infinity, zero, not-a-number and denormalized operand to generate the appropriate status flag.

### Main Section (Exponent Subtractor/Significand Divider)

The difference of the exponents and the quotient of the significands is computed including the IEEE guard, round and sticky bits. This operation requires eight CLK cycles from the initial rising edge of SD. To avoid disruption, the next SD must not begin for eight CLK cycles. After the unrounded, unnormalized intermediate result leaves this section, the user may exercise SD to bring in the next set of operands from the input block.

### Round/Renormalize/Limit Section

The significand of the quotient is rounded and readjusted so that the Most Significant Bit (MSB) occupies the nominal hidden bit position. If necessary, the exponent is adjusted to compensate for the renormalization shift. The final exponent is compared to the IEEE limits of 0 and 255 to generate the appropriate output condition and exception flag $S_{2-0}$.

**Table 5. Status Outputs**

| $S_{2-0}$ | Mnemonic | Exceptions |
|---|---|---|
| 00X | OK | No exceptions |
| 01X | UNF | Exponent underflow |
| 10X | OVF | Exponent overflow or divide by zero |
| 110 | INV | Invalid operands or invalid operation |
| 111 | DIN | Denormalized operand |

**Table 6. Divider Exception Flags and Outputs**

| A Operand (Dividend) | B Operand (Divisor) | | | | |
|---|---|---|---|---|---|
| | ZERO | DNRM | NRM/WNRM | INF | NaN |
| ZERO | INV, NaN | OK, ZERO | OK, ZERO | OK, ZERO | INV, NaN |
| DNRM | OVF, INF | INV[1], NaN | OK[1], ZERO | OK, ZERO | INV, NaN |
| NRM/WNRM | OVF, INF | OVF[1], INF | See Note 2 | OK, ZERO | INV, NaN |
| INF | OK, INF | OK, INF | OK, INF | INV, NaN | INV, NaN |
| NaN | INV, NaN | INV, NaN | INV, NaN | INV, NaN | INV, NaN |

Notes:

1. In IEEE mode, DIN ($S_{2-0}$ = 111) is the status flag output.
2. In the case of NRM/WNRM divided by NRM/WNRM.
   OVF: Output is OVF, +NRM.MAX if (RM,RZ) and TRESULT > NRM.MAX.
   OVF, -NRM.MAX if (RP,RZ) and TRESULT < -NRM.MAX.
   OVF, +INF if (RN,RP) and TRESULT > NRM.MAX.
   OVF, -INF if (RN,RM) and TRESULT < -NRM.MAX.
   UNF: Output is zero with UNF if | TRESULT | < NRM.MIN (FAST mode).
   Output is WNRM with UNF if | TRESULT | < NRM.MIN (IEEE mode).
   ELSE: Output is OK with normalized value.
   NRM.MIN ≤ | TRESULT | ≤ NRM.MAX.
3. Terms used in this table include:
   OK = No exceptions raised.
   NRM = Normalized number.
   DNRM = Denormalized number.
   WNRM = Wrapped number.
   INF = Infinity (±, Exponent = $FF_H$, Significand = $000000_H$).
   NaN = Not-A-Number (±, Exponent = $FF_H$, Significand = $600000_H$).
   TRESULT = Normalized, rounded, true result before limiting.
   NRM.MAX = Maximum allowable positive normalized number ($2^{+128} - 2^{+104}$ or Sign = 0, Exponent = $FE_H$, Significand = $7FFFFF_H$).
   NRM.MIN = Minimum allowable positive normalized number ($2^{-126}$ or Sign = 0, Exponent = $01_H$, Significand = $000000_H$).

In FAST mode, all underflows are forced to zero and the underflow flag is generated. In IEEE mode, underflowing values are wrapped and the underflow flag is generated. Overflows are limited to the infinities for round toward nearest and to maximum magnitude normalized values for round toward zero.

Round toward positive infinity limits the output to a positive infinity or a negative limit of maximum magnitude, negative normalized number. Round toward negative infinity limits the output to a negative infinity or a positive limit of maximum magnitude, positive normalized number.

J

### Output Multiplexer, Registers and Drivers

The 32-bit output register and 3-bit flag register are clocked by MSCI. The quotient is output through the 16-bit output port via the output multiplexer which selects either the MSW or LSW. The synchronization of MSW or LSW with CLK is set by the LM load instruction. After the SD control is HIGH for two CLK cycles to begin a division, the MSW of the quotient is output after the 12th rising edge of CLK. The output will toggle MSW and LSW with CLK until the quotient from the next division is available. The state of the status flags will remain set until new exception conditions occur. The output drivers are enabled and disabled by the Output Enable ($\overline{OE}$) control.

## Signal Definitions

### Power

$V_{DD}$, GND — The TMC3210 operates from a single +5 Volt supply. All power and ground lines must be connected.

### Data Inputs

$DIN_{15-0}$ — DIN is the 16-bit input to the preload register DL which is loaded on the rising edge of CLK. All data operands (dividends and divisors) are loaded through the DIN port, MSW followed by the LSW.

### Data Outputs

$Q_{15-0}$ — Q is the 16-bit output from the output register which is clocked by MSCI. The output multiplexer is internally synchronized to select MSW then LSW of the quotient which is output through three-state output drivers.

### Clock

CLK — The CLK frequency is twice the internal clock rate to allow for input/output data multiplexing. All operations are with respect to the rising edge CLK. The A and B input registers, pipeline registers and output registers are clocked by internal MSCI which is generated by dividing CLK by two.

### Controls

$I_{1-0}$ — The Mode/Format Instructions determine the rounding mode during a Load Mode, and select the input data formats when the operands are loaded. The rounding mode controls must be held for both CLK cycles during the loading of the Mode register. The format controls must be held for two CLK cycles during the loading of the last operand for a division.

$L_{1-0}$ — The Load Instructions generate LA, LB and LM which enable the A, B and Mode input registers respectively. The load controls are read on every rising edge of CLK. All data transfers into these input registers take place on the rising edge of CLK following the load controls commanding the data transfer. $L_{1-0}$ must be valid for two CLK cycles since the MSW and LSW must be loaded in two consecutive cycles. The LM instruction establishes the internal synchronization of CLK with MSCI and should not be asserted during a division.

$\overline{OE}$ — Output Enable is a registered control which enables the quotient and status outputs when LOW. When $\overline{OE}$ is HIGH, the outputs are in the high-impedance state. $\overline{OE}$ is read on the rising edge of CLK. The state of the output drivers will change after the next rising edge of CLK. Therefore, two CLK cycles are required to enable or disable the three-state drivers.

SD — Start Divide is an active HIGH control which begins the four MSCI clock cycle division. SD must remain HIGH for two CLK cycles and be asserted during or after the loading of the last operand of the divide. Subsequent SD may begin eight CLK cycles after the SD of the previous division. During the loading of the Mode register, SD selects whether FAST or IEEE mode is used in handling underflows.

### Status Outputs

$S_{2-0}$ — The status flags indicate the presence of exception conditions with the input operands or output quotient. The flags are valid while both the MSW and the LSW are output as long as the output buffer is enabled.

## Package Interconnections

| Signal Type | Signal Name | Function | J4 Package |
|---|---|---|---|
| Power | $V_{DD}$ | Supply Voltage | 45, 48 |
| | GND | Ground | 13, 23, 24, 44 |
| Data Input | $DIN_{15-0}$ | Input Data Word | 15, 14, 12-1, 47, 46 |
| Data Output | $Q_{15-0}$ | Output Quotient Word | 25-40 |
| Clock | CLK | Clock | 22 |
| Controls | $I_{1-0}$ | Mode/Format Instructions | 20, 19 |
| | $L_{1-0}$ | Load Instructions | 18, 17 |
| | $\overline{OE}$ | Output Enable | 21 |
| | SD | Start Divide | 16 |
| Flags | $S_{2-0}$ | Status Outputs | 41-43 |

### Data Format

The TMC3210 conforms to IEEE Standard 754, Version 10.0 data format for 32-bit arithmetic. The divider requires two clock cycles to transfer a data word since the input and output buses are 16-bit wide.

### Standard IEEE 32-Bit Floating-Point Format

The IEEE Standard 754, Version 10.0 specifies a 32-bit data format for floating-point arithmetic. In this format the MSB (bit 31) is the sign bit, the next eight bits (bits 30-23) are the exponent field and the 23 LSBs are the fractional significand field (bits 22-0). The "hidden bit" completes the 24-bit significand.

### Sign Bit

The MSB carries the sign information. A HIGH for a sign bit indicates a negative number and a LOW indicates a positive number.

### Exponent Field

The 8-bit exponent field determines whether the floating-point number is a signed infinity, a NaN, a zero, a denormalized number or a normalized floating-point number.

The exponent values 0 and 255 are special. If the exponent field is all ones (1111 1111, $255_{10}$) and the fraction (bits 22-0) is zero, the number is evaluated as infinity x $(-1)^S$ with S being the sign bit. Any exponent of 255 with a nonzero fraction is a NaN. A NaN is generally used to communicate error information such as invalid operation or uninitialized memory and has no numerical value.

When the exponent field is all zeros (0000 0000) and the fraction is also zero, the number is a true floating-point zero. Note that this data format allows both positive and negative zeros which are computationally treated identically. When the exponent is zero and the fraction is nonzero, the number is a denormalized floating-point number evaluated as:

$$\text{Number} = (-1)^S \times 2^{E-126} \times (0.F)$$

where S is the sign bit, E is the value of the exponent field (base 10) and F is the value of the fractional field.

If the exponent field is neither all zeros nor all ones, the floating-point number is normalized and evaluated as:

$$\text{Number} = (-1)^S \times 2^{E-127} \times (1.F)$$

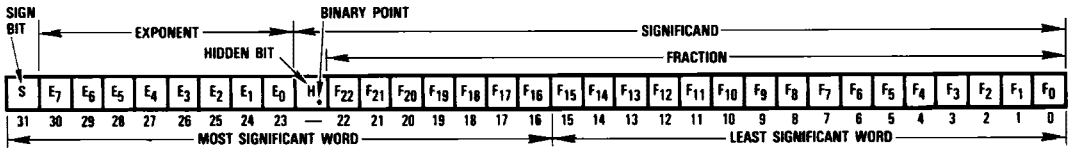
Note that the exponent bias has changed from 126 to 127 and that 1.0 has been added to the fractional field. The exponent can assume values which run from -126 to +127 (0 to 254 biased by 127). Note that both exponent fields of zero and one map onto the exponent value of -126. These provisions ensure a smooth transition from normalized numbers through gradual underflow into the denormalized numbers.

### Fractional Field

Bits 22–0 comprise the fractional field (mantissa). There is a binary point assumed between bit 22 and the implied "hidden" bit 23. For a nonzero exponent, the hidden bit assumes a value of "1." For a zero exponent, the hidden bit has a value of "0." Bit 22 carries a binary weighting of $2^{-1}$. The following bits carry decreasing binary weights down to the LSB (bit 0) which carries the weight of $2^{-23}$. This is identical to treating the fractional part (bits 22–0) like an integer F multiplied by $2^{-23}$. The fractional part of the floating-point number is either 0 + F (in the case of a zero exponent), or 1 + F (in the case of a nonzero exponent).

The difference between the smallest normalized number (exponent = 1, fractional part = 0) and the largest denormalized number (exponent = 0, fractional part = all ones) is one LSB. The smallest normalized number is: exponent = −126, significand = 1.00...00 written as exponent = $01_H$, significand = $000000_H$. The largest denormalized number is: exponent = −126, significand = 0.11...11 written as exponent = $00_H$, significand = $7FFFFF_H$.

**Figure 1. IEEE 32-Bit Floating-Point Format**



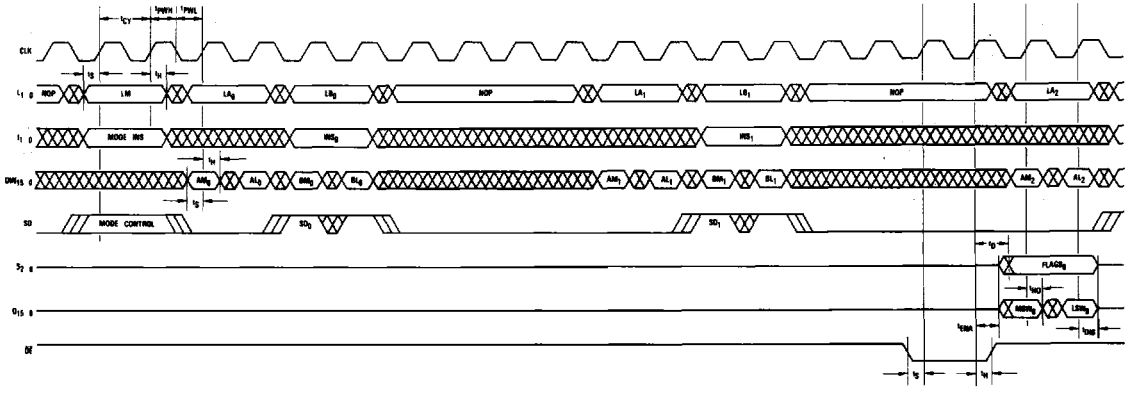


| Exponent | Fraction | Value | Name | Mnemonic |
|---|---|---|---|---|
| 255 | Not all zeros | -- | Not-A-Number | NaN |
| 255 | All zeros | $(-1)^S \times \infty$ | Signed Infinity | INF |
| 1 through 254 | Any | $(-1)^S \times (1.F) \times 2^{E-127}$ | Normalized Number | NRM |
| 0 | Not all zeros | $(-1)^S \times (0.F) \times 2^{E-126}$ | Denormalized Number | DNRM |
| 0 | All zeros | $(-1)^S \times 0.0$ | Zero | ZERO |

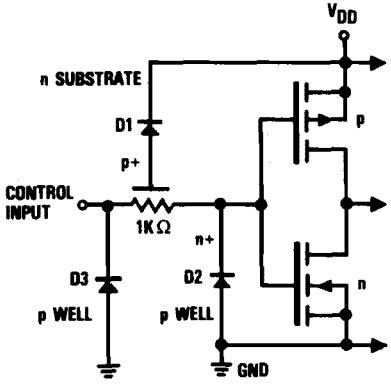
Note:

1. H, the hidden bit, is one except for zero and denormalized numbers when it is zero.

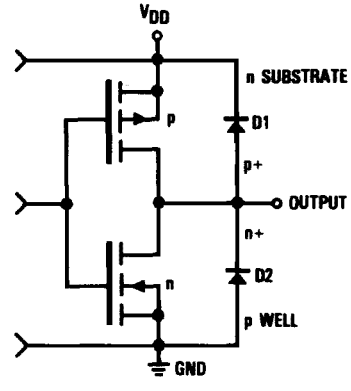
## Figure 2. Timing Diagram



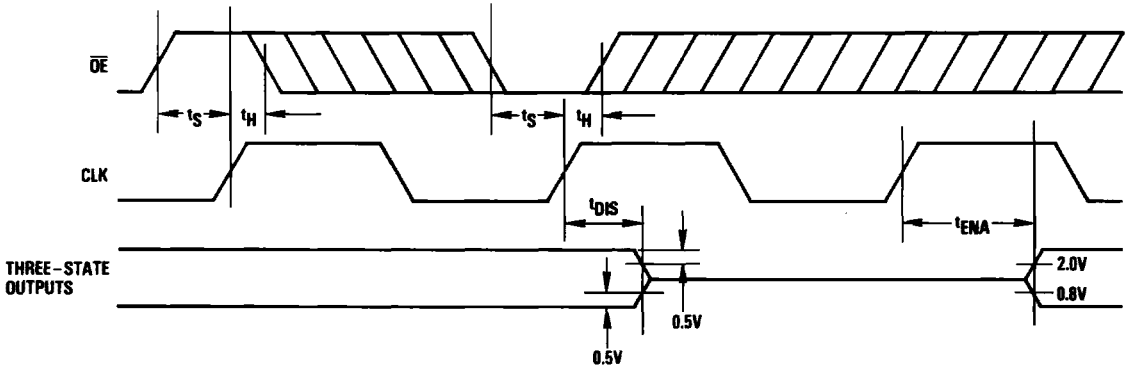
## Figure 3. Equivalent Input Circuit




## Figure 4. Equivalent Output Circuit




## Figure 5. Threshold Levels For Three-State Measurement



## Absolute maximum ratings (beyond which the device may be damaged) [1]

**Supply Voltage** ..... −0.5 to +7.0V

**Input Voltage** ..... −0.5 to ($V_{DD}$ +0.5)V

**Output**

Applied voltage [2] ..... −0.5 to ($V_{DD}$ +0.5)V

Forced current [3,4] ..... −1.0 to +6.0mA

Short-circuit duration (single output in HIGH state to ground) ..... 1 sec

**Temperature**

Operating, case ..... −60 to +130°C

junction ..... 175°C

Lead, soldering (10 seconds) ..... 300°C

Storage ..... −65 to +150°C

Notes:

1. Absolute maximum ratings are limiting values applied individually while all other parameters are within specified operating conditions. Functional operation under any of these conditions is NOT implied.
2. Applied voltage must be current limited to specified range, and measured with respect to GND.
3. Forcing voltage must be limited to specified range.
4. Current is specified as conventional current flowing into the device.

## Operating conditions

| Parameter | | Temperature Range | | | | | | Units |
|---|---|---|---|---|---|---|---|---|
| | | Standard | | | Extended | | | |
| | | Min | Nom | Max | Min | Nom | Max | |
| $V_{DD}$ | Supply Voltage | 4.75 | 5.0 | 5.25 | 4.5 | 5.0 | 5.5 | V |
| $T_A$ | Ambient Temperature, Still Air | 0 | | 70 | | | | °C |
| $T_C$ | Case Temperature | | | | −55 | | 125 | °C |

## DC characteristics within specified operating conditions[1]

| Parameter | | Test Conditions | Temperature Range | | | | Units |
|---|---|---|---|---|---|---|---|
| | | | Standard | | Extended | | |
| | | | Min | Max | Min | Max | |
| $I_{DDQ}$ | Supply Current, Quiescent | $V_{DD}$ = Max, $V_{IN}$ = 0V | | 10 | | 10 | mA |
| $I_{DDU}$ | Supply Current, Unloaded | $V_{DD}$ = Max, $\overline{OE}$ = 5V | | | | | |
| | | f = 20MHz | | 50 | | 70 | mA |
| | | f = 10MHz | | 25 | | 35 | mA |
| $I_{IL}$ | Input Current, Logic LOW | $V_{DD}$ = Max, $V_{IN}$ = 0V | | −10 | | −40 | μA |
| $I_{IH}$ | Input Current, Logic HIGH | $V_{DD}$ = Max, $V_{IN}$ = $V_{DD}$ | | 10 | | 40 | μA |
| $V_{IL}$ | Input Voltage, Logic LOW | | | 0.8 | | 0.8 | V |
| $V_{IH}$ | Input Voltage, Logic HIGH | | 2.0 | | 2.0 | | V |
| $V_{OL}$ | Output Voltage, Logic LOW | $V_{DD}$ = Min, $I_{OL}$ = 4mA | | 0.4 | | 0.4 | V |
| $V_{OH}$ | Output Voltage, Logic HIGH | $V_{DD}$ = Min, $I_{OH}$ = −2mA | 2.4 | | 2.4 | | V |
| $I_{OZL}$ | Hi-Z Output Leakage Current, Output LOW | $V_{DD}$ = Max, $V_{IN}$ = 0V | | −40 | | −40 | μA |
| $I_{OZH}$ | Hi-Z Output Leakage Current, Output HIGH | $V_{DD}$ = Max, $V_{IN}$ = $V_{DD}$ | | 40 | | 40 | μA |
| $I_{OS}$ | Short-Circuit Output Current | $V_{DD}$ = Max, Output HIGH, one pin to ground, one second duration max. | | −100 | | −120 | mA |
| $C_I$ | Input Capacitance | $T_A$ = 25°C, f = 1MHz | | 10 | | 10 | pF |
| $C_O$ | Output Capacitance | $T_A$ = 25°C, f = 1MHz | | 10 | | 10 | pF |

Note:

1. Actual test conditions may vary from those shown, but guarantee operation as specified.

## AC characteristics within specified operating conditions

| Parameter | | Test Conditions | Temperature Range | | | | Units |
|---|---|---|---|---|---|---|---|
| | | | Standard | | Extended | | |
| | | | Min | Max | Min | Max | |
| $t_{CY}$ | Cycle Time | $V_{DD}$ = Min | | 50 | | 55 | ns |
| $t_{PWL}$ | Clock Pulse Width, LOW | $V_{DD}$ = Min | 30 | | 35 | | ns |
| $t_{PWH}$ | Clock Pulse Width, HIGH | $V_{DD}$ = Min | 15 | | 15 | | ns |
| $t_S$ | Input Setup Time | | 15 | | 15 | | ns |
| $t_H$ | Input Hold Time | | 0 | | 3 | | ns |
| $t_D$ | Output Delay | $V_{DD}$ = Min, $C_{LOAD}$ = 40pF | | 20 | | 25 | ns |
| $t_{HO}$ | Output Hold Time | $V_{DD}$ = Max, $C_{LOAD}$ = 40pF | 5 | | 5 | | ns |
| $t_{ENA}$ | Three-State Output Enable Delay[1] | $V_{DD}$ = Min, $C_{LOAD}$ = 40pF | | 20 | | 25 | ns |
| $t_{DIS}$ | Three-State Output Disable Delay[1] | $V_{DD}$ = Min, $C_{LOAD}$ = 40pF | | 25 | | 30 | ns |

Note:

1. All transitions are measured at a 1.5V level except for $t_{DIS}$ and $t_{ENA}$.

## Ordering Information

| Product Number | Temperature Range | Screening | Package | Package Marking |
|---|---|---|---|---|
| TMC3210J4C | STD – $T_A$ = 0°C to 70°C | Commercial | 48 Pin Hermetic Ceramic DIP | 3210J4C |
| TMC3210J4V | EXT – $T_C$ = –55°C to 125°C | MIL-STD-883 | 48 Pin Hermetic Ceramic DIP | 3210J4V |