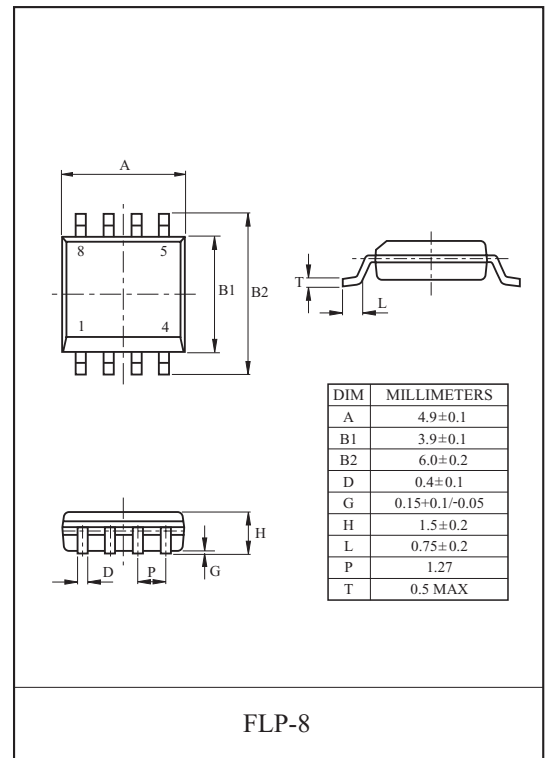


General Description

Switching regulator and DC-DC converter applications.
It is mainly suitable for power management in notebook, portable equipment and battery powered systems.

FEATURES

- N-Channel
 - : $V_{DSS}=30V$, $I_D=7A$.
 - : $R_{DS(ON)}=17m\ \Omega$ (Typ.) @ $V_{GS}=10V$.
 - : $R_{DS(ON)}=22m\ \Omega$ (Typ.) @ $V_{GS}=4.5V$.
- P-Channel
 - : $V_{DSS}=-30V$, $I_D=-5.5A$.
 - : $R_{DS(ON)}=35m\ \Omega$ (Typ.) @ $V_{GS}=-10V$.
 - : $R_{DS(ON)}=51m\ \Omega$ (Typ.) @ $V_{GS}=-4.5V$.
- Super high dense cell design for extremely low $R_{DS(ON)}$.
- Reliable and rugged.

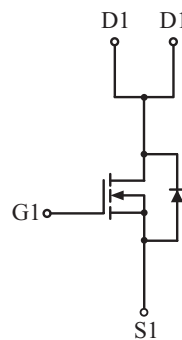
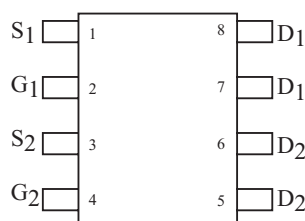


MAXIMUM RATING (Ta=25 °C)

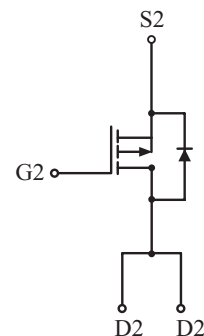
CHARACTERISTIC		SYMBOL	N-Ch	P-Ch	UNIT
Drain-Source Voltage		V_{DSS}	30	-30	V
Gate-Source Voltage		V_{GSS}	±20	±20	V
Drain Current	DC	I_D^*	7	-5.5	A
	Pulsed	I_{DP}	28	-20	
Drain Power Dissipation	Ta=25 °C	P_D^*	2		W
	Ta=100 °C		0.8		
Maximum Junction Temperature		T_j	150		°C
Storage Temperature Range		T_{stg}	-55 ~ 150		°C
Thermal Resistance, Junction to Case		R_{thJA}^*	62.5		°C/W

* : Surface Mounted on FR4 Board, $t \leq 10$ sec.

PIN CONNECTION (TOP VIEW)



N-Channel MOSFET



P-Channel MOSFET

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ELECTRICAL CHARACTERISTICS (Ta=25 °C)

CHARACTERISTIC	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT	
Static							
Drain-Source Breakdown Voltage	BV _{DSS}	I _D =±250 μA, V _{GS} =0V	N-Ch	30	-	-	V
			P-Ch	-30	-	-	
Drain Cut-off Current	I _{DSS}	V _{DS} =24V, V _{GS} =0V	N-Ch	-	-	1	μA
		V _{DS} =-24V, V _{GS} =0V	P-Ch	-	-	-1	
Gate Threshold Voltage	V _{th}	V _{DS} =V _{GS} , I _D =±250 μA	N-Ch	1	1.5	2	V
			P-Ch	-1	-1.5	-2	
Gate Leakage Current	I _{GSS}	V _{GS} =±20V, V _{DS} =0V	N-Ch P-Ch	-	-	±100	nA
Drain-Source ON Resistance	R _{DS(ON)} ^(Note 1)	V _{GS} =10V, I _D =7A V _{GS} =4.5V, I _D =5A V _{GS} =-10V, I _D =-5.5A V _{GS} =-4.5V, I _D =-4A	N-Ch	-	17	24	m Ω
				-	22	30	
			P-Ch	-	35	56	
				-	51	78	
Source-Drain Diode Forward Voltage	V _{SD} ^(Note 1)	I _{DR} =2A, V _{GS} =0V I _{DR} =-2.3A, V _{GS} =0V	N-Ch	-	0.7	1.3	V
			P-Ch	-	-0.7	-1.3	
Dynamic ^(Note 2)							
Total Gate Charge	Q _g	N-Channel V _{DS} =15V, I _D =7A V _{GS} =10V	N-Ch	-	19	28	nC
			P-Ch	-	33	43	
Gate-Source Charge	Q _{gs}	P-Channel V _{DS} =-15V, I _D =-5.5A V _{GS} =-10V	N-Ch	-	1.6	-	
			P-Ch	-	5	-	
Gate-Drain Charge	Q _{gd}	(Fig.1)	N-Ch	-	3.6	-	
			P-Ch	-	4	-	
Turn-on Delay time	t _{d(on)}	N-Channel V _{DD} =15V, I _D =2A V _{IN} =10V, R _G =6 Ω R _L =7.5 Ω	N-Ch	-	11	20	ns
			P-Ch	-	12	24	
Turn-on Rise time	t _r	(Fig.2)	N-Ch	-	17	28	
			P-Ch	-	15	29	
Turn-off Delay time	t _{d(off)}	P-Channel V _{DD} =-15V, I _D =-2A V _{IN} =-10V, R _G =6 Ω R _L =7.5 Ω	N-Ch	-	36	62	
			P-Ch	-	35	60	
Turn-off Fall time	t _f	(Fig.2)	N-Ch	-	20	36	
			P-Ch	-	15	30	
Input Capacitance	C _{iss}	N-Channel V _{DS} =25V, V _{GS} =0V f=1.0MHz	N-Ch	-	835	-	pF
			P-Ch	-	950	-	
Reverse Transfer Capacitance	C _{rss}	P-Channel V _{DS} =-25V, V _{GS} =0V f=1.0MHz	N-Ch	-	15	-	
			P-Ch	-	110	-	
Output Capacitance	C _{oss}	f=1.0MHz	N-Ch	-	145	-	
			P-Ch	-	160	-	

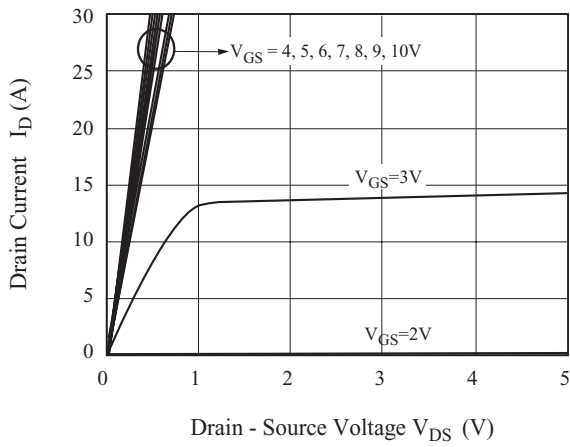
Note 1) Pulse test : Pulse width ≤300 μs, duty cycle ≤2%

Note 2) Guaranteed by design, not subject to production testing.

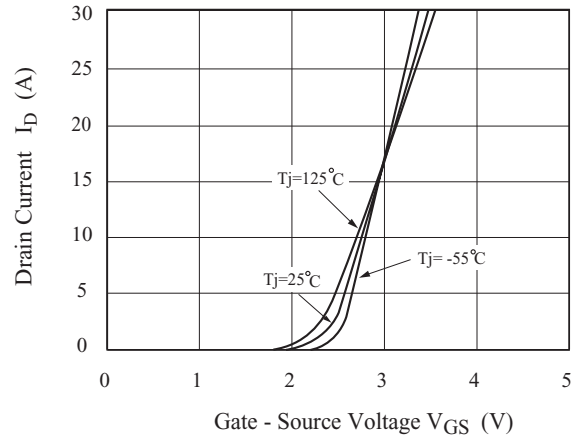
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N-Channel

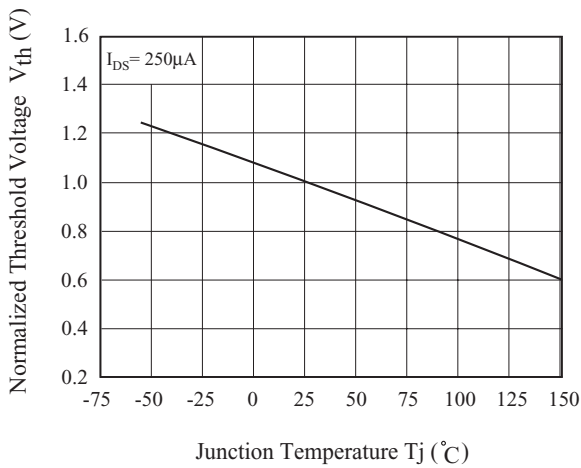
$I_D - V_{DS}$



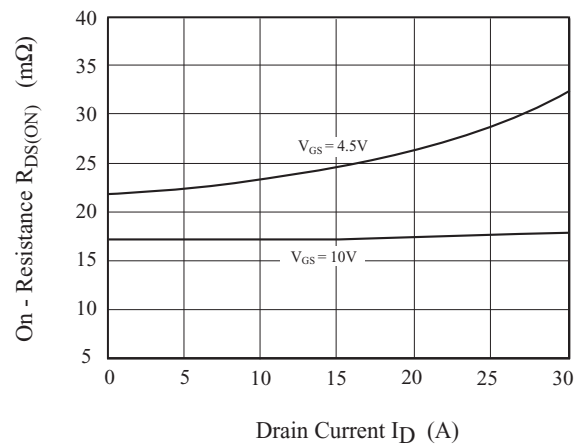
$I_D - V_{GS}$



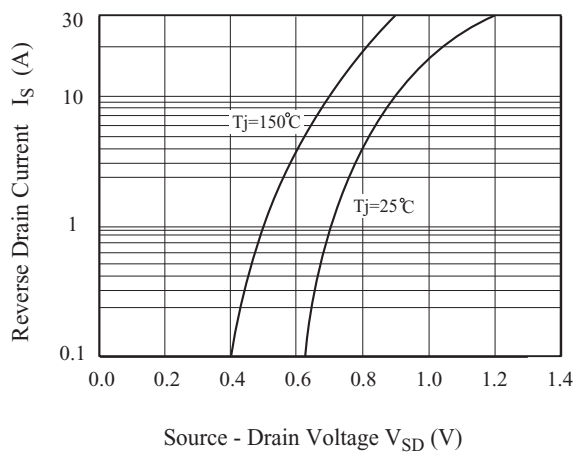
$V_{th} - T_j$



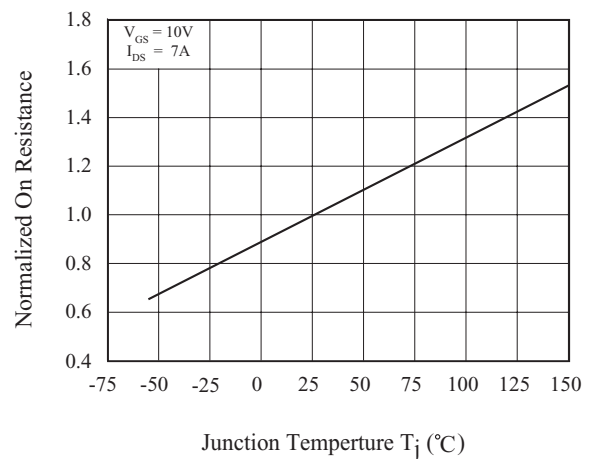
$R_{DS(ON)} - I_D$



$I_S - V_{SD}$

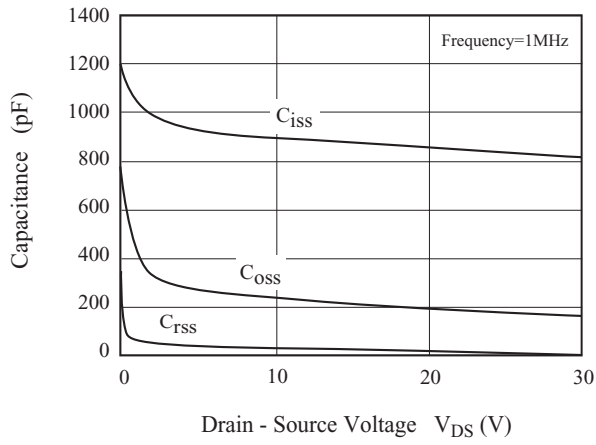


$R_{DS(ON)} - T_j$

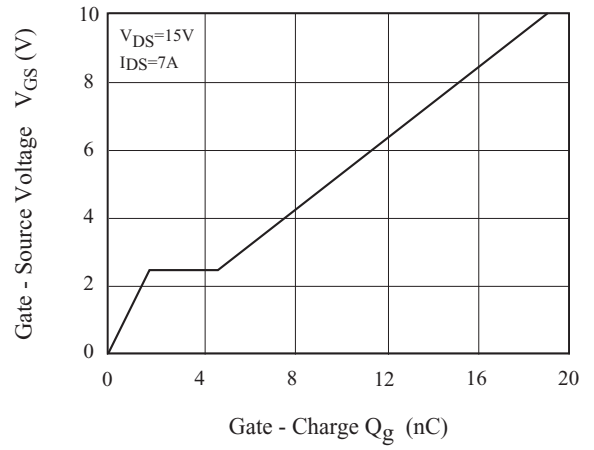


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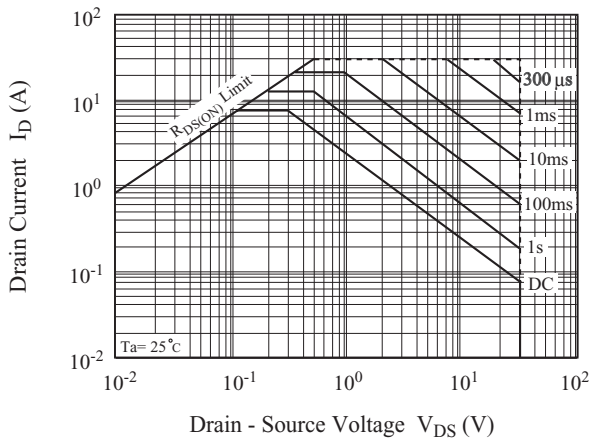
C - V_{DS}



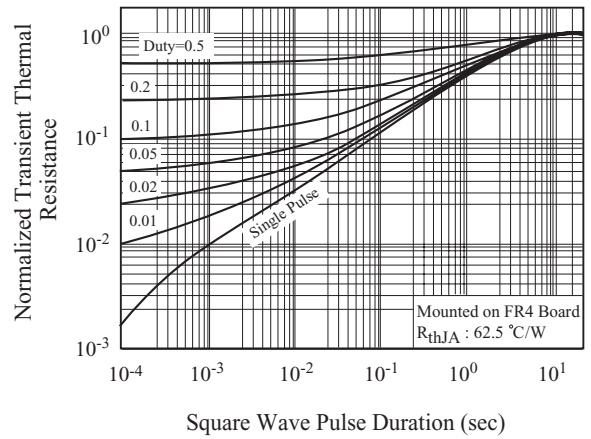
Q_g - V_{GS}



Safe Operation Area

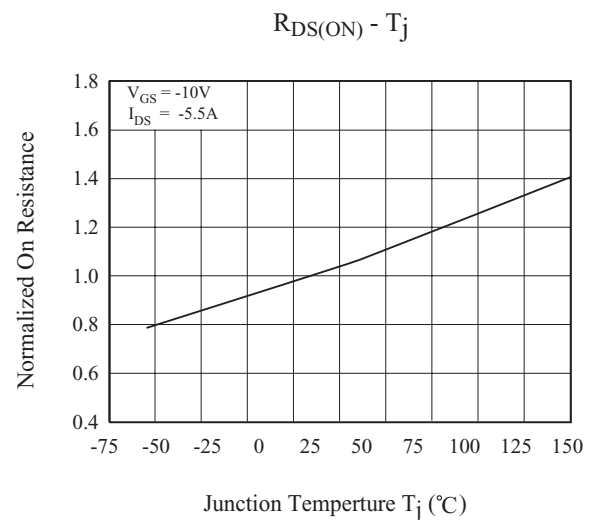
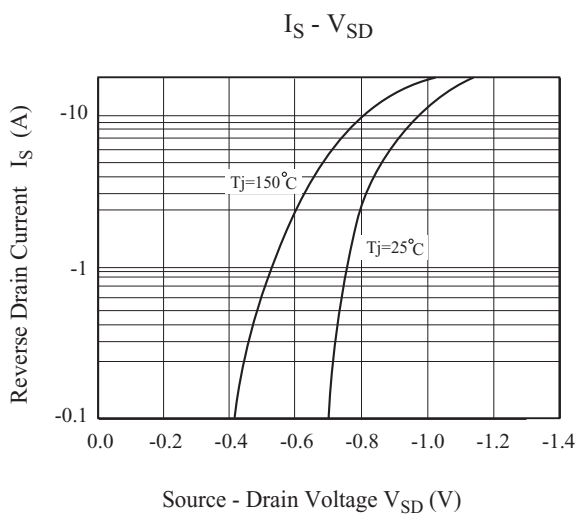
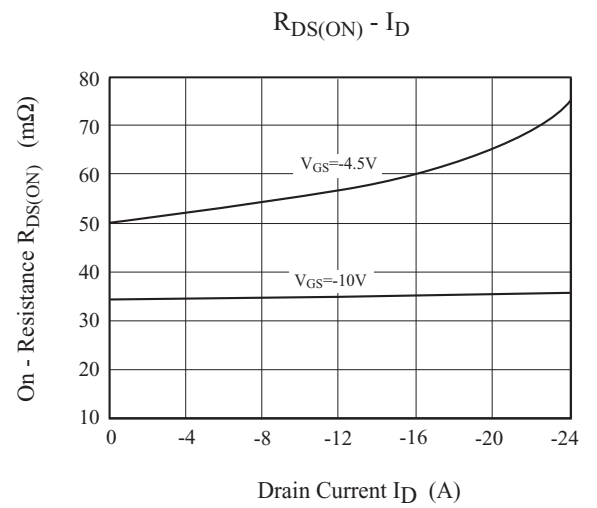
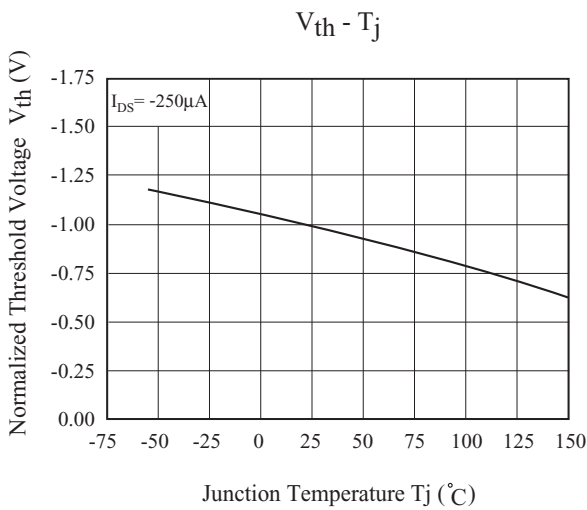
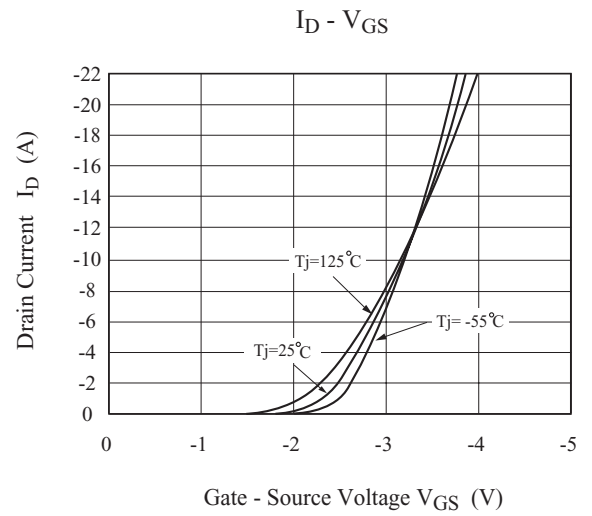
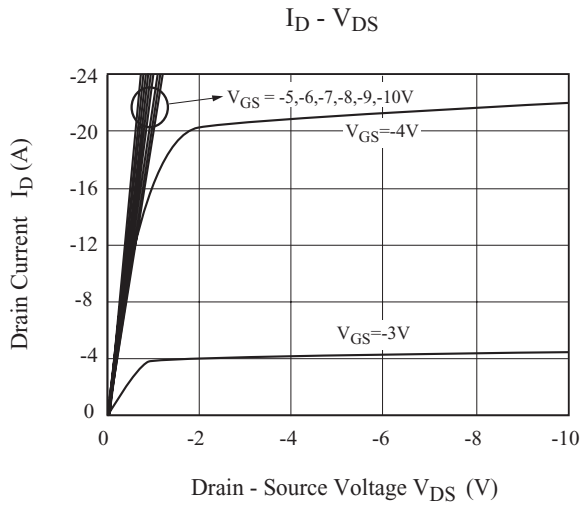


R_{th}



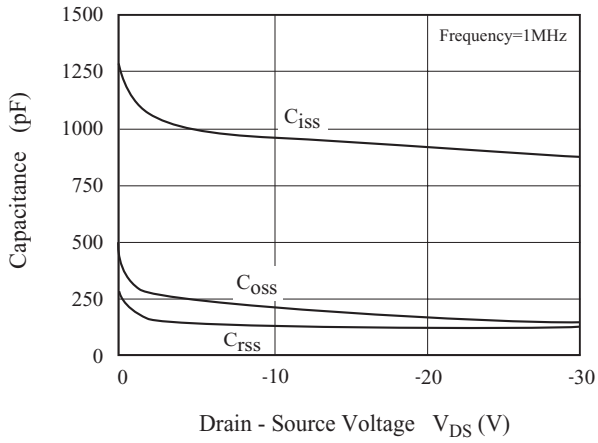
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P-Channel

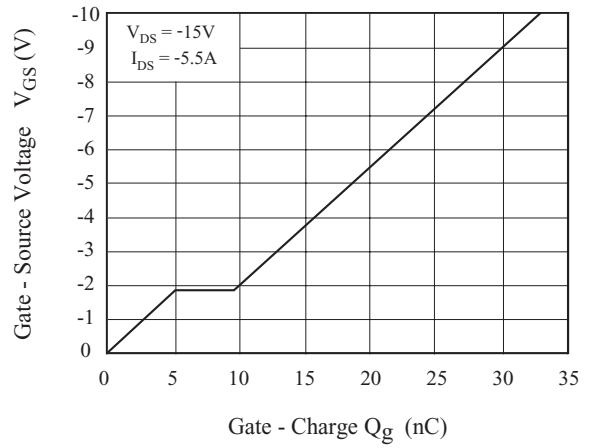


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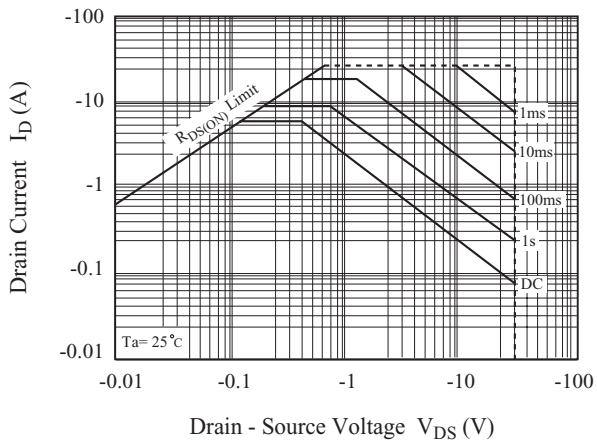
C - V_{DS}



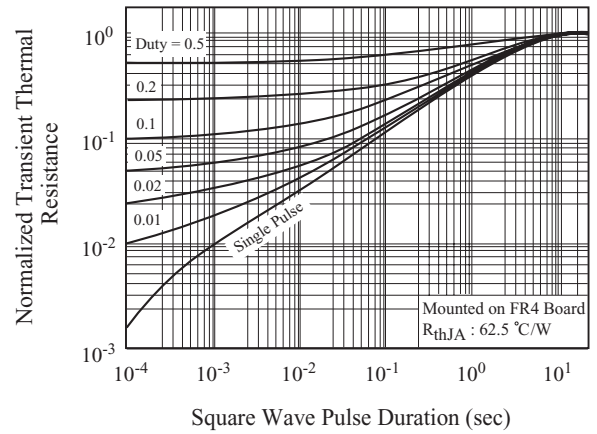
Q_g - V_{GS}



Safe Operation Area



R_{th}



N -Channel

Fig. 1 Gate Charge

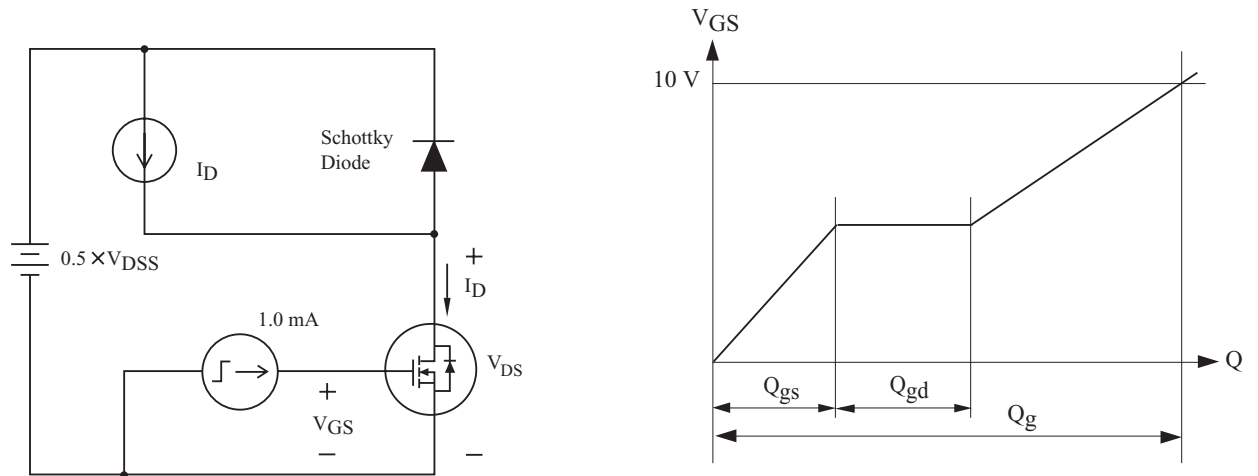
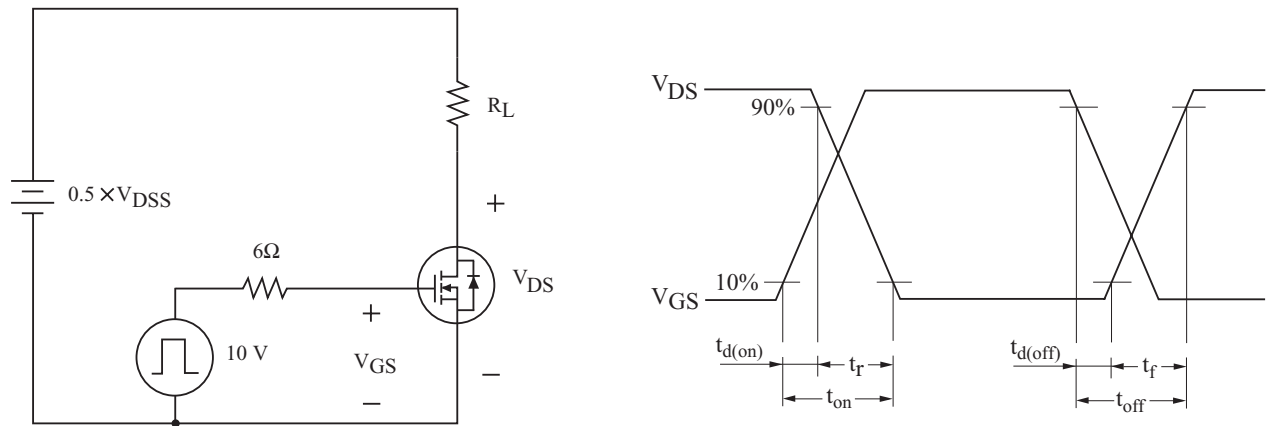


Fig. 2 Resistive Load Switching



P -Channel

Fig. 1 Gate Charge

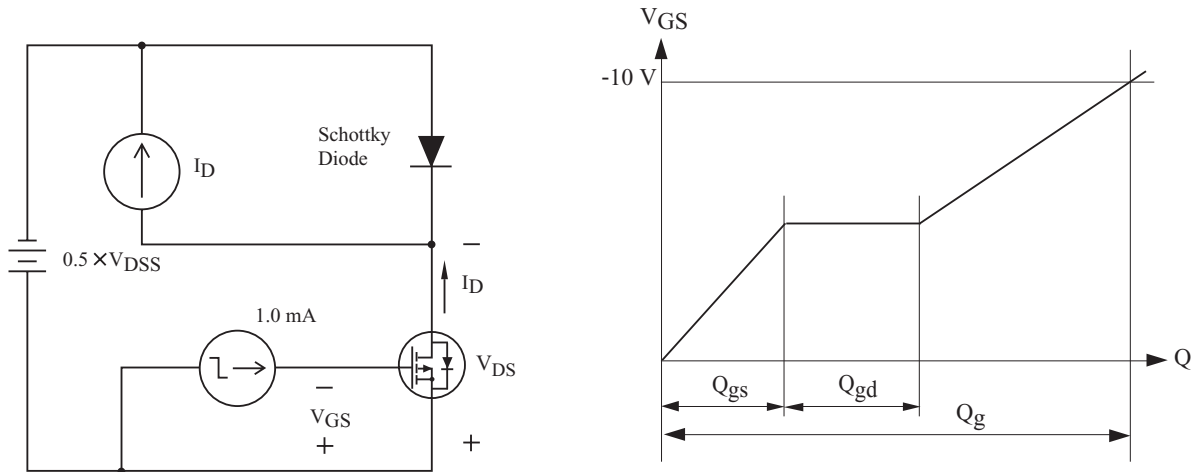


Fig. 2 Resistive Load Switching

