

DDR3 SDRAM RDIMM

MT36JDZS51272PZ – 4GB

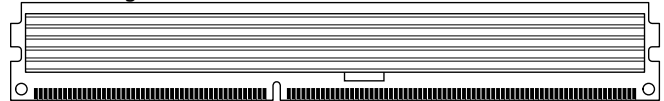
MT36JDZS1G72PZ – 8GB

Features

- DDR3 functionality and operations supported as defined in the component data sheet
- 240-pin, very low-profile registered dual in-line memory module (VLP RDIMM)
- Fast data transfer rates: PC3-12800, PC3-10600, PC3-8500, or PC3-6400
- 4GB (512 Meg x 72), 8GB (1 Gig x 72)
- $V_{DD} = 1.5V \pm 0.075V$
- $V_{DDSPD} = +3.0V$ to $+3.6V$
- Supports ECC error detection and correction
- Nominal and dynamic on-die termination (ODT) for data and strobe signals
- Dual rank, using 2Gb or 4Gb TwinDie™ devices
- 8 internal device banks
- Fixed burst chop (BC) of 4 and burst length (BL) of 8 via the mode register set (MRS)
- On-board I²C temperature sensor with integrated serial presence-detect (SPD) EEPROM
- Gold edge contacts
- Halogen-free
- Fly-by topology
- Terminated control, command, and address bus

Figure 1: 240-Pin VLP RDIMM (MO-269 R/C N)

Module height: 18.75mm (0.738in)



Options

- Operating temperature¹
 - Commercial ($0^{\circ}C \leq T_A \leq +70^{\circ}C$)
 - Industrial ($-40^{\circ}C \leq T_A \leq +85^{\circ}C$)
- Package
 - 240-pin DIMM (halogen-free)
- Frequency/CAS latency
 - 1.25ns @ CL = 11 (DDR3-1600)
 - 1.5ns @ CL = 9 (DDR3-1333)
 - 1.87ns @ CL = 7 (DDR3-1066)

Marking

None
I
Z
-1G6
-1G4
-1G1

Note: 1. Contact Micron for industrial temperature module offerings.

Table 1: Key Timing Parameters

| Speed Grade | Industry Nomenclature | Data Rate (MT/s) | | | | | | | t _{RCD} (ns) | t _{RP} (ns) | t _{RC} (ns) |
|-------------|-----------------------|------------------|---------|--------|--------|--------|--------|--------|-----------------------|----------------------|----------------------|
| | | CL = 11 | CL = 10 | CL = 9 | CL = 8 | CL = 7 | CL = 6 | CL = 5 | | | |
| -1G6 | PC3-12800 | 1600 | 1333 | 1333 | 1066 | 1066 | 800 | 667 | 13.125 | 13.125 | 48.125 |
| -1G4 | PC3-10600 | – | 1333 | 1333 | 1066 | 1066 | 800 | 667 | 13.125 | 13.125 | 49.125 |
| -1G1 | PC3-8500 | – | – | – | 1066 | 1066 | 800 | 667 | 13.125 | 13.125 | 50.625 |
| -1G0 | PC3-8500 | – | – | – | 1066 | – | 800 | 667 | 15 | 15 | 52.5 |
| -80B | PC3-6400 | – | – | – | – | – | 800 | 667 | 15 | 15 | 52.5 |



Table 2: Addressing

| Parameter | 4GB | 8GB |
|----------------------|---------------------------|-------------------------|
| Refresh count | 8K | 8K |
| Row address | 16K A[13:0] | 32K A[14:0] |
| Device bank address | 8 BA[2:0] | 8 BA[2:0] |
| Device configuration | 2Gb TwinDie (512 Meg x 4) | 4Gb TwinDie (1 Gig x 4) |
| Column address | 2K A[11,9:0] | 2K A[11,9:0] |
| Module rank address | 2 S#[1:0] | 2 S#[1:0] |

Table 3: Part Numbers and Timing Parameters – 4GB Modules

Base device: MT41J512M4,¹ 2Gb TwinDie DDR3 SDRAM

| Part Number ² | Module Density | Configuration | Module Bandwidth | Memory Clock/ Data Rate | Clock Cycles (CL- ^t RCD- ^t RP) |
|--------------------------|----------------|---------------|------------------|----------------------------|---------------------------------------------------------|
| MT36JDZS51272P(I)Z-1G6__ | 4GB | 512 Meg x 72 | 12.8 GB/s | 1.25ns/1600 MT/s | 11-11-11 |
| MT36JDZS51272P(I)Z-1G4__ | 4GB | 512 Meg x 72 | 10.6 GB/s | 1.5ns/1333 MT/s | 9-9-9 |
| MT36JDZS51272P(I)Z-1G1__ | 4GB | 512 Meg x 72 | 8.5 GB/s | 1.87ns/1066 MT/s | 7-7-7 |

Table 4: Part Numbers and Timing Parameters – 8GB Modules

Base device: MT41J1GM4,¹ 4Gb TwinDie DDR3 SDRAM

| Part Number ² | Module Density | Configuration | Module Bandwidth | Memory Clock/ Data Rate | Clock Cycles (CL- ^t RCD- ^t RP) |
|--------------------------|----------------|---------------|------------------|----------------------------|---------------------------------------------------------|
| MT36JDZS1G72P(I)Z-1G6__ | 8GB | 1 Gig x 72 | 12.8 GB/s | 1.25ns/1600 MT/s | 11-11-11 |
| MT36JDZS1G72P(I)Z-1G4__ | 8GB | 1 Gig x 72 | 10.6 GB/s | 1.5ns/1333 MT/s | 9-9-9 |
| MT36JDZS1G72P(I)Z-1G1__ | 8GB | 1 Gig x 72 | 8.5 GB/s | 1.87ns/1066 MT/s | 7-7-7 |

- Notes: 1. The data sheet for the base device can be found on Micron’s Web site.
 2. All part numbers end with a two-place code (not shown) that designates component and PCB revisions. Consult factory for current revision codes. Example: MT36JDZS1G72PZ-1G1M1.



Pin Assignments

Table 5: Pin Assignments

| 240-Pin DDR3 VLP RDIMM Front | | | | | | | | 240-Pin DDR3 VLP RDIMM Back | | | | | | | |
|------------------------------|--------------------|-----|-----------------|-----|--------------------|-----|-----------------|-----------------------------|-----------------|-----|-----------------|-----|-----------------|-----|--------------------|
| Pin | Symbol | Pin | Symbol | Pin | Symbol | Pin | Symbol | Pin | Symbol | Pin | Symbol | Pin | Symbol | Pin | Symbol |
| 1 | V _{REFDQ} | 31 | DQ25 | 61 | A2 | 91 | DQ41 | 121 | V _{SS} | 151 | V _{SS} | 181 | A1 | 211 | V _{SS} |
| 2 | V _{SS} | 32 | V _{SS} | 62 | V _{DD} | 92 | V _{SS} | 122 | DQ4 | 152 | DQS12 | 182 | V _{DD} | 212 | DQS14 |
| 3 | DQ0 | 33 | DQS3# | 63 | NF | 93 | DQS5# | 123 | DQ5 | 153 | DQS12# | 183 | V _{DD} | 213 | DQS14# |
| 4 | DQ1 | 34 | DQS3 | 64 | NF | 94 | DQS5 | 124 | V _{SS} | 154 | V _{SS} | 184 | CK0 | 214 | V _{SS} |
| 5 | V _{SS} | 35 | V _{SS} | 65 | V _{DD} | 95 | V _{SS} | 125 | DQS9 | 155 | DQ30 | 185 | CK0# | 215 | DQ46 |
| 6 | DQS0# | 36 | DQ26 | 66 | V _{DD} | 96 | DQ42 | 126 | DQS9# | 156 | DQ31 | 186 | V _{DD} | 216 | DQ47 |
| 7 | DQS0 | 37 | DQ27 | 67 | V _{REFCA} | 97 | DQ43 | 127 | V _{SS} | 157 | V _{SS} | 187 | EVENT# | 217 | V _{SS} |
| 8 | V _{SS} | 38 | V _{SS} | 68 | Par_In | 98 | V _{SS} | 128 | DQ6 | 158 | CB4 | 188 | A0 | 218 | DQ52 |
| 9 | DQ2 | 39 | CB0 | 69 | V _{DD} | 99 | DQ48 | 129 | DQ7 | 159 | CB5 | 189 | V _{DD} | 219 | DQ53 |
| 10 | DQ3 | 40 | CB1 | 70 | A10 | 100 | DQ49 | 130 | V _{SS} | 160 | V _{SS} | 190 | BA1 | 220 | V _{SS} |
| 11 | V _{SS} | 41 | V _{SS} | 71 | BA0 | 101 | V _{SS} | 131 | DQ12 | 161 | DQS17 | 191 | V _{DD} | 221 | DQS15 |
| 12 | DQ8 | 42 | DQS8# | 72 | V _{DD} | 102 | DQS6# | 132 | DQ13 | 162 | DQS17# | 192 | RAS# | 222 | DQS15# |
| 13 | DQ9 | 43 | DQS8 | 73 | WE# | 103 | DQS6 | 133 | V _{SS} | 163 | V _{SS} | 193 | S0# | 223 | V _{SS} |
| 14 | V _{SS} | 44 | V _{SS} | 74 | CAS# | 104 | V _{SS} | 134 | DQS10 | 164 | CB6 | 194 | V _{DD} | 224 | DQ54 |
| 15 | DQS1# | 45 | CB2 | 75 | V _{DD} | 105 | DQ50 | 135 | DQS10# | 165 | CB7 | 195 | ODT0 | 225 | DQ55 |
| 16 | DQS1 | 46 | CB3 | 76 | S1# | 106 | DQ51 | 136 | V _{SS} | 166 | V _{SS} | 196 | A13 | 226 | V _{SS} |
| 17 | V _{SS} | 47 | V _{SS} | 77 | ODT1 | 107 | V _{SS} | 137 | DQ14 | 167 | NC | 197 | V _{DD} | 227 | DQ60 |
| 18 | DQ10 | 48 | V _{TT} | 78 | V _{DD} | 108 | DQ56 | 138 | DQ15 | 168 | RESET# | 198 | NC | 228 | DQ61 |
| 19 | DQ11 | 49 | V _{TT} | 79 | NC | 109 | DQ57 | 139 | V _{SS} | 169 | CKE1 | 199 | V _{SS} | 229 | V _{SS} |
| 20 | V _{SS} | 50 | CKE0 | 80 | V _{SS} | 110 | V _{SS} | 140 | DQ20 | 170 | V _{DD} | 200 | DQ36 | 230 | DQS16 |
| 21 | DQ16 | 51 | V _{DD} | 81 | DQ32 | 111 | DQS7# | 141 | DQ21 | 171 | A15 | 201 | DQ37 | 231 | DQS16# |
| 22 | DQ17 | 52 | BA2 | 82 | DQ33 | 112 | DQS7 | 142 | V _{SS} | 172 | A14 | 202 | V _{SS} | 232 | V _{SS} |
| 23 | V _{SS} | 53 | Err_Out# | 83 | V _{SS} | 113 | V _{SS} | 143 | DQS11 | 173 | V _{DD} | 203 | DQS13 | 233 | DQ62 |
| 24 | DQS2# | 54 | V _{DD} | 84 | DQS4# | 114 | DQ58 | 144 | DQS11# | 174 | A12 | 204 | DQS13# | 234 | DQ63 |
| 25 | DQS2 | 55 | A11 | 85 | DQS4 | 115 | DQ59 | 145 | V _{SS} | 175 | A9 | 205 | V _{SS} | 235 | V _{SS} |
| 26 | V _{SS} | 56 | A7 | 86 | V _{SS} | 116 | V _{SS} | 146 | DQ22 | 176 | V _{DD} | 206 | DQ38 | 236 | V _{DDSPD} |
| 27 | DQ18 | 57 | V _{DD} | 87 | DQ34 | 117 | SA0 | 147 | DQ23# | 177 | A8 | 207 | DQ39 | 237 | SA1 |
| 28 | DQ19 | 58 | A5 | 88 | DQ35 | 118 | SCL | 148 | V _{SS} | 178 | A6 | 208 | V _{SS} | 238 | SDA |
| 29 | V _{SS} | 59 | A4 | 89 | V _{SS} | 119 | SA2 | 149 | DQ28 | 179 | V _{DD} | 209 | DQ44 | 239 | V _{SS} |
| 30 | DQ24 | 60 | V _{DD} | 90 | DQ40 | 120 | V _{TT} | 150 | DQ29 | 180 | A3 | 210 | DQ45 | 240 | V _{TT} |

Pin Descriptions

The pin description table below is a comprehensive list of all possible pins for all DDR3 modules. All pins listed may not be supported on this module. See Pin Assignments for information specific to this module.

Table 6: Pin Descriptions

| Symbol | Type | Description |
|-----------------|-------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Ax | Input | Address inputs: Provide the row address for ACTIVE commands, and the column address and auto precharge bit (A10) for READ/WRITE commands, to select one location out of the memory array in the respective bank. A10 sampled during a PRECHARGE command determines whether the PRECHARGE applies to one bank (A10 LOW, bank selected by BAx) or all banks (A10 HIGH). The address inputs also provide the op-code during a LOAD MODE command. See the Pin Assignments Table for density-specific addressing information. |
| BAx | Input | Bank address inputs: Define the device bank to which an ACTIVE, READ, WRITE, or PRECHARGE command is being applied. BA define which mode register (MR0, MR1, MR2, or MR3) is loaded during the LOAD MODE command. |
| CKx, CKx# | Input | Clock: Differential clock inputs. All control, command, and address input signals are sampled on the crossing of the positive edge of CK and the negative edge of CK#. |
| CKEx | Input | Clock enable: Enables (registered HIGH) and disables (registered LOW) internal circuitry and clocks on the DRAM. |
| DMx | Input | Data mask (x8 devices only): DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH, along with that input data, during a write access. Although DM pins are input-only, DM loading is designed to match that of the DQ and DQS pins. |
| ODTx | Input | On-die termination: Enables (registered HIGH) and disables (registered LOW) termination resistance internal to the DDR3 SDRAM. When enabled in normal operation, ODT is only applied to the following pins: DQ, DQS, DQS#, DM, and CB. The ODT input will be ignored if disabled via the LOAD MODE command. |
| Par_In | Input | Parity input: Parity bit for Ax, RAS#, CAS#, and WE#. |
| RAS#, CAS#, WE# | Input | Command inputs: RAS#, CAS#, and WE# (along with S#) define the command being entered. |
| RESET# | Input (LVCMOS) | Reset: RESET# is an active LOW asynchronous input that is connected to each DRAM and the registering clock driver. After RESET# goes HIGH, the DRAM must be reinitialized as though a normal power-up was executed. |
| Sx# | Input | Chip select: Enables (registered LOW) and disables (registered HIGH) the command decoder. |
| SAx | Input | Serial address inputs: Used to configure the temperature sensor/SPD EEPROM address range on the I ² C bus. |
| SCL | Input | Serial clock for temperature sensor/SPD EEPROM: Used to synchronize communication to and from the temperature sensor/SPD EEPROM on the I ² C bus. |
| CBx | I/O | Check bits: Used for system error detection and correction. |
| DQx | I/O | Data input/output: Bidirectional data bus. |
| DQSx, DQSx# | I/O | Data strobe: Differential data strobes. Output with read data; edge-aligned with read data; input with write data; center-aligned with write data. |

Table 6: Pin Descriptions (Continued)

| Symbol | Type | Description |
|--------------------|------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| SDA | I/O | Serial data: Used to transfer addresses and data into and out of the temperature sensor/SPD EEPROM on the I ² C bus. |
| TDQSx, TDQSx# | Output | Redundant data strobe (x8 devices only): TDQS is enabled/disabled via the LOAD MODE command to the extended mode register (EMR). When TDQS is enabled, DM is disabled and TDQS and TDQS# provide termination resistance; otherwise, TDQS# are no function. |
| Err_Out# | Output (open drain) | Parity error output: Parity error found on the command and address bus. |
| EVENT# | Output (open drain) | Temperature event: The EVENT# pin is asserted by the temperature sensor when critical temperature thresholds have been exceeded. |
| V _{DD} | Supply | Power supply: 1.5V ±0.075V. The component V _{DD} and V _{DDQ} are connected to the module V _{DD} . |
| V _{DDSPD} | Supply | Temperature sensor/SPD EEPROM power supply: 3.0–3.6V. |
| V _{REFCA} | Supply | Reference voltage: Control, command, and address V _{DD} /2. |
| V _{REFDQ} | Supply | Reference voltage: DQ, DM V _{DD} /2. |
| V _{SS} | Supply | Ground. |
| V _{TT} | Supply | Termination voltage: Used for control, command, and address V _{DD} /2. |
| NC | – | No connect: These pins are not connected on the module. |
| NF | – | No function: These pins are connected within the module, but provide no functionality. |



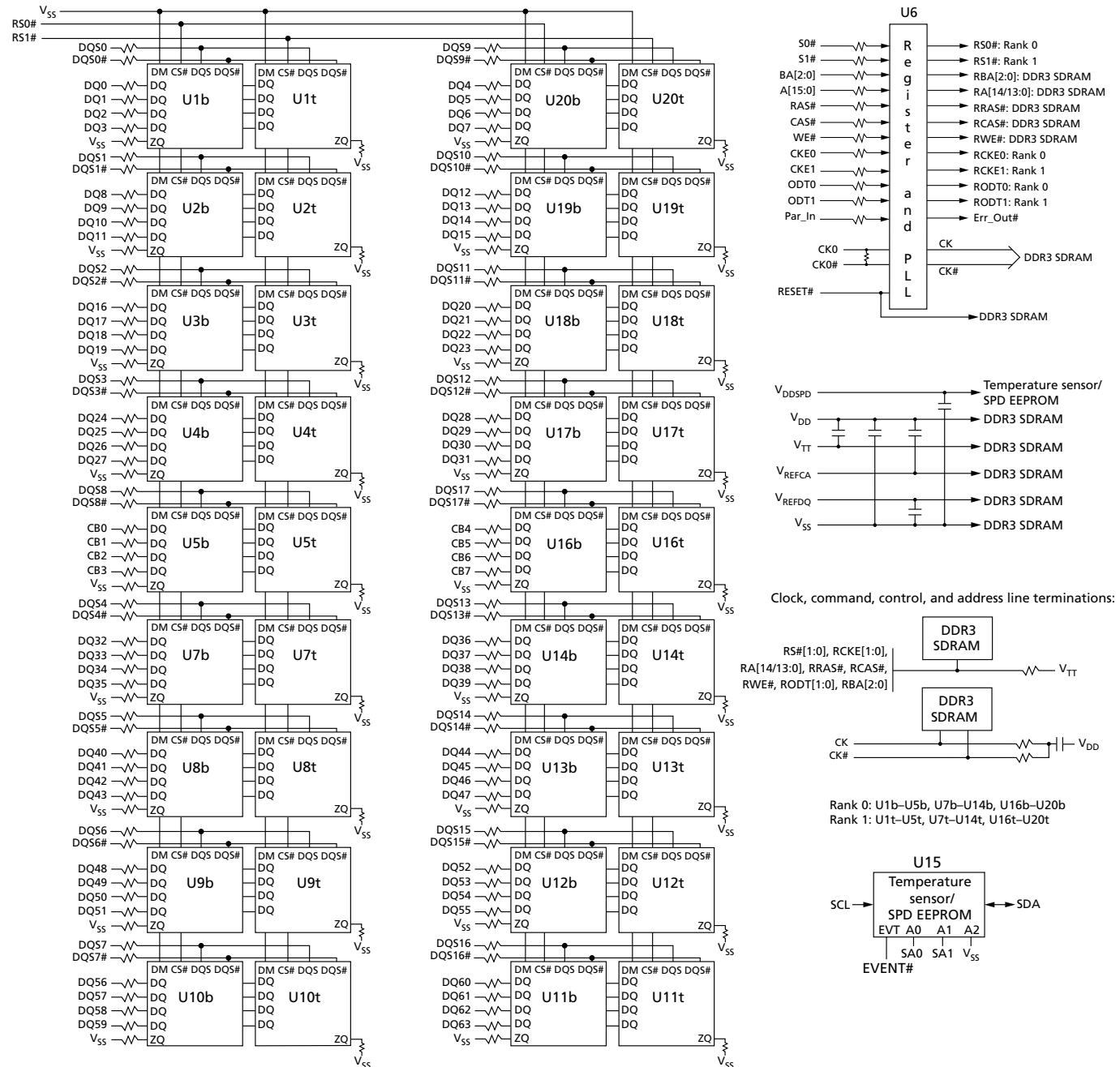
DQ Map

Table 7: Component-to-Module DQ Map

| Component Reference Number | Component DQ | Module DQ | Module Pin Number | Component Reference Number | Component DQ | Module DQ | Module Pin Number |
|----------------------------|--------------|-----------|-------------------|----------------------------|--------------|-----------|-------------------|
| U1 | 0 | 2 | 9 | U11 | 0 | 61 | 228 |
| | 1 | 1 | 4 | | 1 | 62 | 233 |
| | 2 | 3 | 10 | | 2 | 60 | 227 |
| | 3 | 0 | 3 | | 3 | 63 | 234 |
| U2 | 0 | 10 | 18 | U12 | 0 | 53 | 219 |
| | 1 | 9 | 13 | | 1 | 54 | 224 |
| | 2 | 11 | 19 | | 2 | 52 | 218 |
| | 3 | 8 | 12 | | 3 | 55 | 225 |
| U3 | 0 | 18 | 27 | U13 | 0 | 45 | 210 |
| | 1 | 17 | 22 | | 1 | 46 | 215 |
| | 2 | 19 | 28 | | 2 | 44 | 209 |
| | 3 | 16 | 21 | | 3 | 47 | 216 |
| U4 | 0 | 26 | 36 | U14 | 0 | 37 | 201 |
| | 1 | 25 | 31 | | 1 | 38 | 206 |
| | 2 | 27 | 37 | | 2 | 36 | 200 |
| | 3 | 24 | 30 | | 3 | 39 | 207 |
| U5 | 0 | CB2 | 45 | U16 | 0 | CB5 | 159 |
| | 1 | CB1 | 40 | | 1 | CB6 | 164 |
| | 2 | CB3 | 46 | | 2 | CB4 | 158 |
| | 3 | CB0 | 39 | | 3 | CB7 | 165 |
| U7 | 0 | 34 | 87 | U17 | 0 | 29 | 150 |
| | 1 | 33 | 82 | | 1 | 30 | 155 |
| | 2 | 35 | 88 | | 2 | 28 | 149 |
| | 3 | 32 | 81 | | 3 | 31 | 156 |
| U8 | 0 | 42 | 96 | U18 | 0 | 21 | 141 |
| | 1 | 41 | 91 | | 1 | 22 | 146 |
| | 2 | 43 | 97 | | 2 | 20 | 140 |
| | 3 | 40 | 90 | | 3 | 23 | 147 |
| U9 | 0 | 50 | 105 | U19 | 0 | 13 | 132 |
| | 1 | 49 | 100 | | 1 | 14 | 137 |
| | 2 | 51 | 106 | | 2 | 12 | 131 |
| | 3 | 48 | 99 | | 3 | 15 | 138 |
| U10 | 0 | 58 | 114 | U20 | 0 | 5 | 123 |
| | 1 | 57 | 109 | | 1 | 5 | 128 |
| | 2 | 59 | 115 | | 2 | 6 | 122 |
| | 3 | 56 | 108 | | 3 | 7 | 129 |

Functional Block Diagram

Figure 2: Functional Block Diagram



Note: 1. The ZQ ball on each DDR3 component is connected to an external $240\Omega \pm 1\%$ resistor that is tied to ground. It is used for the calibration of the component's ODT and output driver.

General Description

DDR3 SDRAM modules are high-speed, CMOS dynamic random access memory modules that use internally configured 8-bank DDR3 SDRAM devices. DDR3 SDRAM modules use DDR architecture to achieve high-speed operation. DDR3 architecture is essentially a $8n$ -prefetch architecture with an interface designed to transfer two data words per clock cycle at the I/O pins. A single read or write access for the DDR3 SDRAM module effectively consists of a single $8n$ -bit-wide, one-clock-cycle data transfer at the internal DRAM core and eight corresponding n -bit-wide, one-half-clock-cycle data transfers at the I/O pins.

DDR3 modules use two sets of differential signals: DQS, DQS# to capture data and CK and CK# to capture commands, addresses, and control signals. Differential clocks and data strobes ensure exceptional noise immunity for these signals and provide precise crossing points to capture input signals.

Fly-By Topology

DDR3 modules use faster clock speeds than earlier DDR technologies, making signal quality more important than ever. For improved signal quality, the clock, control, command, and address buses have been routed in a fly-by topology, where each clock, control, command, and address pin on each DRAM is connected to a single trace and terminated (rather than a tree structure, where the termination is off the module near the connector). Inherent to fly-by topology, the timing skew between the clock and DQS signals can be easily accounted for by using the write-leveling feature of DDR3.

Registering Clock Driver Operation

Registered DDR3 SDRAM modules use a registering clock driver device consisting of a register and a phase-lock loop (PLL). The device complies with the JEDEC standard "Definition of the SSTE32882 Registering Clock Driver with Parity and Quad Chip Selects for DDR3 RDIMM Applications."

The register section of the registering clock driver latches command and address input signals on the rising clock edge. The PLL section of the registering clock driver receives and redrives the differential clock signals (CK, CK#) to the DDR3 SDRAM devices. The register(s) and PLL reduce clock, control, command, and address signals loading by isolating DRAM from the system controller.

Parity Operations

The registering clock driver includes an even parity function for checking parity. The memory controller accepts a parity bit at the Par_In input and compares it with the data received on A[15:0], BA[2:0], RAS#, CAS#, and WE#. Valid parity is defined as an even number of ones (1s) across the address and command inputs (A[15:0], BA[2:0], RAS#, CAS#, and WE#) combined with Par_In. Parity errors are flagged on Err_Out#.

Address and command parity is checked during all DRAM operations and during control word WRITE operations to the registering clock driver. For SDRAM operations, the address is still propagated to the SDRAM even when there is a parity error. When writing to the internal control words of the registering clock driver, the write will be ignored if parity is not valid. For this reason, systems must connect the Par_In pins on the DIMM and provide correct parity when writing to the registering clock driver control word configuration registers.



Temperature Sensor with Serial Presence-Detect EEPROM

Thermal Sensor Operations

The temperature from the integrated thermal sensor is monitored and converts into a digital word via the I²C bus. System designers can use the user-programmable registers to create a custom temperature-sensing solution based on system requirements. Programming and configuration details comply with JEDEC standard No. 21-C page 4.7-1, "Definition of the TSE2002av, Serial Presence Detect with Temperature Sensor."

Serial Presence-Detect EEPROM Operation

DDR3 SDRAM modules incorporate serial presence-detect. The SPD data is stored in a 256-byte EEPROM. The first 128 bytes are programmed by Micron to comply with JEDEC standard JC-45, "Appendix X: Serial Presence Detect (SPD) for DDR3 SDRAM Modules." These bytes identify module-specific timing parameters, configuration information, and physical attributes. The remaining 128 bytes of storage are available for use by the customer. System READ/WRITE operations between the master (system logic) and the slave EEPROM device occur via a standard I²C bus using the DIMM's SCL (clock) SDA (data), and SA (address) pins. Write protect (WP) is connected to V_{SS}, permanently disabling hardware write protection. For further information refer to Micron technical note TN-04-42, "Memory Module Serial Presence-Detect."

Electrical Specifications

Stresses greater than those listed may cause permanent damage to the module. This is a stress rating only, and functional operation of the module at these or any other conditions outside those indicated in each device's data sheet is not implied. Exposure to absolute maximum rating conditions for extended periods may adversely affect reliability.

Table 8: Absolute Maximum Ratings

| Symbol | Parameter | Min | Max | Units |
|-------------------|----------------------------------------------|------|-------|-------|
| V_{DD} | V_{DD} supply voltage relative to V_{SS} | -0.4 | 1.975 | V |
| V_{IN}, V_{OUT} | Voltage on any pin relative to V_{SS} | -0.4 | 1.975 | V |

Table 9: Operating Conditions

| Symbol | Parameter | Min | Nom | Max | Units | Notes | |
|------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------------------------------------------------|---------------------|------------------------------------|---------------|--------------------|---------|
| V_{DD} | V_{DD} supply voltage | 1.425 | 1.5 | 1.575 | V | | |
| I_{VT} | Termination reference current from V_{TT} | -600 | - | 600 | mA | | |
| V_{TT} | Termination reference voltage (DC) – command/address bus | $0.49 \times V_{DD} - 20\text{mV}$ | $0.5 \times V_{DD}$ | $0.51 \times V_{DD} + 20\text{mV}$ | V | 1 | |
| I_i | Input leakage current; Any input $0\text{V} \leq V_{IN} \leq V_{DD}$; V_{REF} input $0\text{V} \leq V_{IN} \leq 0.95\text{V}$ (All other pins not under test = 0V) | Address inputs, RAS#, CAS#, WE#, S#, CKE, ODT, BA, CK, CK# | TBD | TBD | TBD | μA | |
| | | DM | -4 | 0 | 4 | | |
| I_{OZ} | Output leakage current; $0\text{V} \leq V_{OUT} \leq V_{DD}$; DQ and ODT are disabled; ODT is HIGH | -10 | 0 | 10 | μA | | |
| I_{VREF} | V_{REF} supply leakage current; $V_{REFDQ} = V_{DD}/2$ or $V_{REFCA} = V_{DD}/2$ (All other pins not under test = 0V) | -36 | 0 | 36 | μA | | |
| T_A | Module ambient operating temperature | Commercial | 0 | - | 70 | $^{\circ}\text{C}$ | 2, 3 |
| | | Industrial | -40 | - | 85 | $^{\circ}\text{C}$ | |
| T_C | DDR3 SDRAM component case operating temperature | Commercial | 0 | - | 95 | $^{\circ}\text{C}$ | 2, 3, 4 |
| | | Industrial | -40 | - | 95 | $^{\circ}\text{C}$ | |

- Notes:
- V_{TT} termination voltage in excess of the stated limit will adversely affect the command and address signals' voltage margin and will reduce timing margins.
 - T_A and T_C are simultaneous requirements.
 - For further information, refer to technical note [TN-00-08: "Thermal Applications,"](#) available on Micron's Web site.
 - The refresh rate is required to double when $85^{\circ}\text{C} < T_C \leq 95^{\circ}\text{C}$.

DRAM Operating Conditions

Recommended AC operating conditions are given in the DDR3 component data sheets. Component specifications are available on Micron's Web site. Module speed grades correlate with component speed grades, as shown below.

Table 10: Module and Component Speed Grades

DDR3 components may exceed the listed module speed grades; module may not be available in all listed speed grades

| Module Speed Grade | Component Speed Grade |
|--------------------|-----------------------|
| -1G9 | -107 |
| -1G6 | -125 |
| -1G4 | -15E |
| -1G1 | -187E |
| -1G0 | -187 |
| -80C | -25E |
| -80B | -25 |

Design Considerations

Simulations

Micron memory modules are designed to optimize signal integrity through carefully designed terminations, controlled board impedances, routing topologies, trace length matching, and decoupling. However, good signal integrity starts at the system level. Micron encourages designers to simulate the signal characteristics of the system's memory bus to ensure adequate signal integrity of the entire memory system.

Power

Operating voltages are specified at the DRAM, not at the edge connector of the module. Designers must account for any system voltage drops at anticipated power levels to ensure the required supply voltage is maintained.



I_{DD} Specifications

Table 11: DDR3 I_{CDD} Specifications and Conditions – 4GB (All Die Revisions)

Values are for the MT41J512M4 DDR3 SDRAM only and are computed from values specified in the 2Gb TwinDie (512 Meg x 4) component data sheet

| Parameter | Combined Symbol | 1600 | 1333 | 1066 | Units |
|------------------------------------------------------------------------------|---------------------|------|------|------|-------|
| Operating current 0: One bank ACTIVATE-to-PRECHARGE | I _{CDD0} | 2016 | 1836 | 1656 | mA |
| Operating current 1: One bank ACTIVATE-to-READ-to-PRECHARGE | I _{CDD1} | 2376 | 2196 | 2016 | mA |
| Precharge power-down current: Slow exit | I _{CDD2P} | 432 | 432 | 432 | mA |
| Precharge power-down current: Fast exit | I _{CDD2P} | 1026 | 936 | 846 | mA |
| Precharge quiet standby current | I _{CDD2Q} | 1422 | 1296 | 1170 | mA |
| Precharge standby current | I _{CDD2N} | 1476 | 1386 | 1206 | mA |
| Precharge standby ODT current | I _{CDD2NT} | 1926 | 1746 | 1566 | mA |
| Active power-down current | I _{CDD3P} | 1026 | 936 | 846 | mA |
| Active standby current | I _{CDD3N} | 1422 | 1332 | 1242 | mA |
| Burst read operating current | I _{CDD4R} | 4806 | 3906 | 3186 | mA |
| Burst write operating current | I _{CDD4W} | 4806 | 4266 | 3726 | mA |
| Refresh current | I _{CDD5B} | 4896 | 4536 | 4176 | mA |
| Self refresh temperature current: MAX T _C = 85°C | I _{CDD6} | 216 | 216 | 216 | mA |
| Self refresh temperature current (SRT-enabled): MAX T _C = 95°C | I _{CDD6ET} | 324 | 324 | 324 | mA |
| All banks interleaved read current | I _{CDD7} | 7506 | 5976 | 4806 | mA |
| Reset current | I _{CDD8} | 504 | 504 | 504 | mA |



Table 12: DDR3 I_{CDD} Specifications and Conditions – 8GB (Die Revision D)

Values are for the MT41J1G4 DDR3 SDRAM only and are computed from values specified in the 4Gb TwinDie (1 Gig x 4) component data sheet

| Parameter | Combined Symbol | 1600 | 1333 | 1066 | Units |
|------------------------------------------------------------------------------|---------------------|------|------|------|-------|
| Operating current 0: One bank ACTIVATE-to-PRECHARGE | I _{CDD0} | 2016 | 1836 | 1656 | mA |
| Operating current 1: One bank ACTIVATE-to-READ-to-PRECHARGE | I _{CDD1} | 2196 | 2106 | 2016 | mA |
| Precharge power-down current: Slow exit | I _{CDD2P} | 432 | 432 | 432 | mA |
| Precharge power-down current: Fast exit | I _{CDD2P} | 846 | 756 | 666 | mA |
| Precharge quiet standby current | I _{CDD2Q} | 936 | 846 | 756 | mA |
| Precharge standby current | I _{CDD2N} | 972 | 882 | 792 | mA |
| Precharge standby ODT current | I _{CDD2NT} | 1116 | 1026 | 936 | mA |
| Active power-down current | I _{CDD3P} | 936 | 846 | 756 | mA |
| Active standby current | I _{CDD3N} | 1026 | 936 | 846 | mA |
| Burst read operating current | I _{CDD4R} | 3276 | 2916 | 2556 | mA |
| Burst write operating current | I _{CDD4W} | 3366 | 3096 | 2736 | mA |
| Refresh current | I _{CDD5B} | 4086 | 3816 | 3636 | mA |
| Self refresh temperature current: MAX T _C = 85°C | I _{CDD6} | 432 | 432 | 432 | mA |
| Self refresh temperature current (SRT-enabled): MAX T _C = 95°C | I _{CDD6ET} | 540 | 540 | 540 | mA |
| All banks interleaved read current | I _{CDD7} | 8136 | 7236 | 6336 | mA |
| Reset current | I _{CDD8} | 504 | 504 | 504 | mA |



Table 13: DDR3 I_{CDD} Specifications and Conditions – 8GB (Die Revision M)

Values are for the MT41J1G4 DDR3 SDRAM only and are computed from values specified in the 4Gb TwinDie (1 Gig x 4) component data sheet

| Parameter | Combined Symbol | 1600 | 1333 | 1066 | Units |
|------------------------------------------------------------------------------|---------------------|------|------|------|-------|
| Operating current 0: One bank ACTIVATE-to-PRECHARGE | I _{CDD0} | 1476 | 1386 | 1296 | mA |
| Operating current 1: One bank ACTIVATE-to-READ-to-PRECHARGE | I _{CDD1} | 1656 | 1566 | 1476 | mA |
| Precharge power-down current: Slow exit | I _{CDD2P} | 432 | 432 | 432 | mA |
| Precharge power-down current: Fast exit | I _{CDD2P} | 882 | 792 | 702 | mA |
| Precharge quiet standby current | I _{CDD2Q} | 936 | 846 | 756 | mA |
| Precharge standby current | I _{CDD2N} | 990 | 900 | 810 | mA |
| Precharge standby ODT current | I _{CDD2NT} | 1026 | 936 | 846 | mA |
| Active power-down current | I _{CDD3P} | 1116 | 1026 | 936 | mA |
| Active standby current | I _{CDD3N} | 1206 | 1116 | 1026 | mA |
| Burst read operating current | I _{CDD4R} | 2754 | 2484 | 2286 | mA |
| Burst write operating current | I _{CDD4W} | 2556 | 2286 | 2016 | mA |
| Refresh current | I _{CDD5B} | 3726 | 3636 | 3546 | mA |
| Self refresh temperature current: MAX T _C = 85°C | I _{CDD6} | 432 | 432 | 432 | mA |
| Self refresh temperature current (SRT-enabled): MAX T _C = 95°C | I _{CDD6ET} | 540 | 540 | 540 | mA |
| All banks interleaved read current | I _{CDD7} | 4536 | 4266 | 3996 | mA |
| Reset current | I _{CDD8} | 504 | 504 | 504 | mA |



Registering Clock Driver Specifications

Table 14: Registering Clock Driver Electrical Characteristics

SSTE32882 devices or equivalent

| Parameter | Symbol | Pins | Min | Nom | Max | Units |
|---------------------------------------------|----------------|---------------------------|------------------------------------|---------------------|------------------------------------|-------|
| DC supply voltage | V_{DD} | – | 1.425 | 1.5 | 1.575 | V |
| DC reference voltage | V_{REF} | – | $0.49 \times V_{DD} - 20\text{mV}$ | $0.5 \times V_{DD}$ | $0.51 \times V_{DD} + 20\text{mV}$ | V |
| DC termination voltage | V_{TT} | – | $0.49 \times V_{DD} - 20\text{mV}$ | $0.5 \times V_{DD}$ | $0.51 \times V_{DD} + 20\text{mV}$ | V |
| AC high-level input voltage | $V_{IH(AC)}$ | Control, command, address | $V_{REF} + 175\text{mV}$ | – | $V_{DD} + 400\text{mV}$ | V |
| AC low-level input voltage | $V_{IL(AC)}$ | Control, command, address | –0.4 | – | $V_{REF} - 175\text{mV}$ | V |
| DC high-level input voltage | $V_{IH(DC)}$ | Control, command, address | $V_{REF} + 100\text{mV}$ | – | $V_{DD} + 0.4$ | V |
| DC low-level input voltage | $V_{IL(DC)}$ | Control, command, address | –0.4 | – | $V_{REF} - 100\text{mV}$ | V |
| High-level input voltage | $V_{IH(CMOS)}$ | RESET#, MIRROR | $0.65 \times V_{DD}$ | – | V_{DD} | V |
| Low-level input voltage | $V_{IL(CMOS)}$ | RESET#, MIRROR | 0 | – | $0.35 \times V_{DD}$ | V |
| Differential input crosspoint voltage range | $V_{IX(AC)}$ | CK, CK#, FBIN, FBIN# | $0.5 \times V_{DD} - 175\text{mV}$ | $0.5 \times V_{DD}$ | $0.5 \times V_{DD} + 175\text{mV}$ | V |
| Differential input voltage | $V_{ID(AC)}$ | CK, CK# | 350 | – | $V_{DD} + \text{TBD}$ | mV |
| High-level output current | I_{OH} | Err_Out# | – | – | TBD | mA |
| Low-level output current | I_{OL} | Err_Out# | TBD | – | TBD | mA |

Note: 1. Timing and switching specifications for the register listed are critical for proper operation of the DDR3 SDRAM RDIMMs. These are meant to be a subset of the parameters for the specific device used on the module.



Temperature Sensor with Serial Presence-Detect EEPROM

The temperature sensor continuously monitors the module's temperature and can be read back at any time over the I²C bus shared with the SPD EEPROM. Refer to JEDEC standard No. 21-C page 4.7-1, "Definition of the TSE2002av, Serial Presence Detect with Temperature Sensor."

Serial Presence-Detect

For the latest SPD data, refer to Micron's SPD page: www.micron.com/SPD.

Table 15: Temperature Sensor with SPD EEPROM Operating Conditions

| Parameter/Condition | Symbol | Min | Max | Units |
|----------------------------------------------|--------------------|------|------------------------|-------|
| Supply voltage | V _{DDSPD} | 3.0 | 3.6 | V |
| Supply current: V _{DD} = 3.3V | I _{DD} | – | 2.0 | mA |
| Input high voltage: Logic 1; SCL, SDA | V _{IH} | 1.45 | V _{DDSPD} + 1 | V |
| Input low voltage: Logic 0; SCL, SDA | V _{IL} | – | 0.55 | V |
| Output low voltage: I _{OUT} = 2.1mA | V _{OL} | – | 0.4 | V |
| Input current | I _{IN} | –5.0 | 5.0 | μA |
| Temperature sensing range | – | –40 | 125 | °C |
| Temperature sensor accuracy (class B) | – | –1.0 | 1.0 | °C |

Table 16: Temperature Sensor and EEPROM Serial Interface Timing

| Parameter/Condition | Symbol | Min | Max | Units |
|---------------------------------------------------------|---------------------|-----|------|-------|
| Time bus must be free before a new transition can start | t _{BUF} | 4.7 | – | μs |
| SDA fall time | t _F | 20 | 300 | ns |
| SDA rise time | t _R | – | 1000 | ns |
| Data hold time | t _{HD:DAT} | 200 | 900 | ns |
| Start condition hold time | t _{H:STA} | 4.0 | – | μs |
| Clock HIGH period | t _{HIGH} | 4.0 | 50 | μs |
| Clock LOW period | t _{LOW} | 4.7 | – | μs |
| SCL clock frequency | t _{SCL} | 10 | 100 | kHz |
| Data setup time | t _{SU:DAT} | 250 | – | ns |
| Start condition setup time | t _{SU:STA} | 4.7 | – | μs |
| Stop condition setup time | t _{SU:STO} | 4.0 | – | μs |

EVENT# Pin

The temperature sensor also adds the EVENT# pin (open-drain). Not used by the SPD EEPROM, EVENT# is a temperature sensor output used to flag critical events that can be set up in the sensor's configuration register.

EVENT# has three defined modes of operation: interrupt mode, compare mode, and critical temperature mode. Event thresholds are programmed in the 0x01 register using a hysteresis. The alarm window provides a comparison window, with upper and lower limits set in the alarm upper boundary register and the alarm lower boundary register, respectively. When the alarm window is enabled, EVENT# will trigger whenever the temperature is outside the MIN or MAX values set by the user.

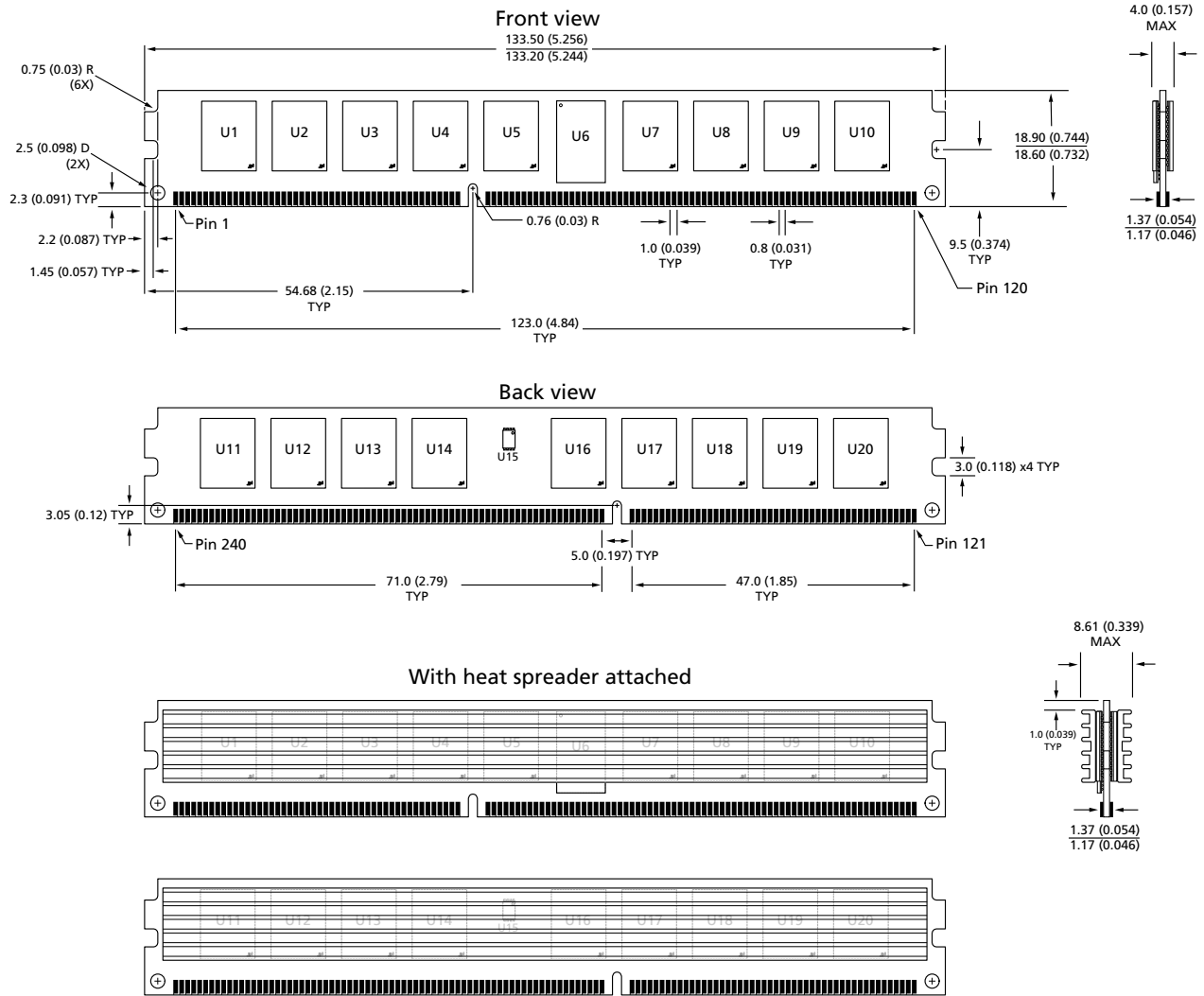
The interrupt mode enables software to reset EVENT# after a critical temperature threshold has been detected. Threshold points are set in the configuration register by the user. This mode triggers the critical temperature limit and both the MIN and MAX of the temperature window.

The compare mode is similar to the interrupt mode, except EVENT# cannot be reset by the user and returns to the logic HIGH state only when the temperature falls below the programmed thresholds.

Critical temperature mode triggers EVENT# only when the temperature has exceeded the programmed critical trip point. When the critical trip point has been reached, the temperature sensor goes into comparator mode, and the critical EVENT# cannot be cleared through software.

Module Dimensions

Figure 3: 240-Pin DDR3 RDIMM



- Notes: 1. All dimensions are in millimeters (inches); MAX/MIN or typical (TYP) where noted.
 2. The dimensional diagram is for reference only.

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This data sheet contains minimum and maximum limits specified over the power supply and temperature range set forth herein. Although considered final, these specifications are subject to change, as further product development and data characterization sometimes occur.