# HIGH-SPEED, UNITY-GAIN BUFFER/DRIVER AMPLIFIER

## FEATURES

- **Replaces All 0033's**
- **High Speed**
  - **— Bandwidth ..... DC to 100 MHz**
  - **— Slew Rate ..... 1500 V/μs**
- **Settling Time to ±1% (2V step) ..... 25 ns**
- **Low Quiescent Current ..... ±14 mA**

## APPLICATIONS

- **Input-Buffering Flash ADCs**
- **CRT Deflection Yoke Drive**
- **Coaxial Line Driver**
- **Critical Military, Biomedical and Process Control Environments**

## GENERAL DESCRIPTION

The TP0033 is a high-speed, high-input impedance, unity-gain buffer amplifier that is pin, package and performance equivalent to the ubiquitous LH0033. This device matches or exceeds the performance of its counterpart in all applications, yet typically draws just ±14 mA quiescent current, versus ±20 mA typical for the LH0033.

The TP0033 has a FET input stage which provides high-input impedance ($10^{11}\Omega$), low-input bias current (0.5 nA), and low initial input offset voltage (±10 mV). The device operates with supply voltages from ±5V to ±20V (single supply operation is permissible). With nominal ±15V supplies, the TP0033 delivers a guaranteed output of ±12V into 1 kΩ. Other key large-signal specifications are 1500 V/μs slew rate and 25 ns settling time for the unit to settle a 2V step (typical "flash" ADC full-scale input) to within ±1% (±20 mV) of final value.

A 100 MHz bandwidth, 2.9 ns rise time and 1.2 ns propagation delay are key small-signal specifications that further demonstrate the TP0033's suitability for high-frequency, signal-buffering applications.

The TP0033 is housed in a 12-pin TO-8 can. The standard device is specified for –25°C to +85°C operation. The High Reliability (HR) version is specified for –55°C to +125°C operation.

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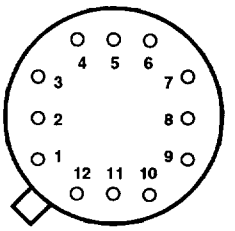
## PIN CONFIGURATION

| Pin No. | Designation | Pin No. | Designation |
|---|---|---|---|
| 1 | $+V_{CC}$ | 7 | OFFSET TRIM |
| 2 | NC | 8 | NC |
| 3 | NC | 9 | $-V_{CC}$ |
| 4 | NC | 10 | $V^-$ |
| 5 | INPUT | 11 | OUTPUT |
| 6 | OFFSET PRESET | 12 | $V^+$ |

NC = No internal connection




BOTTOM VIEW

## TP0033

### ABSOLUTE MAXIMUM RATINGS

$+V_{CC}$– $(-V_{CC})$ Supply Voltage ..... 40V
$V_I$ Input Voltage ..... $\pm V_{CC}$
$P_D$ Power Dissipation (See Figure 9) ..... 1.5W
$T_C$ Operating Temperature Range (Case)
TP0033 ..... –25°C to +85°C
TP0033-HR ..... –55°C to +125°C
$T_{STG}$ Storage Temperature Range ..... –65°C to +150°C

### DC CHARACTERISTICS: (Note 1) $V_{CC}$ = ±15V, $R_L$ = 1 kΩ, $R_S$ = 100Ω, $T_C$ = 25°C, unless otherwise noted.

| | | | TP0033 | | | TP0033-HR | | | |
|---|---|---|---|---|---|---|---|---|---|
| **Symbol** | **Parameter** | **Test Conditions** | **Min** | **Typ** | **Max** | **Min** | **Typ** | **Max** | **Unit** |
| $A_{V/V}$ | Voltage Gain | | **0.96** | 0.98 | **1.00** | **0.96** | 0.98 | **1.00** | V/V |
| $V_{OS}$ | Input Offset Voltage | | — | ±5 | **±10** | — | ±5 | **±10** | mV |
| | | $T_{MIN}$ to $T_{MAX}$ | — | — | — | — | — | **±15** | mV |
| $V_{OS}$ TC | Input Offset Voltage Drift vs Temperature | Average, $T_{MIN}$ to $T_{MAX}$ | — | ±50 | — | — | ±50 | **±250** | µV/°C |
| $I_B$ | Input Bias Current | | — | ±0.5 | **±2.5** | — | ±0.5 | **±2.5** | nA |
| | | $T_{MIN}$ to $T_{MAX}$ | — | — | — | — | — | **±50** | nA |
| PSRR | Power Supply Rejection Ratio | | — | 60 | — | — | 60 | — | dB |
| $Z_I$ | Input Impedance | | $10^{10}$ | $10^{11}$ | — | $10^{10}$ | $10^{11}$ | — | Ω |
| $V_O$ | Output Voltage Swing | | **±12** | ±13 | — | **±12** | ±13 | — | V |
| | | $R_L$ = 100 | **±9** | — | — | **±9** | — | — | V |
| | | $V_{CC}$ = ±5V | — | 6 | — | — | 6 | — | VP-P |
| $I_{SC}$ | Output Short-Circuit Current | (Note 2) | — | N/A | — | — | N/A | — | mA |
| $R_O$ | Output Resistance (DC Open-Loop) | | — | 6 | **10** | — | 6 | **10** | Ω |
| $V_{CC}$ | Supply Voltage Range (Operating) | | ±5 | ±15 | ±20 | ±5 | ±15 | ±20 | V |
| $I_{CC}$ | Quiescent Supply Current | | — | ±14 | **±22** | — | ±14 | **±22** | mA |
| | | $V_{CC}$ = ±5V | — | ±12 | — | — | ±12 | — | mA |
| $P_D$ | Quiescent Power Dissipation | | — | 420 | **660** | — | 420 | **660** | mW |
| | | $V_{CC}$ = ±5V | — | 120 | — | — | 120 | — | mW |

**NOTES:** 1. Limits printed in **boldface** type are guaranteed and 100% production tested. Limits in normal font are guaranteed but not 100% production tested.
2. The TP0033 is not output short-circuit protected and neither are other vendors' 0033's.
Peak instantaneous output current must not exceed ±250 mA.
Continuous output current must not exceed ±100 mA.

### AC CHARACTERISTICS: (Note 1) $V_{CC}$ = ±15V, $R_L$ = 1 kΩ, $R_S$ = 50Ω, $T_C$ = 25°C, unless otherwise noted.

| | | | TP0033 | | | TP0033-HR | | | |
|---|---|---|---|---|---|---|---|---|---|
| **Symbol** | **Parameter** | **Test Conditions** | **Min** | **Typ** | **Max** | **Min** | **Typ** | **Max** | **Unit** |
| $S_R$ | Slew Rate | | 1000 | 1500 | — | 1000 | 1500 | — | V/µs |
| BW | Bandwidth (-3 dB) | $V_{IN}$ = 1.0 VRMS | — | 100 | — | — | 100 | — | MHz |
| $\Phi_{NL}$ | Phase Non-Linearity | BW = 1 Hz to 20 MHz | — | 2 | — | — | 2 | — | ° |
| $t_s$ | Settling Time | 2V step/1% | — | 25 | — | — | 25 | — | ns |
| $t_r$ | Rise Time | $\Delta V_{IN}$ = 0.5V | — | 2.9 | — | — | 2.9 | — | ns |
| $t_{pd}$ | Propagation Delay | $\Delta V_{IN}$ = 0.5V | — | 1.2 | — | — | 1.2 | — | ns |
| THD | Total Harmonic Distortion | f > 1 kHz | — | <0.1 | — | — | <0.1 | — | % |

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## APPLICATIONS INFORMATION

### Offset Adjustment

The TP0033 is factory-trimmed for low initial offset voltage. This is achieved by laser trimming and is implemented by tying pin 6 (offset preset) to pin 7 (offset adjust input). If the offset needs adjusting for any reason (see "Single or Unbalanced Power Supplies"), it can be done by using the offset null scheme shown in Figure 1. If an adjustable offset is not needed, pin 7 must be tied to pin 6. (Pin 7 cannot be left open.)

### Current Limiting

The output of the TP0033 is not short-circuit protected and should not exceed ±100 mA steady-state or ±250 mA peak instantaneous current. For overcurrent protection, the maximum output current of the TP0033 can be limited by the use of current-limiting resistors as shown in Figure 2, or by an active current-source circuit as shown in Figure 3. Whether or not the current is limited, pins 1 and 9 must be connected to $+V_{CC}$ and $-V_{CC}$, respectively.

### Wiring Recommendations

The TP0033, like any high-speed device, is sensitive to layout inductances; therefore, ground planes are recommended. For best performance, each power supply should be individually decoupled; i.e., bypassed to ground. If pin 1 is tied directly to pin 12 and pin 9 is tied directly to pin 10 (Figure 1), connect low-inductance (0.1 µF) ceramic disc capacitors directly to pins 10 and 12 and ground them as closely as possible to the case. If pins 1 and 12 or pins 9 and 10 are not tied together, each pin should be decoupled by a low-inductance (0.1 µF) ceramic disc capacitor, grounded as close as possible to the case.

### Reactive Loading

The TP0033 output can drive large (several thousand pF) capacitive loads and long, properly terminated coaxial lines without tendency to oscillate. Peak capacitive output current levels should not exceed 250 mA.

### Single or Unbalanced Power Supplies

The TP0033 can operate from unbalanced power supplies, such as the +5V/–12V rails prevalent in MOS-based logic systems. An output offset voltage will result, but is correctable by the nulling method shown in Figure 1. It is predictable (with sufficient accuracy) as follows:

$$\text{Offset (V)} = (1-\text{Gain})\ (|+V_{CC}| - |-V_{CC}|)/2$$

gain is typically 0.985; therefore:

$$\text{Offset (V)} = 0.0075\ (|+V_{CC}| - |-V_{CC}|)$$

### Heat Sinking

Idling in a +25°C ambient environment, the TP0033 has an approximate case temperature of +65°C. For best performance, a heat sink (Thermalloy 2240 or equivalent) is recommended, particularly for extended temperature operation.

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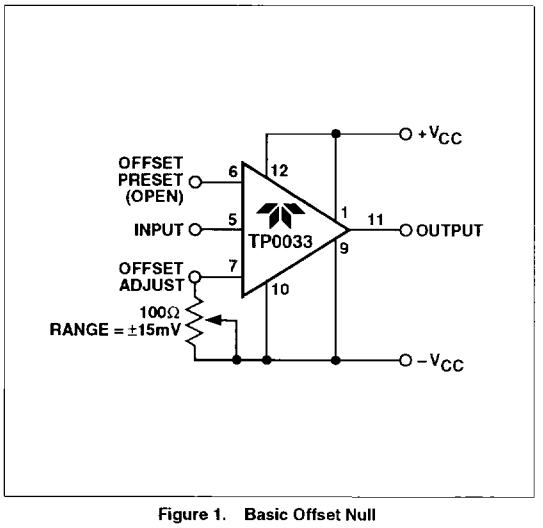


Figure 1. Basic Offset Null

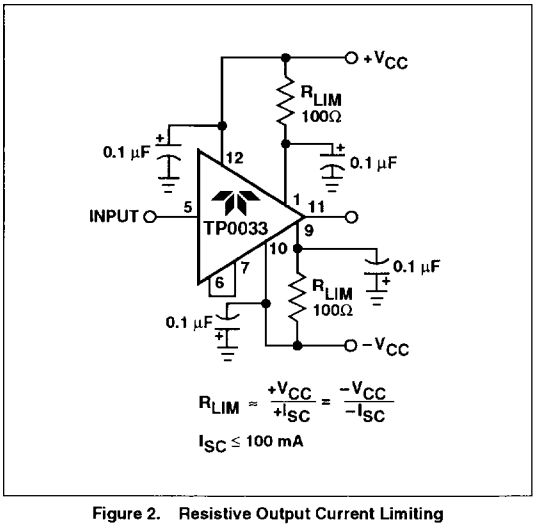


Figure 2. Resistive Output Current Limiting

## TP0033

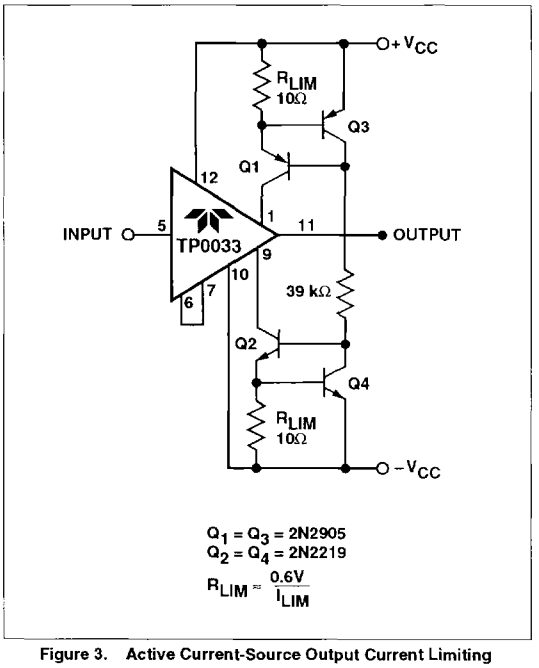


Figure 3. Active Current-Source Output Current Limiting

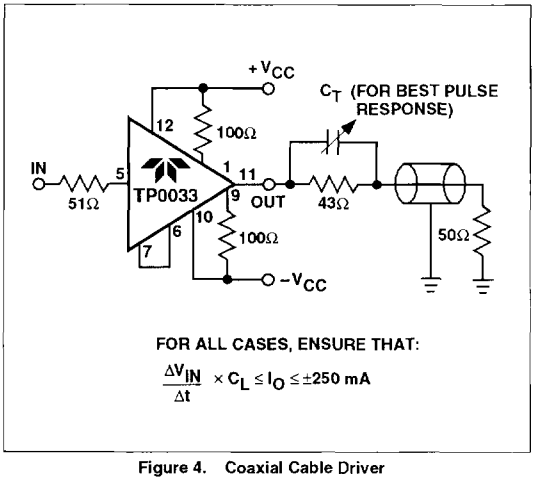


Figure 4. Coaxial Cable Driver

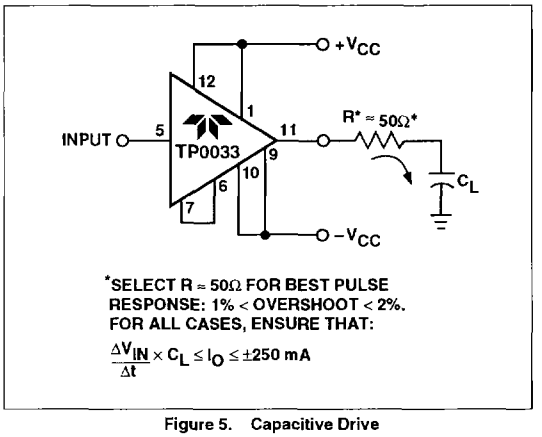


Figure 5. Capacitive Drive

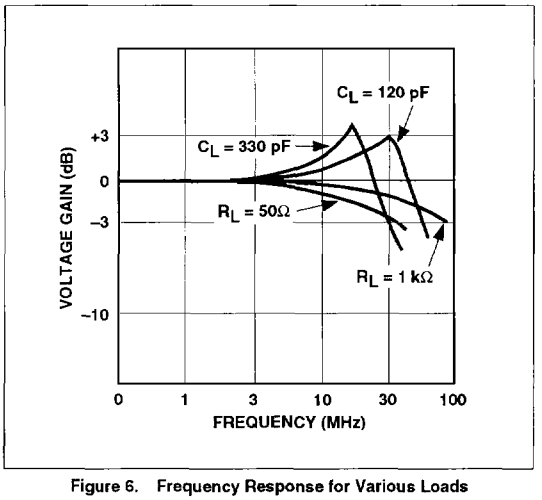


Figure 6. Frequency Response for Various Loads

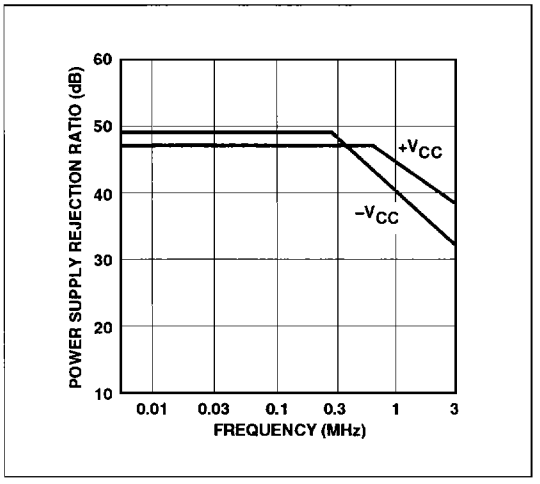


Figure 7. Power Supply Rejection Ratio

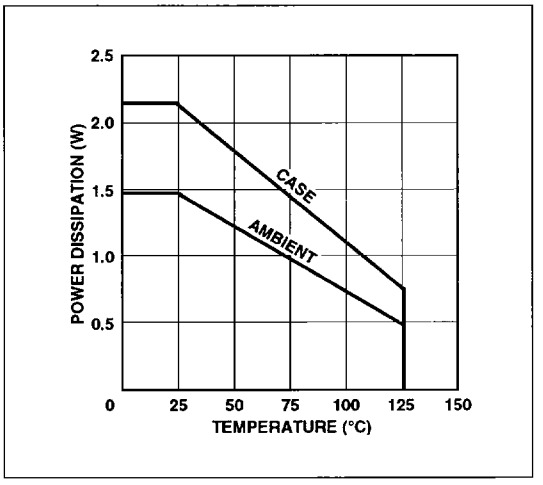


Figure 9. Maximum Power Dissipation

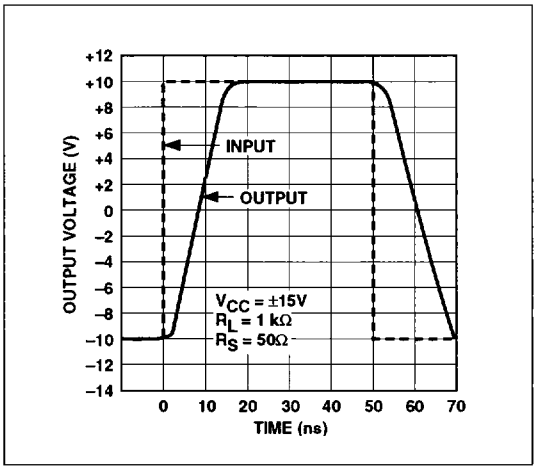


Figure 8. Large Signal Response